



**THE DATASHEET OF  
TISP4080J3BJR-S**



BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS



TISP4xxxJ3BJ Overvoltage Protector Series

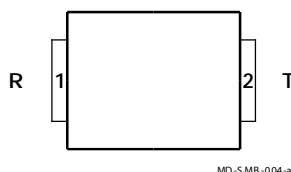
Ion-Implanted Breakdown Region  
 -Precise and Stable Voltage  
 -Low Voltage Overshoot Under Surge

Designed for Transformer Center Tap  
 (Ground Return) Overvoltage Protection  
 -Enables GR-1089-CORE Compliance  
 -High Holding Current Allows Protection  
 of Data Lines with d.c. Power Feed

Can be Used to Protect Rugged  
 Modems Designed for Exposed  
 Applications Exceeding TIA-968-A

Device Name	V <sub>DRM</sub> V	V <sub>(BO)</sub> V
TISP4070J3BJ	58	70
TISP4080J3BJ	65	80
TISP4095J3BJ	75	95
TISP4115J3BJ	90	115
TISP4125J3BJ	100	125
TISP4145J3BJ	120	145
TISP4165J3BJ	135	165
TISP4180J3BJ	145	180
TISP4200J3BJ	155	200
TISP4219J3BJ	180	219
TISP4250J3BJ	190	250
TISP4290J3BJ	220	290
TISP4350J3BJ	275	350
TISP4395J3BJ	320	395

SMB Package (Top View)



Device Symbol



Rated for International Surge Wave Shapes

Wave Shape	Standard	I <sub>TSP</sub> A
2/10 μs	GR-1089-CORE	1000
8/20 μs	IEC 61000-4-5	800
10/160 μs	TIA-968-A	400
10/700 μs	ITU-T K.20/21/45	350
10/560 μs	TIA-968-A	250
10/1000 μs	GR-1089-CORE	200

Additional Information

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Agency Recognition

Description	
UL	File Number: <a href="#">E215609</a>

UL Recognized Component

Description

The range of TISP4xxxJ3BJ devices are designed to limit overvoltages on telecom lines. The TISP4xxxJ3BJ is primarily designed to address GR-1089-CORE compliance on data transmission lines with d.c. power feeding. When overvoltage protection is applied to transformer coupled lines from the transformer center tap to ground, the total ground return current can be 200 A, 10/1000 and 1000 A, 2/10. The high 150 mA holding current is set above common d.c. feed system levels to allow the TISP4xxxJ3BJ to reset following a disturbance.

These devices allow signal voltages, without clipping, up to the maximum off-state voltage value, V<sub>DRM</sub>, see Figure 1. Voltages above V<sub>DRM</sub> are limited and will not exceed the breakover voltage, V<sub>(BO)</sub>, level. If sufficient current flows due to the overvoltage, the device switches into a low voltage on-state condition, which diverts the current from the overvoltage through the device. When the diverted current falls below the holding current, I<sub>H</sub>, level the devices switches off and restores normal system operation.

How to Order

Device	Package	Carrier	Order As	Marking Code	Standard Quantity
TISP4xxxJ3BJ	SMB	Embossed Tape Reeled	TISP4xxxJ3BJR-S	4xxxJ3	3000

Insert xxx corresponding to device name.



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\*RoHS Directive 2015/863, Mar 31, 2015 and Annex.

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# TISP4xxxJ3BJ Overvoltage Protector Series

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## Absolute Maximum Ratings, $T_A = 25\text{ °C}$ (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage	'4070J3BJ	±58	V
	'4080J3BJ	±65	
	'4095J3BJ	±75	
	'4115J3BJ	±90	
	'4125J3BJ	±100	
	'4145J3BJ	±120	
	'4165J3BJ	±135	
	'4180J3BJ	±145	
	'4200J3BJ	±155	
	'4219J3BJ	±180	
	'4250J3BJ	±190	
	'4290J3BJ	±220	
	'4350J3BJ	±275	
	'4395J3BJ	±320	
Non-repetitive peak impulse current (see Notes 1 and 2) 2/10 $\mu\text{s}$ (GR-1089-CORE, 2/10 $\mu\text{s}$ voltage wave shape) 8/20 $\mu\text{s}$ (IEC 61000-4-5, combination wave generator, 1.2/50 $\mu\text{s}$ voltage wave shape) 10/160 $\mu\text{s}$ (TIA-968-A, 10/160 $\mu\text{s}$ voltage wave shape) 4/250 $\mu\text{s}$ (ITU-T K.20/21, 10/700 $\mu\text{s}$ voltage waveshape, simultaneous) 5/310 $\mu\text{s}$ (ITU-T K.20/21, 10/700 $\mu\text{s}$ voltage wave shape, single) 5/320 $\mu\text{s}$ (TIA-968-A, 9/720 $\mu\text{s}$ voltage waveshape, single) 10/560 $\mu\text{s}$ (TIA-968-A, 10/560 $\mu\text{s}$ voltage wave shape) 10/1000 $\mu\text{s}$ (GR-1089-CORE, 10/1000 $\mu\text{s}$ voltage wave shape)	$I_{PPSM}$	±1000 ±800 ±400 ±370 ±350 ±350 ±250 ±200	A
Non-repetitive peak on-state current (see Notes 1 and 2) 20 ms, 50 Hz (full sine wave)	$I_{TSM}$	50	A
Initial rate of rise of on-state current. Linear current ramp. Maximum ramp value < 50 A	$di_T/dt$	800	A/ $\mu\text{s}$
Junction temperature	$T_J$	-40 to +150	°C
Storage temperature range	$T_{stg}$	-65 to +150	°C

NOTES: 1. Initially the device must be in thermal equilibrium with  $T_J = 25\text{ °C}$ .

2. These non-repetitive rated currents are peak values of either polarity. The surge may be repeated after the device returns to its initial conditions.

## Electrical Characteristics, $T_A = 25\text{ °C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{DRM}$ Repetitive peak off-state current	$V_D = V_{DRM}$ $T_A = 25\text{ °C}$ $T_A = 85\text{ °C}$			±5 ±10	$\mu\text{A}$
$V_{(BO)}$ AC Breakover voltage	$dv/dt = \pm 250\text{ V/ms}$ , $R_{SOURCE} = 300\ \Omega$			±70 ±80 ±95 ±115 ±125 ±145 ±165 ±180 ±200 ±219 ±250 ±290 ±350 ±395	V

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# TISP4xxxJ3BJ Overvoltage Protector Series

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## Electrical Characteristics, $T_A = 25\text{ °C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit		
$V_{(BO)}$ Ramp breakover voltage	dv/dt $\leq \pm 1000\text{ V}/\mu\text{s}$ , Linear voltage ramp, Maximum ramp value = $\pm 500\text{ V}$ di/dt = $\pm 20\text{ A}/\mu\text{s}$ , Linear current ramp, Maximum ramp value = $\pm 10\text{ A}$			'4070J3BJ	$\pm 77$		
				'4080J3BJ	$\pm 88$		
				'4095J3BJ	$\pm 104$		
				'4115J3BJ	$\pm 125$		
				'4125J3BJ	$\pm 135$		
				'4145J3BJ	$\pm 156$		
				'4165J3BJ	$\pm 177$		
				'4180J3BJ	$\pm 192$		
				'4200J3BJ	$\pm 212$		
				'4219J3BJ	$\pm 231$		
				'4250J3BJ	$\pm 263$		
				'4290J3BJ	$\pm 303$		
				'4350J3BJ	$\pm 364$		
'4395J3BJ	$\pm 409$						
$I_{(BO)}$ Breakover current	dv/dt = $\pm 250\text{ V}/\text{ms}$ , $R_{SOURCE} = 300\ \Omega$			'4070J3BJ thru '4115J3BJ '4125J3BJ thru '4219J3BJ '4250J3BJ thru '4395J3BJ	$\pm 900$ $\pm 800$ $\pm 600$	mA	
$I_H$ Holding current	$I_T = \pm 5\text{ A}$ , di/dt = $\pm 30\text{ mA}/\text{ms}$	$\pm 150$			$\pm 600$	mA	
dv/dt Critical rate of rise of off-state voltage	Linear voltage ramp Maximum ramp value $< 0.85V_{DRM}$	$\pm 5$				kV/ $\mu\text{s}$	
$I_D$ Off-state current	$V_D = \pm 50\text{ V}$ $T_A = 85\text{ °C}$				$\pm 10$	$\mu\text{A}$	
$C_O$ Off-state capacitance	f = 1 MHz, $V_d = 1\text{ V rms}$ , $V_D = 0$			'4070J3BJ thru '4115J3BJ	195	235	
				'4125J3BJ thru '4219J3BJ	120	145	
				'4250J3BJ thru '4395J3BJ	105	125	
	f = 1 MHz, $V_d = 1\text{ V rms}$ , $V_D = -1\text{ V}$				'4070J3BJ thru '4115J3BJ	180	215
					'4125J3BJ thru '4219J3BJ	110	132
					'4250J3BJ thru '4395J3BJ	95	115
	f = 1 MHz, $V_d = 1\text{ V rms}$ , $V_D = -2\text{ V}$				'4070J3BJ thru '4115J3BJ	165	200
					'4125J3BJ thru '4219J3BJ	100	120
					'4250J3BJ thru '4395J3BJ	90	105
	f = 1 MHz, $V_d = 1\text{ V rms}$ , $V_D = -50\text{ V}$				'4070J3BJ thru '4115J3BJ	85	100
					'4125J3BJ thru '4219J3BJ	50	60
					'4250J3BJ thru '4395J3BJ	42	50
	f = 1 MHz, $V_d = 1\text{ V rms}$ , $V_D = -100\text{ V}$ (see Note 3)				'4125J3BJ thru '4219J3BJ	40	50
					'4250J3BJ thru '4395J3BJ	35	40

NOTE: 3. To avoid possible clipping, the TISP4125J3BJ is tested with  $V_D = -98\text{ V}$ .

## Thermal Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$ Junction to ambient thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$ (see Note 4)			90	$^{\circ}\text{C}/\text{W}$

NOTE: 4. EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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Parameter Measurement Information

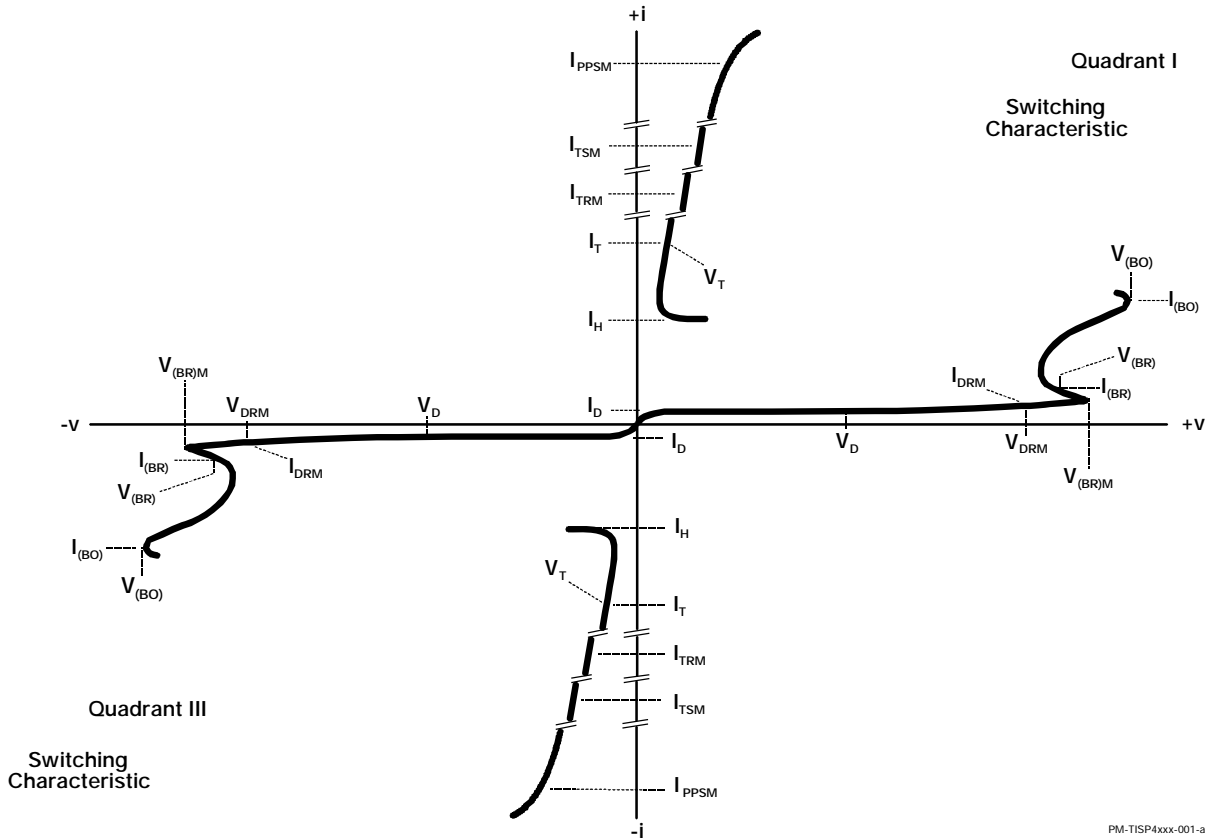


Figure 1. Voltage-Current Characteristic for T and R Terminals  
All Measurements are Referenced to the R Terminal

PM-TISP4xxx-001-a

## Typical Characteristics

**OFF-STATE CURRENT  
vs  
JUNCTION TEMPERATURE**

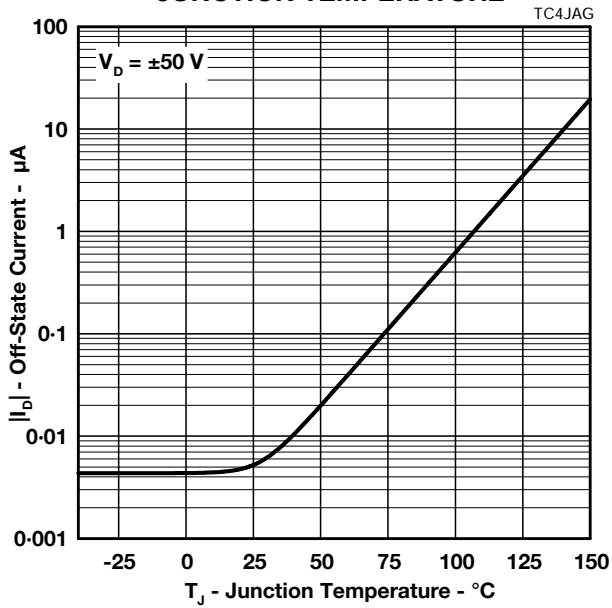


Figure 2.

**NORMALIZED BREAKOVER VOLTAGE  
vs  
JUNCTION TEMPERATURE**

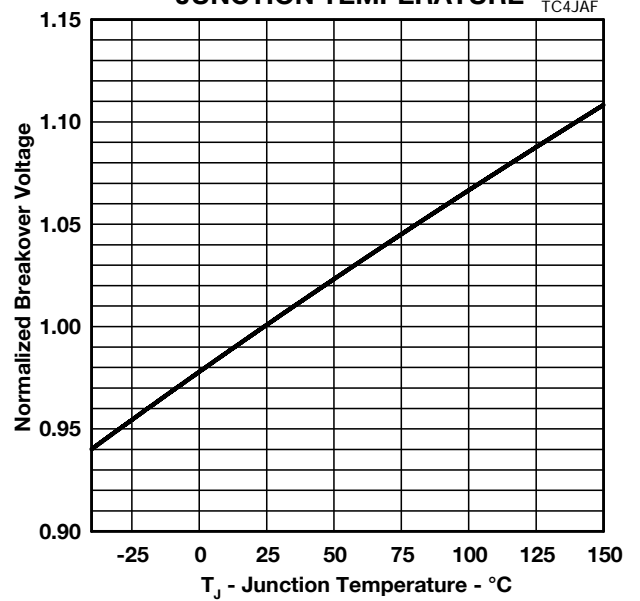


Figure 3.

**NORMALIZED HOLDING CURRENT  
vs  
JUNCTION TEMPERATURE**

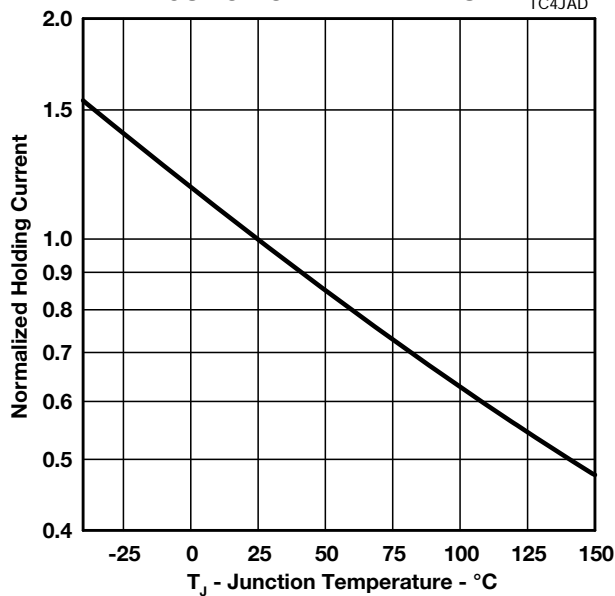


Figure 4.

**NORMALIZED CAPACITANCE  
vs  
OFF-STATE VOLTAGE**

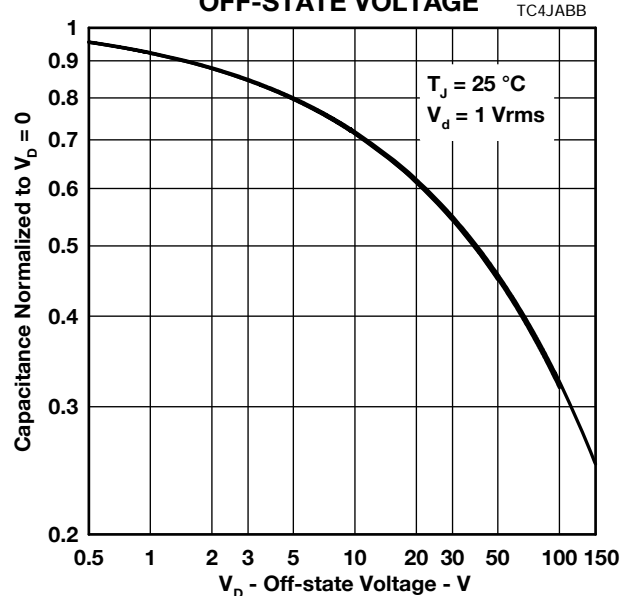


Figure 5.

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## Rating and Thermal Characteristics

### NON-REPETITIVE PEAK ON-STATE CURRENT VS CURRENT DURATION

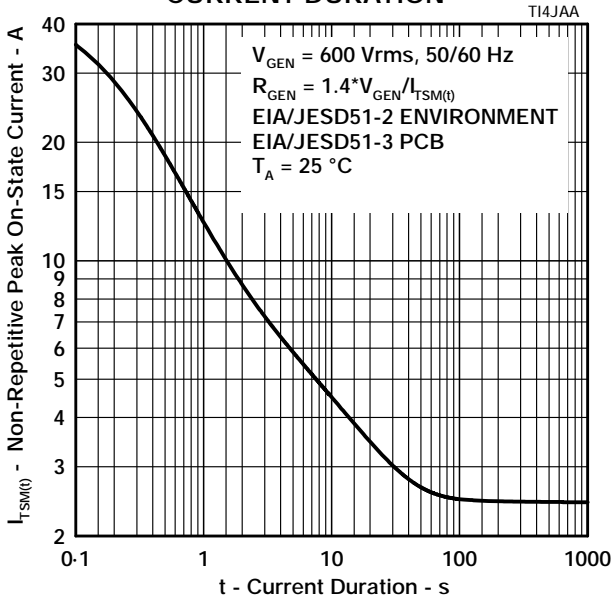


Figure 6.

### V<sub>DRM</sub> DERATING FACTOR VS MINIMUM AMBIENT TEMPERATURE

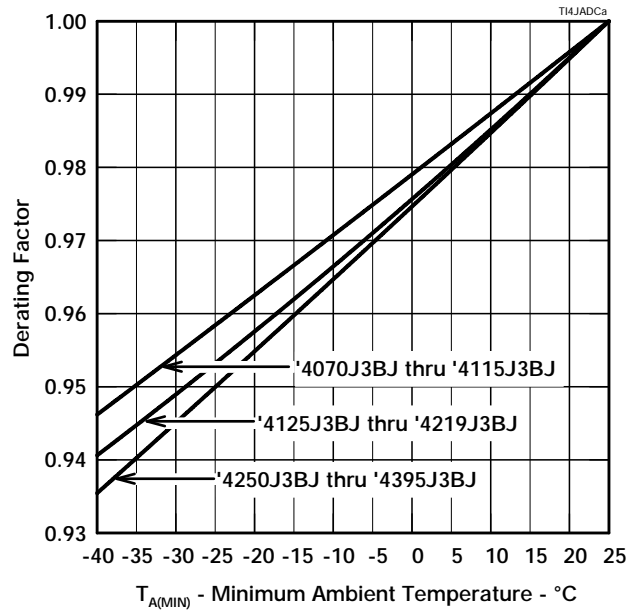


Figure 7.

## Applications Information

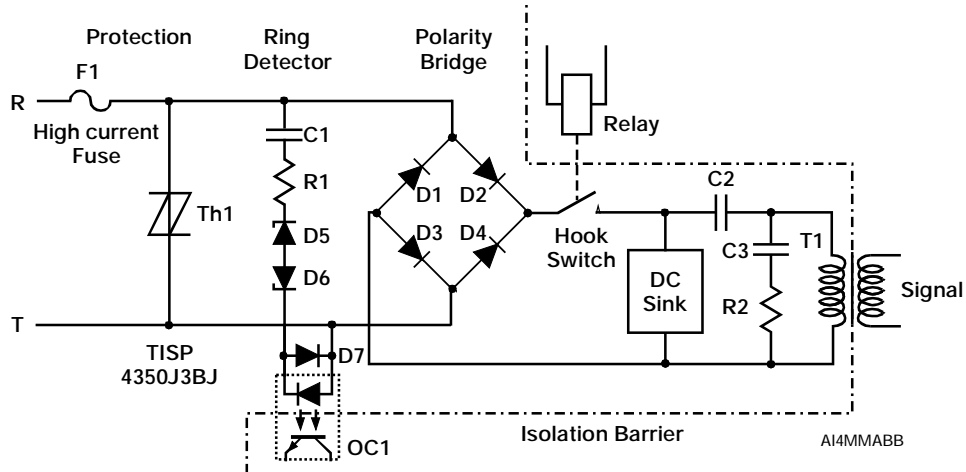


Figure 8. Typical Application Circuit

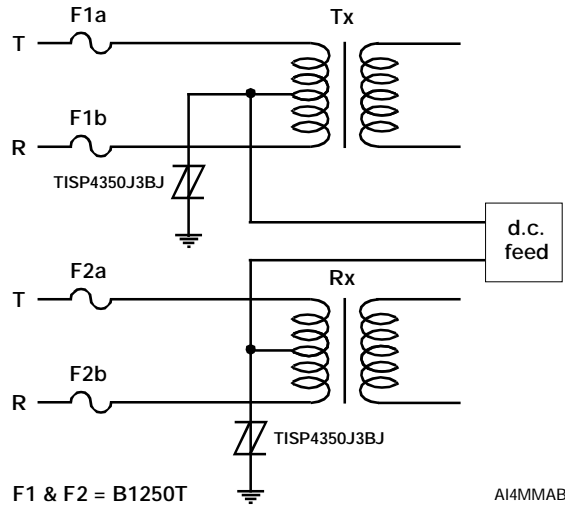


Figure 9. Typical Application Circuit

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