THE DATASHEET OF

TDA7528TR

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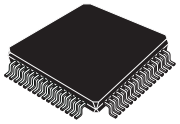
TDA7528

FM/AM car-radio receiver front-end for IF-sampling systems with fully integrated VCO

Features

- High-performance AM/FM front-end chip for IF-sampling car-radio tuners
- Compatible with AM(LW, MW, SW) / FM(EU, US, JAPAN, OIRT) / Weather Band / HD-Radio / DRM applications
- Ready for multi-tuner applications (phase diversity, background tuner)
- Dual input FM-mixer with high image rejection, specialized for different front-end circuits
- Integrated AM preamplifier and tank for lower-cost applications
- Fully integrated tuning PLL with two VCO's for diversity systems
- World tuning capable
- Integrated IF tank
- AGC controlled IF amplifier with four inputs for connection of up to four ceramic filters
- Fully electronically adjustable
- I^2C/SPI controlled



LQFP64

Description

The TDA7528 is a front-end module for use in car radio receivers with digital IF processing, using the STA3004, respectively the STA3005 backend IC.

Its field of use includes all the current radio broadcast services in the range of 50kHz to 163MHz for AM radio, FM radio and US weather band. Digital standards such as DRM and HD radio can also be handled. A single supterheterodyne architecture with 10.7 MHz IF-frequency provides high dynamic range.

The IMR mixer has separate input and output stages for AM frequency bands up to 30 MHz and for FM frequencies above 30 MHz.

The integrated AM-preamplifier and the fully integrated low-pass filter enable low cost applications. Two FM inputs with different noise / IP3 parameter, provide full flexibility for the pre-stage circuitry. Each mixer output is able to drive two IF-filters, which can be selected by the different IF-amplifier inputs.

The fast tuning PLL controls two different VCO, which are designed to operate without frequency overlap.

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Order code	Package	Packing
TDA7528	LQFP64 exposed pad (10x10x1.4 mm)	Tray

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1 Product description

1.1 Summary

The TDA7528 is a front-end module for use in car radio receivers on the 50 kHz - 108 MHz and 161 MHz - 163 MHz frequency bands. Its field of use includes all the current radio broadcast services worldwide on long, medium and short wave, CB radio, FM radio on the OIRT, Japanese and ITU frequency bands and the American weather band. Both analogue AM and FM and digital standards such as DRM and HD radio (IBOC) can be handled.

The receiver is designed as a single super-heterodyne with an intermediate frequency of 10.7 MHz. The IF signal is digitized, filtered and demodulated in the appropriate backend IC. The combination of two independently-operating front-ends with the backend makes phase diversity operation possible or the simultaneous reception of two freely-selectable frequencies with any combination of types of demodulation.

The TDA7528 IMR mixer has separate input- and output-stages for AM frequency bands up to 30 MHz (narrowband services) and for FM frequencies above 30 MHz (broadband signals).

As an option, the AM path can be operated with an integrated preamplifier stage and an integrated low-pass filter to reduce interfering input signals on the IF and image frequencies. The mixer has two FM inputs with different properties. The more sensitive (lower noise) input is intended for the use of a passive pre-selection stage and the high level, advanced IP3 input for an active preamplifier stage. The mixer outputs have a single ended low impedance design to drive one or two IF filters with different bandwidths. A switchable gain IF amplifier, independent IF AGC and an integrated anti-aliasing stage drive the IF A/D converter of the backend. Programmable RF AGCs to actuate adjustable preamplifier stages and two D/A converters for tuning external filter stages complete the reception path.

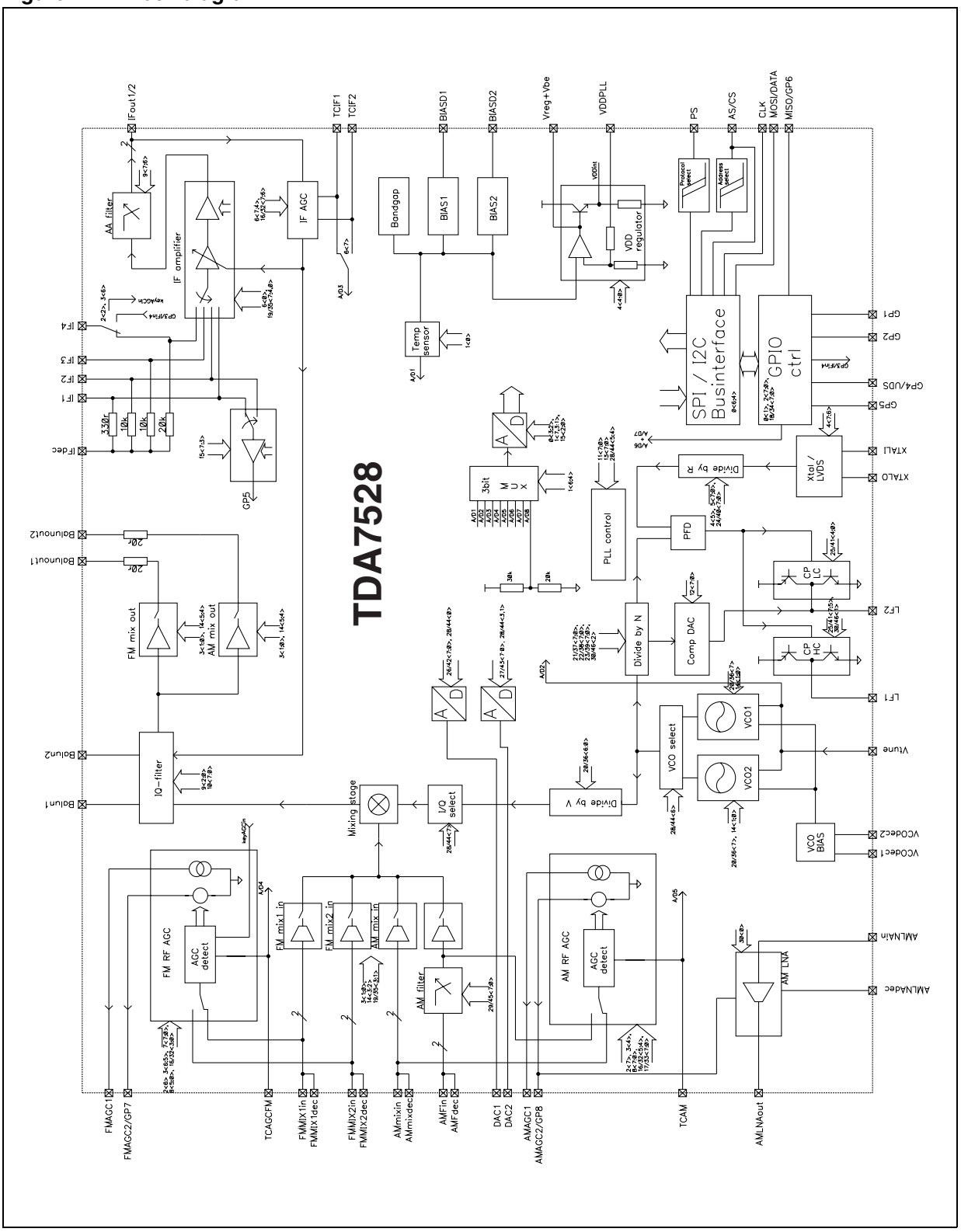
Two fully-integrated VCOs are included in the TDA7528, oscillating in a range around 3.7 GHz and 4.7 GHz respectively. The output signal of the selected VCO drives a programmable divider generating the LO signal for the mixer stage. The PLL, integrated with the exception of the loop filter, facilitates reception on all the above-mentioned frequencies, rapid frequency changes in the standard tuning steps of 50 kHz for FM, 9 or 10 kHz for LW and MW and 5 kHz for SW. The smallest available tuning steps are 12.5 kHz for FM and 1 kHz for all AM bands.

The TDA7528 is controlled by a serial command interface, switchable between SPI and I^2C protocol. The external reference source is typically 74.1 MHz. However, the TDA7528 also has its own reference oscillator.

All the necessary calibration steps can be carried out electronically during production. An integrated temperature sensor facilitates the adaptation of various parameters during operation, like IF gain or AGC threshold.

1.2 Block diagram

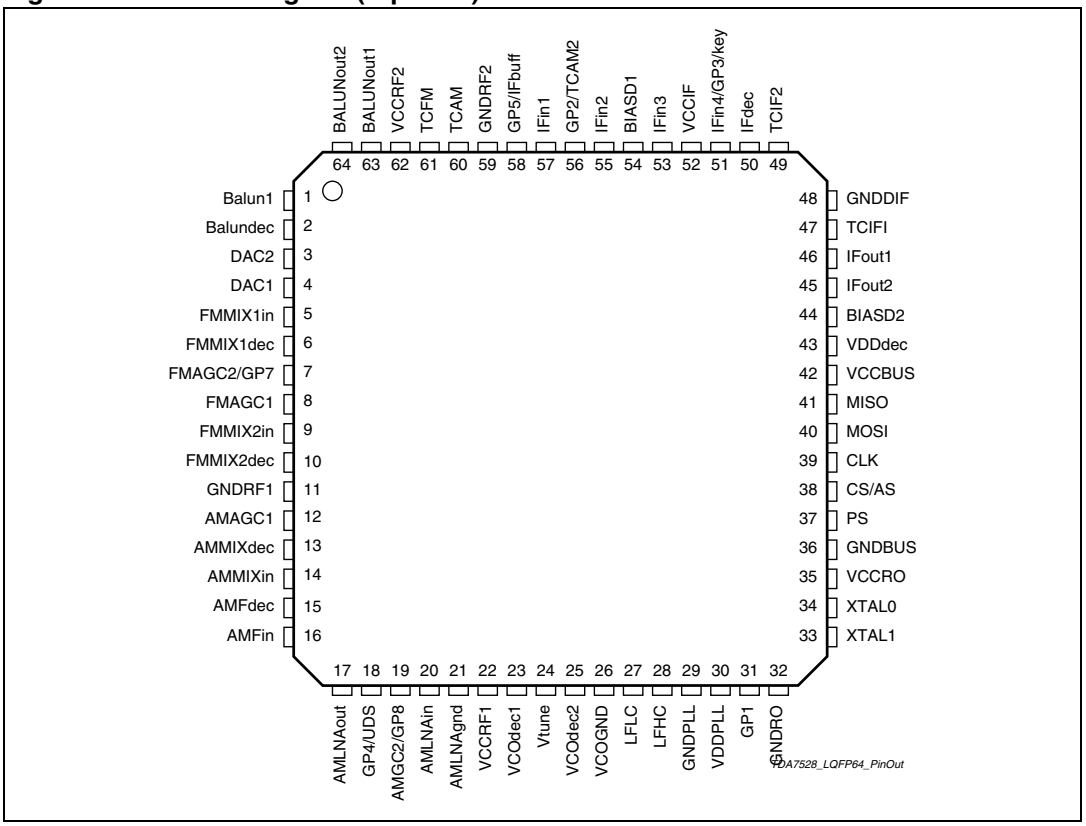
Figure 1. Block diagram



2 Pin description

2.1 Pin connection

Figure 2. Pinout diagram (top view)



2.2 Pin description

Table 2. Pin function description

Pin #	Pin name	Description
1	BALUN1	Active balun input 1
2	BALUNdec	Active balun input 2 (decoupling)
3	DAC2	Tuning DAC 2 output
4	DAC1	Tuning DAC 1 output
5	FMMIX1in	FM mixer input – high gain stage = mode 1
6	FMMIX1dec	FM mixer decouple
7	FMAGC2/GP7	FM AGC voltage output / alternative GP7 output
8	FMAGC1	FM AGC current output for PIN diode
9	FMMIX2in	FM Mixer input – low gain stage = mode2

Table 2. Pin function description (continued)

Pin #	Pin name	Description
10	FMMIX2dec	FM Mixer decouple
11	GNDRF1	GND RF1 section
12	AMAGC1	AMAGC PIN diode driver output
13	AMMIXdec	AM mixer decouple
14	AMMIXin	AM mixer input
15	AMFdec	Decoupling of AM filter
16	AMFin	Input of AM filter
17	AMLNAout	AM LNA output
18	GP4/UDS	GPIO 4 / UDS input
19	AMAGC2/GP8	AM AGC voltage output / alternative GP8 output
20	AMLNAin	AM LNA input
21	AMLNAGND	AM LNA Ground
22	VCCRF1	Supply RF1 section
23	VCOdec1	BIAS decouple for VCO
24	Vtune	VCO tuning voltage
25	VCOdec2	BIAS decouple for VCO
26	GNDVCO	VCO Ground
27	LFLC	Loop filter low current output
28	LFHC	Loop filter high current output
29	GNDPLL	PLL Ground
30	VDDPLL	Supply PLL
31	GP1	GPIO 1
32	GNDRO	Ground PLL digital part
33	XTALI	Reference oscillator input
34	XTALO	Reference oscillator output
35	VCCRO	Supply PLL digital part
36	BUSGND	BUS interface Ground
37	PS	Protocol Select
38	CS/AS	Chip select / Address select
39	CLK	SPI / I2C clock
40	MOSI	SPI data input / I2C Data
41	MISO	SPI data output / GP6
42	VCCBUS	Supply of BUS interface
43	VDDdec	Decouple of internal 3.3V (=3,3V + Vbe)
44	BIASD2	Decoupling for biasing

Table 2. Pin function description (continued)

Pin #	Pin name	Description
45	IFout2	Differential IF output 2
46	IFout1	Differential IF output 1
47	TCIF1	time constant IF AGC for AM
48	GNDIF	ground IF section
49	TCIF2	time constant IF AGC for FM
50	IFdec	Decouple of IF amplifier
51	IFin4 / GP3	IF input 4 (= AM IBOC input) / GPIO 3
52	VCCIF	Supply IF section
53	IFin3	IF input 3 (= AM analog input)
54	BIASD1	Decoupling for biasing
55	IFin2	IF input 2 (= FM IBOC input)
56	GP2/TCAM2	GPIO 2 / input for 2nd order time constant of AM AGC
57	IFin1	IF input 1 (= FM analog input)
58	GP5/IFbuff	GPIO 5 / IF buffer amplifier output
59	GNDRF2	GND RF2 section = active balun GND
60	TCAM	AM AGC time constant
61	TCFM	FM AGC time constant
62	VCCRF2	Supply voltage RF2 section
63	Balunout1	Active balun output 1 = FM output
64	Balunout2	Active balun output 2 = AM output

3 Electrical characteristics

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	5.5	V
V_{DD}	Supply voltage	3.6	V
T_{amb}	Ambient temperature range	-40 to 125	°C
T_s	Storage temperature	-55 to 150	°C
T_j	Max. junction temperature	150	°C

Operating temperature and supply voltage range: -40 °C to 105 °C; 4.7 V to 5.35 V.
All specification parameter are fulfilled in this temperature and supply voltage range, unless otherwise specified. Typical values reflect average measurement at T_{amb} = 25 °C, V_{CC} = 5.0 V and V_{DD} = 3.3 V.

3.2 General parameters

Table 4. General parameters electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ	Max	Unit
V_{CC}	5V supply voltage	Full performance	4.7	5	5.35	V
		Fully functional but with reduced performance	4.6	-	4.7	V
V_{DD}	3.3V supply voltage	When used with external 3.3 V power supply regulator	3.1	3.3	3.5	V
	V_{CC} slew rate range	-	0.01	-	1000	V/ms
I_{CC}	Supply current @5V typ	FM typical application	-	160	200	mA
		AM external pre-stage	-	160	200	mA
		AM integrated pre-stage	-	175	215	mA
I_{CCmax}	Max supply current	FM, max application, (FM typ + Xtal, IF-buffer, AMAGC)	-	170	215	mA
I_{CC_pwd}	Supply current @5V in power down mode	-	-	7	11	mA
P_{max}	Power dissipation	FM typical application	-	650	950	mW
		AM external pre-stage	-	650	950	mW
		AM integrated pre-stage		710	1015	mW
T_{amb}	Ambient temperature range	Full performance, unless otherwise specified	-40	-	105	°C
T_{extend}	Extended ambient temperature range	Signal path functional with reduced performance	105	-	125	°C

3.3 Power management and voltage regulator

The TDA7528 has a single 5 V supply. The 3.3 V supply for the VCO must be derived from an external NPN transistor controlled by the internal voltage regulator. It is also possible to use an external 3.3 V regulator. In this case, special care has to be taken on this 3.3V .

3.3.1 Power management

The TDA7528 detects whether all the voltages are high enough and stable when the operating power supply is applied. The power-on reset is tripped and all the control registers are set to "low" if this condition is not met.

As long as the voltages remain within the permissible range, the SPI/I^2C interface is active (in the I^2C mode this can be detected by the µP through the acknowledge signal on every communication with the bus master).

The SPI-/I^2C interface is in power-on mode when the operating voltage is applied to the TDA7528.

The following function groups can be switched on/off via SPI/I^2C:

- PLL {divider R, N and V, PFD, charge pump, VCO1 (3,7 GHz-VCO) or VCO2 (4,7 GHz-VCO), Reference-Oscillator or LVDS input buffer}
- FM/AM-mixer and active balun, FM-AGC
- D/A-converter_1
- D/A-converter_2
- AM-LNA
- AM-low pass filter
- AM-AGC
- IF-section {IF-amplifier, anti-aliasing-filter, IF-AGC}
- GPIO
- temperature-sensor,
- Sensor ADC

3.3.2 Power-on circuit and low supply voltage detector

Power-on circuit:

The power-on circuit produces a reset whenever one of the following voltages is below it's POR level. (BIASD1, BIASD2 < 1.2 V; VDDPLL < 2.4V; VCCIF < 3.8 V)

Low supply voltage detector:

The "PWR_STABLE_read" status bit has the value "0" after power on. This bit is set to "1" by an SPI/I2C write command from the microcontroller in initialization communication to the "PWR_STABLE_write" bit. The microcontroller cannot reset the "PWR_STABLE_read" bit. A "0" transmitted in the "PWR_STABLE_write" bit has no effect.

If the power supply falls below the programmed threshold all registers are set to their power-on default, including that the "PWR_STABLE_read" bit is set to "0". By this the microcontroller can verify at any time whether a critical drop in voltage (value "0") has taken place since the last TDA7528 read out of this bit. The threshold voltage can be calibrated

indirect by measuring the DAC1 (9 bit) output voltage for DAC1=0x200 or the DAC2 (8 bit) output voltage for DAC2=0x100).

The PWR_STABLE functionality can be switched on/off. The default value is the switched off mode.

Table 5. Voltage sag detection electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ	Max	Unit
V_{STHmin}	Min. supply voltage threshold	-40 to 150 °C, $T_j \leq 150$ °C	4.1	4.3	4.5	V
V_{STHmax}	Max supply voltage threshold	-	4.4	4.6	4.9	V
-	Step size	-	-	100	-	mV
t_c	Time constant	-	-	1	-	µs

3.3.3 Voltage regulator

The internal voltage regulator drives the external transistor for the 3.3V supply of the VCO and PLL. The 3.3 V voltage regulator for the bus interface and the reference oscillator is fully integrated.

Table 6. Voltage regulator electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ	Max	Unit
V_{DD}	3.3V supply voltage	Internal voltage regulator with external power transistor	3.1	3.3	3.5	V
I_{DD}	current of external V_{DD}	Current through external transistor or from external 3.3 V supply	-	60	80	mA

When an external 3.3 V supply is used for the VCO and PLL supply, special care has to be taken on the supply voltages during the ramp-up phase:

- the 3.3 V supply must never be higher than the 5 V supply;
- the difference between 5 V and 3.3 V must never exceed 3.6 V.

The second prerequisite is automatically met using a 3.3 V Z-diode between the 5 V and the 3.3 V supplies.

3.4 FM - Section

3.4.1 IMR and active balun

The IMR mixer has two software-selectable FM inputs (referred to as mode 1 and mode 2). These inputs are implemented with different gains, noise figures, IIP3, maximum input signal.

There are two single ended outputs of the IMR mixer. One is dedicated to FM (Balunout1) and the other to AM (Balunout2). It is not recommended to use both outputs in parallel.

Table 7. IMR and active balun electrical characteristics

(All parameter are referred to Balunout1, unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
G_{mix1} G_{mix2}	Gain vs. Balunout1 Gain vs. Balunout1	Mode 1 (unloaded gain) Mode 2 (unloaded gain)	20 13	22 15	24 17	dB
G_{mix1} G_{mix2}	Gain vs. Balunout2 Gain vs. Balunout2	Mode 1 (unloaded gain) Mode 2 (unloaded gain)	16 9	18 11	20 13	dB
-	Absolute gain error	@ 100 MHz @ 25°C	-	-	± 1.0	dB
-	Gain error vs. frequency	Freq. range @ 25°C 47,0 to 74,0 MHz 76,0 to 90,0 MHz 87,5 to 108,0 MHz 30,0 to 170,0 MHz	-	-	 ± 0,5 ± 0,5 ± 0,5 ± 2,0	dB
-	Gain error vs. temperature	-40 °C to 105 °C	-	-	± 2,0	dB
-	Gain attenuation range	Controlled by IF-AGC	17.5	20	-	dB
-	Input impedance	Mode 1 Mode 2	5 5	-	-	kΩ
-	Input resistance	Mode 1 Mode 2	30 9.5	50 12.5	 19.5	kΩ
-	Output impedance	Active balun	15	20	30	Ω
-	External load	Full current: reg14[5] = 0 Red. current: reg14[5] = 1	320 600	-	-	Ω Ω
V_{out_max}	Max. output voltage	1dB below 1dB compression point	121	123	-	dBµV
V_{in_max}	Max. input voltage	Mode 1 Mode 2 1dB below 1dB compression point	100 108	-	-	dBµV
V_{noise}(1)	Input noise voltage – mode1 Input noise voltage – mode2	Rsource=1.5 kΩ, noiseless in 65 MHz-170 MHz range Rsource = 800 Ω, noiseless in 65 MHz-170 MHz range	-	3.1 5	3.7 6	nV/√ Hz
d_{noise}	vnoise*atten*dnoise	AGC noise behavior @ 6 dB attenuation	-	6	-	dB

Table 7. IMR and active balun electrical characteristics (continued)

(All parameter are referred to Balunout1, unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
IIP3[1]	3rd order intercept point Reg9[5:4]=00	Mode 1 up to Vin/tone = 90 dBµV Mode 2 up to Vin/tone = 98 dBµV up to 95 °C junction temperature	123 126 130	125 133	-	dBµV
	3rd order intercept point in reduced current mode	Mode 1; reg14[3:2]=01	-	120	-	dBµV
		Mode 2; reg14[3:2]=01 60 °C up to 125 °C junction temperature	130	132	-	
		Mode 1; reg14[3:2]=10	-	117	-	
		Mode 2; reg14[3:2]=10 junction temperature > 90 °C	129	130	-	
IIP2[1]	2nd order intercept point	Mode 1 Mode 2	144 157	-	-	dBµV
IFattn	IF- output attenuation (without external circuitry)	@ 26.35 MHz @ 100 MHz	1 9	2	-	dB
-	IF rejection	-	38	-	-	dB
V_{LO_IN}	LO signal @ mixer input	R_{source} =1.5 kΩ @ fundamental LO freq. @ LO harmonics	-	-	10 40	dBµV
V_{LO_OUT}	LO signal @ balun output	Incl. LC-tank with Q=2, R_{load} = 1.0 kΩ @ fundamental LO freq. @ LO harmonics	-	-	66 60	dBµV
I_{QG}	I/Q gain adjust Min. Max.	4bit	-	-0.7 0.7	-	dB
-	gain step	-	-	0.1	-	dB
P_{IQ}	I/Q phase adjust Min. Max.	4bit	-	-1.2 1.2	-	°
-	Phase step	-	-	0.2	-	°
-	Center frequency adjust Min. Max.	3bit	-	-2.4 2.4	-	MHz
-	Frequency step	-	-	0.6	-	MHz
IRR	Image rejection ratio	without gain/phase adjust	30	45	-	dB
		with freq/gain adjust @ 25°C	45	-	-	
		with freq/gain/phase adjust vs. complete temp. range	40	-	-	

1. Parameter not guaranteed by production test

3.4.2 FM AGC

The time constant of the FM AGC is defined by an external capacitor and the programmable internal currents (details given in the *Table 8*). The currents can be selected independently for AGC attack and decay. By this a symmetrical behavior rather than a 2...250 times faster attack behavior can be programmed.

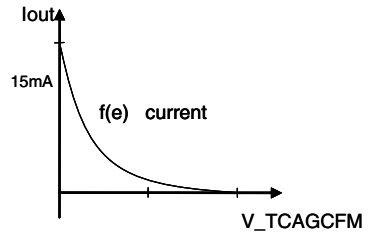
Control behavior:

The FM-RF-AGC is realized with two output pins which control the gain of the corresponding pre-stage.

The control behavior can be programmed to the following modes:

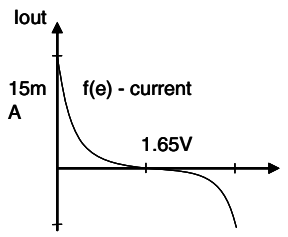
1. **Controlled current output mode 1**
   data byte FMAGC[3:0] = 1000
   positive current I = f(e): after reaching the AGC threshold voltage the current output delivers a current I = f(e) up to -15 mA in a voltage range from 0.2V up to V_{CC}-1.5 V.

Figure 3. FM AGC - Controlled current output mode 1



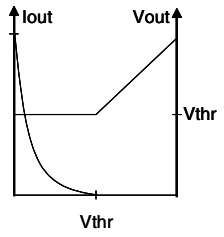
2. **Controlled current output mode 2**
   data byte FMAGC[3:0] = 1100
   Below the AGC threshold voltage the AGC output sinks a constant current of 5 mA. When the RF input level crosses the AGC threshold voltage the current is reduced down to 0mA with a quasi-log. behavior. At half control voltage the current becomes positive and reaches up to -15 mA following an exponential function.

Figure 4. FM AGC - Controlled current output mode 2



3. **Constant current mode**
   data byte FMAGC[3:0] = 0100
   The output current can be set to 2 mA source current. The AGC detector is in power-down mode and only the pin diode driver is active.
4. **Controlled Voltage / current output**
   data byte FMAGC[3:0] = 1011
   voltage and current mode with hand-over: the Vthr level is programmable in the range of 0.2 V to 2.6 V.

Figure 5. FM AGC - Controlled Voltage / current output



5. **Calibration mode**
   data byte FMAGC[3:0] = 0010
   calibration mode for voltage output: The voltage Vthr can be switched directly to the voltage output pin.

All other possible bit combinations of data byte FMAGC[3:0] are not recommended.

The voltage output can be configured as GPO.

The FMAGC2 output (voltage output) is short-circuit protected by a current limiter. The FMAGC1 output (current output) needs an external resistor for current limitation. The current output is voltage-tolerant up to V_{CC}, the voltage output up to V_{DD}.

The microcontroller can read the voltage at the AGC capacitor via the serial control interface. On request of the microcontroller the measurement is done by applying the time constant capacitor voltage to the central ADC (specified in chapter *3.10*) and gives information to calculate the AGC-attenuation.

The FM AGC system is controlled by a peak detector.

The Key AGC function is controlled by a D/A converter in the backend.

Table 8. FM-AGC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
Lthr	Threshold RF level Min. Threshold	Referred to mixer input	-	-	-	-
		Mode 1 - high gain mixer	-	86	-	dBµV
		Mode 2 – low gain mixer	-	92	-	
	Max Threshold	Mode 1 - high gain mixer	-	100	-	
		Mode 2 – low gain mixer	-	106	-	
-	Threshold steps	4 bit control	0.5	1	1.5	dB
-	Threshold error	30 to170 MHz @ 25 °C	-1.5	-	1,5	dB
-	Total threshold error	30.0 to 170.0 MHz	-3	-	3	dB
-	Temperature behavior of AGC thresholds	-	-	0.011	-	dB/°C
-	Frequency range	-	30	-	170	MHz
-	Pin diode source current ($I \approx -1.5$ mA * (exp(V_{DD}-V_{AGCTC})-1))	V_{AGCTC} < 1V (due to exponential behavior, external resistor needed)	-	-	-10	mA
-	Pin diode sink current ($I \approx 1$ mA * (exp(V_{AGCTC}-1.65V)-1))	V_{AGCTC} = V_{DD} (due to exponential behavior, external resistor needed)	3	-	-	mA

Table 8. FM-AGC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
-	Pin diode source current in constant current mode	-	-	-2	-1	mA
-	Min. voltage	AGC control pin 1 @ positive current mode @ pos/neg current mode	-	-	0.2 0.4	V
-	Max. voltage	AGC control pin 1	V_{CC}-1.5	V_{CC}-1.3	-	V
-	Max. source current	AGC control pin 2; voltage output	1	-	-	mA
-	Min. sink current	AGC control pin 2; voltage output	-	-100	-	µA
-	Max. output voltage in analog voltage mode (follower mode)	AGC control pin 2 @ I_{load} = 1 mA	V_{DD}-0.3	-	V_{DD}	V
-	Min. output voltage in analog voltage mode	AGC control pin 2 @ I_{load} = -50 µA	-	-	1	V
$Vthr_{min}$	Vthr_min	-	0.1	0.2	0.3	V
$Vthr_{max}$	Vthr_max	-	2.4	2.6	2.8	V
-	Step size of Vthr	6bit	-	40	-	mV
DNL	nonlinearity of Vthr	-	-0.5		0.5	LSB
-	I attack for 6dB control error	Mode A1 Mode A2 Mode A3	30 150 0.75	50 250 1.25	80 400 2.0	µA
-	I decay max	Mode D1 Mode D2 Mode D3	-6 -30 -150	-4 -20 -100	-2.5 -12 -60	µA
-	Typical AGC time constant for attack(1)	C_{AGCTC} = 1 µF, mode A2 AGC conductance versus V_{AGCTC}= 20 dB/V	-	0.5	-	ms
-	Typical AGC time constant for decay(1)	C_{AGCTC} = 1 µF, mode D2 AGC conductance versus V_{AGCTC}= 20 dB/V	-	15	-	ms
-	Threshold shift keyed AGC	Control input range = 0.2 to 1 V	-	19	-	dB/V
-	Keyed AGC range	-	10	-	-	dB

1. The time constant is defined as the 1τ value after a 6 dB level step

3.5 AM - Section

3.5.1 AM LNA

Table 9. AM LNA electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
gm	Transconductance	@ 25°C	10	15	20	mS
-	Gain error vs. frequency	Freq. range 150 to 350 kHz 520 to 1710 kHz 2.0 to 30.0 MHz 0.05 to 30.0 MHz	-	-	 ± 0.5 ± 0.5 ± 1.0 ± 2.5	dB
-	Input impedance	-	500	1000		kΩ
vnoise(1)	Input noise voltage	@ 1 MHz @ 150 kHz	-	1.7 2.6	2	nV/√ Hz
IIP3(1)	3rd order intercept point	@ gain 20 dB	123	128	-	dBµV
IIP2	2nd order intercept point	@ gain 20 dB	127	132	-	dBµV
AGC	AGC range	-	8	-	-	dB

1. Parameter not guaranteed by production test

3.5.2 Switchable LPF 4th order

Table 10. Switchable LPF 4th order electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
f_{LP1}	LP corner frequency 1	Mode 1(1)	1.71	-	1.95	MHz
f_{LP2}	LP corner frequency 2	Mode 2(1)	6.2	-	7.1	MHz
f_{LP3}	LP corner frequency 3	Mode 3(1)	14.0	-	16.0	MHz
f_{LP4}	LP corner frequency 4	Mode 4(1)	22.0	-	25.5	MHz
f_{LP5}	LP corner frequency 5	Mode 5(1)	26.1	-	31.0	MHz
G	Gain incl. mix vs. Balunout1	-	3	4.5	6	dB
G	Gain incl. mix vs. Balunout2	-	-1	0.5	2	dB
-	Passband ripple(2)	-	-	-	-	-
-	Stop band attenuation	Mode=1 @ 10.7 MHz (LW+MW) @ >22MHz Mode=2 @ >28 MHz (KW low) @ >87.5 MHz Mode=3 @ >43 MHz (KW mid) @ >87.5 MHz Mode=4 @ >74 MHz (KW high) @ >87.5 MHz Mode=5 @ >74 MHz (11m) @ >87.5 MHz	40 60 30 60 20 45 25 30 20 25	-	-	dB

Table 10. Switchable LPF 4th order electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
Vnoise(2)	Input noise voltage incl. IMR noise	@ 1 to 30 MHz, @ 25°C @ 0.15 to 1 MHz, @ 25°C	-	30 33	34 37	nV/√ Hz
IIP3	3rd order intercept point	Up to 10 MHz input frequency	137	140	-	dBµV
IIP2(2)	2nd order intercept point	Up to 10 MHz input frequency	160	-	-	dBµV

1. Corner frequency needs calibration
2. Parameter not guaranteed by production test

3.5.3 IMR and active balun

All parameter are referred to Balunout2, unless otherwise specified

Table 11. IMR and active balun electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
G	Gain	vs. Balunout2	7	9	11	dB
		vs. Balunout1	11	13	15	dB
-	Gain error	@ 1 MHz --> 10.7MHz	-	-	± 1.0	dB
-	Gain Error vs. frequency	freq. range 150 to 350 kHz 520 to 1710 kHz 2.0 to 30.0 MHz 0.05 to 30.0 MHz	-	-	 ± 0,5 ± 0,5 ± 1.0 ± 2,0	dB
-	Gain error vs. temperature	–40°C to 105 °C	-	-	± 2,0	dB
-	Gain attenuation range	IFAGC controlled	17.5	20		dB
-	Input impedance	For ext. LNA input	9.2	11.8	17.2	kΩ
-	Output impedance	-	15	20	30	Ω
-	Max. external load	-	400	-	-	Ω
Vmax	Max. output voltage	1 dB below 1 dB compression point	121	123	-	dBµV
Vin_max	Max. input voltage	Single tone two tone	101 98	-	-	dBµV dBµV
Vin_max	Max. input voltage	@4.6 V-4.7 V single tone two tone	 99 96	-	-	 dBµV dBµV
vnoise(1)	Input noise voltage	@ full gain 150 kHz-30 MHz		5.8	7.0	nV/√ Hz
IIP3(1)	3rd order intercept point	@ full gain Reg14[5:4] = 00 up to 95 °C junction temperature	128 131	134	-	dBµV

Table 11. IMR and active balun electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
-	3rd order intercept point in reduced current mode	Reg14[5:4] = 01 60 °C up to 125 °C junction temperature	131	133	-	dBµV
		Reg14[5:4] = 10 junction temperature > 90 °C	131	132	-	dBµV
IIP2(1)	2nd order intercept point	-	159	-	-	dBµV
-	IF-output attenuation	@ 26.35 MHz	1	-	-	dB
-	IF rejection	-	40	48	-	dB
V_{LO_IN}(1)	LO signal @ mixer input	R_{source} =1.5 kΩ @ fundamental LO freq @ harmonics of LO freq.	-	-	10 30	dBµV
V_{LO_OUT}	LO signal @ balun output using mixer input	Incl. LC-tank with Q=2, R_{load} = 1.0 kΩ @ fundamental LO freq. with 1 kΩ input termination resistor (1) @ harmonics of LO freq.	-	-	95 80 66	dBµV
	LO signal @ balun output, using low pass filter	Incl. LC-tank with Q=2, Rload=1.0 kΩ @ fundamental LO freq. @ harmonics of LO freq.	-	-	85 66	
I_{QG}	I/Q gain adjust Min. Max.	4 bit	-	-0.7 0.7	-	dB
-	Gain step	-	-	0.1	-	dB
PIQ	I/Q phase adjust Min. Max.	4bit	-	-0.25 0.25	-	°
-	phase step	-	-	0.25	-	°
-	Center frequency adjust Min. Max.	3bit	-	-2.4 2.4	-	MHz
-	Frequency step	-	-	0.6	-	MHz
IRR	Image rejection ratio	Without gain/phase adjust	30	45	-	dB
IRR	Image rejection ratio	With gain/phase adjust @ 25°C	45	-	-	dB
IRR	Image rejection ratio	With gain/phase adjust vs. complete temp. range	40	-	-	dB

1. Parameter not guaranteed by production test

3.5.4 AM AGC

The time constant of the AM AGC is defined by an external capacitor and the programmable internal currents (details given in the *Table 12*).

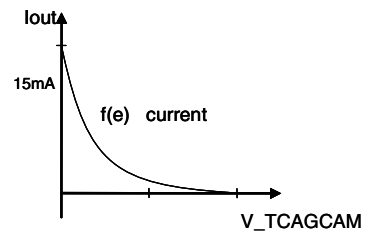
Control behavior:

The AM RF AGC is realized with two output pins which controls the gain of the corresponding pre-stage.

The control behavior can be programmed to the following modes:

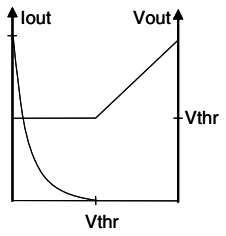
1. **Controlled current output mode 1**
   data byte AMAGC[3:0] = 1000
   positive current I = f(e): after reaching the AGC threshold voltage the current output delivers a current I = f(e) up to 15 mA in a voltage range from 0.1 V up to V_{CC}-1.5 V.

Figure 6. AM AGC - Controlled current output mode 1



2. **Constant current mode**
   data byte AMAGC[3:0] = 0100
   constant current mode: the output current can be set to 2 mA source current. The AGC detector is in power-down mode and only the pin diode driver is active.
3. **Voltage and current mode with hand-over**
   a) internal feedback
   data byte AMAGC[3:0] = 1001
   voltage and current mode with hand-over: the Vthr level is programmable in the range 1 V to 2.6 V.
   This mode can be used in combination with both the internal and the external LNA. In combination with the internal AM LNA, the maximum output voltage is limited to 2.7 V.

Figure 7. AM AGC - Voltage and current mode with hand-over



   b) external feedback
   data byte AMAGC[3:0] = 1011
   Voltage and current mode with hand-over: the Vthr level is programmable in the range 0.2 to 2.6 V. The voltage Vthr is the internal reference voltage for the

external feedback to pin GP4/UDS. This mode can only be used with an external LNA.

4. **Calibration mode for voltage output**
   a) internal feedback
   data byte AMAGC[3:0] = 1110
   calibration mode for voltage output (mode 3.a.): the voltage Vthr can be switched directly to the voltage output pin. The reference voltage is programmable in the range described in 3.a.
   b) external feedback
   data byte AMAGC[3:0] = 0010
   calibration mode for external feedback (mode 3.b.): the output voltage is set to a value, that the feedback on GP4(UDS is equal to Vthr. The reference voltage is programmable in the range described in 3.b.

All other possible bit combinations of data byte AMAGC[3:0] are prohibited.

The voltage output can be configured as GPO.

The AMAGC2 output (voltage output) is short-circuit protected by a current limiter. The AMAGC1 output (current output) needs an external resistor. The current output is voltage-tolerant up to VCC, the voltage output up to VDD.

The microcontroller (STA3005 backend) can read the voltage at the AGC capacitor via the serial control interface. On the microcontroller request, the measurement is done by connecting the time constant capacitor to the central ADC (specified in chapter *3.10*); the information can be used to calculate the AGC attenuation.

The AM AGC system is controlled by an average detector.

The AM AGC can be enabled independently in AM and FM mode

Table 12. AM-AGC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
Lthr	Threshold RF level Min. Threshold	Referred to mixer input	-	-	-	-
		AM mixer input	-	89	-	dBµV
		AM filter input	-	94	-	dBµV
	Max Threshold	AM mixer input	-	101.5	-	dBµV
		AM filter input	-	106.5	-	dBµV
-	Threshold steps	4 bit control	0.4	0.9	1.4	dB
-	Absolute threshold error	0.5 to 30.0 MHz @ 25 °C	-1	-	2	dB
-	Total threshold error	0.5 to 30.0 MHz	-2	-	3	dB
-	Absolute threshold error	0.1 to 0.5 MHz @ 25 °C	-0.5	-	3	dB
-	Total threshold error	0.1 to 0.5 MHz	-2	-	3.5	dB
-	Temperature drift of AGC thresholds	-	-	0.011	-	dB/°C
-	Frequency range	Reduced performance	0.05	-	0.1	MHz
-	frequency range	-	0.1	-	30	MHz

Table 12. AM-AGC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
-	Pin diode source current ($I \approx 1.5$ mA * (exp(V_{DD}-V_{AGCTC})-1))	AGC control pin 1 V_{AGCTC} < 1 V external resistor necessary	-	-	-10	mA
-	Min. voltage	AGC control pin	-	-	0.2	V
-	Pin diode source current in constant current mode	-	-	-2	-1	mA
-	Max. voltage	AGC control pin 1	VCC-1.5	VCC-1.3		V
-	Max. source current	AGC control pin 2; voltage output	-	-	-1	mA
-	Min. sink current	AGC control pin 2; voltage output	90	-	-	µA
-	Max. output voltage in analog voltage mode (follower mode)	AGC control pin 2 @ I_{load} = 1 mA	V_{DD}-0.3	-	V_{DD}	V
-	Min. output voltage in analog voltage mode	AGC control pin 2 @ I_{load} = -50 µA	-	-	1	V
$Vthr_{min}$	Vthr_min	-	0.1	0.2	0.3	V
$Vthr_{max}$	Vthr_max	-	2.4	2.6	2.8	V
-	Step size of Vthr	6 bit		40		mV
DNL	Nonlinearity of Vthr	-	-0.5		0.5	LSB
-	TC current for 6 dB control error	Mode T1 Mode T2 Mode T3	2.5 12 60	4 20 100	6.5 32 160	µA
-	I attack in fast attack mode @ 10 dB control error	Active if control deviation is more than 7 dB	0.9	1.7	2.3	mA
-	Typical AGC time constant(1)	C_{AGCTC} = 1µF, mode T2 AGC conductance versus V_{AGCTC}= 20 dB/V	-	15	-	ms

1. The time constant is defined as the 1τ value, means when the AGC is settled to 63% after a 6dB step

3.6 IF - Section

3.6.1 IF-Amplifier

Table 13. IF-Amplifier with anti aliasing filter and ADC buffer electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
Gain	Min. programmable gain Max programmable gain	Input 1-3 (FM,HD,AM) Input 4 (HD-Radio AM) Input 1-3 (FM,HD,AM) Input 4 (HD-Radio AM)	-	23 16 37 30	-	dB
Gstep	Gain step	3 bit control	1	2	3	dB
Gmin	Minimum gain of IF-Amplifier in AGC mode Input 1-3 Input 4	Full AGC reaction V_{TCIF} < 1V	14 7	17 10	19 12	dB
Gerr	Gain error	@ 10.7 MHz, AAfilt<1:0> =10	-2	-	2	dB
		with AAfilt<1:0> = 00	-4	-	2	dB
f_{cut}	Cut off frequency without calibration	-3 dB without calibration	10	15	21	MHz
f_{cut_cal}	Cut off frequency after calibration	-3 dB with calibration	13	15	17	MHz
-	Stop band attenuation with calibration	@ 26.35 MHz @ 47.75 MHz	15 30	-	-	dB
-	Pass band ripple	@ 400kHz bandwidth	-	-	0.5	dB
Rin_input1	Input impedance input 1	FM –input	265	330	400	Ω
Rin_input2	Input impedance input 2	HD-Radio FM input	5.5	10	18	kΩ
Rin_input3	Input impedance input 3	AM input	5.5	10	18	kΩ
Rin_input4	Input impedance input 4	HD-Radio AM input	11	20	34	kΩ
Vout_max	Max. output voltage	R_L ≥180 Ω	117	-	-	dBµV
IIP3(1)	3rd order intercept point	Input stage 1-3 Input stage 4	120 128	125 132	-	dBµV
OIP3(1)	3rd order intercept point	Up to 116 dBµV output voltage, without AGC attenuation, R_L ≥180 Ω	142	145	-	dBµV
IIP2(1)	2nd order intercept point	Input stage 1-3 input stage 4	147 157	-	-	dBµV
Vnoise_input 1(1)	Input noise voltage @ 330 Ω input	@ source impedance 330 Ω noiseless, @31 dB gain	-	3.5	4.2	nV/√ Hz
Vnoise_input 2(1)	Input noise voltage @ 3.3 kΩ input	@ source impedance 470 Ω noiseless, @ 31 dB gain	-	3.8	4.6	nV/√ Hz

Table 13. IF-Amplifier with anti aliasing filter and ADC buffer electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
Vnoise_input 3(1)	Input noise voltage @ 10 kΩ input	@ source impedance 2.2 kΩ noiseless, @31 dB gain, with external 2.7 kΩ input termination resistor	-	5	6	nV/√ Hz
Vnoise_input 4(1)	Input noise voltage @ 10kW input	@ source impedance 2.2 kΩ noiseless, @ 24 dB gain, with external 2.7 kΩ input termination resistor	-	7.5	8.5	nV/√ Hz
Iout,max	Max. output current	With resistive load	4	-	-	mA
Zout	Output impedance	-	-	20	40	Ω
-	Isolation between different IF input ports(1)	@ Input impedance 2.5kΩ	30	-	-	dB

1. Parameter not guaranteed by production test

3.6.2 IF-AGC

The IF AGC system is controlled in AM with an average detector and in FM with a peak detector.

The time constant is defined with two external capacitors and programmable internal currents (details given in the table below).

The microcontroller can read the voltage at the AGC capacitor via the serial control interface. On request of the microcontroller the measurement is done by applying the time constant capacitor voltage to the central ADC (specified in chapter *3.10*) and gives information to calculate the AGC-attenuation.

Table 14. IF-AGC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
Lthr	AGC threshold IF level	Referred to differential output of ADC buffer	-	-	-	-
	Min. AGC threshold	FM	-	105	-	dBµV
		AM	-	99	-	dBµV
	Max AGC threshold	FM, Max. recommended AGC threshold 115 dBµV	-	119	-	dBµV
		AM, Max. recommended AGC threshold 109 dBµV	-	113	-	dBµV
-	Threshold steps	3 bit	1.5	2	2.5	dB
-	Absolute threshold error	10.7 MHz @ 25 °C (up to 117 dBµV output voltage)	-1	-	1	dB
-	Total threshold error	10.7 MHz (up to 117dB µV output voltage)	-2.5	-	2.5	dB
-	Temp drift of AGC threshold	FM-mode AM mode	-	0.008 0.0		dB/°C
-	IF gain deviation	Remaining gain control error	-	-	1	dB
-	Fast attack mode in AM-mode	Active if control deviation is more than 7dB	0.3	0.5	1	ms
-	Time constant in AM mode(1) symmetric behavior (attack = decay)	With external 2.2 µF capacitor, IF gain = 31 dB input 1-3; 24 dB input4 mode S1 (slow) mode S2 (fast)	 55 5.5	 110 11	 220 22	 ms ms
-	Time constant in FM mode(2) asymmetric behavior	With external 220 nF capacitor, IF gain = 31 dB input1-3; 24 dB input4 decay mode U1 / U2 attack mode U1 (slow) attack mode U2 (fast)	 7 150 30	 15 300 60	 32 600 120	 ms µs µs

1. The AGC time constant for AM is the 1τ value, means when the AGC is settled to 63% after a 6dB step
2. The AGC time constant for FM is the time needed to settle the AGC to 90% for a 6dB level step

3.6.3 IF buffer amplifier

The IF buffer amplifier is a programmable, single ended amplifier. The input for the IF buffer amplifier can be selected by software between IFin1 and IFin2. The output of the amplifier is multiplexed with GPIO5

Table 15. IF buffer amplifier electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
Gmin	Min. gain	Series resistance 220 Ω, terminated with 330 Ω	-	-11	-	dB
Gmax	Max. gain	Series resistance 220 Ω, terminated with 330 Ω	-	3	-	dB
Gstep	Gain step	3bit	-	2	-	dB
-	Absolute gain error	-	-3		3	dB
-	Relative gain error	Step by step	-1.5		1.5	dB
vnoise(1)	Input noise voltage	@ 10.7 MHz, 3 dB gain	-	8.5	15	nV/√ Hz
IIP3(1)	3rd order intercept point	@ gain 3 dB,Vout=1 Vpp with 500 Ω ≤ R_L ≤ 600 Ω	115	120	-	dBµV
-	3 dB bandwidth	-	-	50	-	MHz
-	Output DC voltage	-	1.6	-	2.1	V
-	External output load	-	400	550	1000	Ω
-	Output impedance	-	80	140	250	Ω

1. Parameter not guaranteed by production test

3.7 Phase Locked Loop

Table 16. Phase Locked Loop electrical characteristics

Parameter	Test condition	Min.	Typ	Max	Units
Settling time FM(1)	Δf < 0.01 % @ f_{PFD} = 300 kHz fractional mode, with loop filter according application schematic @ f_{PFD} = 100 kHz integer mode	-	 300	500 500	µs
	VCC = 4.6 – 4.7V, f_{PFD} = 300kHz, loop filter according application schematic f_{PFD} = 100 kHz	-	300 500	600 600	µs
Spurious suppression	Suppression of spurious with compensation DAC low current charge pump 50 µA ≤ Icp ≤ 750 µA	5	20	-	dB

1. Parameter not guaranteed by production test, depends on loop filter circuitry and CP current settings. For further information see application note information

3.7.1 VCO

Table 17. VCO electrical characteristics

Symbol	Parameter	Test condition, comments	Min.	Typ	Max	Units
f_{osc}	Frequency range VCO1	Tuning range, incl. switch between upper and lower range 0.2 V ≤ V_{tune} ≤ 4.2 V	4480	-	4970	MHz
	Frequency range VCO2	Tuning range, incl. switch between upper and lower range 0.2 V ≤ V_{tune} ≤ 4.2 V	3430	-	4010	MHz
-	Phase Noise of LO	At any LO frequency between 55.1 MHz and 118.7 MHz, VCO free running, NV=8 (VCO2), NV=10 (VCO1) @ 10 Hz @ 100 Hz @ 1 kHz @ 10 kHz @ 100 kHz	-	-40 -60 -86 -106 -126	-	dBc Hz
-	Phase Noise of LO min. requirements for AM,DRM	At any LO frequency between 10.7 MHz and 40.0 MHz VCO free running NV=25 (VCO2), NV=30 (VCO1) @ 1 Hz @ 10 Hz @ 100 Hz @ 1 kHz @ 10 kHz @ 100 kHz	-	-33 -40 -80 -90 -100 -120	-	dBc Hz
-	Deviation error(1)	FM reception, deem phase 50µs, f_{NF}=20 Hz to 20 kHz @ min. VCO frequency NV=8 (VCO2), NV=10 (VCO1) f_{PFD}=300 kHz(2), loop filter according application schematic f_{PFD}=1.9 MHz(3)	-	8	8	Hz
-	KVCOmax/KVCOmin	For tuning voltage range 0.2 V – 4.2 V	-	5	7	-
PSRR(1)	Power supply ripple rejection ratio	-	20	-	-	dB
V_{VCO_OUT}(1)	VCO signal emission	@ tuning voltage input, 1 kΩ load	-	-	60	dBµV

1. Parameter not guaranteed by production test
2. Adaptation of low current CP values needed
3. With appropriate loop filter circuit

3.7.2 Reference oscillator / reference frequency input buffer

Table 18. Reference oscillator / reference frequency input buffer electrical characteristics

Parameter	Test condition, comments	Min.	Typ	Max	Units
Reference oscillator mode – fundamental crystal					
Oscillation frequency	Fundamental mode	-	74.1	-	MHz
Phase noise	@ 1 Hz @ 10 Hz @ 100 Hz @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz	-	-20 -50 -80 -110 -130 < -130 < -130	-	dBc dBc dBc dBc dBc dBc dBc
Frequency stability	Degradation generated by the oscillator	-20	-	20	ppm
Single ended input					
Input frequency	-	-	-	75	MHz
Input voltage range	Single ended mode	200	-	1000	mV_{PP}
Input impedance	Single ended mode	10	-	-	kΩ
Reference frequency input buffer mode					
reference input frequency	differential input	0.1	-	150	MHz
max input voltage high	-	-	-	1475	mV
min. input voltage low	-	925	-	-	mV
Input differential voltage	-	247	-	454	mV
Input offset voltage	-	1125	-	1275	mV
input impedance	-	150	-	-	kΩ

3.7.3 Divider

The mixer divider V is followed by a division-by-4-stage that generates 0°/90°/-90° LO signals for the IMR mixer (90°/-90° mode to switch between upper or lower sideband suppression in the IMR).

The main divider N can be operated in integer mode or in fractional mode. Three fraction factors are programmable: 2, 3 and 6. A fractional compensation circuit is located at the charge pump. The compensation acts for the low current only.

Table 19. Divider electrical characteristics

Symbol	Parameter	Test condition, comments	Min.	Typ	Max	Units
Mixer divider V – integer values						
N_V	Divider value divider_V	7 bit	5	-	131	-
Main divider N – fractional 2, 3 and 6 / integer divider						
N_N	Divider value divider_N	22bit (32/33 pre scaler)	1024	-	4194304	-
Reference divider R – integer values						
N_R	Divider value divider_R	16 bit	1	-	65535	-

3.7.4 Phase frequency detector and charge pump

Table 20. Phase frequency detector and charge pump electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
PFD						
f_{PFD}	PFD input frequency	-	2	-	3000	kHz
Charge pump						
I_{sink}	Sink current fractional compensation only for low current modes (bit 5 – bit 8)	High current mode bit1 high current mode bit2 High current mode bit3 High current mode bit4 Low current mode bit1 Low current mode bit2 Low current mode bit3 Low current mode bit4 Low current mode bit5	-	-0.65 -1,3 -2,5 -4,6 -65 -130 -260 -520 -980	-	mA mA mA mA µA µA µA µA µA
I_{source}	Source current fractional compensation only for low current modes (bit 5 – bit 8)	High current mode bit1 high current mode bit2 High current mode bit3 High current mode bit4 low current mode bit1 Low current mode bit2 Low current mode bit3 Low current mode bit4 Low current mode bit5	-	0.65 1.3 2.5 4.6 65 130 260 520 980	-	mA mA mA mA µA µA µA µA µA
-	Current error	-	-	-	±30	%
V_{OH}	Output voltage high	-	V_{CC}-0.3	-	V_{CC}	V
V_{OL}	Output voltage low	-	-0.05	-	0.15	V

3.8 Temperature sensor

Table 21. Temperature sensor electrical characteristics

Parameter	Test condition	Min.	Typ	Max	Units
Temperature range	-	-40	-	150	°C
Resolution (1)	°C / LSB (no direct measurement possible)	4.5	5.1	5.7	°C
Absolute error	-	-	-	±15	°C
Relative error	No direct measurement possible	-	0.5	-	LSB

1. Not guaranteed by production test

3.9 D/A-converter

The TDA7528 contains two D/A-Converters for tuning the filters of the FM pre-stage. The converter 1 has a resolution of 8 bit; converter 2 has a resolution of 9 bit.

Table 22. D/A-converter electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ	Max	Units
V_{out}	Output voltage minimum voltage	Unloaded output	-	0.6	0.8	V
	Maximum voltage	-	V_{CC}-0.15	V_{CC}-0.1	-	
-	Output impedance	-	-	2	-	kΩ
-	Max. output current	-	400	-	-	µA
-	Average voltage step converter 1	Resolution 8 bit	-	18	-	mV
-	Average voltage step converter 2	Resolution 9 bit	-	9	-	mV
-	Additional error vs. temperature	-	-2	-	2	LSB
-	INL	-	-2	-	2	LSB
-	DNL	-	-0.5	-	0.5	LSB
-	Output noise	@ C_L=1nF and 2.2kΩ	-	100	200	µV
-	Conversion time	@ C_L=1nF	-	20	40	µs
VSRR	Supply voltage ripple rejection ratio	@ 1kHz	20	-	-	dB

3.10 A/D-converter

The TDA7528 contains a 6bit SAR A/D-Converter for sensing several analog values of the tuner. The following analog sources can be switched to the ADC input by software command:

- Temperature sensor
- TCFM
- TCAM
- TCIF1/2 (depends on which one is active)
- VCO tuning voltage (=3/5 * Vtune)
- GP1
- GP2
- Internal VCC divider (2/5 * VCC)

The ADC is clocked by an integrated RC-oscillator, or the PLL reference frequency.

Table 23. A/D-converter

Symbol	Parameter	Test condition, comments	Min.	Typ	Max	Units
-	INL	Referred to internal VDD	-2	-	2	LSB
-	DNL	-	-0.5	-	0.5	LSB
-	Input voltage range	-	0	-	V_{DD}	V
f_{Osc}	Oscillation frequency 2bit programmable	RCfreq<1:0> = 00 RCfreq<1:0> = 01 RCfreq<1:0> = 10 RCfreq<1:0> = 11	 1.72	0.68 1.31 1.9 2.5	-	MHz MHz MHz MHz
-	frequency error	-	-	-	±40	%
t_{ADC}	Conversion time(1)	12 clock cycles	-	-	7	µs

1. With RC-oscillator frequency = 2.5MHz

3.11 GPIO - general purpose I/O interface pins

The TDA7528 has eight GPIO - general purpose - control pins (GP1...GP8) to switch external stages (output), e.g amplifiers, or to read the status of external stages (input), e.g. control voltages. Some control pins are multiplexed with other functions that are not necessary in every tuner design.

Table 24. GPIO - general purpose I/O interface pins electrical characteristics

Pin name	GPIO functionality						Multiplexed functionality details are given in the corresponding chapters
	GPIO-output				GPIO-input		
	High level		Low level		Functionality	voltage	
	voltage	Source current	voltage	Sink current			
GP1	3,3V	1 mA	0V	1 mA	Analog input A/D-converter	0 ... 3,3V	
GP2	3,3V	1 mA	0V	1 mA	Analog input A/D-converter	0 ... 3,3V	AMAGC 2nd TC input
GP3	3.3V	0.1 mA	0V	10 mA	-	-	FM key AGC input
GP4	3.3V	0.1 mA	0V	10 mA	-	-	AM cascode U_{DS} input
GP5	3,3V	1 mA	0V	1 mA	Digital Input	0 / 3,3V	IF buffer output
GP6	3,3V	1 mA	0V	1 mA	Digital Input	0 / 3,3V	SPI MISO output
GP7	3,3V	1 mA	0V	1 mA	-	-	FM-AGC voltage output
GP8	3,3V	1 mA	0V	1 mA	-	-	AM-AGC voltage output

Table 25. GPIO test conditions

Parameter	Test condition	Min.	Typ	Max	Units
High level output voltage	@ 100kΩ load to GND	V_{DD}-0.3	-	V_{DD}	V
Low level output voltage	@ 100kΩ load to V_{DD}	-0.05	-	0.3	V
High level source current	GP1 / GP2 / GP5 … GP8: @ 1kΩ load to GND	0.5	1	-	mA
High level source current	GP3 / GP4 @ 1kΩ load to GND	0.08	0.25	-	mA
Low level sink current	GP1 / GP2 / GP5 … GP8: @ 1kΩ load to V_{DD}	0.8	1.5	-	mA
Low level sink current	GP3 / GP4: @ 100Ω load to V_{DD}	8.0	10	-	mA
Input impedance	digital input mode	100	-		kΩ
Input voltage range	GP1 / GP2	0	-	3.5	V
High level input voltage	GP5 / GP6 used as digital input	2.2	-	3.5	V
Low level input voltage	GP5 / GP6 used as digital input	-0.05	-	1.0	V

3.11.1 Serial data interface

The TDA7528 features a serial data port for communication with the microcontroller. It is used to program the TDA7528 and to convey the read-out values of its detectors. This port supports data communication using the SPI and the I^2C protocols.

Pin configuration of the serial data interface:

Table 26. Pin configuration of the serial data interface

Signal #	Pin	SPI signal	Pin	I^2C signal
Signal 1	PS	Protocol Select SPI/I^2C	PS	Protocol Select SPI/I^2C
Signal 2	CS	Chip Select	AS	Address Select
Signal 3	CLK	Clock	CLK	Clock
Signal 4	MOSI	Master Out – Slave In	DATA	bidirectional Data
Signal 5	MISO	Master In – Slave Out	GP6	General Purpose Out

The "PS"-pin (Protocol Select) determines which communication protocol is used for communication between the microcontroller and the TDA7528. The information is not latched, so any level change at this pin immediately affects the protocol used by the TDA7528.[(a)]

3.11.2 Communication using the I^2C protocol

For I^2C communication, pin "PS" needs to be open. Pin "AS" (Address Select) determines which I^2C address or group of addresses (see below) is used for communication between the microcontroller and TDA7528. Three different external connections are defined to represent three groups of addresses. The information is not latched, so any level change at this pin immediately affects the address used by the TDA7528.[(b)]

a. Protocol changes are not permitted during a communication sequence unless the I^2C STOP condition is established or in SPI mode the CS line is deactivated, because the consequences are not predictable. Usually there is no need for any protocol change during operation, so the PS pin is connected to either GND or left open

b. Address changes are not permitted during an I^2C communication sequence unless the I^2C STOP condition is established, because the consequences are not predictable. Usually there is no need for any address change during operation, so the AS pin is connected to either GND, an 20k pull down resistor or left open.

I²C addresses

Table 27. I²C addresses

Tuner:	Tuner 3	Tuner 2	Tuner 1
”AS”-pin connection	open	20k +/- 50% pull down	GND
address:	1100 1xxd	1100 x1xd	1100 xx1d
MSB ... LSB	-	-	-
1100 000d	-	-	-
1100 001d	-	-	R / W
1100 010d	-	R / W	-
1100 011d	-	W	W
1100 100d	R / W	-	-
1100 101d	W	-	W
1100 110d	W	W	-
1100 111d	W	W	W

x = must be "0" for reading, can be "1" or "0" for writing to the TDA7528

d = determinates the direction of data transfer, reading or writing

R / W = indicates the address to write to and/or to read from a TDA7528

W = indicates those addresses that can be used to transmit equal data to several TDA7528s, e.g. to program an synchronous AF jump of two tuners. A read out has no purpose for these addresses.

3.11.3 Communication using the SPI protocol

For SPI communication, pin "PS" needs to be connected to GND.

No IC address is transmitted in SPI mode, as in this mode the chip is selected through its CS (Chip Select) line.

SPI-Protocol: CPOL=1, CPHA=1

Table 28. Communication using the SPI protocol electrical characteristics

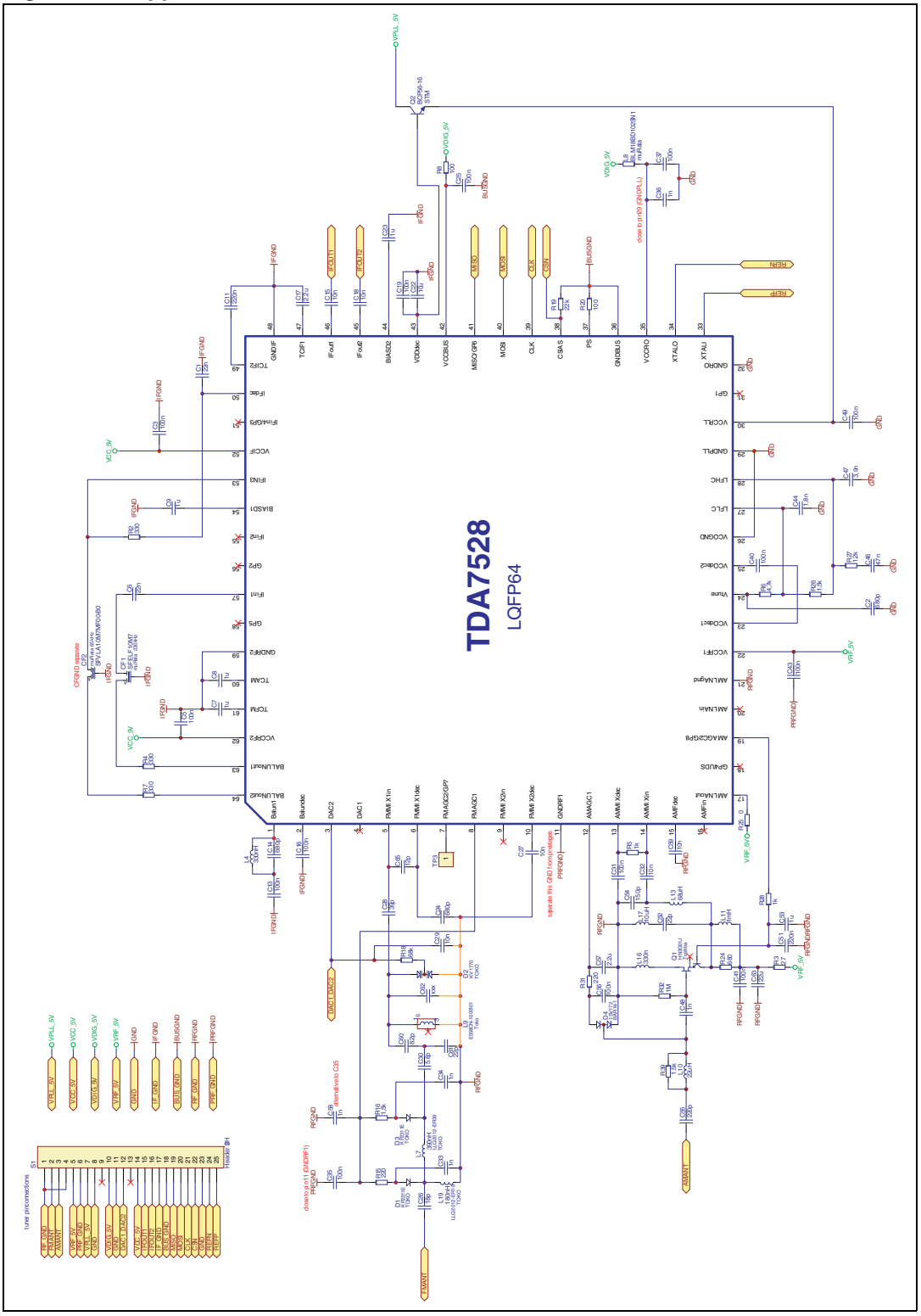
Parameter	Test condition	Min.	Typ	Max	Units
Clock frequency	Guaranteed range @ SPI Guaranteed range @ I²C	4 1	-	-	MHz MHz
Inter byte time	-	-	-	0	
Power-on delay time	Ready for communication after power-on reset	-	-	10	ms
High level output voltage	Output signals	V_{DD}-0.3	-	V_{DD}	V
Low level output voltage	Output signals	-0.05	-	0.3	V
High level source current	Output signals	-	0.1	-	mA
low level sink current	Output signals	-	1	-	mA
High level input voltage	Input signals, except AS	2.3	-	3.5	V
Low level input voltage	Input signals, except AS	-0.05	-	1.0	V
Internal pull up resistor	AS pin	16.5	20	24	kΩ
Internal pull up resistor	PS pin	16.5	20	24	kΩ

Table 28. Communication using the SPI protocol electrical characteristics

Parameter	Test condition	Min.	Typ	Max	Units
Input impedance	Input signals, except AS,PS	100	-	-	kΩ
Power-on impedance	All signals, except AS, PS	100	-	-	kΩ

4 Application information

Figure 8. Application information



5 Programming information

5.1 Address organization

Figure 9. Address organization

Name	No	r/w	MSB	6	5	4	3	2	1	LSB
Short reg	**0**	r/w	x	PWRSTABLEw	ShAGC	ShPLL	ADCstart	ADCen	GPIOen	PWR
ADCctrl	1	r/w	ADCclk	ADCs2	ADCs1	ADCs0		RCenable	ADCautomode	Temp_pwr
GPIOmode	2	r/w	GPO8	GPO7	GPIO6	GPIO5	GPO4	GPO3	GPIO2	GPIO1
AGCmixCtrl	3	r/w		KeyAGCen	FMAGCpwr	AMAGCpwr			Mixout1	Mixout2
Supply	4	r/w	refmode1	refmode0	DivRen	VCCmon_adj1	VCCmon_adj0	En_VCCmon	VDD_korr	VDD_int_ext
DivR1	5	r/w	divr15	divr14	divr13	divr12	divr11	divr10	divr9	divr8
IFAGC	6	r/w	IFAGC_FM_AM	IFAGCthr2	IFAGCthr1	IFAGCthr0				IFsection_pwr
FMAGC	7	r/w	FMthr3	FMthr2	FMthr1	FMthr0	FMAGCmodeC1	FMAGCmodeC0	FMAGCmodeV1	FMAGCmodeV0
FM_AM_Vthr	8	r/w	AMAGCfat	AM2nd_order	Vthr5	Vthr4	Vthr3	Vthr2	Vthr1	Vthr0
MIXalign1	9	r/w	AAfilt1	AAfilt0			Mix_ctrl	IMRF2	IMRF1	IMRF0
MIXalign2	10	r/w	IMRph3	IMRph2	IMRph1	IMRph0	IMRG3	IMRG2	IMRG1	IMRG0
PLLctrl	11	r/w	DZ2	DZ1	DS2	DS1	VCOext	PLLtest2	PLLtest	PLLpwr
PLLctrl2	12	r/w	CompDAC3	CompDAC2	CompDAC1	CompDAC0	CompDACtest2	CompDACtest1	CompDACtest0	CompDACdisable
PLLtest	13	r/w	POL	PFD_D1	PFD_D0	PLLT4	PLLT3	PLLT2	PLLT1	PLLT0
Misc1	14	r/w	AGCtest1	AGCtest0	BalunoutIMP	Ired_Balun	IredH	IredL	VCOMag1	VCOMag0
Misc2	15	r/w	IFbufG2	IFbufG1	IFbufG0	IFbufin	IFbufPWR	RC_test	RCfreq_1	RCfreq_0
AGCtc_A	16	r/w	IFAGCtcAM	IFAGCtcFM	AMtc1	AMtc0	FMtc3	FMtc2	FMtc1	FMtc0
AMAGC_A	17	r/w	AMthr3	AMthr2	AMthr1	AMthr0	AMAGCmodeC1	AMAGCmodeC0	AMAGCmodeV1	AMAGCmodeV0
GPIOm_A	18	r/w	GPO8hl	GPO7hl	GPIO6hl	GPIO5hl	GPO4hl	GPO3hl	GPIO2hl	GPIO1hl
IFCTRL_A	19	r/w	IFin0_Std_IBOC	IFAmpgainA2	IFAmpgainA1	IFAmpgainA0	MixinFM	MixinAM_LPF	MixinFMAM	IFin1_AM_FM
DivV_A	20	r/w	VCO1r	divVA6	divVA6	divVA6	divVA6	divVA6	divVA6	divVA0
DivN_A1	21	r/w	divnA20	divnA19	divnA18	divnA17	divnA16	divnA15	divnA14	divnA13
DivN_A2	22	r/w	divnA12	divnA11	divnA10	divnA9	divnA8	divnA7	divnA6	divnA5
DivN_A3	23	r/w	divnA4	divnA3	divnA2	divnA1	divnA0	fracA2	fracA1	fracA0
DivR2_A	24	r/w	divr7	divr6	divr5	divr4	divr3	divr2	divr1	divr0
CPcur_A	25	r/w	CPAh3	CPAh2	CPAh1	CPAl4	CPAl3	CPAl2	CPAl1	CPAl0
DAC1_A	26	r/w	DAC1A8	DAC1A7	DAC1A6	DAC1A5	DAC1A4	DAC1A3	DAC1A2	DAC1A1
DAC2_A	27	r/w	DAC2A8	DAC2A7	DAC2A6	DAC2A5	DAC2A4	DAC2A3	DAC2A2	DAC2A1
PLL_DAC_A	28	r/w	IQselA	VCOsw	CPctrl1	CPctrl0	DAC2A0		DAC2off	DAC1off
AMFilt_A	29	r/w	AMfiltA7	AMfiltA6	AMfiltA5	AMfiltA4	AMfiltA3	AmfiltA2	AMfiltA1	AMfiltA0
Misc3_A	30	r/w					DIVVtest	divnA21	CPAh0	AMLNApwrA
ADCtest_A	31	r/w	IF test	ADC test	ADCDAC5	ADCDAC4	ADCDAC3	ADCDAC2	ADCDAC1	ADCDAC0
AGCtc_B	32	r/w	this byte is valid on the output if bit SHAGC is set to '1', otherwise byte Nr. 16 is valid on the output							
AMAGC_B	33	r/w	all bytes from 33 to 47 are valid on the output if SHPLL is set to '1', otherwise byte 17 to 31 are valid on the output							
GPIOm_B	34	r/w								
IFCTRL_B	35	r/w								
DivV_B	36	r/w								
DivN_B1	37	r/w								
DivN_B2	38	r/w								
DivN_B3	39	r/w								
DivR2_B	40	r/w								
CPcur_B	41	r/w								
DAC1_B	42	r/w								
DAC2_B	43	r/w								
PLL_DAC_B	44	r/w								
AMFilt_B	45	r/w								
Misc3_B	46	r/w								
ADCtest_B	47	r/w								
READ_Status	48	r			GPIO6r	GPIO5r	PWR_stable	MaskSet0	MaskSet1	MaskSet2
READ_ADC	49	r		ADCok	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Shadow-register

initialization registers, to be changed after power on
depends on reception band (FM / MW / SW / ...)
to be changed with each frequency change
additional controls, changed indipendent from reception
IF buffer control
test registers, not to be changed at all

Note: The power on value of all registers is zero.

5.2 Data byte specification

5.2.1 Short_reg (0)

Table 29. Short_reg (0)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**Global PWR** Power down the IC Power on the IC
-	-	-	-	-	-	0 1	-	**GPIO enable** all GPIO in tristate all GPIO enable
-	-	-	-	-	0 1	-	-	**ADCen** 6bit ADC on 6bit ADC off
-	-	-	-	0 1	-	-	-	**ADCstart** N/A Starts a single AD conversion
-	-	-	0 1	-	-	-	-	**ShPLL** PLL register from 17 to 31 are valid PLL register from 33 to 47 are valid
-	-	0 1	-	-	-	-	-	**ShAGC** AGC TC register 16 is valid AGC TC register 32 is valid
-	0 1	-	-	-	-	-	-	**Power stable** N/A sets the power stable read bit
0	-	-	-	-	-	-	-	**Has to be 0**

5.2.2 ADCctrl (1)

Table 30. ADCctrl (1)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**Temperature sensor power** Enabled Disabled
-	-	-	-	-	-	0 1	-	**ADC auto mode** automatic restart disable automatic restart enable
-	-	-	-	-	0 1	-	-	**RC oscillator enable** enable disable
-	-	-	-	X	-	-	-	**ADCstart (like bit 0.3)**
-	0 1 0 1 0 1 0 1	0 0 1 1 0 0 1 1	0 0 0 0 1 1 1 1	-	-	-	-	**ADC input selection** Temp sensor FM AGC AM AGC IF AGC VCO tuning voltage (3/5 * Vtune) GP1 GP2 2/5 * VCC
0 1	-	-	-	-	-	-	-	**ADC clock selection** ADC clock source = RC osc ADC clock source = refdiv output

5.2.3 GPIO mode (2)

Table 31. GPIO mode (2)

MSB							LSB	GPIO function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**GPIO1 input / output** Analog input to AD converter digital output
-	-	-	-	-	-	0 1	-	**GPIO2 input / output** Analog input to AD converter Digital output
-	-	-	-	-	0 1	-	-	**GPIO3 input / output** Analog Input Digital output
-	-	-	-	0 1	-	-	-	**GPIO4 input / output** Analog Input Digital output
-	-	-	0 1	-	-	-	-	**GPIO5 input / output** Digital input if IF buffer amplifier = OFF, analog output if IF buffer amplifier = ON Digital output
-	-	0 1	-	-	-	-	-	**GPIO6 input / output** Digital input (or MISO output in SPI mode) Digital output (or MISO output in SPI mode)
-	0 1	-	-	-	-	-	-	**GPIO7 input / output** Digital output FM AGC voltage output
0 1	-	-	-	-	-	-	-	**GPIO8 input / output** Digital output AM AGC voltage output

5.2.4 AGC and mixer control (3)

Table 32. AGC and mixer control (3)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	0 0 1 1	0 1 0 1	**Mixout 1 / 2** All Off = power down mixer section Mixout 2 active Mixout 1 active Forbidden state
-	-	-	-	0	0	-	-	**Has to be 0**
-	-	-	0 1	-	-	-	-	**AM AGC On / Off** Off On
-	-	0 1	-	-	-	-	-	**FM AGC On / Off** Off On
-	0 1	-	-	-	-	-	-	**Keyed AGC enable** Keyed AGC off keyed AGC on
0		-	-	-	-	-	-	**Has to be 0**

5.2.5 Supply control (4)

Table 33. Supply control (4)

MSB							LSB	Divider R value
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**VDD regulator connection intern / extern** external VDD source for VDDPLL is used VDDPLL is derived from onboard NPN transistor
-	-	-	-	-	-	0 1	-	**VDD regulator voltage correction** internal VDD 150mV lower internal VDD corrected if external source used
-	-	-	-	-	0 1	-	-	**Enable low voltage detection on VCC** VCC low voltage detection off VCC low voltage detection on
-	-	-	0 0 1 1	0 1 0 1	-	-	-	**Threshold of low voltage detection** 4.3V 4.4V 4.5V 4.6V
-	-	0 1	-	-	-	-	-	**Divider R enable** Divider R off; => DivR value = 1 Divider R on
0 0 1 1	0 1 0 1	-	-	-	-	-	-	**Reference oscillator mode** off single ended mode differential LVDS input controlled XO-mode

5.2.6 Divider R MSB (5)

Table 34. Divider R MSB (5)

MSB							LSB	Divider R value
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
X	-	-	-	-	-	-	X	**Divider R value** DivR8 : : DivR15

5.2.7 IF AGC control (6)

Table 35. IF AGC control (6)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**IF section On / Off** Off On
-	-	-	-	0	0	0	-	Has to be 0
-	0 0 : : 1	0 0 : : 1	0 1 : : 1	-	-	-	-	**IF AGC threshold** IF output level = 99dBµV(AM) / 105dBµV (FM) IF output level = 101dBµV(AM) / 107dBµV (FM) : : IF output level = 113dBµV(AM) / 119dBµV (FM)
0 1	-	-	-	-	-	-	-	**IF AGC mode FM / AM selection** FM mode AM mode

5.2.8 FM AGC (7)

Table 36. FM AGC (7)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	0 1 1 0 1 0	0 0 1 1 0 0	0 0 0 0 1 1	0 0 0 0 1 0	**AGC output mode** Off positive current output (mode 1) pos / neg current output (mode 2) constant 2mA current output (mode 3) voltage and current output with hand over (mode 4) calibration mode for voltage output (mode 5)
0 0 : : 0 1 1 : : 1	0 0 : : 1 0 0 : : 1	0 0 : : 1 0 0 : : 1	0 1 : : 1 0 1 : : 1	-	-	-	-	**FM AGC threshold** mixer input level = 93dBµV (FM1) / 99dBµV (FM2) Mixer input level = 94dBµV (FM1) / 100dBµV (FM2) : : Mixer input level = 100dBµV (FM1)/ 106dBµV (FM2) Mixer input level = 93dBµV (FM1)/ 99dBµV (FM2) Mixer input level = 92dBµV (FM1)/ 98dBµV (FM2) : : Mixer input level = 86dBµV (FM1)/ 92dBµV (FM2)

5.2.9 AGC voltage threshold (8)

Table 37. AGC voltage threshold (8)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-							**Transfer voltage from voltage out to current out**
		0	0	0	0	0	0	200mV
		0	0	0	0	0	1	237.5mV
		:	:	:	:	:	:	:
		:	:	:	:	:	:	:
		1	1	1	1	1	0	2.5625V
		1	1	1	1	1	1	2.6V
-	0	-	-	-	-	-	-	**AMAGC 2nd order lowpass**
	1							AMAGC voltage is derived from TCAM
								AMAGC voltage is derived from GP2 (for 2nd order lowpass function)
0	-	-	-	-	-	-	-	**AM fast attack**
1								Off
								On

5.2.10 Mixer alignment 1 (9)

Table 38. Mixer alignment 1 (9)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-				**IQ-filter frequency adjust**
					0	0	0	+2.4MHz
					0	0	1	+1.8MHz
					:	:	:	:
					1	0	0	0
					:	:	:	:
					1	1	1	-1.8MHz
-	-	-	-	0	-	-	-	**Only for test, has to be ‘0’**
-	-	0	0	-	-	-	-	**Has to be 0**
								AA filter frequency adjust
1	0	-	-	-	-	-	-	20.00 MHz
0	0							14.75 MHz
0	1							10.87 MHz

5.2.11 Mixer alignment 2 (10)

Table 39. Mixer alignment 2 (10)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								IQ-filter gain adjust
				0	1	1	1	-0.7dB
				0	1	1	0	-0.6dB
				0	1	0	1	-0.5dB
-	-	-	-	:	:	:	:	:
				0	0	0	0	0dB
				1	0	0	0	0dB
				:	:	:	:	:
				1	1	1	0	+0.6dB
				1	1	1	1	+0.7dB
								IQ-filter phase adjust
0	0	0	0					0
0	0	0	1					+0.2 deg
0	0	1	0					+0.2 deg
0	0	1	1					+0.4 deg
0	1	0	0					+0.6 deg
:	:	:	:					:
0	1	1	1	-	-	-	-	+1.2 deg
1	0	0	0					-1.2 deg
1	0	0	1					-1.0 deg
1	0	1	0					-1.0 deg
1	0	1	1					-0.8 deg
1	1	0	0					-0.6 deg
:	:	:	:					:
1	1	1	0					-0.2 deg
1	1	1	1					0

5.2.12 PLL control 1 (11)

Table 40. PLL control 1 (11)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**PLL enable** PLL Off PLL On
-	-	-	-	0	0	0	-	**Only for test, has to be 0**
-	-	0 : 1 0	0 : 1 1	-	-	-	-	**Delay of high current CP** longest : shortest default for optimum PLL performance
0 : 1 0	0 : 1 1	-	-	-	-	-	-	**Slope of high current CP** slowest : fastest default for optimum PLL performance

5.2.13 PLL control 2 (12)

Table 41. PLL control 2 (12)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**Compensation DAC disable** compensation DAC on (use in fractional mode) compensation DAC off (use in integer mode)
-	-	-	-	0	0	0		**Only for test, has to be '0'**
0 1 0 1 0 : 1 0 1 0 1 : 1 **1**	0 0 1 1 0 : 1 0 0 1 1 : 1 **0**	0 0 0 0 1 : 1 0 0 0 0 : 1 **0**	0 0 0 0 0 : 0 1 1 1 1 : 1 **1**	-	-	-	-	**Current trimming of compensation DAC** compensation current -44% compensation current -37.5 % compensation current -31.25% compensation current -25% compensation current -18.7% : default current +/-0% compensation current +6.25% compensation current +12.5% compensation current +18.75% compensation current +25% : compensation current +50% **optimum value**

5.2.14 PLL test (13)

Table 42. PLL test (13)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	1	0	1	**PLL test** PLL in standard operation mode
-	-	-	0	0	-	-	-	**Only for test, has to be 0**
-	0	1	-	-	-	-	-	**PFD** Default delay settings
0	-	-	-	-	-	-	-	**Only for test, has to be 0**

5.2.15 Misc 1 (14)

Table 43. Misc 1 (14)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	0 0 1 1	0 1 0 1	**VCO magnitude** 1V - default 2V 3V 4V
-	-	-	-	0 0 1 1	0 1 0 1	-	-	**Current reduction of mixer** full current -2mA -4mA do not use
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Current reduction of active balun** full current (necessary for 2 IF-filters) -2mA (2 IF-filters, reduced output voltage) -4mA (for 1IF filter) -6,5mA (1 IF filter, reduced output voltage)
0	0	-	-	-	-	-	-	**Only for test, has to b 0**

5.2.16 Misc 2 (15)

Table 44. Misc 2 (15)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	0 0 1 1	0 1 0 1	**Oscillation frequency of RC oscillator** 0.68 MHz 1.31 MHz 1.9 MHz 2.5 MHz
-	-	-	-	-	0			**Only for test, has to be 0**
-	-	-	-	0 1	-	-	-	**IF buffer amplifier enable** IF buffer amplifier off IF buffer amplifier on (GPIO5 need to be digital input)
-	-	-	0 1	-	-	-	-	**IF buffer amplifier input selector** input = IFin1 input = IFin2
0 0 0 0 1 : 1	0 0 1 1 0 : 1	0 1 0 1 0 : 1	-	-	-	-	-	**IF buffer amplifier gain** -11dB -9dB -7dB -5dB -3dB : 3dB

5.2.17 AGC time constant settings (16 / 32)

Table 45. AGC time constant settings (16 / 32)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	0 0 1	0 1 0	**FM AGC decay time constant** D3 (125ms) D2 (25ms) D1 (5ms)
-	-	-	-	0 0 1	0 1 0	-	-	**FM AGC attack time constant** A3 (12.5) A2 (2.5) A1 (0.5)
-	-	0 0 1	0 1 0	-	-	-	-	**AM AGC time constant** T3 (125ms) T2 (25ms) T1 (5ms)
-	0 1	-	-	-	-	-	-	**IF AGC time constant FM** U 1 (250µs attack) U 2 (50µs attack)
0 1	-	-	-	-	-	-	-	**IF AGC time constant AM** S1 (100ms) S2 (10ms)

5.2.18 AMAGC control (17 / 33)

Table 46. AMAGC control (17 / 33)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								AM AGC output mode
				0	0	0	0	Off
				1	0	0	0	Positive current output for PIN diode (mode1)
				0	1	0	0	Constant 2mA output (mode2)
-	-	-	-	1	0	0	1	Voltage and current output / internal sense (mode3a)
				1	0	1	1	Voltage and current output /external sense (mode3b)
				1	1	1	0	Calibration for mode 3a (mode4a)
				0	0	1	0	Calibration for mode 3b (mode 4b)
								AM AGC thresholds
0	0	0	0					Input level = 95.3 dBµV (mixer); 100.3 dBµV (filter)
0	0	0	1					Input level = 96.2 dBµV (mixer); 101.2 dBµV (filter)
:	:	:	:					:
:	:	:	:					:
0	1	1	1	-	-	-	-	Input level = 101.5 dBµV (mixer); 106.5 dBµV (filter)
1	0	0	0					Input level = 95.3 dBµV (mixer); 100.3 dBµV (filter)
1	0	0	1					Input level = 94.4 dBµV (mixer); 99.4 dBµV (filter)
:	:	:	:					:
:	:	:	:					:
1	1	1	1					Input level = 89 dBµV (mixer); 94 dBµV (filter)

5.2.19 GPIO output level control (18 / 34)

Table 47. GPIO output level control (18 / 34)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								GPIOx high / low output level
							0	GPIO1 low
							1	GPIO1 high
						0		GPIO2 low
						1		GPIO2 high
	:	:	:	:	:			:
	X	X	X	X	X			GPIOx low / high
	:	:	:	:	:			:
0								GPIO8 low
1								GPIO8 high

5.2.20 IF control (19 / 35)

Table 48. IF control (19 / 35)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								IF input selection
0							0	IF input AM IBOC (=IFin4)
0	-	-	-	-	-	-	1	IF input FM IBOC (=IFin2)
1							0	IF input AM analog (=IFin3)
1							1	IFinput FM analog (=IFin1)
								Mixer input FM / AM selection
-	-	-	-	-	-	0	-	AM input active
						1		FM input active
								Mixer input selection for AM
-	-	-	-	-	0	-	-	AM mixer input
					1			AM low pass filter input
								Mixer input selection for FM
-	-	-	-	0	-	-	-	FM1 mixer input
				1				FM2 mixer input
								IF amplifier Gain
	0	0	0					23dB (input1-3) / 16dB (input4)
	0	0	1					25dB (input1-3) / 18dB (input4)
-	:	:	:	-	-	-	-	:
	1	1	0					35dB (input1-3) / 28dB (input4)
	1	1	1					37dB (input1-3) / 30dB (input4)

5.2.21 VCO divider (V-divider) (20 / 36)

Table 49. VCO divider (V-divider) (20 / 36)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Divider V value
							X	V0
						X		V1
					X			V2
				X				V3
			X					V4
		X						V5
	X							V6
								VCO range selection
0	-	-	-	-	-	-	-	Range 2
1								Range 1

Note: Effective V-divider value = 4(V+4), V-patterns xxx0000 are not allowed.*

5.2.22 PLL main divider (N-divider) 1 (21 / 37)

Table 50. PLL main divider (N-divider) 1 (21 / 37)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Divider N value
							X	M8
						X		M9
					X			M10
				X				M11
			X					M12
		X						M13
	X							M14
X								M15

5.2.23 PLL main divider (N-divider) 2 (22 / 38)

Table 51. PLL main divider (N-divider) 2 (22 / 38)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Divider N value
							X	M0
						X		M1
					X			M2
				X				M3
			X					M4
		X						M5
	X							M6
X								M7

5.2.24 PLL main divider (N-divider) 3 (23 / 39)

Table 52. PLL main divider (N-divider) 3 (23 / 39)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								Divider N value
							X	K0
						X		K1
					X			K2
				X				A0
			X					A1
		X						A2
	X							A3
X								A4

5.2.25 PLL Divider ratio calculation

Table 53. PLL Divider ratio calculation

M counter							A counter					K (fractional)			Notes
M16 (1)	M15	…	M7	…	M1	M0	A4	A3	A2	A1	A0	K2	K1	K0	N= 32*P + A + K/6 M=32 N= M*P + A + K/6 M>32 (P=32)

1. Bit M16 is D2 of reg30

5.2.26 Divider R LSB (24/40)

Table 54. Divider R LSB (24/40)

MSB							LSB	Divider R value
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
X	-	-	-	-	-	-	X	**Divider R value** DivR0 : : DivR7

5.2.27 Charge pump current (25 / 41)

Table 55. Charge pump current (25 / 41)

MSB							LSB	FUNCTION
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-		X	X	X	X	X	**Low current charge pump** 65 µA 130 µA 260 µA 520 µA 980 µA
X	X	X	-	-	-	-	-	**High current charge pump** 1mA 2mA 4mA

5.2.28 Tuning DAC 1 (26 / 42)

Table 56. Tuning DAC 1 (26 / 42)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								DAC 1 voltage 7..0
							X	DAC1_0
						X		DAC1_1
					X			DAC1_2
				X				DAC1_3
			X					DAC1_4
		X						DAC1_5
	X							DAC1_6
X								DAC1_7

*Note: DAC 1 output voltage = 600mV + DAC1val * 18mV*

5.2.29 Tuning DAC 2 (27 / 43)

Table 57. Tuning DAC 2 (27 / 43)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								DAC 2 voltage 8..1
							X	DAC2_1
						X		DAC2_2
					X			DAC2_3
				X				DAC2_4
			X					DAC2_5
		X						DAC2_6
	X							DAC2_7
X								DAC2_8

*Note: DAC 2 output voltage = 600mV + DAC2val * 9mV*

5.2.30 Different controls (28 / 44)

Table 58. Different controls (28 / 44)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-	0 1	**DAC 1 On / Off** Off On
-	-	-	-	-	-	0 1	-	**DAC 2 On / Off** Off On
-	-	-	-	-	X	-	-	**Not used**
-	-	-	-	X	-	-	-	**DAC 2_0**
-	-	-	0	-	-	-	-	**Only for test, has to be 0**
-	-	0 1	-	-	-	-	-	**Charge pump control** high current controlled from phase error - default high current on
-	0 1	-	-	-	-	-	-	**VCO 1 / VCO 2 select** VCO 2 used (3.7GHz) VCO 1 used (4.7GHz)
0 1	-	-	-	-	-	-	-	**IQ phase select** I anticipates Q (low side injection) Q anticipates I (high side injection)

5.2.31 AM filter adjust (29 / 45)

Table 59. AM filter adjust (29 / 45)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								AM filter corner frequency (-3dB point)
0	**0**	**0**	**0**	0	0	0	0	1.2 MHz
0	**0**	**0**	**1**	0	0	0	0	1.28 MHz
0	**0**	**1**	**0**	0	0	0	0	1.36 MHz
0	**0**	**1**	**1**	0	0	0	0	1.46 MHz
0	**1**	**0**	**0**	0	0	0	0	1.58 MHz
0	**1**	**0**	**1**	0	0	0	0	1.71 MHz
0	**1**	**1**	**0**	0	0	0	0	1.86 MHz
0	**1**	**1**	**1**	0	0	0	0	2.04 MHz
1	**0**	**0**	**0**	**0**	0	0	0	2.38 MHz
1	**0**	**0**	**0**	**1**	0	0	0	2.52 MHz
1	**0**	**0**	**1**	**0**	0	0	0	2.69 MHz
1	**0**	**0**	**1**	**1**	0	0	0	2.87 MHz
1	**0**	**1**	**0**	**0**	0	0	0	3.11 MHz
1	**0**	**1**	**0**	**1**	0	0	0	3.36 MHz
1	**0**	**1**	**1**	**0**	0	0	0	3.66 MHz
1	**0**	**1**	**1**	**1**	0	0	0	4.00 MHz
1	1	**0**	**0**	**0**	**0**	0	0	4.64 MHz
1	1	**0**	**0**	**0**	**1**	0	0	4.91 MHz
1	1	**0**	**0**	**1**	**0**	0	0	5.23 MHz
1	1	**0**	**0**	**1**	**1**	0	0	5.57 MHz
1	1	**0**	**1**	**0**	**0**	0	0	6.03 MHz
1	1	**0**	**1**	**0**	**1**	0	0	6.48 MHz
1	1	**0**	**1**	**1**	**0**	0	0	7.05 MHz
1	1	**0**	**1**	**1**	**1**	0	0	7.68 MHz
1	1	1	**0**	**0**	**0**	**0**	0	8.87 MHz
1	1	1	**0**	**0**	**0**	**1**	0	9.36 MHz
1	1	1	**0**	**0**	**1**	**0**	0	9.92 MHz
1	1	1	**0**	**0**	**1**	**1**	0	10.53 MHz
1	1	1	**0**	**1**	**0**	**0**	0	11.35 MHz
1	1	1	**0**	**1**	**0**	**1**	0	12.16 MHz
1	1	1	**0**	**1**	**1**	**0**	0	13.12 MHz
1	1	1	**0**	**1**	**1**	**1**	0	14.20 MHz

Table 59. AM filter adjust (29 / 45) (continued)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
								AM filter corner frequency (-3dB point)
1	1	1	1	0	0	0	0	16.31 MHz
1	1	1	1	0	0	0	1	17.03 MHz
1	1	1	1	0	0	1	0	18.07 MHz
1	1	1	1	0	0	1	1	18.95 MHz
1	1	1	1	0	1	0	0	20.31 MHz
1	1	1	1	0	1	0	1	21.43 MHz
1	1	1	1	0	1	1	0	23.10 MHz
1	1	1	1	0	1	1	1	24.56 MHz
1	1	1	1	1	0	0	0	27.91 MHz
1	1	1	1	1	0	0	1	30.12 MHz
1	1	1	1	1	0	1	0	33.56 MHz
1	1	1	1	1	0	1	1	36.80 MHz
1	1	1	1	1	1	0	0	42.56 MHz
1	1	1	1	1	1	0	1	47.89 MHz
1	1	1	1	1	1	1	0	57.14 MHz
1	1	1	1	1	1	1	1	67.17 MHz

5.2.32 Misc 3 (30 / 46)

Table 60. Misc 3 (30 / 46)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	-	-		**AMLNA on / off**
							0	AMLNA off
							1	AMLNA on
-	-	-	-	-	-		-	**High current chargepump**
						X		0.5 mA
-	-	-	-	-		-	-	**PLL N divider MSB**
					X			M16
-	-	-	-	0	-	-	-	**Only for test, has to be 0**
0	0	0	0	-	-	-	-	**Has to be 0**

5.2.33 AD converter test (31 / 47)

Table 61. AD converter test (31 / 47)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	0	0	0	0	**Only for test, has to be 0**

5.2.34 Read 1 (48)

Table 62. Read 1 (48)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	-	-	-	0 : 1 : 1	0 : 0 : 1	0 : 1 : 1	**Mask set revision** 1st : 6th = latest one : 8th
-	-	-	-	0 1	-	-	-	**PWR stable read bit** Supply voltage not OK, if bit was set once Supply voltage OK
-	-	-	0 1	-	-	-	-	**GPIO 5 level** low high
-	-	0 1	-	-	-	-	-	**GPIO 6 level** low high
-	X	-	-	-	-	-	-	**not used**
X	-	-	-	-	-	-	-	**not used**

5.2.35 Read 2 (49)

Table 63. Read 2 (49)

MSB							LSB	Function
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
-	-	X	X	X	X	X	X	**AD converter result** ADC0 ADC1 ADC2 ADC3 ADC4 ADC5
-	0 1	-	-	-	-	-	-	**AD converter result status** Not OK (readout before converter finished) OK
X	-	-	-	-	-	-	-	**not used**

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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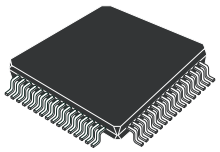
Figure 10. LQFP64 (10x10x1.4mm) exposed pad down mechanical data and package dimensions (exposed pad size for D2 and E2: 4.5mm max.)

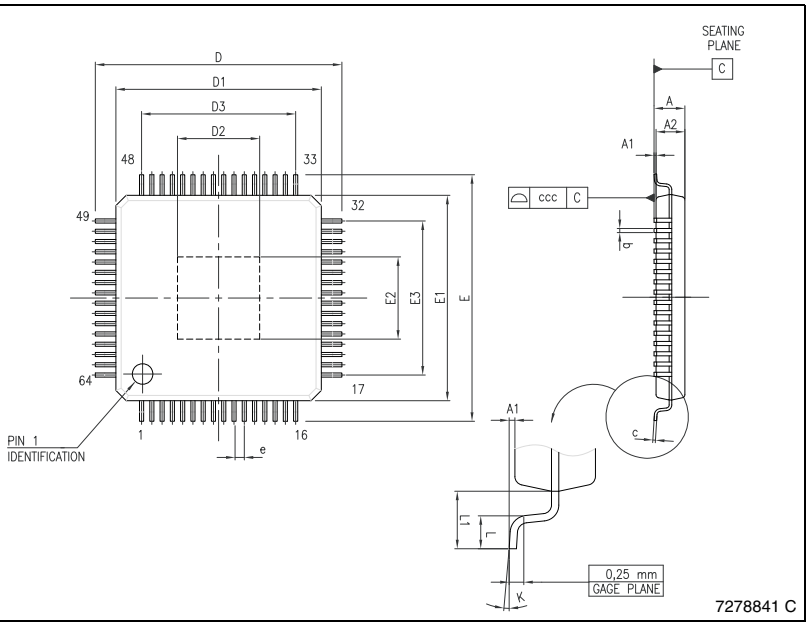
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D2	According to Pad size					
D3		7.500			0.2953	
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E2	According to Pad size					
E3		7.500			0.2953	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k		3.500	7.000		0.1378	0.2756
ccc			0.080			0.0031

Note: 1. Exact shape of each corner is optional.

OUTLINE AND MECHANICAL DATA



LQFP64 (10x10x1.4mm)
Exposed Pad Down



7 Revision history

Table 64. Document revision history

Date	Revision	Changes
25-Jan-2007	1	Initial release.
08-Mar-2007	2	Corrected typ. value of “I decay max (mode D1)” in the *Table 8* on page 20. Updated *Table 41 on page 50*.
19-Mar-2007	3	Corrected the Rev. number on page 1.
01-Oct-2007	4	Modified *Table 56 on page 58*.
26-Jun-2008	5	Modified *Table 18 on page 32*, *Table 31 on page 44*, *Table 44 on page 52*. Updated note below *Table 49 on page 55*.
17-Dec-2009	6	Modified *Table 28: Communication using the SPI protocol electrical characteristics on page 38*.
24-Sep-2013	7	Updated disclaimer.

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