



**THE DATASHEET OF
SKY87203-11-631LF**



DATA SHEET

SKY87203: 3.5 A Constant On-Time, Step-Down DC-DC Converter

Applications

- Portable devices
- Access points
- Set-top boxes

Features

- Input voltage range: 2.7 V to 6.0 V
- Output voltage range: 0.9 V to 4.0 V
- Variable switching frequency: 600 kHz to 1.5 MHz
- Up to 3.5 A continuous output current
- 95% peak efficiency
- Typical switch on resistance: 50 mΩ PMOS, 40 mΩ NMOS
- 80% light load efficiency
- Power sequencing
- Cycle-by-cycle over-current protection
- Auto-discharge at power-off
- Over-temperature protection
- Control loop stabilization with low ESR ceramic capacitors
- Soft start
- Low profile, QFN (12-pin, 2 mm × 2 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

Description

The SKY87203 is a variable switching frequency, 3.5 A constant on-time, synchronous step-down converter. The device provides an output voltage from 0.9 V to 4.0 V from input voltage ranging from 2.7 V to 6.0 V, while keeping excellent line and load regulation and maximizing efficiency.

The constant on-time control allows easy loop stabilization with minimal external components while providing fast transient response.

Power sequencing is controlled by the EN and PG pins.

The SKY87203 has cycle-by-cycle current limits and thermal shutdown to protect against fault conditions.

The SKY87203 is available in a 12-pin, 2 mm × 2 mm Quad Flat No-Lead (QFN) package. A typical application circuit is shown in Figure 1. The pin configuration and packages are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.



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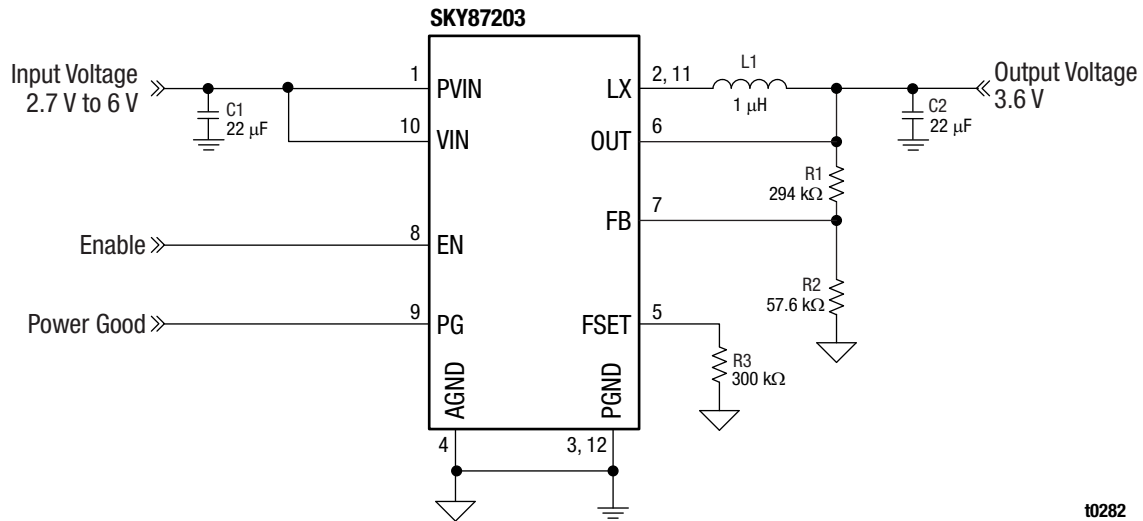


Figure 1. Typical Application Circuit

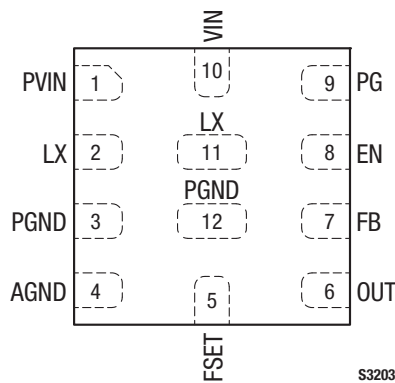


Figure 2. SKY87203-11 Pinout – 12-Pin QFN Package (Top View)

Table 1. SKY87203 Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	PVIN	Power supply.	7	FB	Feedback voltage pin. Used to control the converter output voltage according to the ratio of the feedback resistor.
2	LX	Switch node, connected to inductor.	8	EN	Enable pin, active high.
3	PGND	Power ground.	9	PG	Power good pin. Open drain with internal pull-up resistor.
4	AGND	Analog ground.	10	VIN	Analog supply pin.
5	FSET	Switching frequency adjust pin. Connect with a resistor to ground. If this pin is left floating, the switching frequency is 1.2 MHz for an input voltage equal to 5 V and an output voltage equal to 1.2 V.	11	LX	Switch node, connected to inductor.
6	OUT	Output voltage sensing pin.	12	PGND	Power ground.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY87203 are provided in Table 2. Recommended operating conditions are specified in Table 3. Electrical specifications are provided in Table 4.

Table 2. SKY87203 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Power pins (PVIN, VIN to ground)	V _{IN}	-0.3	+6.5	V
Switching voltage (LX to ground)	V _{LX}	-0.3	V _{IN} + 0.3	V
Signal pins (FB, OUT, EN, PG to ground)	V _{FB} , V _{OUT} , V _{EN} , V _{PG}	-0.3	+6.5	V
Maximum continuous current for load switch	I _{MAX}		3.5	A
Junction temperature	T _J		+150	°C
Storage temperature	T _{STG}	-65	+150	°C
Soldering temperature (at leads, 10 sec)	T _{LEAD}		+260	°C
Thermal resistance, junction-to-ambient	θ _{JA}		80	°C/W
Thermal resistance, junction-to-case	θ _{JC}		16	°C/W
Power dissipation @ 25 °C	P _D		1.6	W

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. SKY87203 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input voltage range	V _{IN}	2.7		6.0	V
Output voltage range	V _{OUT}	0.9		4.0	V

Table 4. SKY87203 Electrical Specifications (1 of 2) (Note 1)
(V_{IN} = 5.0 V, T_A = -40 °C to +85 °C [Typical Values are T_A = +25 °C], Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Input shutdown current	I _{SHDN}	V _{EN} = 0 V		0		μA
Quiescent supply current	I _Q	V _{EN} = 2 V, V _{FB} = 0.63 V, V _{IN} = 3.6 V		40		μA
Feedback voltage	V _{FB}	2.7 V ≤ V _{IN} ≤ 6.0 V	0.591	0.600	0.609	V
Feedback input bias current	I _{FB}	V _{FB} = 0.6 V		10		nA
High side switch on resistance (Note 2)	R _{DS(ON)_P}			50		mΩ
Low side switch on resistance (Note 2)	R _{DS(ON)_N}			40		mΩ
Switch leakage		V _{EN} = 0 V, V _{IN} = 6.0 V, V _{LX} = 0 V and 6.0 V		0	2	μA
PFET current limit			3.6	4.5	6.0	A
Dampening resistor	R _{DAMP}			200		Ω

Table 4. SKY87203 Electrical Specifications (2 of 2) (Note 1)
(VIN = 5.0 V, TA = -40 °C to +85 °C [Typical Values are TA = +25 °C], Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
On time	ton	VIN = 5.0 V, VOUT = 1.2 V RFSET = 600 kΩ, PWM Mode (0.6 MHz)		430		ns
		VIN = 5.0 V, VOUT = 1.2 V RFSET = 300 kΩ, PWM Mode (1.2 MHz)		220		ns
		VIN = 3.6 V, VOUT = 1.2 V RFSET = 300 kΩ, PWM Mode (1.2 MHz)		277		ns
		VIN = 5.0 V, VOUT = 1.2 V FSET = floating, PWM Mode (1.2 MHz)		210		ns
		VIN = 5.0 V, VOUT = 1.2 V RFSET = 240 kΩ, PWM Mode (1.5 MHz)		170		ns
Minimum off time	toff			30		ns
Soft-start time	tss_on			1		ms
VIN discharge N-MOSFET switch on resistance (Note 2)	Rdson_DSCHG	VIN (falling) = UVLO		10		Ω
VIN discharge time	VIN_DSCHG	UVLO ≥ VIN (falling) ≥ 1 V		90	200	ms
PG pin upper trip threshold		VFB ≥ 0.66 V		+10		%
PG pin lower trip threshold		VFB ≤ 0.54 V		-10		%
PG pin delay				90		μs
PG pin sink current capability	VPG_LO				0.4	V
PG pin logic high voltage	VPG_HI		4.9			V
PG pin internal pull-up resistor	RPG			500		kΩ
Output voltage discharge resistor	RDSCHG			100		Ω
Under-Voltage Lock Out	UVLO	VIN rising	2.35	2.50	2.65	V
UVLO hysteresis				400		mV
EN pin input voltage: Logic low Logic high	VEN_L		1.2		0.4	V
	VEN_H					V
EN pin input current		VEN = 2 V		2		μA
		VEN = 0 V		0		μA
Thermal shutdown				150		°C
Thermal hysteresis (Note 2)				30		°C

Note 1: Performance is guaranteed only under the conditions listed in this table.

Note 2: Specification guaranteed by design.

Typical Performance Characteristics

Typical performance characteristics of the SKY87203 are illustrated in Figures 3 through 21. The output voltage is 3.6 V.

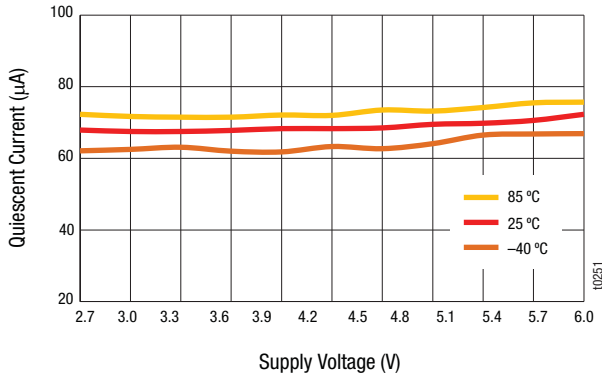


Figure 3. Quiescent Current (Close Loop) vs Supply Voltage

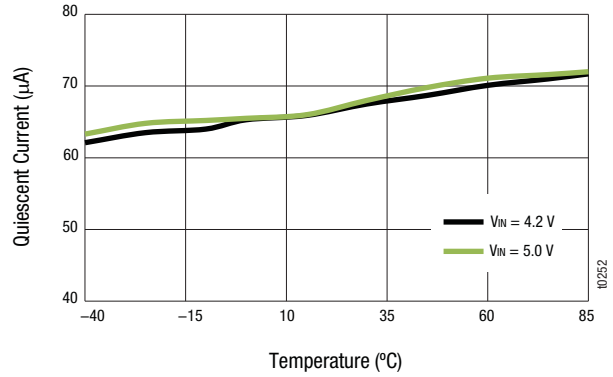


Figure 4. Quiescent Current (Close Loop) vs Temperature

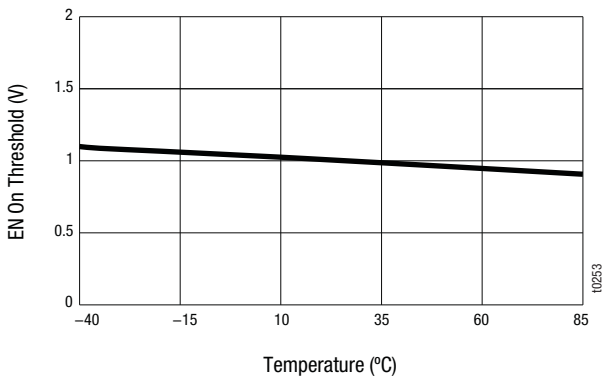


Figure 5. EN On Threshold vs Temperature
(VIN = 5 V, Load = 0 mA)

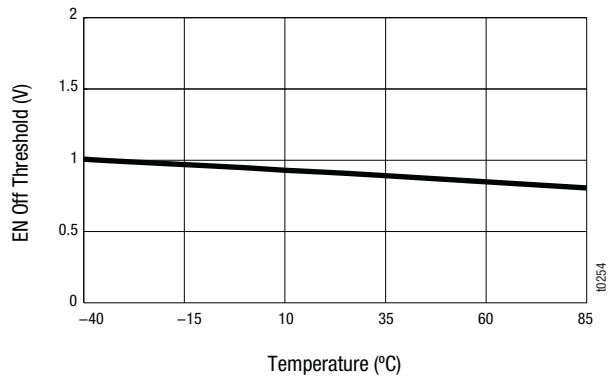


Figure 6. EN Off Threshold vs Temperature
(VIN = 5 V, Load = 0 mA)

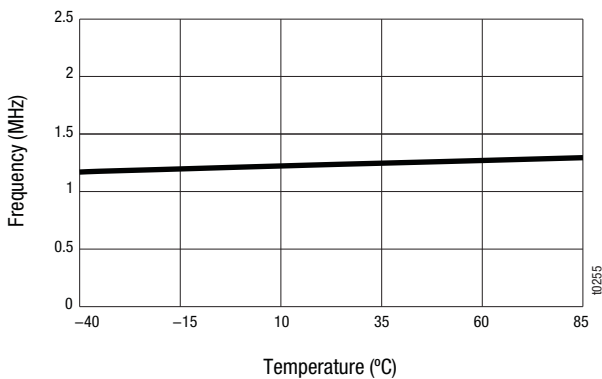


Figure 7. Frequency vs Temperature
(VIN = 5 V, Load = 500 mA)

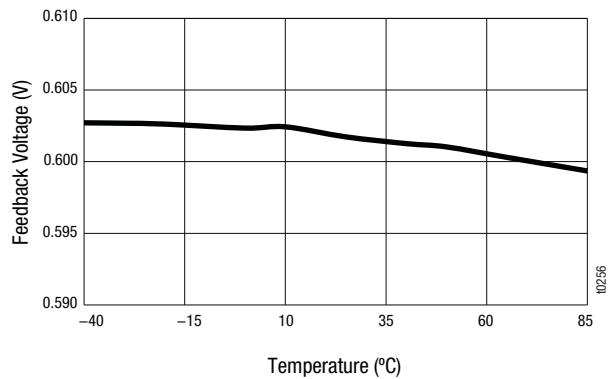


Figure 8. Feedback Voltage vs Temperature
(VIN = 5 V, Load = 0 mA)

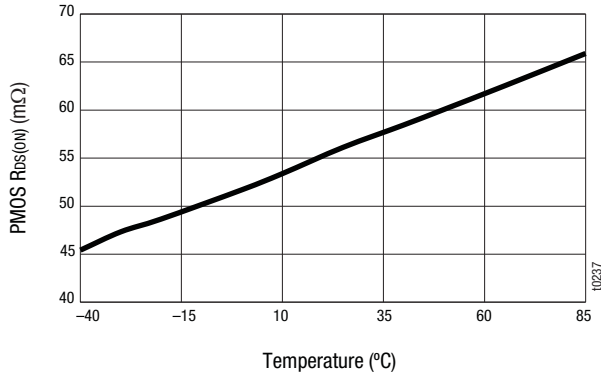


Figure 9. PMOS Rds(ON) vs Temperature (VIN = 5 V)

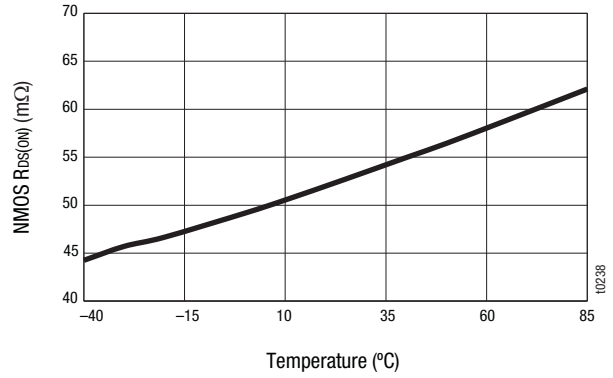


Figure 10. NMOS Rds(ON) vs Temperature (VIN = 5 V)

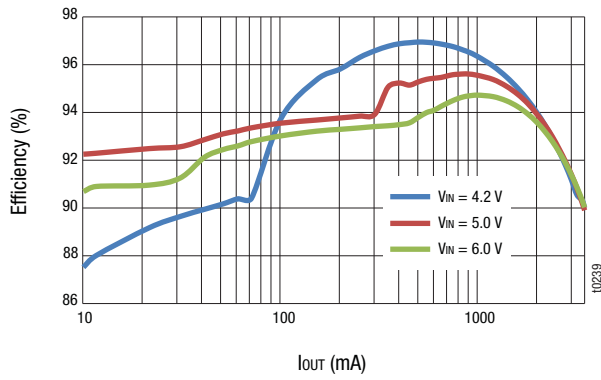


Figure 11. Efficiency vs Iout

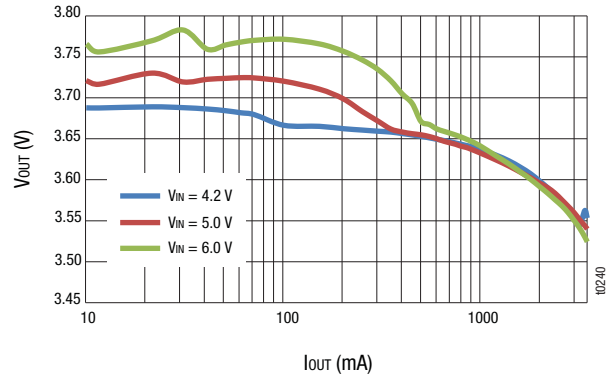


Figure 12. Vout vs Iout

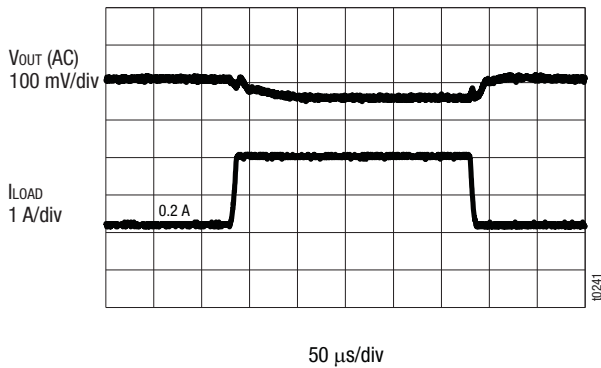


Figure 13. Load Transient (Load = 0.2 A to 2 A)

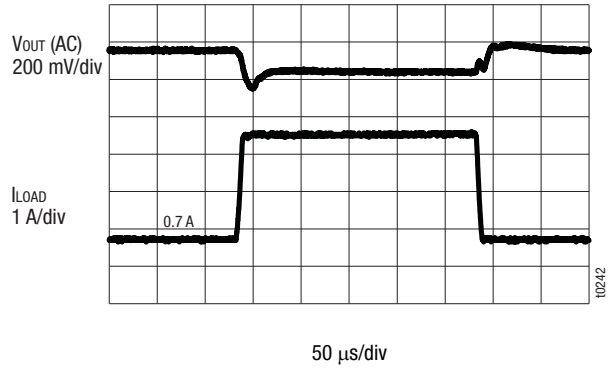


Figure 14. Load Transient (Load = 0.7 A to 3.5 A)

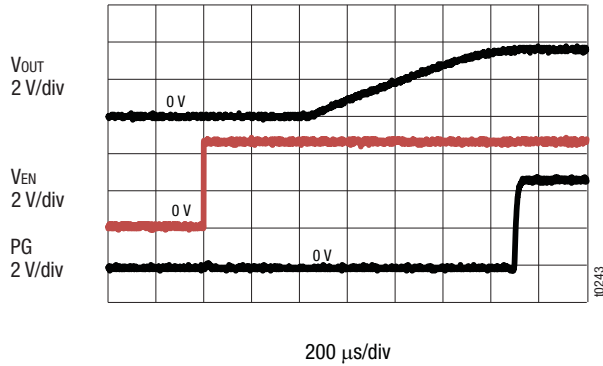


Figure 15. Power Good Delay

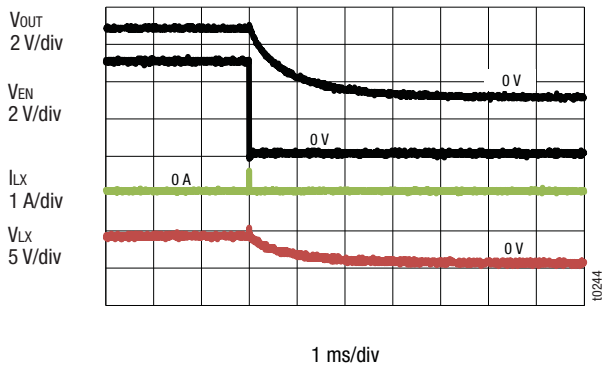


Figure 16. Shutdown Waveform (Load = 0 A)

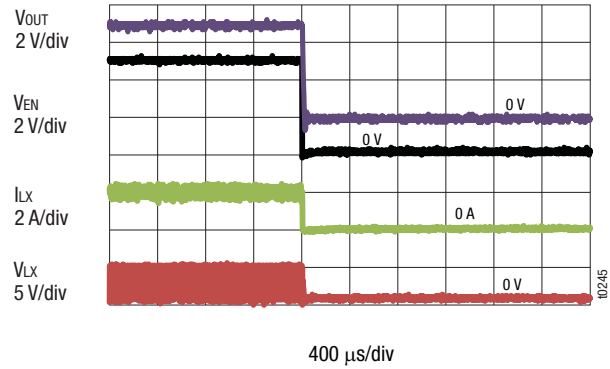


Figure 17. Shutdown Waveform (Load = 2 A)

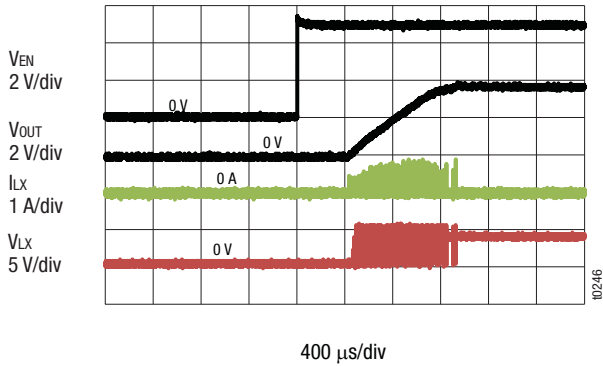


Figure 18. Soft Start Waveform (Load = 0 A)

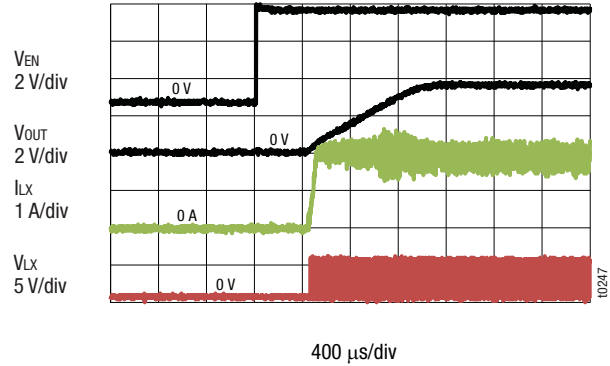


Figure 19. Soft Start Waveform (Load = 2 A)

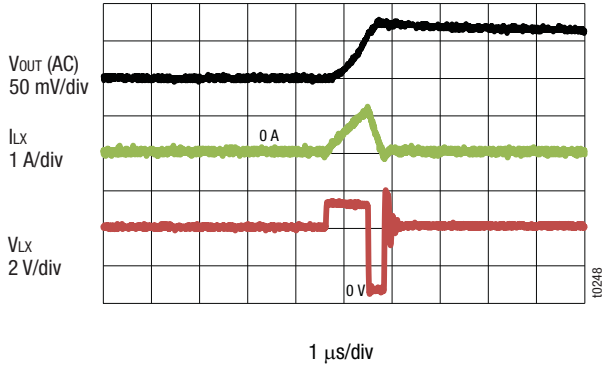


Figure 20. Typical Switching Waveform (0 A Load)

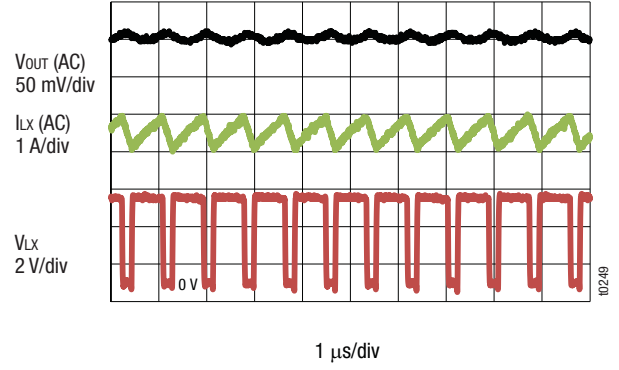
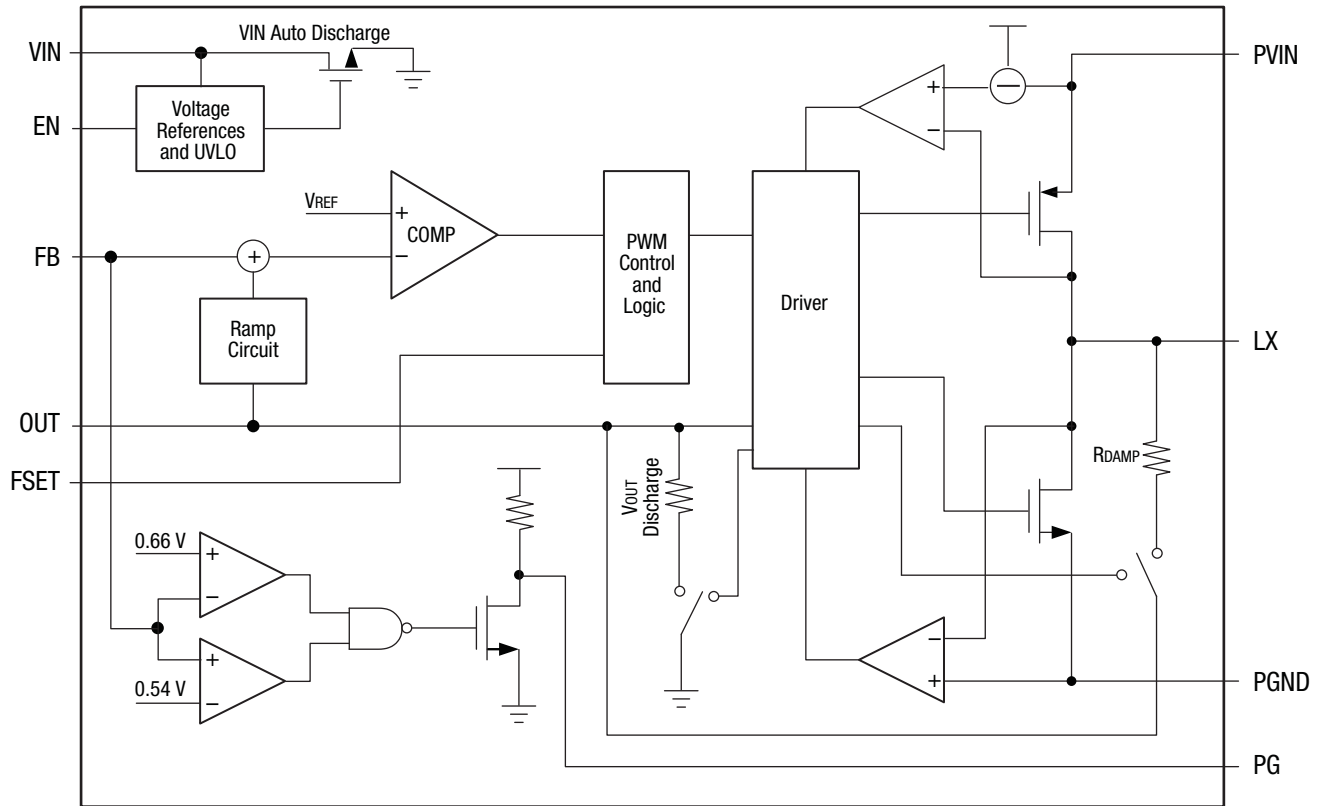


Figure 21. Typical Switching Waveform (2 A Load)



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Figure 22. SKY87203 Functional Block Diagram

Functional Description

The SKY87203 is an adaptive constant on-time, adjustable voltage step-down DC-DC converter. A constant on-time control architecture offers a simpler control loop and faster transient response than a fixed-frequency Pulse Width Modulation (PWM) control architecture.

The constant on-time converter maintains a constant output frequency because the “on” time is inversely proportional to the supply voltage. As the input voltage decreases, the “on” time is increased, maintaining a relatively constant period.

The device is enabled using the EN input. When the EN pin is pulled high, the converter starts up under the control of a 1 ms soft start routine. Under light load conditions, the switch enters pulse-skipping mode to ensure regulation is maintained. This effectively changes the switching frequency.

To maintain a wide input voltage range, the switching period is extended when either the minimum “off” or “on” time is reached. The frequency is also affected when switching operates in discontinuous mode. The “on” time of the switching pulses can be estimated using the following equation:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.833 \mu\text{s}$$

The minimum off time is fixed at 30 ns to prevent runaway inductor current during load transients.

A functional block diagram of the SKY87203 is shown in Figure 22.

Constant On-Time (COT) Operation

In normal continuous conduction mode, where the inductor current (I_L) never reaches zero, the high-side MOSFET is turned on for a fixed interval (t_{ON}) determined by the COT sub-circuit (a one-shot timer) within the PWM Control and Logic functional block.

During that fixed interval, the inductor current starts to ramp up. At the end of the t_{ON} period, the high-side MOSFET is turned off and the low-side MOSFET is turned on causing the inductor current to ramp down. Until this point, the voltage on the FB pin (V_{FB}) goes below the reference voltage (V_{REF}) on the comparator, which restarts the one-shot timer and initiates the next cycle.

The ideal t_{ON} time in continuous conduction mode is determined by the following relationships:

$$\text{Duty cycle (D)} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{On time (} t_{ON} \text{)} = D \times \frac{I}{f_{SW}}$$

If switching frequency (f_{sw}) = 1.2 MHz, the on-time equation can be rewritten as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.833 \mu\text{s}$$

The COT circuit generates an “on” time proportional to the ideal duty cycle and holds the switching frequency constant. However, due to nonlinearities in the COT circuit, propagation delays, and non-ideal switch voltage drops due to output current loads, the actual operating frequency can vary slightly.

When DC current loads are less than half of the peak-to-peak current ripple in the inductor, the inductor current can drop to zero or even become negative. When this happens, the SKY87203 operates in discontinuous conduction mode.

During the “off” time, the low-side MOSFET is on and the discontinuous conduction mode comparator monitors the current. When the current is zero, the low-side MOSFET is turned off, which prevents the current from going negative.

Both the high-side MOSFET and the low-side MOSFET remain off with the output capacitor supplying the load current until the FB pin voltage goes below the reference voltage, triggering a new switching cycle. The switching frequency decreases in light load conditions.

Waveforms for both continuous conduction mode and discontinuous conduction mode are shown in Figure 23.

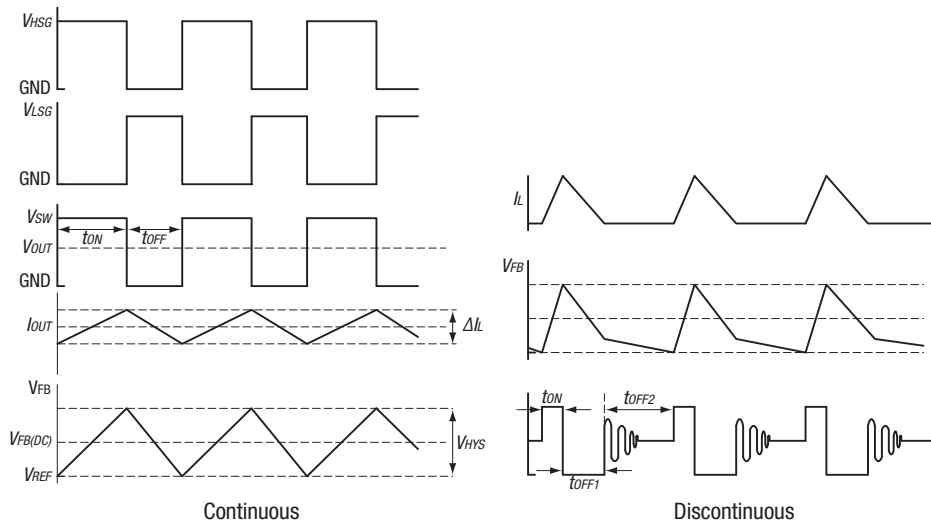


Figure 23. Continuous and Discontinuous Mode Wave Forms

Light Load Operation

In discontinuous conduction mode, the SKY87203 uses a passive damping scheme to reduce the amplitude and duration of ringing that occurs at the switching node (LX).

Enable and Soft Start

When the input voltage is greater than the Under-Voltage Lockout (UVLO) threshold, the SKY87203 is enabled by pulling the EN pin higher than 1.2 V. If the EN pin is left floating or pulled down to ground, the regulator is disabled. There is an internal 1 MΩ resistor from the EN pin to ground.

The SKY87203 step-down regulator soft-start control prevents output voltage overshoot and limits inrush current when either the input power or the enable input is applied. After the regulator is enabled, the SKY87203 ramps up the internal target voltage with a controlled slew rate of 1 ms.

When the EN signal is pulled low, the regulator forces the converter into a low-power, non-switching state, and forces the switching node into a high-impedance shutdown state.

PG (Power Good) Pin

The SKY87203 has an open drain with a 500 kΩ pull-up resistor pin indicator (PG). When the FB pin is within ±10 percent of regulation voltage, the PG pin is pulled up to V_{IN} by the internal resistor. If the FB pin voltage is not within ±10 percent of regulation voltage, the PG pin is pulled down to ground by an internal MOSFET. The MOSFET has a maximum R_{DS(ON)} of less than 100 Ω.

Current Limit and Short Circuit Protection

The SKY87203 includes protection for overload condition and short-circuit conditions by current-limiting the high-side MOSFETs.

The SKY87203 enters over-load protection mode or short-circuit protection mode when the inductor current hits the current limit (4.5 A). The device will try to recover from the short circuit by entering a “hiccup” mode, in which the regulator disables the output power stage, discharges the soft-start capacitor, and automatically tries a soft start again. If the overload or the short-circuit condition still holds after a soft start ends, the SKY87203 repeats this protection operation cycle until the short circuit disappears and the output rises back to the regulation level.

Flexible Switching Frequency Select Function

The SKY87203 has a flexible switching frequency select function to satisfy the variable application requirement. If this pin is left floating, the switching frequency is 1.2 MHz. A resistor (R3) is connected between the FSET pin and ground to adjust the switching frequency according to the following relationship:

$$\text{Frequency} = 1.2 \text{ MHz} \times (300 \text{ k}\Omega / R3)$$

Application Information

Setting the Output Voltage

The SKY87203 output voltage is adjustable from 0.9 V up to 4.0 V by connecting the FB pin to the center tap of a resistor-divider between the output and ground (see Figure 24). The resistive feedback voltage divider sets the output voltage according to the following relationship:

$$R_{FB2} = \frac{R_{FB1}}{\left(\frac{V_{OUT}}{0.6V}\right) - 1}$$

As shown in Table 5, the values for both RFB1 and RFB2 are rounded to the nearest 1 percent resistor value, and typically selected to be between 10 kΩ and 200 kΩ. The lower resistance value improves the noise immunity, but results in higher feedback current (which reduces the efficiency).

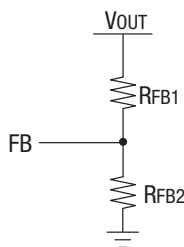


Figure 24. Feedback Resistive Divider Circuit

Table 5. Adjustable Resistor Values

Output Voltage (V)	RFB2 (kΩ 1%) (RFB1 = 200 kΩ 1%)
1.0	300
1.2	200
1.8	100
2.5	63.2
3.3	44.2

VIN Auto Discharge

The SKY87203 has a VIN auto-discharge function for USB applications in which a large inrush current supplied by a large VIN capacitor during a hot plugging operation exceeds the allowed USB current limit. When VIN voltage falls below the UVLO threshold, an N-MOSFET switch discharges the VIN to ground until VIN is less than 1 V. The discharge time is typically 90 ms for the condition UVLO ≥ VIN ≥ 1 V.

For example, a 500 μF bulk input capacitor needs about 80 ms to discharge an input voltage from 2.1 V to 1.0 V as illustrated in Figure 25.

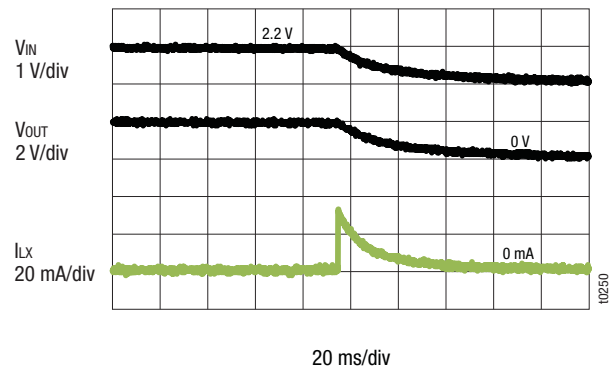


Figure 25. VIN Auto Discharge

Inductor Selection

Inductor values ranging from 0.82 μH to 4.7 μH are recommended for most SKY87203 applications. Given the desired input and output voltages, the inductor value and switching frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, Effective Series Resistance (ESR) losses in the output capacitors, and output voltage ripple. Highest efficiency operation is obtained at low frequency with a small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency, and operating frequency.

A reasonable starting point is to choose a ripple current that is about 30 percent of the maximum output current, $I_{OUT(MAX)}$. The largest ripple current occurs at the highest input voltage, V_{IN} . To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to the following relationship:

$$L = \left(\frac{V_{OUT}}{f_{SW} \times \Delta I_{L(MAX)}} \right) \times \left(I - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

The maximum inductor peak current is calculated according to:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_{L(MAX)}}{2}$$

Manufacturer specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions.

The saturation current is a very important parameter for inductor selection. It must be more than the maximum peak current through the inductor – an adequate margin is important for a safe application.

Some inductors that meet the peak and average current rating requirements still result in excessive losses due to a high Direct Current Resistance (DCR). Always consider the losses associated with DCR and their effect on the total regulator efficiency when selecting an inductor.

Recommended inductors are listed in Table 6.

Output Capacitor Selection

The output capacitor limits the output ripple and provides current during large load transitions. A 22 μ F X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and Equivalent Series Inductance (ESL) characteristics necessary for low output ripple.

The key parameters for selecting the output capacitors are capacitance, ESR, ESL, and voltage ratings. Output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due

to the capacitor's ESL. Estimate the output voltage ripple due to the output capacitance, ESR, and ESL as follows:

$$V_{OUT(RIPPLE)} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

Where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times ESR$$

$$V_{RIPPLE(ESL)} = (V_{IN} - V_{OUT}) \times \frac{ESL}{L} = V_{IN} \times \frac{ESL}{L}$$

The peak to peak inductor current, ΔI_L , is:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

The capacitive ripple and ESR ripple are phase shifted from each other. Depending on the type of output capacitor chemistry, one of them typically dominates. When ceramic capacitors are used that generally have low ESR, $V_{RIPPLE(C)}$ dominates. When electrolytic capacitors are used, $V_{RIPPLE(ESR)}$ dominates.

Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

After a load step occurs, the output capacitor must support the difference between the load requirement and inductor current. Once the average inductor current increases to the DC load level, the output voltage recovers. Therefore, based on limitations in the ability to discharge the inductor, a minimum output voltage deviation may be determined by the following:

$$V_{SOAR(C)} = \frac{\Delta I_{OUT}^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

$$V_{SOAR(ESR)} = \Delta I_{OUT} \times ESR$$

Where V_{SOAR} is the output voltage overshoot and undershoot deviation.

Table 6. Recommended Inductor Selection

Manufacturer	Part Number	Inductance (μ H)	Saturation Current (A)	Temperature Current (A)	Typical DCR (m Ω)	Size W x L x H (mm)
Sumida	0520CDMCD5-1R0MC	1	8	5.9	17	5.75 x 5.45 x 2
Sumida	0420CDMCD5-1R0MC	1	6.8	5.5	17	4.75 x 4.35 x 2
Würth	74404063010	1	7.5	5.2	10	6 x 6 x 2.6
Toko	FDSD0515-H-1R0M	1	8.7	6.1	25	5.2 x 4.9 x 1.5

The ceramic output capacitor provides low ESR and low ESL, which results in low output ripple dominated by capacitive ripple voltage ($\Delta V_{OUT(c)}$). However, due to the lower capacitance value, the load transient response is significantly worse. Therefore, ceramic output capacitors are generally recommended only for designs with soft load transients (slow di/dt and/or small load steps).

Tantalum and electrolytic capacitors can provide a high capacitance, low-cost solution. The bulk capacitance provides minimal output voltage drop/soar after load transients occur.

Input Capacitor Selection

Typically, the input impedance is so low (or has other input capacitance distributed throughout the system) that a single 22 μ F (X7R or X5R) ceramic capacitor located near the SKY87203 is sufficient. However, additional input capacitance may be necessary depending on the impedance of the input supply.

To estimate the required input capacitance, determine the acceptable input ripple level (V_{PP}) and solve the following equation:

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \times \left(I - \frac{V_{OUT}}{V_{IN}} \right)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR \right) \times f_{SW}} = \frac{D \times (I - D)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR \right) \times f_{SW}}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when evaluating ceramic bypass capacitors. Besides the capacitance requirement, the RMS current rating of the input capacitor must be able to support the pulsed current drawn by the step-down regulator. The input RMS current requirement may be determined by:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(I - \frac{V_{OUT}}{V_{IN}} \right)} = I_{OUT} \times \sqrt{D \times (I - D)}$$

The terms D and “1 – D” appear in both input ripple voltage and input capacitor RMS current equations. The maximum value for D occurs when $V_{OUT} = 0.5 \times V_{IN}$ (50 percent duty cycle). This results in a set of “worst case” capacitance and RMS current design requirements:

$$C_{IN} = \frac{I}{4 \times \left(\frac{V_{PP}}{I_{OUT}} - ESR \right) \times f_{SW}}$$

$$I_{RMS(MAX)} = \frac{I_{OUT}}{2}$$

The input capacitor provides a low impedance loop for the pulsed current drawn by the SKY87203. Low ESR/ESL (X7R and X5R) ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as close as possible to the high-side MOSFET. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor can be seen in the Evaluation Board layout.

Recommended input capacitors are listed in Table 7.

Layout Recommendations

For best performance of the SKY87203, the following guidelines should be followed when designing the PCB layout:

- Make the power trace as short and wide as possible, including the input/output power lines and switching node, etc.
- While the two-layer PCB is enough for most applications, large and integral multilayer ground planes are ideal for high-power applications. Large areas of copper have lower resistance and help to dissipate heat.
- Put the input and output capacitor as close as possible to the IC to get the best filter result.
- Feedback and shutdown circuits should not be close to large AC signals involving the power inductor and switching node. Place the feedback resistors close to the output terminals.
- Connect the analog and power grounds together with a single short line. Connect all low-current loop grounds to analog ground to decrease the power ground noise on the analog ground and to achieve better load regulation.

Table 7. Recommended Input/Output Capacitor Selection

Manufacturer	Part Number	Capacitance (μ F)	Voltage (V)	Temperature Coefficient	Case
Murata	GRM188R71H104KA93D	0.1	50.0	X7R	0603
Murate	GRM21BR70J106ME76	10.0	6.3	X7R	0805
Murata	GRM219R61A226MEA0	22.0	10.0	X5R	0805
Murate	GRM1885C1H220JA01	22.0	50.0	COG	0603
KEMET	T520D477M006ATE025	470.0	6.3	$\pm 20\%$ Tol, $-55\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$	7343

Evaluation Board Description

The SKY87203 Evaluation Board is used to test the performance of the SKY87203 step-down DC-DC converter. An Evaluation Board schematic diagram is provided in Figure 26. Layer details for the SKY87203 Evaluation Board are shown in Figure 27. Component values for the SKY87203 Evaluation Board are listed in Table 8.

Package Dimensions

The PCB layout footprint for the SKY87203 is provided in Figure 28. Typical case markings for the SKY87203 are shown in Figure 29. Package dimensions for the 12-pin, 2 mm × 2 mm QFN package are shown in Figure 30. Tape and reel dimensions are shown in Figure 31.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY87203 is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, and document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

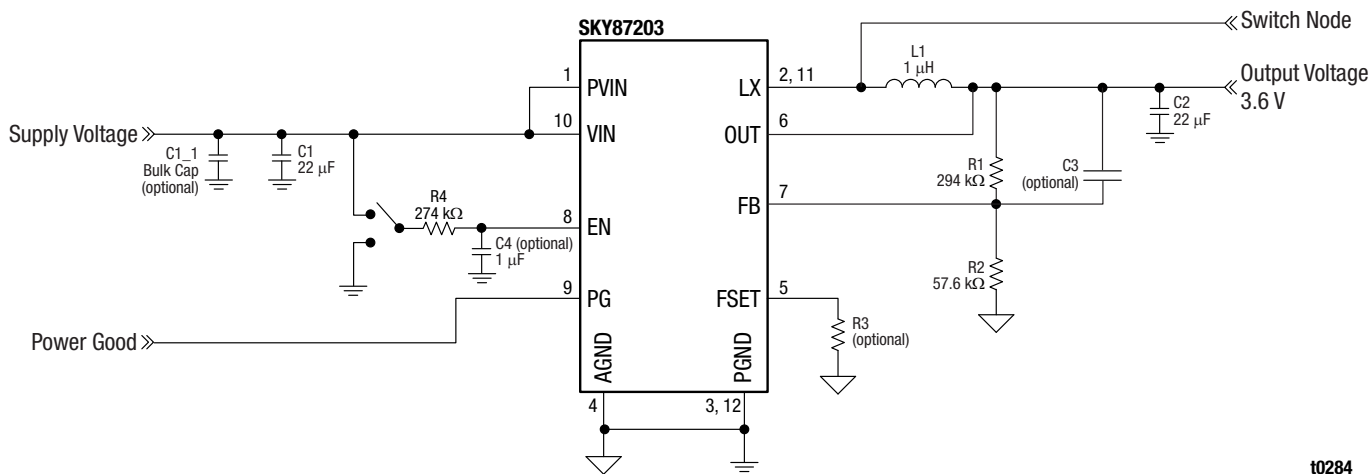
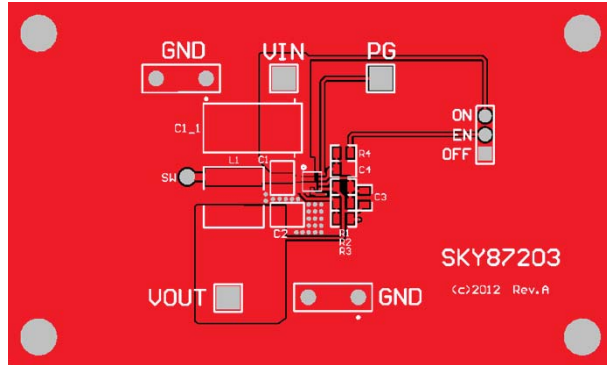
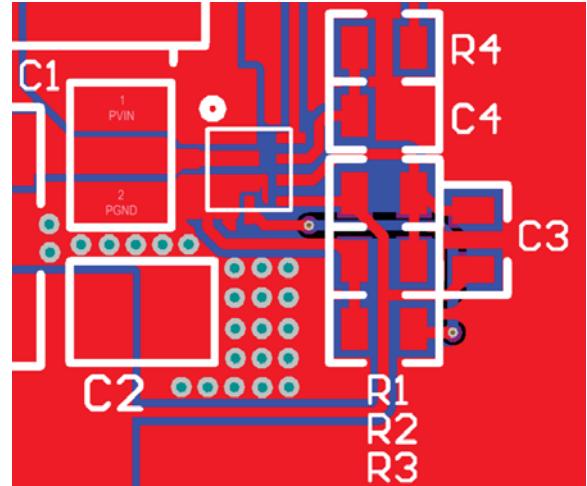


Figure 26. SKY87203 Evaluation Board Schematic

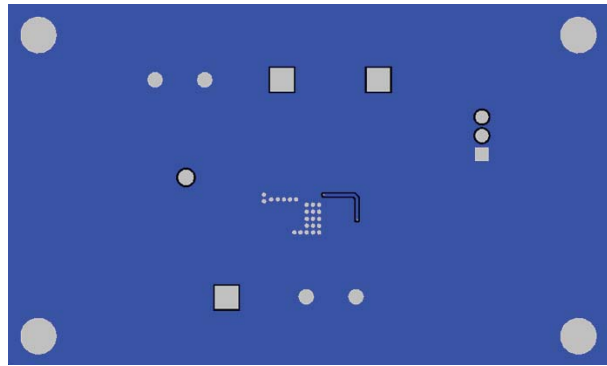
t0284



Top Layer



Detailed View



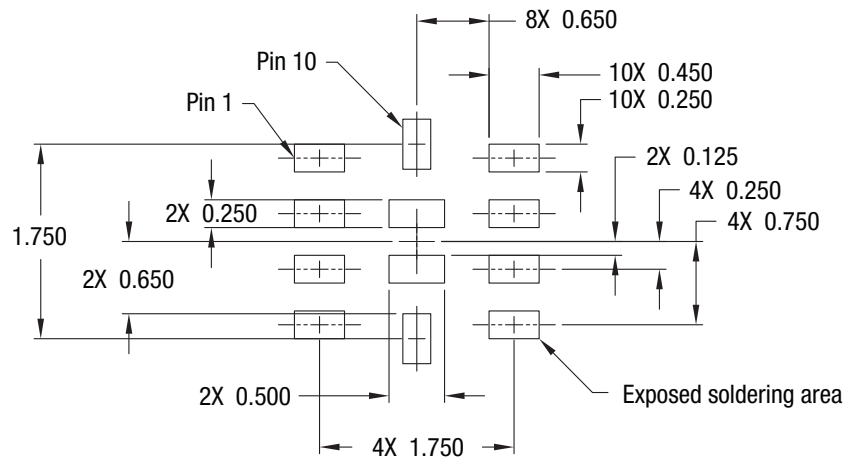
Bottom Layer

t0593

Figure 27. SKY87203 Evaluation Board Assembly Drawing

Table 8. Evaluation Board Bill of Materials (BOM)

Component	Value	Part Number	Manufacturer	Description
C1, C2	22 μ F	GRM219R61A226MEA0	Murata	Ceramic, 0805, X5R, 10 V, 20%
R1	294 $k\Omega$	RC0603FR-07294KL	Yageo	1/10 W, 1%, 0603, SMD
R2	57.6 $k\Omega$	RC0603FR-07457K6L	Yageo	1/10 W, 1%, 0603, SMD
R4	274 $k\Omega$	RC0603FR-07274KL	Yageo	1/10 W, 1%, 0603, SMD
L1	1 μ H	0520CDMCD5-1R0MC	Sumida	8 A, 17 $m\Omega$, SMD



Notes:

1. All dimensions are in millimeters.
2. The suggested land pattern should be used as a guideline only.
3. The assembly house should use a land pattern that fits their SMT process and environment.
4. Some of the key factors that affect the land pattern and solder stencil aperture opening are solder paste size, solder stencil thickness, and reflow profile.

t0587

Figure 28. SKY87203 PCB Layout Footprint

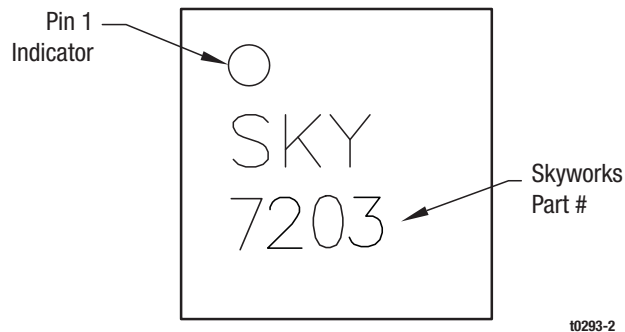
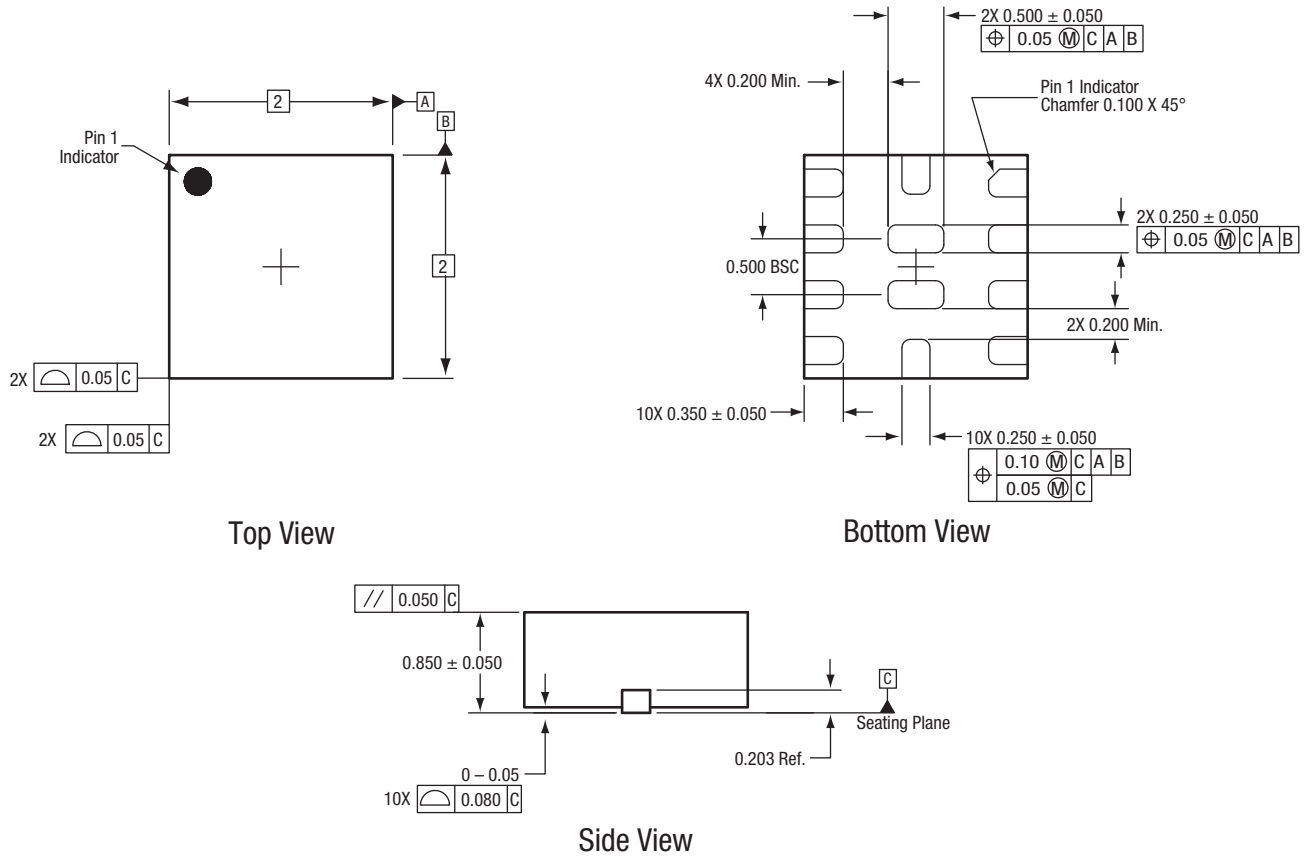


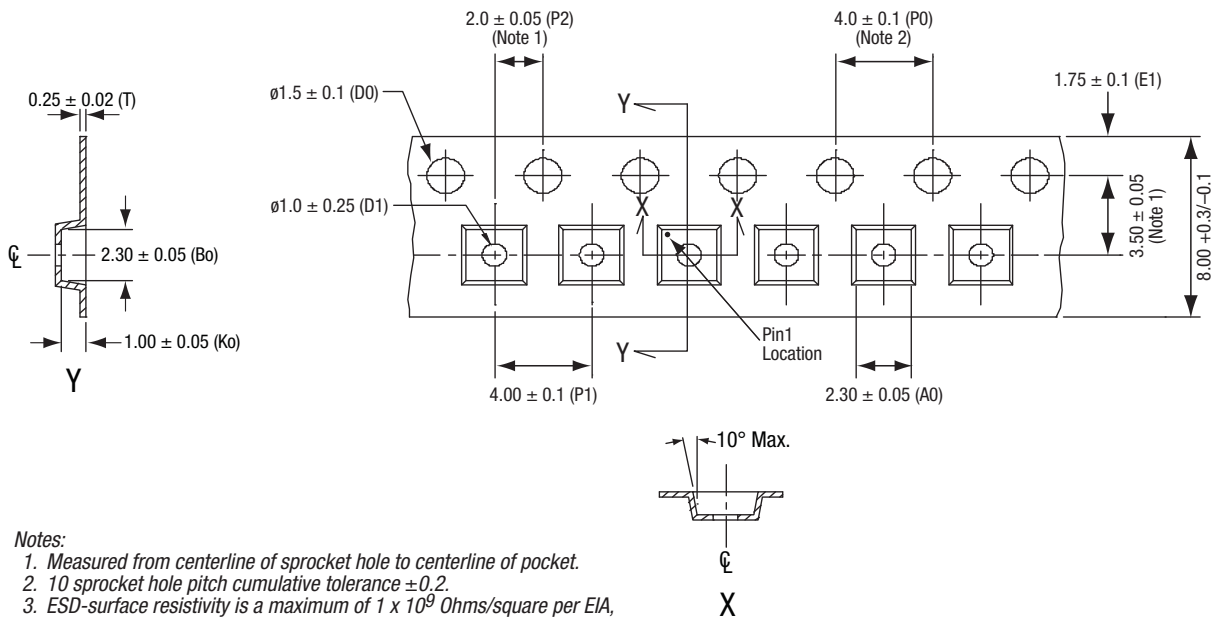
Figure 29. SKY87203 Typical Case Markings (Top View)



All measurements are in millimeters.

S3183

Figure 30. SKY87203 12-Pin QFN Package Dimensions



Notes:

1. Measured from centerline of sprocket hole to centerline of pocket.
2. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
3. ESD-surface resistivity is a maximum of 1×10^9 Ohms/square per EIA, JEDEC TNR Specification.
4. All measurements are in millimeters.

S3188

Figure 31. SKY87203 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY87203 Step-Down DC-DC Converter	SKY87203-11-631LF	SKY87203-11-631LF-EVB

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