



**THE DATASHEET OF
SA5534ADR2G**



NE5534, SA5534, SE5534, NE5534A, SA5534A, SE5534A

Operational Amplifier, Low Noise, Single

The NE/SA/SE5534/5534A are single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability, and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.).

Features

- Small-Signal Bandwidth: 10 MHz
- Output Drive Capability: 600 Ω , 10 V_{RMS} at V_S = ± 18 V
- Input Noise Voltage: 4 nV/ $\sqrt{\text{Hz}}$
- DC Voltage Gain: 100000
- AC Voltage Gain: 6000 at 10 kHz
- Power Bandwidth: 200 kHz
- Slew Rate: 13 V/ μs
- Large Supply Voltage Range: ± 3.0 to ± 20 V
- Pb-Free Packages are Available

Applications

- Audio Equipment
- Instrumentation and Control Circuits
- Telephone Channel Amplifiers
- Medical Equipment

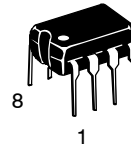


ON Semiconductor®

<http://onsemi.com>

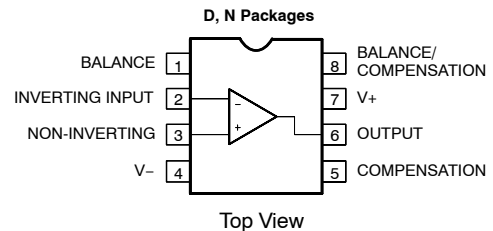


SOIC-8
D SUFFIX
CASE 751



PDIP-8
N SUFFIX
CASE 626

PIN CONNECTIONS



DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NE5534, SA5534, SE5534, NE5534A, SA5534A, SE5534A

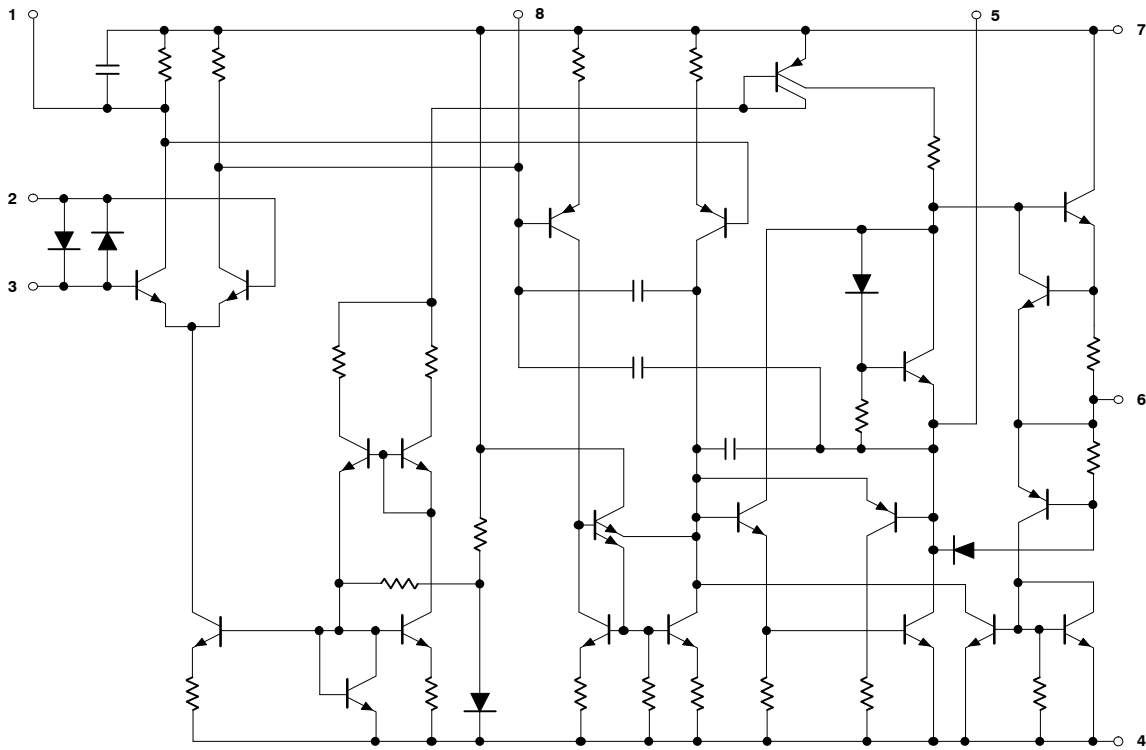


Figure 1. Equivalent Schematic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_S	± 22	V
Input Voltage	V_{IN}	$\pm V_{Supply}$	V
Differential Input Voltage (Note 1)	V_{DIFF}	± 0.5	V
Operating Temperature Range NE SA SE	T_{amb}	0 to +70 -40 to +85 -55 to +125	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}C$
Junction Temperature	T_j	150	$^{\circ}C$
Power Dissipation at 25 $^{\circ}C$	P_D	N Package D Package	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	N Package D Package	$^{\circ}C/W$
Output Short-Circuit Duration (Note 2)	-	Indefinite	-
Lead Soldering Temperature (10 sec max)	T_{slid}	230	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Diodes protect the inputs against overvoltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6 V. Maximum current should be limited to ± 10 mA.
2. Output may be shorted to ground at $V_S = \pm 15$ V, $T_{amb} = 25^{\circ}C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

NE5534, SA5534, SE5534, NE5534A, SA5534A, SE5534A

DC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$; $V_S = \pm 15\text{ V}$, unless otherwise noted.) (Notes 3, 4 and 5)

Characteristic	Symbol	Test Conditions	NE/SA5534/5534A			SE5534/5534A			Unit
			Min	Typ	Max	Min	Typ	Max	
Offset Voltage	V_{OS}	Overtemperature	-	0.5	4.0	-	0.5	2.0	mV
			-	-	5.0	-	-	3.0	mV
	$\Delta V_{OS}/\Delta T$		-	5.0	-	-	5.0	-	$\mu\text{V}/^{\circ}\text{C}$
Offset Current	I_{OS}	Overtemperature	-	20	300	-	10	200	nA
			-	-	400	-	-	500	nA
	$\Delta I_{OS}/\Delta T$		-	200	-	-	200	-	$\text{pA}/^{\circ}\text{C}$
Input Current	I_B	Overtemperature	-	500	1500	-	400	800	nA
			-	-	2000	-	-	1500	nA
	$\Delta I_B/\Delta T$		-	5.0	-	-	5.0	-	$\text{nA}/^{\circ}\text{C}$
Supply Current Per Op Amp	I_{CC}	Overtemperature	-	4.0	8.0	-	4.0	6.5	mA
			-	-	10	-	-	9.0	
Common Mode Input Range Common Mode Rejection Ratio Power Supply Rejection Ratio	V_{CM}		± 12	± 13	-	± 12	± 13	-	V
	CMRR		70	100	-	80	100	-	dB
	PSRR		-	10	100	-	10	50	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	A_{VOL}	$R_L \geq 600\ \Omega$, $V_O = \pm 10\text{ V}$ Overtemperature	25	100	-	50	100	-	V/mV
			15	-	-	25	-	-	
Output Swing	V_{OUT}	$R_L \geq 600\ \Omega$ Overtemperature	± 12	± 13	-	± 12	± 13	-	V
			± 10	± 12	-	± 10	± 12	-	
			± 15	± 16	-	± 15	16	-	
			± 13	± 13.5	-	± 13	± 13.5	-	
			± 12	± 12.5	-	± 12	± 12.5	-	
Input Resistance	R_{IN}		30	100	-	50	100	-	k Ω
Output Short Circuit Current	I_{SC}		-	38	-	-	38	-	mA

3. For NE5534/5534A, $T_{MIN} = 0^{\circ}\text{C}$, $T_{MAX} = 70^{\circ}\text{C}$.

4. For SA5534/5534A, $T_{MIN} = -40^{\circ}\text{C}$, $T_{MAX} = +85^{\circ}\text{C}$.

5. For SE5534/5534A, $T_{MIN} = -55^{\circ}\text{C}$, $T_{MAX} = +125^{\circ}\text{C}$.

NE5534, SA5534, SE5534, NE5534A, SA5534A, SE5534A

AC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_S = ± 15 V, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	NE/SA5534/5534A			SE5534/5534A			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Resistance	R _{OUT}	A _V = 30 dB closed-loop f = 10 kHz; R _L = 600 Ω; C _C = 22 pF	–	0.3	–	–	0.3	–	Ω
Transient Response		Voltage-follower V _{IN} = 50 mV R _L = 600 Ω, C _C = 22 pF, C _L = 100 pF							
Rise Time	t _R		–	20	–	–	20	–	ns
Overshoot	–		–	20	–	–	20	–	%
Transient Response		V _{IN} = 50 mV, R _L = 600 Ω, C _C = 47 pF, C _L = 500 pF							
Rise Time	t _R		–	50	–	–	50	–	ns
Overshoot	–		–	35	–	–	35	–	%
Gain	A _V	f = 10 kHz, C _C = 0 f = 10 kHz, C _C = 22 pF	–	6.0 2.2	–	–	6.0 2.2	–	V/mV
Gain Bandwidth Product	GBW	C _C = 22 pF, C _L = 100 pF	–	10	–	–	10	–	MHz
Slew Rate	SR	C _C = 0 C _C = 22 pF	–	13 6.0	–	–	13 6.0	–	V/μs
Power Bandwidth	–	V _{OUT} = ± 10 V, C _C = 0 pF V _{OUT} = ± 10 V, C _C = 22 pF V _{OUT} = ± 14 V, R _L = 600 Ω, C _C = 22 pF, V _{CC} = ± 18 V	–	200 95 70	–	–	200 95 70	–	kHz

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_S = 15 V, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	NE/SA/SE5534			NE/SA/SE5534A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Noise Voltage	V _{NOISE}	f _O = 30 Hz f _O = 1.0 kHz	–	7.0 4.0	–	–	5.5 3.5	7.0 4.5	nV/√Hz
Input Noise Current	I _{NOISE}	f _O = 30 Hz f _O = 1.0 kHz	–	2.5 0.6	–	–	1.5 0.4	–	pA/√Hz
Broadband Noise Figure	–	f = 10 Hz to 20 kHz; R _S = 5.0 kΩ	–	–	–	–	0.9	–	dB
Channel Separation	–	f = 1.0 kHz; R _S = 5.0 kΩ	–	110	–	–	110	–	dB

TYPICAL PERFORMANCE CHARACTERISTICS

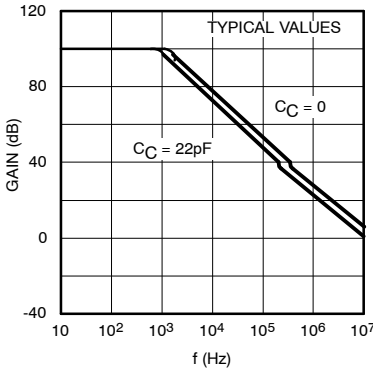


Figure 2. Open-Loop Frequency Response

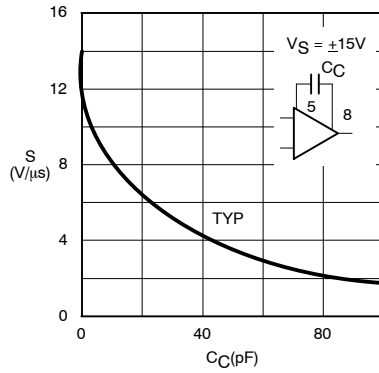


Figure 3. Slew Rate as a Function of Compensation Capacitance

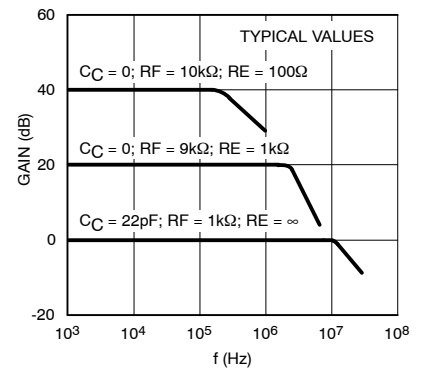


Figure 4. Closed-Loop Frequency Response

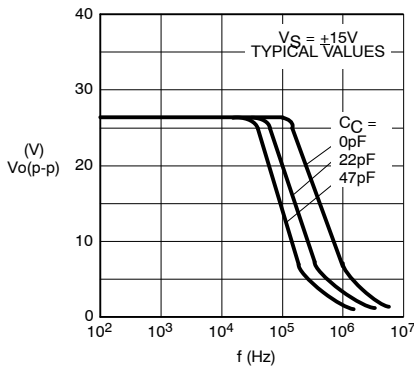


Figure 5. Large-Signal Frequency Response

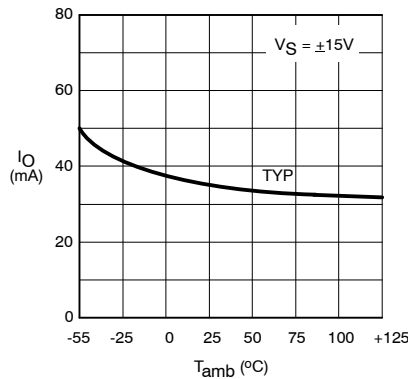


Figure 6. Output Short-Circuit Current

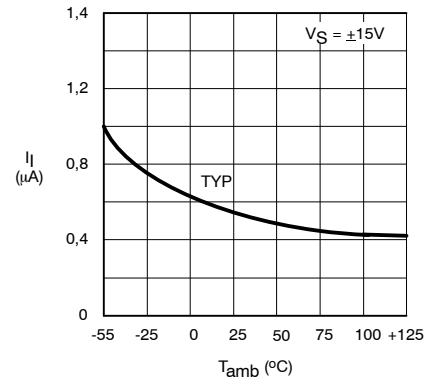


Figure 7. Input Bias Current

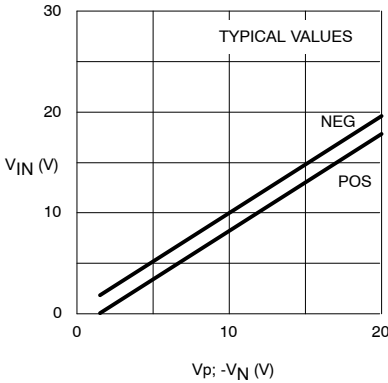


Figure 8. Input Common-Mode Voltage Range

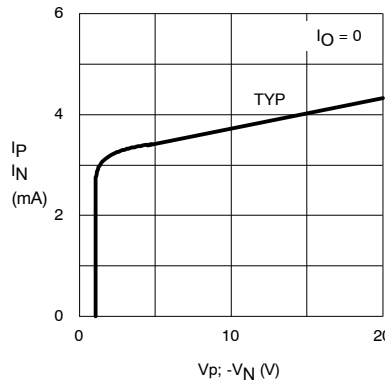


Figure 9. Supply Current Per Op Amp

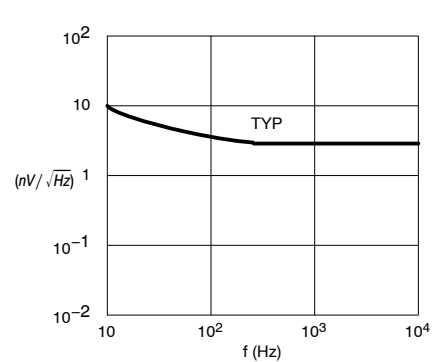


Figure 10. Input Noise Voltage Density

TYPICAL PERFORMANCE CHARACTERISTICS

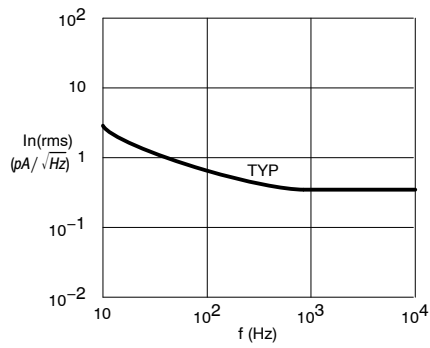


Figure 11. Input Noise Current Density

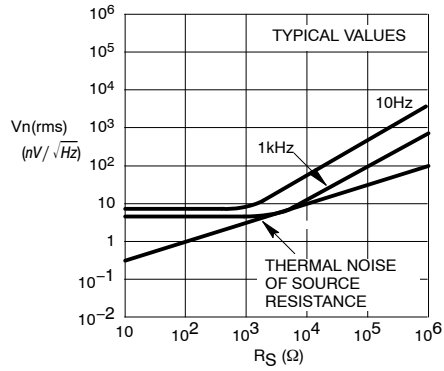


Figure 12. Total Input Noise Density

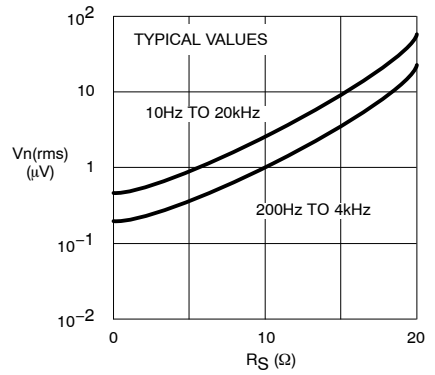


Figure 13. Broadband Input Noise Voltage

TEST LOAD CIRCUITS

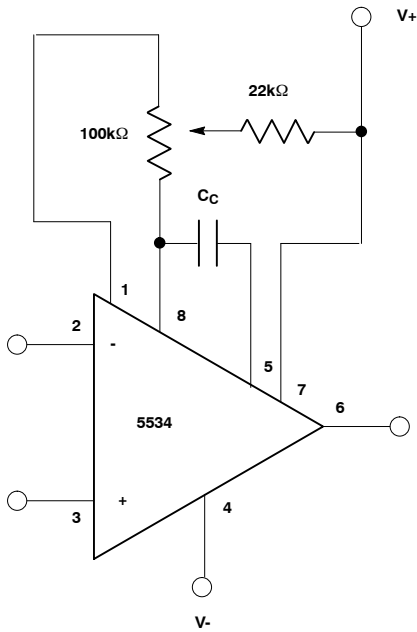


Figure 14. Frequency Compensation and Offset Voltage Adjustment Circuit

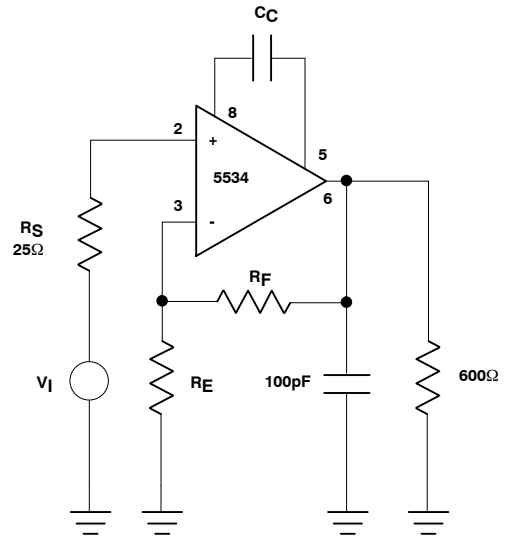


Figure 15. Closed-Loop Frequency Response

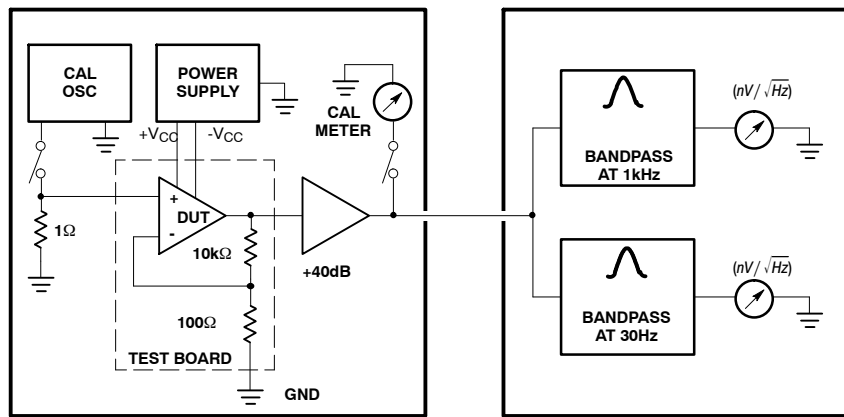
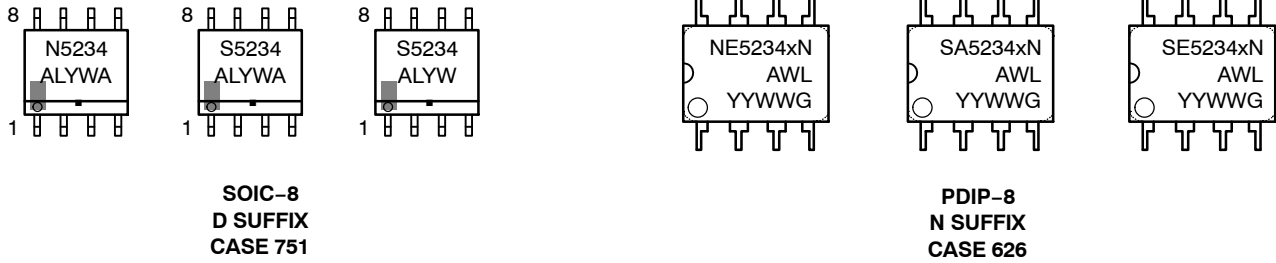


Figure 16. Noise Test Block Diagram

NE5534, SA5534, SE5534, NE5534A, SA5534A, SE5534A

MARKING DIAGRAMS



x = Blank or A
 A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package

ORDERING INFORMATION

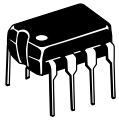
Device	Description	Temperature Range	Shipping [†]
NE5534AD	8-Pin Plastic Small Outline (SO-8) Package	0 to +70°C	98 Units / Rail
NE5534ADG	8-Pin Plastic Small Outline (SO-8) Package (Pb-Free)	0 to +70°C	98 Units / Rail
NE5534ADR2	8-Pin Plastic Small Outline (SO-8) Package	0 to +70°C	2500 / Tape & Reel
NE5534ADR2G	8-Pin Plastic Small Outline (SO-8) Package (Pb-Free)	0 to +70°C	2500 / Tape & Reel
NE5534AN	8-Pin Plastic Dual In-Line Package (PDIP-8)	0 to +70°C	50 Units / Rail
NE5534ANG	8-Pin Plastic Dual In-Line Package (PDIP-8) (Pb-Free)	0 to +70°C	50 Units / Rail
NE5534D	8-Pin Plastic Small Outline (SO-8) Package	0 to +70°C	98 Units / Rail
NE5534DG	8-Pin Plastic Small Outline (SO-8) Package (Pb-Free)	0 to +70°C	98 Units / Rail
NE5534DR2	8-Pin Plastic Small Outline (SO-8) Package	0 to +70°C	2500 / Tape & Reel
NE5534DR2G	8-Pin Plastic Small Outline (SO-8) Package (Pb-Free)	0 to +70°C	2500 / Tape & Reel
NE5534N	8-Pin Plastic Dual In-Line Package (PDIP-8)	0 to +70°C	50 Units / Rail
NE5534NG	8-Pin Plastic Dual In-Line Package (PDIP-8) (Pb-Free)	0 to +70°C	50 Units / Rail
SA5534AD	8-Pin Plastic Small Outline (SO-8) Package	-40 to +85°C	98 Units / Rail
SA5534ADG	8-Pin Plastic Small Outline (SO-8) Package (Pb-Free)	-40 to +85°C	98 Units / Rail
SA5534ADR2	8-Pin Plastic Small Outline (SO-8) Package	-40 to +85°C	2500 / Tape & Reel
SA5534ADR2G	8-Pin Plastic Small Outline (SO-8) Package (Pb-Free)	-40 to +85°C	2500 / Tape & Reel
SA5534AN	8-Pin Plastic Dual In-Line Package (PDIP-8)	-40 to +85°C	50 Units / Rail
SA5534ANG	8-Pin Plastic Dual In-Line Package (PDIP-8) (Pb-Free)	-40 to +85°C	50 Units / Rail
SA5534N	8-Pin Plastic Dual In-Line Package (PDIP-8)	-40 to +85°C	50 Units / Rail
SA5534NG	8-Pin Plastic Dual In-Line Package (PDIP-8) (Pb-Free)	-40 to +85°C	50 Units / Rail
SE5534AN	8-Pin Plastic Dual In-Line Package (PDIP-8)	-55 to +125°C	50 Units / Rail
SE5534ANG	8-Pin Plastic Dual In-Line Package (PDIP-8) (Pb-Free)	-55 to +125°C	50 Units / Rail
SE5534N	8-Pin Plastic Dual In-Line Package (PDIP-8)	-55 to +125°C	50 Units / Rail
SE5534NG	8-Pin Plastic Dual In-Line Package (PDIP-8) (Pb-Free)	-55 to +125°C	50 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

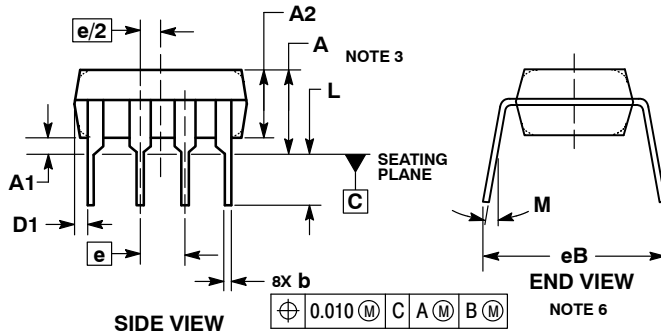
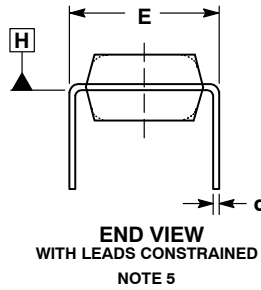
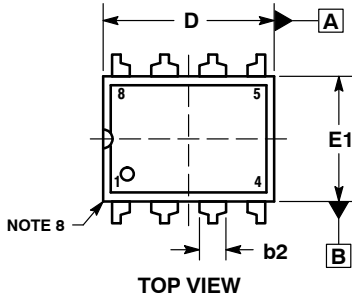
ON Semiconductor®



SCALE 1:1

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015

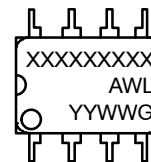


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

- STYLE 1:
1. AC IN
 2. DC + IN
 3. DC - IN
 4. AC IN
 5. GROUND
 6. OUTPUT
 7. AUXILIARY
 8. V_{CC}

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP-8	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

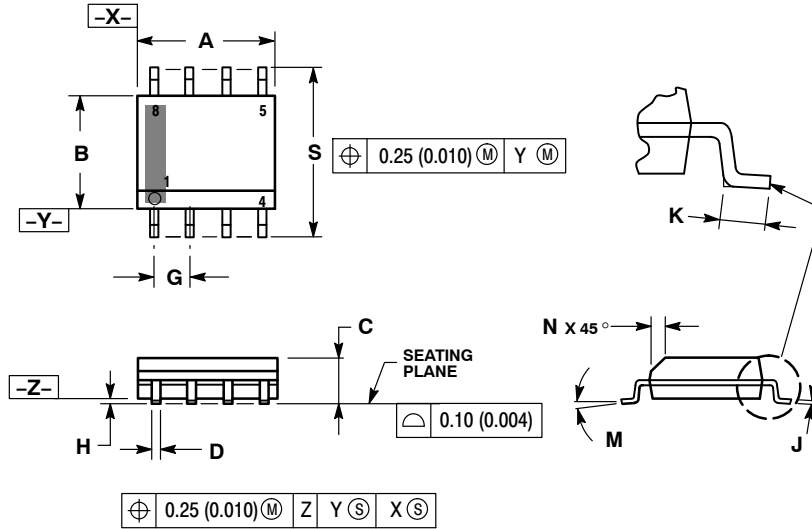
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

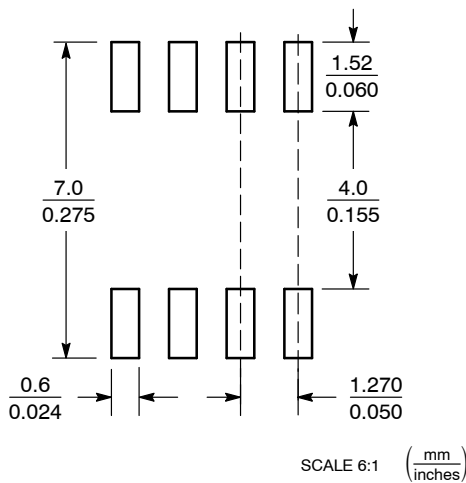
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales



Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SA5534ADR2G on WIN SOURCE](#)

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management