THE DATASHEET OF

PT7C4372AZEEX

Real-time Clock Module (I2C Bus)

Features

- ➔External Quartz Oscillator 32.000 kHz and 32.768 kHz selectable.
- ➔Supports I²C-Bus's high speed mode (400 kHz)
- ➔Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- ➔Select between 12-hr and 24-hr clock display
- ➔Auto calculation of leap years until 2099
- ➔Built-in high-precision clock precision control logic
- ➔Interrupt generation function (cycle time range: 1 month to 0.5 seconds, includes interrupt flags and interrupt stop function)
- ➔Alarm functions (Alarm_A: Day/Hour/Min)
- ➔32-kHz clock output (/INTB output)
- ➔Oscillation stop detection function (used to determine presence of internal data)
- ➔Wide Time keeping voltage range: 1.3 V to 6 V
- ➔Wide interface voltage range: 1.8 V to 6 V
- ➔Low current consumption: 0.4 μA/3.0 V (Typ.)
- ➔Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- ➔Halogen and Antimony Free. "Green" Device (Note 3)
- ➔For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- ➔Packaging (Pb-free & Green):
  - •8-pin, TSSOP (L)
  - •8-pin, SOIC (W)

Description

PT7C4372A and PT7C4372C are I²C bus interface-compliant real-time clocks that have been adjusted for high precision. In addition to providing a function for generating six types of interrupts, a dual alarm function, an oscillation stop detection function (used to determine presence of valid internal data at power-on), they includes a digital clock precision adjustment function that can be used to set various levels of precision.

Since the internal oscillation circuit is driven at a constant voltage, 32-kHz clock output is stable and free of voltage fluctuation effects.

Table 1 shows the diverse functions of the two RTC circuits. More details are shown in section Overview of Functions.

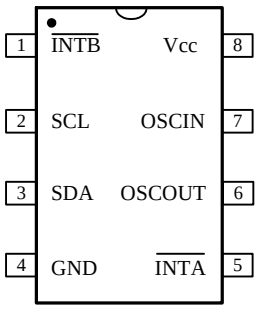
Table 1. Diverse functions of RTC circuits

Item	Function	PT7C4372A/4372C
1	Clock	√
2	Clock adjustment	√ Unit ±3.051ppm for 32.768kHz crystal; ±3.125ppm for 32.000kHz crystal
3	Period interrupt	√ Output from /INTA and /INTB
4	Alarm	√ /INTA: Alarm_A; /INTB: Alarm_B
5	Oscillation detect	√
6	32-kHz clock output	√ via /INTB enabled by register
7	I²C bus interface with CPU	√
8	Crystal	√ External, 32.768kHz or 32.000kHz selectable

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration

PT7C4372A/C

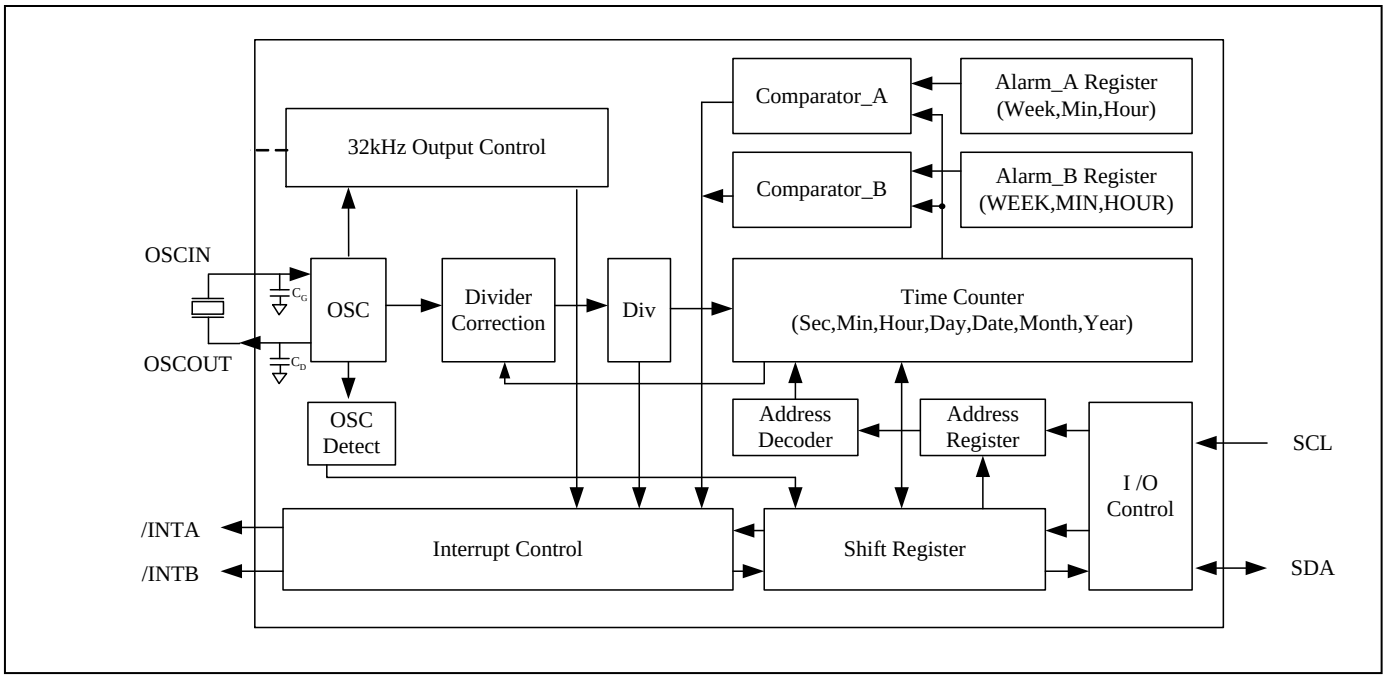


TSSOP
SOIC

Pin Description

Pin#	Pin Name	Type	Description
1	/INTB	O	**Interrupt B (Open Drain).** It outputs alarm interrupts and periodic interrupts.
2	SCL	I	**Serial Clock Line.** It is for I^2C communication. Data input and output across SDA pin is synchronized with this clock. Up to 6V beyond Vcc may be input.
3	SDA	I/O	**Serial Data Line (Open Drain output).** This line is for transferring I^2C bus format data. When input, up to 6V beyond VCC may be used. When output, it is an open drain output pin.
4	GND	P	**Ground**
5	/INTA	O	**Interrupt A (Open Drain).** It outputs alarm interrupts and periodic interrupts.
6	OSCOUT	O	**Oscillator Circuit Output.** Together with OSCIN, an crystal oscillator is connected between them.
7	OSCIN	I	**Oscillator Circuit Input.** See OSCOUT pin description.
8	Vcc	P	**Power**

Block Diagram



Function Description

Overview of Functions

Clock Function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

Clock Precision Adjustment Function

They have two internal oscillation circuit capacitors, so that an oscillation circuit may be configured simply by externally connecting a crystal. Either 32.768kHz or 32.000kHz crystal may be selected to setting the internal register appropriately.
The clock precision can be adjusted forward or back in units of ±3.051 ppm (32.768kHz crystal) or ±3.125 ppm (32.000kHz crystal) and oscillation frequency can be adjusted in ±189 ppm (32.768kHz crystal) or ±194 ppm (32.000kHz crystal).

This function can be used to implement a higher-precision clock function, such as by:

- Enabling higher clock precision throughout the year by taking seasonal clock precision adjustments into account in advance, or
- Enabling correction of temperature-related clock precision variation in systems that include a temperature detecting function.

Periodic Interrupt

- **PT7C4372A/C**

Periodic interrupts can be output via the /INTA and /INTB pins.
Select among five Periodic frequency settings: 2 Hz (every 0.5 seconds), 1 Hz (every second), 1/60 Hz (every minute), 1/3600Hz (every hour), or monthly.
Select among two output waveforms for periodic interrupts: ordinary pulse waveform (2 Hz or 1 Hz) or waveforms (every second, minute, hour, or month) for CPU-level interrupts that can support CPU interrupts.
A polling function is also provided to enable monitoring of pin states via registers.

Alarm Function

- **PT7C4372A/C**

This module is has two alarm system (Alarm_A and Alarm_B) that outputs interrupt signals from /INTA or /INTB to CPU when the day of the week, hour or minute corresponds to the setting. Each of them may output interrupt signal separately at a specified time. The alarm may be selectable between on and off for each day of the week, thus allowing outputting alarm everyday or on a specific day of the week.

The Alarm_A is output from the /INTA pin while the Alarm_B is output from either the /INTA or the /INTB pins. Polling is possible separately for each alarm function.

Oscillation Stop Detection Function, Power Drop Detection Function (Voltage Monitoring Function), And Power-On Reset Detection Function

PT7C4372A/ C have only oscillation stop detection function.
The oscillation stop detection function uses registers to record if clock data is valid or invalid. This function may be used to determine if the PT7C4372A/C supply power has been booted from 0V and if it has been backed up.

Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).
Since the output of the I/O pin of SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.
The SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

32-kHz Clock Output

The 32.768 kHz clock (32.768kHz crystal) or 32.000kHz clock (32.000kHz crystal) can be output via the /INTB by setting corresponding register.

Note: The precision of this 32.768 kHz clock output via the FOUT pin can not be adjusted (even when using the clock precision adjustment function).

Registers

Allocation of Registers

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Second	-*5	S40	S20	S10	S8	S4	S2	S1
1	Minutes	-	M40	M20	M10	M8	M4	M2	M1
2	Hours	-	-	H20 or P, /A	H10	H8	H4	H2	H1
3	Days of the week	-	-	-	-	-	W4	W2	W1
4	Days	-	-	D20	D10	D8	D4	D2	D1
5	Months	-	-	-	M10	M8	M4	M2	M1
6	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
7	Time Trimming	/XSL	F6	F5	F4	F3	F2	F1	F0
8	Alarm_A: Minute	-	AM40	AM20	AM10	AM8	AM4	AM2	AM1
9	Alarm_A: Hour	-	-	AH20 or AP, /A	AH10	AH8	AH4	AH2	AH1
A	Alarm_A: Day	-	AW6	AW5	AW4	AW3	AW2	AW1	AW0
B	Alarm_B: Minute	-	BM40	BM20	BM10	BM8	BM4	BM2	BM1
C	Alarm_B: Hour	-	-	BH20 or BP, /A	BH10	BH8	BH4	BH2	BH1
D	Alarm_B: Day	-	BW6	BW5	BW4	BW3	BW2	BW1	BW0
E	Control 1	AALE	BALE	SL2	SL1	TEST*2	CT2	CT1	CT0
F	Control 2	-	-	/12, 24	ADJ or XSTP*3	/CLEN	CTFG	AAFG	BAFG

Caution points:

*1. All bits marked with "-" are read-only bits. Their value when read is always "0".
*2. The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit.
*3. ADJ is for write and XTSP is for read operation. The XTSP bit is set to “0” by writing data into the control register 2 for normal oscillation. When XSTP is set to “1”, the Time Trimming register, Control 1 register, /CLEN and TEST bits are reset to “0”.
*4. All bits marked with "-" are read-only bits. Their value when read is always "0".

Control Register 1

PT7C4372A

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
E	Control 1	AALE	BALE	SL2	SL1	TEST	CT2	CT1	CT0
	(default)	0	0	0	0	0	0	0	0

PT7C4372C

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
E	Control 1	AALE	BALE	SL2	SL1	TEST	CT2	CT1	CT0
	(default)	0	0	0	0	0	0	1	1

- **AALE, BALE**

Alarm_A, Alarm_B enable bits.

AALE, BALE	Data	Description	
Read / Write	0	Alarm_A (Alarm_B) correspondence action invalid	Default
	1	Alarm_A (Alarm_B) correspondence action valid	

See section "Alarm Function" for more detail.

- **SL2, SL1**

Interrupt output select bits. Two alarm pulses (Alarm_A and alarm_B), periodic interrupt output (INT), 32kHz clock pulses may be output to the /INTA or /INTB pins selectively by SL1 and SL2.

SL2	SL1	Description	
0	0	Output Alarm_A, Alarm_B, INT to the /INTA. Output 32kHz clock pulses to /INTB.	Default
0	1	Output Alarm_A, INT to the /INTA. Output 32kHz clock pulses, Alarm_B to /INTB.	
1	0	Output Alarm_A, Alarm_B to the /INTA. Output 32kHz clock pulses, INT to /INTB.	
1	1	Output Alarm_A to the /INTA. Output 32kHz clock pulses, Alarm_B, INT to /INTB.	

- **TEST**

TEST	Data	Description	
Read / Write	0	Ordinary operation mode	Default
	1	Test mode	

- **CT2, CT1, CT0**

Periodic interrupt output select bits.

CT2	CT1	CT0	Description		
			Wave Form Mode	Cycle / Falling Timing	
0	0	0	-	Off (“H”)	Default
0	0	1	-	Fixed at “L”	
0	1	0	Pulse	2Hz (duty 50%)	
0	1	1	Pulse	1Hz (duty 50%)	
1	0	0	Level	Every second (synchronized with second count up)	
1	0	1	Level	Every minute (Occurs when seconds reach ":00")	
1	1	0	Level	Every hour (Occurs when minutes and seconds reach "00:00")	
1	1	1	Level	Every month (Occurs at 00:00:00 on first day of month)	

See section 6.5 for more detail.

Control Register 2

PT7C4372A

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
F	Control 2	-	-	/12, 24	ADJ or XSTP	/CLEN	CTFG	AAFG	BAFG
	(default)	0	0	Undefined	1	0	0	0	0

D4 when read is used as ADJ, when write is used as XSTP.

PT7C4372C

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
F	Control 2	-	-	/12, 24	ADJ or XSTP	/CLEN	CTFG	AAFG	BAFG
	(default)	0	0	1	1	1	0	0	0

D4 when read is used as ADJ, when write is used as XSTP.

- **/12, 24**

/12, 24 time display selection bit.

/12, 24	Data	Description	
Read/ Write	0	12-hour time display	* Default
	1	24-hour time display	

See section “Alarm Function” for more detail.

PT7C4372C

/12, 24 time display selection bit.

/12, 24	Data	Description	
Read/ Write	0	12-hour time display	
	1	24-hour time display	* Default

See section “Alarm Function” for more detail.

- **ADJ or XSTP**

  ADJ: 30 second adjust bit. Second is adjusted within 122μs (within 125μs when 32.000kHz crystal is used) from writing operation to ADJ.

ADJ	Data	Description
Write	0	Ordinary operation.
	1	Second adjustment. 1) For second range from "00" to "29", second is reset to "00"; 2) For second range from "30" to "59", second is reset to "00" and minute is incremented by 1.

  XSTP: oscillator halt sensing bit.

XSTP	Data	Description	
Read	0	Ordinary oscillation.	
	1	Oscillator halts sensing.	Default

See section "Oscillation Stop Detection".

- **/CLEN**

  PT7C4372A FOUT 32-kHz clock output enabled bit.

/CLEN	Data	Description	
Read	0	32-kHz clock (frequency same as crystal's) output enabled.	Default
	1	32-kHz clock output disabled.	

PT7C4372C FOUT 32-kHz clock output enabled bit.

/CLEN	Data	Description	
Read	0	32-kHz clock (frequency same as crystal's) output enabled.	
	1	32-kHz clock output disabled.	Default

- **CTFG**

CTFG	Data	Description	
Read	0	Periodic interrupt output OFF status; /INTA or /INTB= OFF (Hi-z) Read	Default
	1	Periodic interrupt output ON status; /INTA or /INTB= "L"	
Write	0	A "0" can be written only when the periodic interrupt is in level mode, at which time the /INTA or /INTB pin is set to OFF ("H") status. After a "0" is written, the value still becomes "1" again at the next cycle.	Default
	1	Setting prohibited	

See section "Related Registers" for more detail.

- **AAFG, BAFG**

AAFG,BAFG	Data	Description	
Read	0	Alarm register does not match current time	Default
	1	Alarm register match current time	
Write	0	/INTA or /INTB pin = OFF (H)	Default
	1	Setting prohibited	

See section "Alarm Function" for more detail.

Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
0	Seconds	-	S40	S20	S10	S8	S4	S2	S1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
1	Minutes	-	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
2	Hours	-	-	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Any registered imaginary time should be replaced with correct time; otherwise it will cause the clock counter malfunction.

Days of the week Counter

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
3	Days of the week	-	-	-	-	-	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

"-" indicates write-protected bits. A zero is always read from these bits.

The day counter is a divide-by-7 counter that counts from 00 to 01 and up 06 before starting again from 01.
The correspondence between days and count values is shown below.

Days	W4	W2	W1	Day	Remark
Write / Read	0	0	0	Sunday	00 h
	0	0	1	Monday	01 h
	0	1	0	Tuesday	02 h
	0	1	1	Wednesday	03 h
	1	0	0	Thursday	04 h
	1	0	1	Friday	05 h
	1	1	0	Saturday	06 h
Write prohibit	1	1	1	-	Do not enter a setting for this bit.

Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
4	Days	-	-	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
5	Months	-	-	-	M10	M8	M4	M2	M1
	(default)	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
6	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Any registered imaginary time should be replaced with correct time; otherwise it will cause the clock counter malfunction.

Time Trimming Register

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
7	Time trimming	/XSL	F6	F5	F4	F3	F2	F1	F0
	(default)	0	0	0	0	0	0	0	0

Note: Time trimming function only adjusts clock timing. Oscillation frequency and 32-kHz clock output is not adjusted.

- **/XSL bit**

The /XSL bit is used to select frequency of the crystal.

/XSL	Frequency of the crystal (kHz)
0	32.768
1	32.000

- **F6 to F0**

Implement a higher-precision clock function. See section "**Clock Precision Adjustment Function**".

Alarm Register

See section "Alarm Function" for more details.

- **Alarm_A, Alarm_B Register**

Alarm_A, Alarm_B can output alarm pulses at the time set as the day-of-the-week, hour, minute (e.g. Monday 7:00 a.m. every day of weeks).

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
8	Alarm_A: Minute	-	AM40	AM20	AM10	AM8	AM4	AM2	AM1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
9	Alarm_A: Hour	-	-	AH20, or AP,/A	AH10	AH8	AH4	AH2	AH1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
A	Alarm_A: Day	-	AW6	AW5	AW4	AW3	AW2	AW1	AW0
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
B	Alarm_B: Minute	-	BM40	BM20	BM10	BM8	BM4	BM2	BM1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
C	Alarm_B: Hour	-	-	BH20, or BP,/A	BH10	BH8	BH4	BH2	BH1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
D	Alarm_B: Day	-	BW6	BW5	BW4	BW3	BW2	BW1	BW0
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Clock Precision Adjustment Function

Adjustment Range

Adjustment range (ppm)	Adjustment unit (ppm)	Internal timing of adjustment
-189.1 to +189.1	±3.05 *	Once every 20 seconds at "00", "20", "40" seconds

* Note: add or decrement 2 clock pulses every 20s: 2/(32,768×20) = 3.051ppm (or 3.125ppm when 32.000kHz crystal is used).

Adjustment Amount and Adjustment Value

Adjustment amount (ppm)	Adjustment data		bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	Decimal	Hexadecimal	F6	F5	F4	F3	F2	F1	F0
-189.10	+63	3F h	0	1	1	1	1	1	1
-186.05	+62	3E h	0	1	1	1	1	1	0
-183.00	+61	3D h	0	1	1	1	1	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
-9.15	+4	04 h	0	0	0	0	1	0	0
-6.10	+3	03 h	0	0	0	0	0	1	1
-3.05	+2	02 h	0	0	0	0	0	1	0
OFF	+1	01 h	0	0	0	0	0	0	1
OFF	0	00 h	0	0	0	0	0	0	0
+3.05	-1	7F h	1	1	1	1	1	1	1
+6.10	-2	7E h	1	1	1	1	1	1	0
+9.15	-3	7D h	1	1	1	1	1	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
+183.00	-60	44 h	1	0	0	0	1	0	0
+186.05	-61	43 h	1	0	0	0	0	1	1
+189.10	-62	42 h	1	0	0	0	0	1	0
OFF	-63	41 h	1	0	0	0	0	0	1
OFF	-64	40 h	1	0	0	0	0	0	0

Examples:

(1) Setting time forward

Adjust (advance) the clock precision when FOUT clock output is 32767.7 Hz

- Determine the current amount of variance

  (32767.7 -32768) / 32768 = -9.16×10^{-6}

  *[32768] = Reference values
- Calculate the optimum adjustment data (decimal value) relative to the current variance.

  Adjustment data = variance / adjustment resolution = -9.16 / 3.05 ≈ -3
- Calculate the setting adjustment data (hexadecimal)

  Setting adjustment data = 128 -3 (80 h – 03h) = 125 (7D h)

(2) Setting time backward

Adjust (set back) the clock precision when FOUT clock output is 32768.3 Hz

- Determine the current amount of variance

  (32768.3 -32768) / 32768 = $+9.16 \times 10^{-6}$
- Calculate the optimum adjustment data (decimal value) relative to the current variance.

  Adjustment data = (variance / adjustment resolution) + 1 = (+9.16 / 3.05) + 1 ≈ +4

  *Add 1 since reference value is 01h
- Calculate the setting adjustment data (hexadecimal)

  Setting adjustment data = 04 h

Alarm Function

These part no have Alarm A and Alarm B functions which can all output alarm pulses at the preset days of the week, hours and minutes.

Related Register

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Minutes	-	M40	M20	M10	M8	M4	M2	M1
2	Hours	-	-	H20 or P, /A	H10	H8	H4	H2	H1
3	Days of the week	-	-	-	-	-	W4	W2	W1
8	Alarm_A: Minute	-	AM40	AM20	AM10	AM8	AM4	AM2	AM1
9	Alarm_A: Hour	-	-	AH20 or AP, /A	AH10	AH8	AH4	AH2	AH1
A	Alarm_A: Day	-	AW6	AW5	AW4	AW3	AW2	AW1	AW0
B	Alarm_B: Minute	-	BM40	BM20	BM10	BM8	BM4	BM2	BM1
C	Alarm_B: Hour	-	-	BH20 or BP, /A	BH10	BH8	BH4	BH2	BH1
D	Alarm_B: Day	-	BW6	BW5	BW4	BW3	BW2	BW1	BW0
E	Control 1	AALE	BALE	SL2	SL1	TEST	CT2	CT1	CT0
F	Control 2	-	-	/12, 24	ADJ or XSTP	CLEN	CTFG	AAFG	BAFG

- **AALE, BALE:**

This bit is used to set up the Alarm A/B function (to generate alarms matching day, hour, or minute settings).

AALE, BALE	Data	Description	
Read / Write	0	Alarm_A (Alarm_B) correspondence action invalid	Default
	1	Alarm_A (Alarm_B) correspondence action valid	

* When using the Alarm A (or B) function, first set this AALE (or BALE) bit value as "0" to stop the function. Next, set the day, hour, minute, and set the AAFG (or BAFG) bit to 0. Finally, set "1" to the AALE (or BALE) bit to set the Alarm A (or B) function as valid. The reason for first setting the AALE (or BALE) bit value as "0" is to prevent /INTB or /INTA = "L" output in the event that a match between the current time and alarm setting occurs while the alarm setting is still being made.

- **AAFG, BAFG:**

These bits are valid only when the AALE, BALE bits value are "1". When a match occurs between the Alarm A or Alarm B setting and the current time, the AAFG or BAFG bit value becomes "1" approximately 61 μs afterward. (There is no effect when the AALE or BALE bit becomes "0".) The /INTB or /INTA = "L" status that is set at this time can be set to OFF by writing a "0" to these bits.

AAFG,BAFG	Data	Description	
Read	0	Alarm register does not match current time	Default
	1	Alarm register match current time	
Write	0	/INTA or /INTB pin = OFF (H)	Default
	1	Setting prohibited	

- **SL2, SL1:**

Interrupt output select bits. Two alarm pulses (Alarm_A and alarm_B), periodic interrupt output (INT), 32kHz clock pulses may be output to the /INTA or /INTB pins selectively by SL1 and SL2.

SL2	SL1	Description	
0	0	Output Alarm_A, Alarm_B, INT to the /INTA. Output 32kHz clock pulses to /INTB.	Default
0	1	Output Alarm_A, INT to the /INTA. Output 32kHz clock pulses, Alarm_B to /INTB.	
1	0	Output Alarm_A, Alarm_B to the /INTA. Output 32kHz clock pulses, INT to /INTB.	
1	1	Output Alarm_A to the /INTA. Output 32kHz clock pulses, Alarm_B, INT to /INTB.	

- **/12, 24:**

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12/24	Description	Time
0	12-hour time display	
1	24-hour time display	

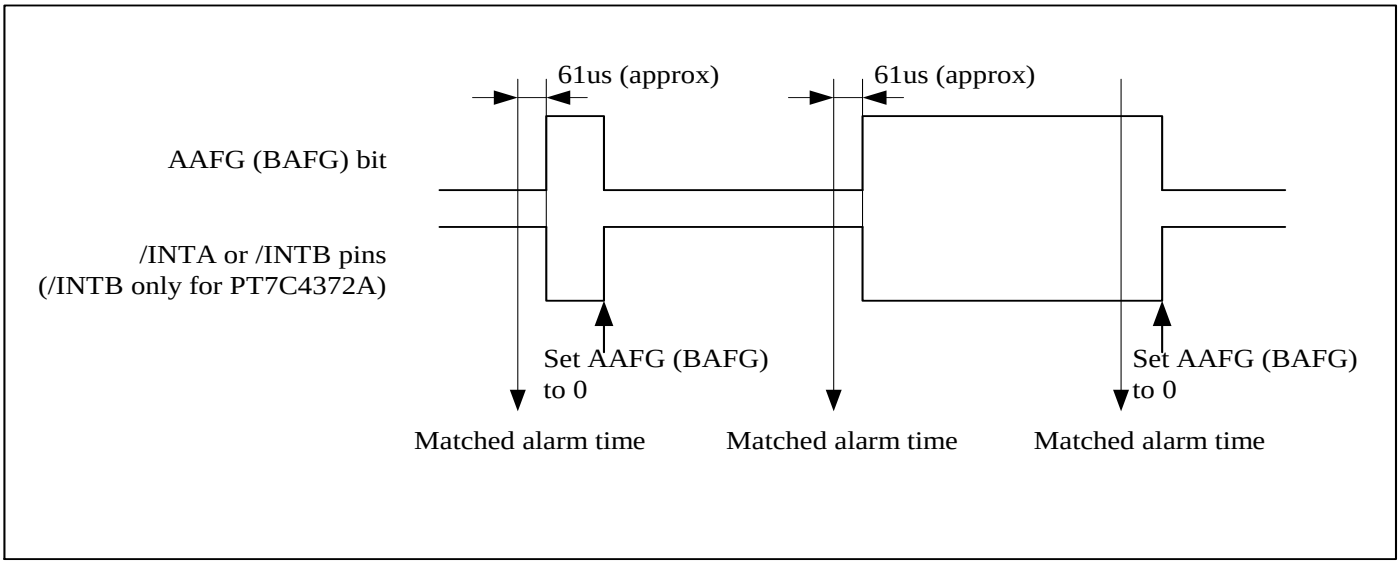
24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	12 (AM 12)	12	32 (PM 12)
01	01 (AM 01)	13	21 (PM 01)
02	02 (AM 02)	14	22 (PM 02)
03	03 (AM 03)	15	23 (PM 03)
04	04 (AM 04)	16	24 (PM 04)
05	05 (AM 05)	17	25 (PM 05)
06	06 (AM 06)	18	26 (PM 06)
07	07 (AM 07)	19	27 (PM 07)
08	08 (AM 08)	20	28 (PM 08)
09	09 (AM 09)	21	29 (PM 09)
10	10 (AM 10)	22	30 (PM 10)
11	11 (AM 11)	23	31 (PM 11)

* Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

Examples:

Alarm time settings	Alarm_A/B: Day-of-the-week							Alarm_A/B: Hour		Alarm_A/B: Minute
	Sun. AW0	Mon. AW1	Tue. AW2	Wed. AW3	Thu. AW4	Fri. AW5	Sat. AW6	24-hour (Hexadecimal)	12-hour (Hexadecimal)	Minute (Hexadecimal)
AM 00:00 every day	1	1	1	1	1	1	1	00	00	00
AM 01:30 every day	1	1	1	1	1	1	1	01	01	30
AM 11:59 on Mon.	0	1	0	0	0	0	0	11	11	59
PM 00:00 on Mon. to Fri.	0	1	1	1	1	1	0	12	32	00
PM 01:30 on Sun.	1	0	0	0	0	0	0	13	21	30
PM 11:59 on Mon, Wed.	0	1	0	1	0	0	0	23	31	59

WAFG, DAFG and /INTA, /INTB Output



Periodic Interrupt Function

Periodic interrupt output can be obtained via PT7C4372A/C: /INTA or /INTB pin. Select among five periodic-cycle settings: 2 Hz (once per 0.5 seconds), 1 Hz (once per second), 1/60 Hz (once per minute), 1/3600 Hz (once per hour), or monthly (on the 1 st of each month).

Select between two output waveforms for periodic interrupts: an ordinary pulse waveform (2 Hz or 1 Hz) or a waveform (every second, minute, hour, or month) for CPU-level interrupts that can support CPU interrupts.

A polling function is also provided to enable monitoring of pin states via registers.

Related Registers

Period interrupts output via PT7C4372A/C: /INTA, /INTB

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E	Control 1	AALE	BALE	SL2	SL1	TEST	CT2	CT1	CT0
F	Control 2	-	-	/12, 24	ADJ or XSTP	/CLEN	CTFG	AAFG	BAFG

- **SL2, SL1**

Interrupt output select bits. Two alarm pulses (Alarm_A and alarm_B), periodic interrupt output (INT), 32kHz clock pulses may be output to the /INTA or /INTB pins selectively by SL1 and SL2.

SL2	SL1	Description	
0	0	Output Alarm_A, Alarm_B, INT to the /INTA. Output 32kHz clock pulses to /INTB.	Default
0	1	Output Alarm_A, INT to the /INTA. Output 32kHz clock pulses, Alarm_B to /INTB.	
1	0	Output Alarm_A, Alarm_B to the /INTA. Output 32kHz clock pulses, INT to /INTB.	
1	1	Output Alarm_A to the /INTA. Output 32kHz clock pulses, Alarm_B, INT to /INTB.	

- **CTFG:**

During a read operation, this bit indicates the /INTA or /INTB pin's periodic interrupt output status. This status can be set as OFF by writing a "0" to this bit when /INTA or /INTB = "H".

CTFG	Data	Description	
Read	0	Periodic interrupt output OFF status; /INTA or /INTB= OFF (Hi-z) Read	Default
	1	Periodic interrupt output ON status; /INTA or /INTB= "L"	
Write	0	A "0" can be written only when the periodic interrupt is in level mode, at which time the /INTA or /INTB pin is set to OFF (“H”) status. After a "0" is written, the value still becomes "1" again at the next cycle.	Default
	1	Setting prohibited	

- **CT2, CT1, CT0:**

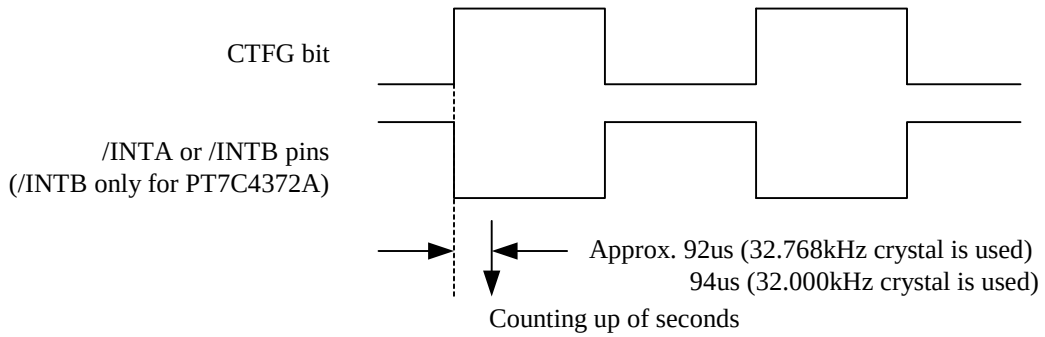
Periodic interrupt output select bits.

CT2	CT1	CT0	Description		
			Wave Form Mode	Cycle / Falling Timing	
0	0	0	-	Off (“H”)	Default
0	0	1	-	Fixed at “L”	
0	1	0	Pulse	2Hz (duty 50%)	
0	1	1	Pulse	1Hz (duty 50%)	
1	0	0	Level	Every second (synchronized with second count up)	
1	0	1	Level	Every minute (Occurs when seconds reach ":00")	
1	1	0	Level	Every hour (Occurs when minutes and seconds reach "00:00")	
1	1	1	Level	Every month (Occurs at 00:00:00 on first day of month)	

Mode-Specific Output Waveforms

1) Pulse Mode:

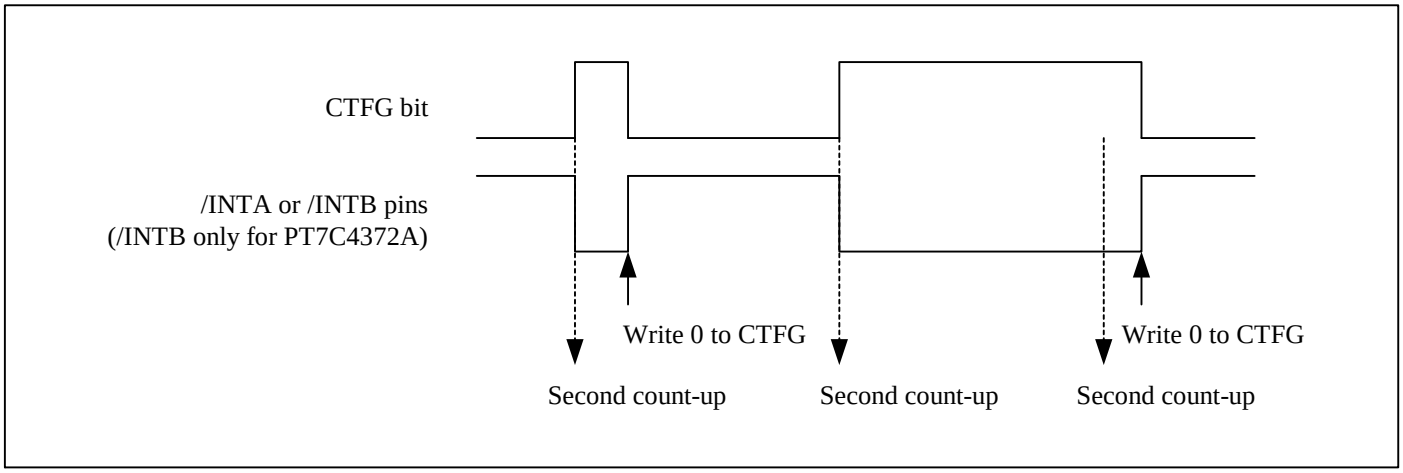
Output 2Hz, 1Hz clock pulse.



Since counting up of seconds and the falling edge has a time lag of approx. 92us (at 32.768kHz) (Approx. 94us when 32.000kHz is used), time with apparently approx. one second of delay from time of the real-time clock may be read when time is read in synchronization with the falling edge of output.

2) Level Mode:

One second, one minute or one month may be selected for an interrupt cycle. Counting up of seconds is matched with falling edge of interrupt output.



3) When the time trimming circuit is used, periodic interrupt cycle changes every 20 seconds.

Pulse mode: The period during which the output pulse is low can be adjusted backward or forward up to ±3.784ms (±3.875ms when 32.000kHz crystal is used).
For example, the duty for the 1-Hz setting can be adjusted ±0.3784% (or ±0.3875% when 32.000kHz crystal is used) from 50%.

Level mode: a one-second period can be adjusted backward or forward up to ±3.784 ms (±3.875ms when 32.000kHz crystal is used).

Various Detection Function

PT7C4372A/C detection function includes oscillation stop detection as well as reporting of detection results in corresponding bits of Control 2 register.
The status of the power supply, oscillation circuit, and clock can be confirmed by checking these results.
*Note with caution that detection functions may not operate correctly when power flickers occur.

Related Register

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F	Control 2	-	-	/12, 24	ADJ or XSTP	/CLEN	CTFG	AAFG	BAFG

Oscillation Stop Detection

When read control register is 2 bit 4, this bit is as XSTP bit sensing oscillator halt. This bit is as 30 second adjust bit when write.

XSTP	Data	Description	
Read	0	Ordinary oscillation.	
	1	Oscillator halts sensing.	Default

This bit senses the oscillator halt. When oscillation is halted after initial power on from 0V or drop in supply voltage, the bit is set to “1” and remains to be “1” after it is restarted. This bit may be used to judge validity of clock and calendar count data after power on or supply voltage drop. When this bit is set to “1”, the Time Trimming register, Control 1 register, /CLEN and TEST bits are reset to “0”. /INTA will stop output and the /INTB will output 32-kHz clock pulses. This bit is set to “0” by setting the control register 2 during ordinary oscillation.

Reading / Writing Data via the I²C Bus Interface

Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on.

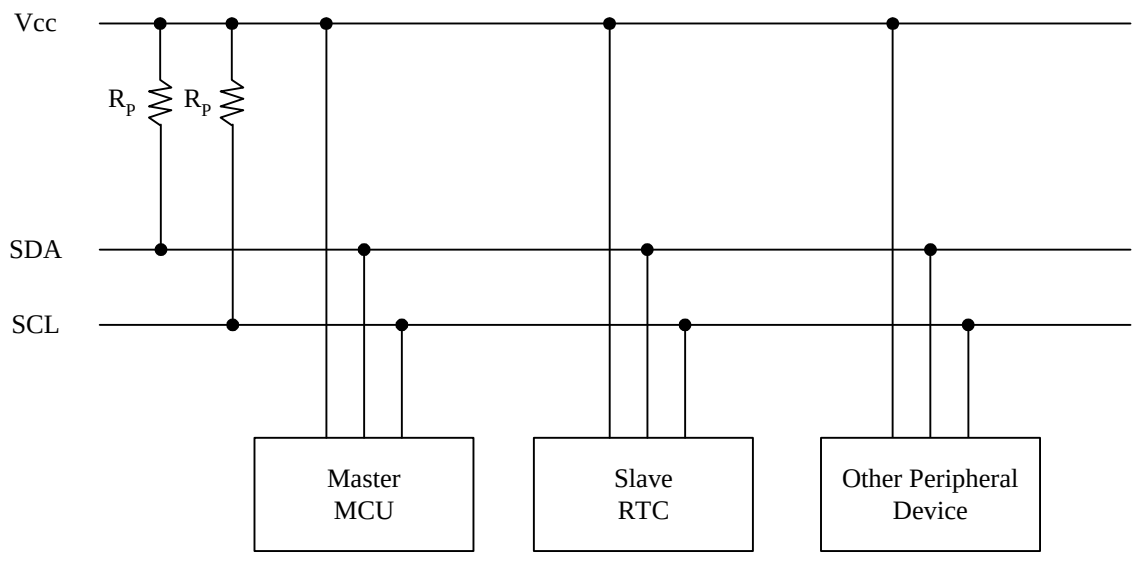
Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.

SCL and SDA are both connected to the Vcc line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

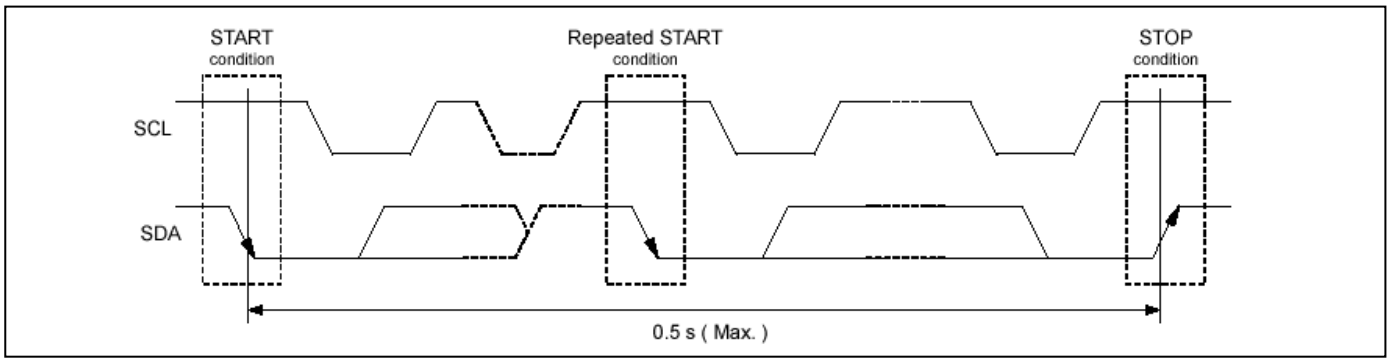
Figure 1. System Configuration



Note: When the master is one, the MCU is ready for driving SCL to "H" and R_p of SCL may not required.

Starting and Stopping I²C Bus Communications

Figure 2. Starting and Stopping on I²C bus



1) START condition, repeated START condition, and STOP condition

a) START condition

SDA level changes from high to low while SCL is at high level

b) STOP condition

SDA level changes from low to high while SCL is at high level

c) Repeated START condition (RESTART condition)

In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution Points

a) The master device always controls the START, RESTART, and STOP conditions for communications.

b) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

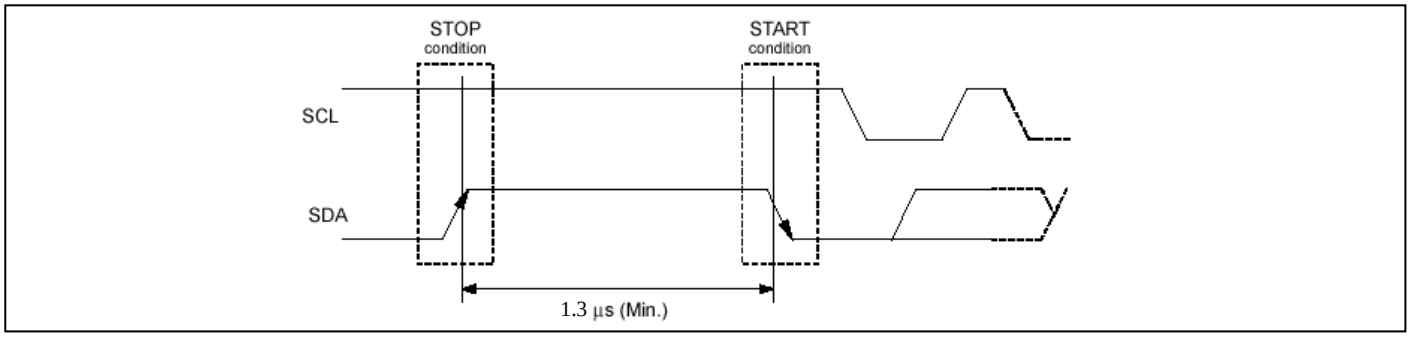
c) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur within 0.5 seconds. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur within 0.5 seconds.)

If this series of operations requires 0.5 to 1.0 seconds or longer, the I²C bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of "1").

Restarting of communications begins with transfer of the START condition again.

d) When communicating with this RTC module, wait at least 1.3 μs between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications). (If any carries occur in the time data during this communication period, corrections are made during this period.)

Figure 3. Interval between Start and Stop

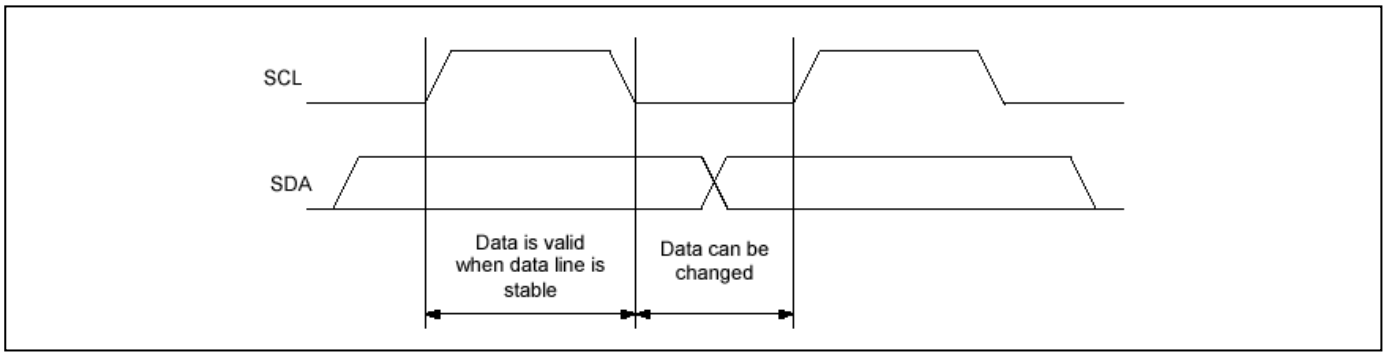


Data Transfers and Acknowledge Responses during I²C-BUS Communication

1) Data Transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition. (However, the transfer time must be no longer than 0.5 seconds and access to the Address Dh (Reserved) register is prohibited.)

The address auto increment function operates during both write and read operations. After address Fh, increment goes to address 0h. Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) captures data while the SCL line is at high level.

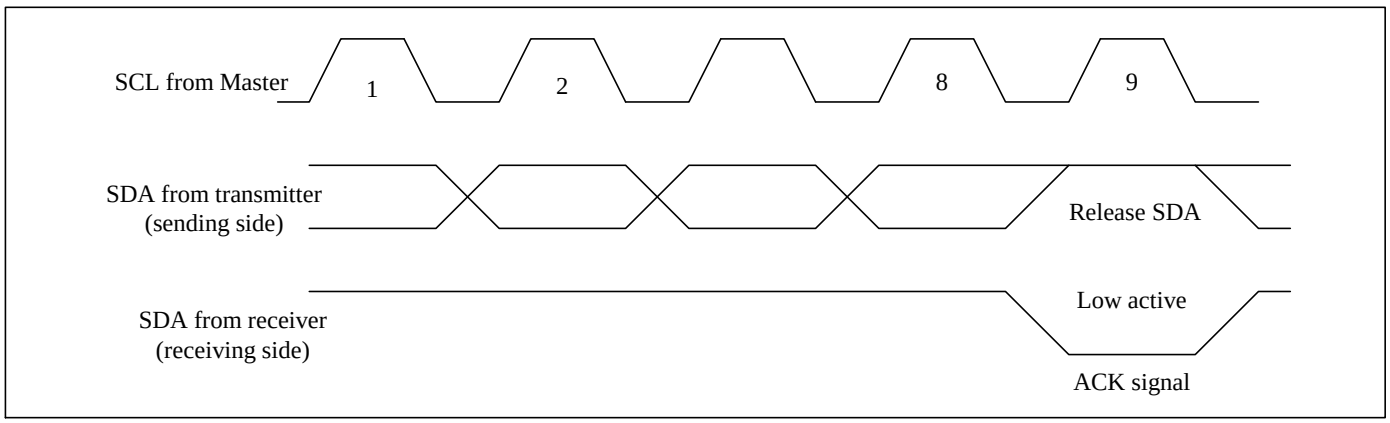


*Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data Acknowledge Response (ACK Signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

Slave Address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.

All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

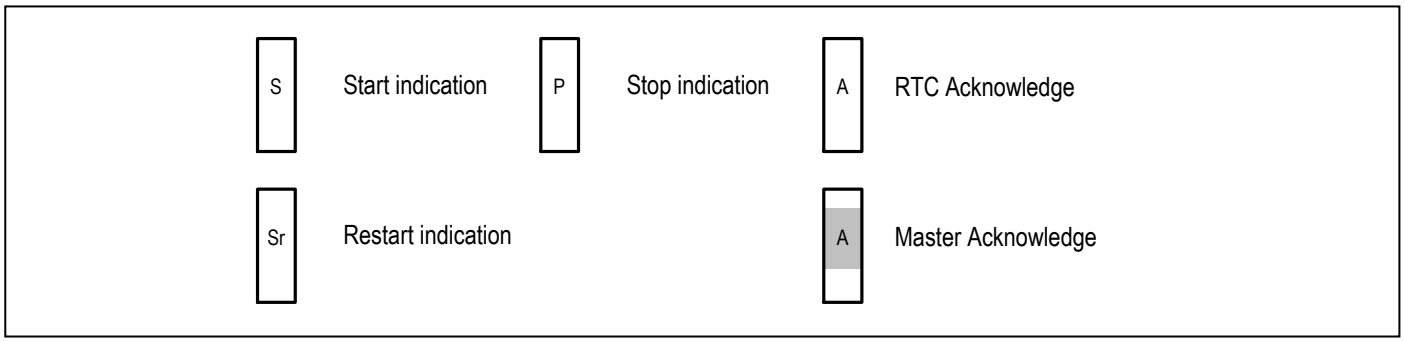
Slave addresses have a fixed length of 7 bits. This RTC's slave address is [0110 010].

An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

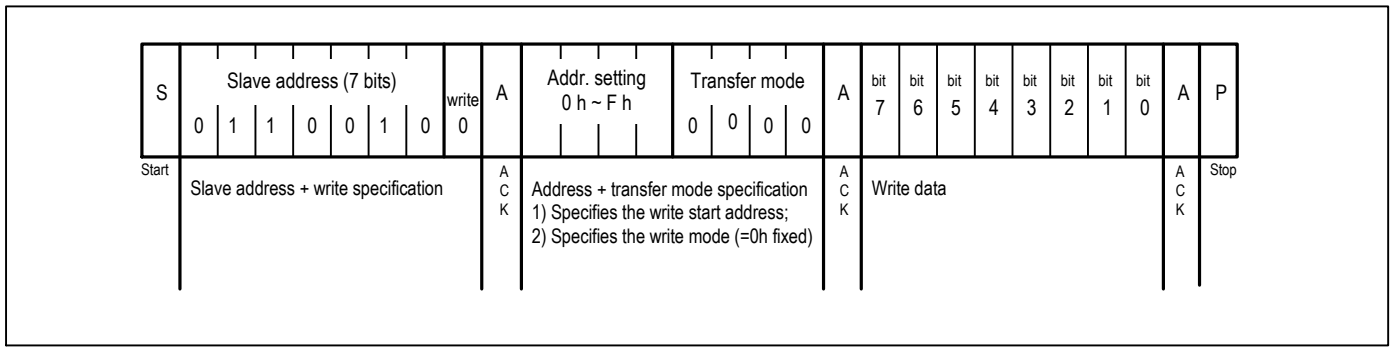
Table

	Transfer data	Slave address							R / W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	65 h	0	1	1	0	0	1	0	1 (= Read)
Write	64 h								0 (= Write)

I²C Bus's Basic Transfer Format

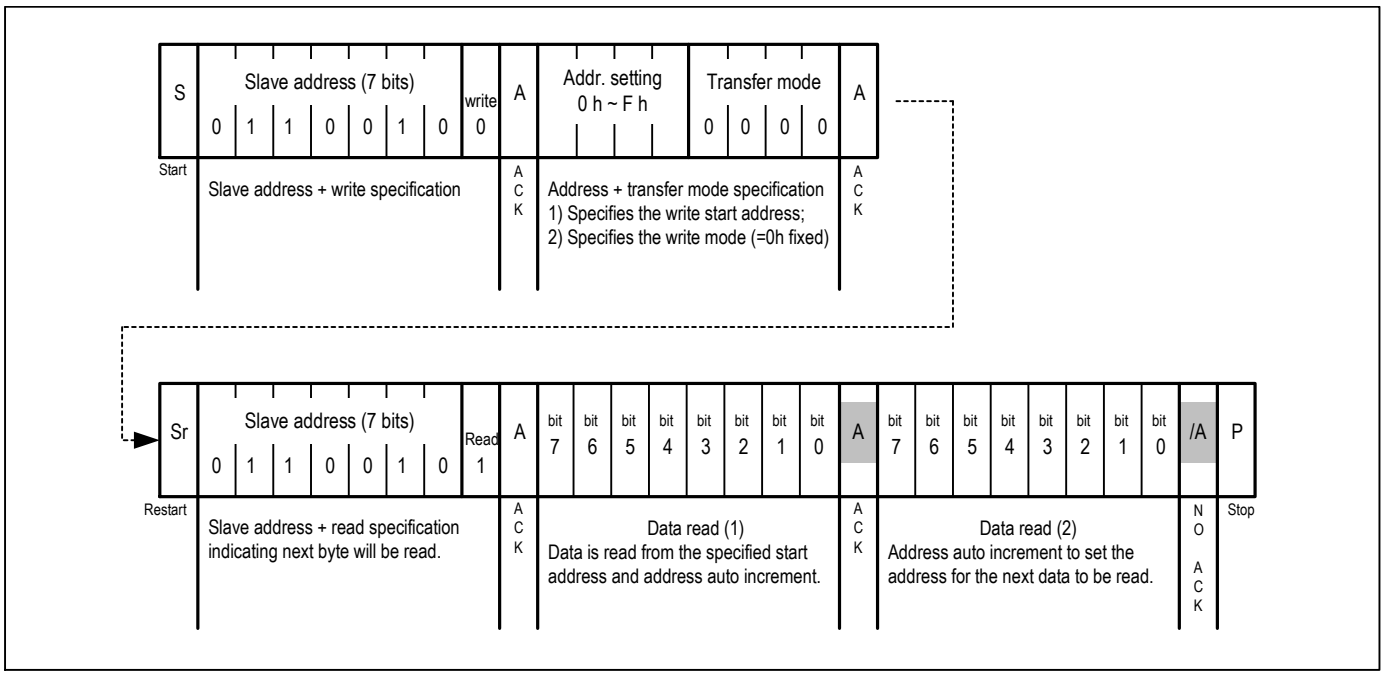


1) Write via I²C bus

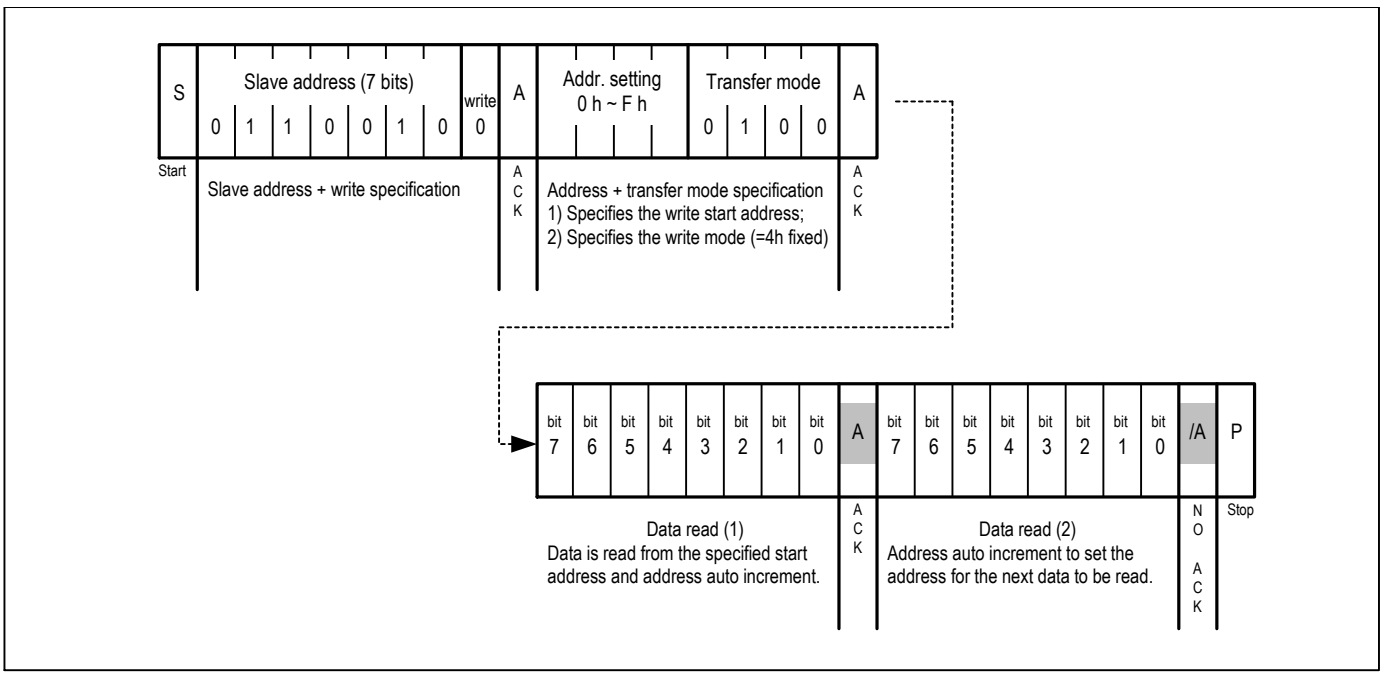


2) Read via I²C bus

a) Standard Read

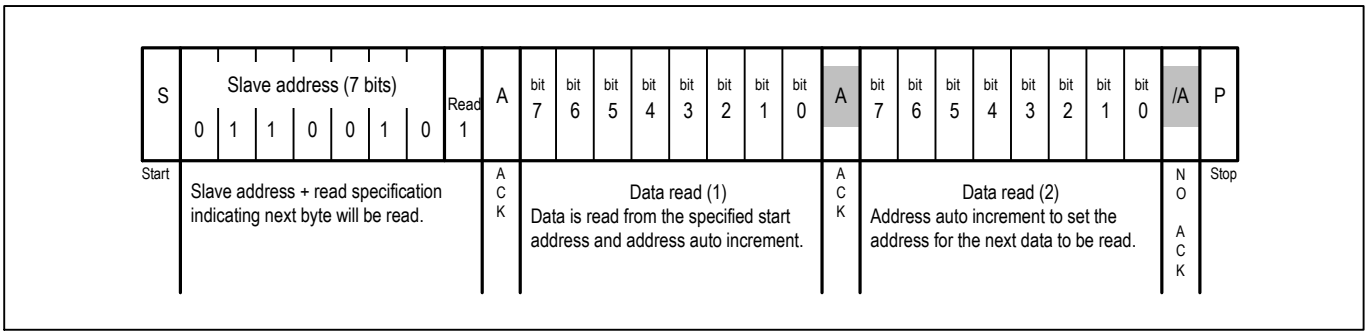


b) Simplified Read



c) Simplified Read with No Start Address Indicating

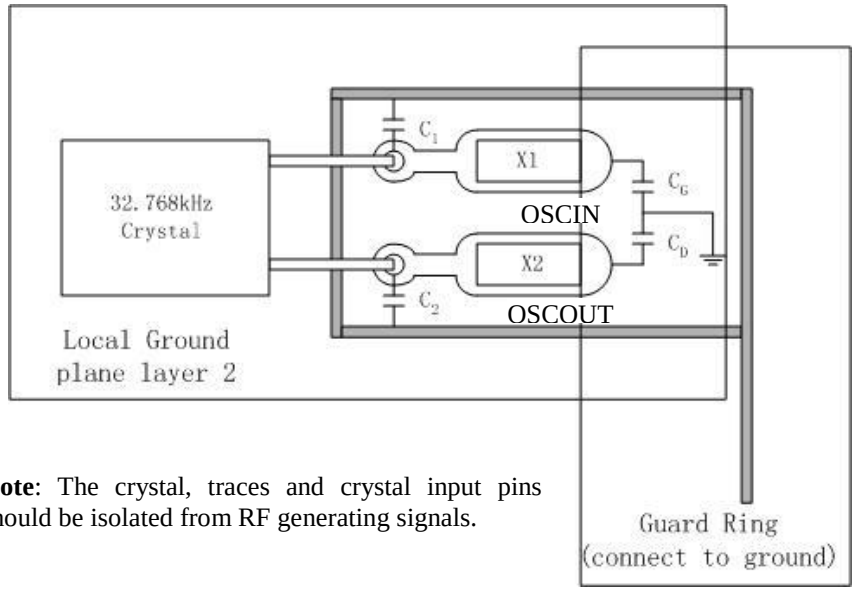
Only when reading from address Fh (Fh → 0h → 1h → 2h, etc.), a read operation can be performed without specifying the read start address or the transfer mode.



Note: The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications. (However, the transfer time must be no longer than 0.5 seconds.)

Configuration of Oscillating Circuit and Timing Trimming

Recommended Layout for Crystal



Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

Considerations in Mounting Components Surrounding Oscillating Circuit

1) Mount the crystal oscillators in the closest possible position to the IC.
2) Avoid laying any signal or power line close to the oscillation circuit (particularly in the area marked with "←A→" in the above figure).
3) Apply the highest possible insulation resistance between the OSCOUT pin and the PCB.
4) Avoid using any long parallel line to wire the OSCIN and OSCOUT pin.
5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	OSCIN to GND	C_G	20	pF
	OSCOUT to GND	C_D	5	pF
Recommended External capacitors for crystal C_L=12.5pF	OSCIN to GND	C_1	4	pF
	OSCOUT to GND	C_2	18	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768kHz, C_1 and C_2 should meet the equation as below:

$$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$$

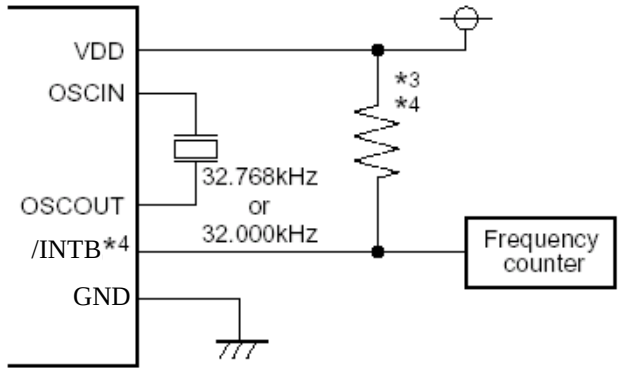
Cpar is all parasitical capacitor between X1 and X2.
C_L is crystal's load capacitance.

Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_L	-	12.5	-	pF

Measurement of Oscillation Frequency

PT7C4372A



*1. Clock pulse of 32.768kHz or 32.000kHz is output from the /INTB output pin on powering on (XSTP is set to 1).

*2. Use a frequency counter having at least 6 digits (7 digits or more recommended).

*3. Pull-up the /INTB output pin to Vcc for the 4372A.

*4. /INTB applies to the 4372A

Oscillation Frequency Adjustment please refers to page 12, **Clock Precision Adjustment Function.**

Maximum Ratings

Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential (Vcc to GND)	-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	-0.3V to (V_{cc}+0.3V)
DC Output Voltage (SDA, /INTA, /INTB pins)	-0.3V to +6.5V
DC Output Current (FOUT)	-0.3V to (V_{cc}+0.3V)
Power Dissipation	320mW (depend on package)
Junction Temperature	125°C max

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Min	Type	Max	Unit
V_{CC}	Power voltage	1.8	-	6	V
V_{OSC}	Timekeeping voltage	1.3	-	5.5	
V_{PUP}	Applied voltage when OFF (SCL, SDA, /INTA, /INTB pins)	-0.3	-	5.5	
T_A	Operating temperature	-40	-	85	℃

Frequency Characteristics

Symbol	Description	Conditions	Rating	Unit
Δf / f	Frequency tolerance	T_A = +25℃ V_{cc} = 3.0 V	Stability AC: 0 ± 5	× 10^{-6}
f / V	Frequency voltage characteristics	T_A = +25℃ V_{cc} = 2 V to 5 V	± 2 Max.	× 10^{-6} / V
Top	Frequency temperature characteristics	T_A = -10℃ to +70℃, V_{cc} = 3.0 V; +25℃ reference	+10 / -120	× 10^{-6}
t_{STA}	Oscillation start up time	T_A = +25℃ V_{cc} = 3 V	3 Max.	s
fa	Aging	T_A = +25℃ V_{CC}=3.0 V; first year	± 5 Max.	× 10^{-6} / year

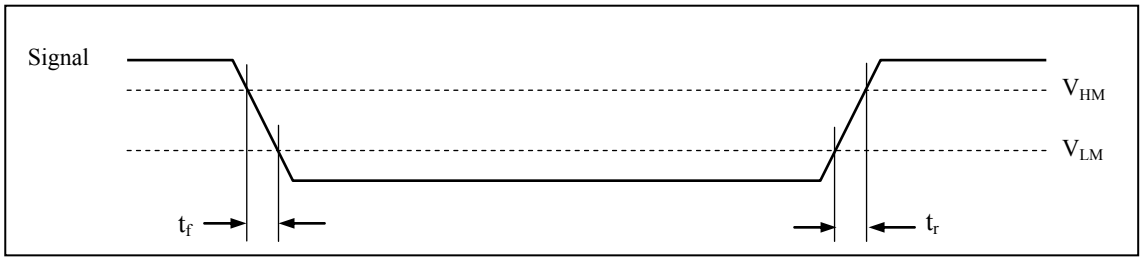
DC Electrical Characteristics

Unless otherwise specified, GND = 0 V, V_{CC} = 3 V, T_A = -40 ℃ to +85 ℃

Sym.	Item	Pin	Conditions	Min	Typ	Max	Unit
I_{CC1}	Current consumption	Vcc	Interface is active at 400kHz	-	-	150	μA
I_{CC2}			Interface is inactive, enable 32768Hz SQW wave output	-	500	1000	nA
I_{CC3}			Interface is inactive, disable 32768Hz SQW wave output	-	400	800	nA
V_{IL}	Low-level input voltage	SCL, SDA, FOE	-	-0.3	-	0.2V_{CC}	V
V_{IH}	High-level input voltage		-	0.8V_{CC}	-	6.0	V
I_{OL}	Low-level output current	/INTA,/INTB	V_{OL} = 0.4	1.0	-	-	mA
		SDA	V_{OL} = 0.6	6.0	-	-	
I_{IL}	Input leakage current	SCL	V_I = 5.5V or GND, V_{CC} = 5.5V	-1	-	1	μA
I_{OZ}	Output current when OFF	SDA, /INTA,/INTB	V_O = 5.5V or GND, V_{CC} = 5.5V	-1	-	1	μA

AC Electrical Characteristics

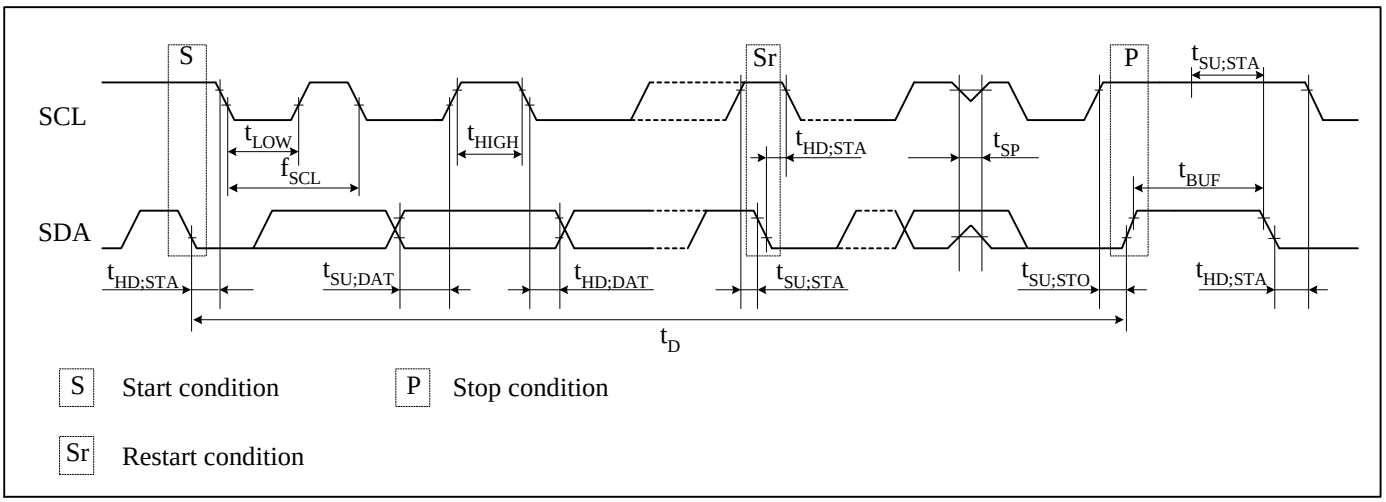
Sym	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.2 V_{CC}	V



*Unless otherwise specified: GND = 0 V, V_{CC} = 2 V to 5.5 V, T_A = -40 ℃ to +85 ℃, C_L = 50 pF

Symbol	Item	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	-	-	400	kHz
$t_{SU;STA}$	START condition set-up time	0.6	-	-	μs
$t_{HD;STA}$	START condition hold time	0.6	-	-	μs
$t_{SU;DAT}$	Data set-up time (RTC read/write)	200	-	-	ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35	-	-	ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0	-	-	μs
$t_{SU;STO}$	STOP condition setup time	0.6	-	-	μs
t_{BUF}	Bus idle time between a START and STOP condition	1.3	-	-	μs
t_{LOW}	When SCL = "L"	1.3	-	-	μs
t_{HIGH}	When SCL = "H"	0.6	-	-	μs
t_r	Rise time for SCL and SDA	-	-	0.3	μs
t_f	Fall time for SCL and SDA	-	-	0.3	μs
t_{SP}*	Allowable spike time on bus	-	-	50	ns
t_D	Duration of staring to stopping	-	-	0.5	s

*** Note:** only reference for design



Part Marking (PT7C4372A)

W Package

W: Die Rev
Y: Year
W: Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code

L Package

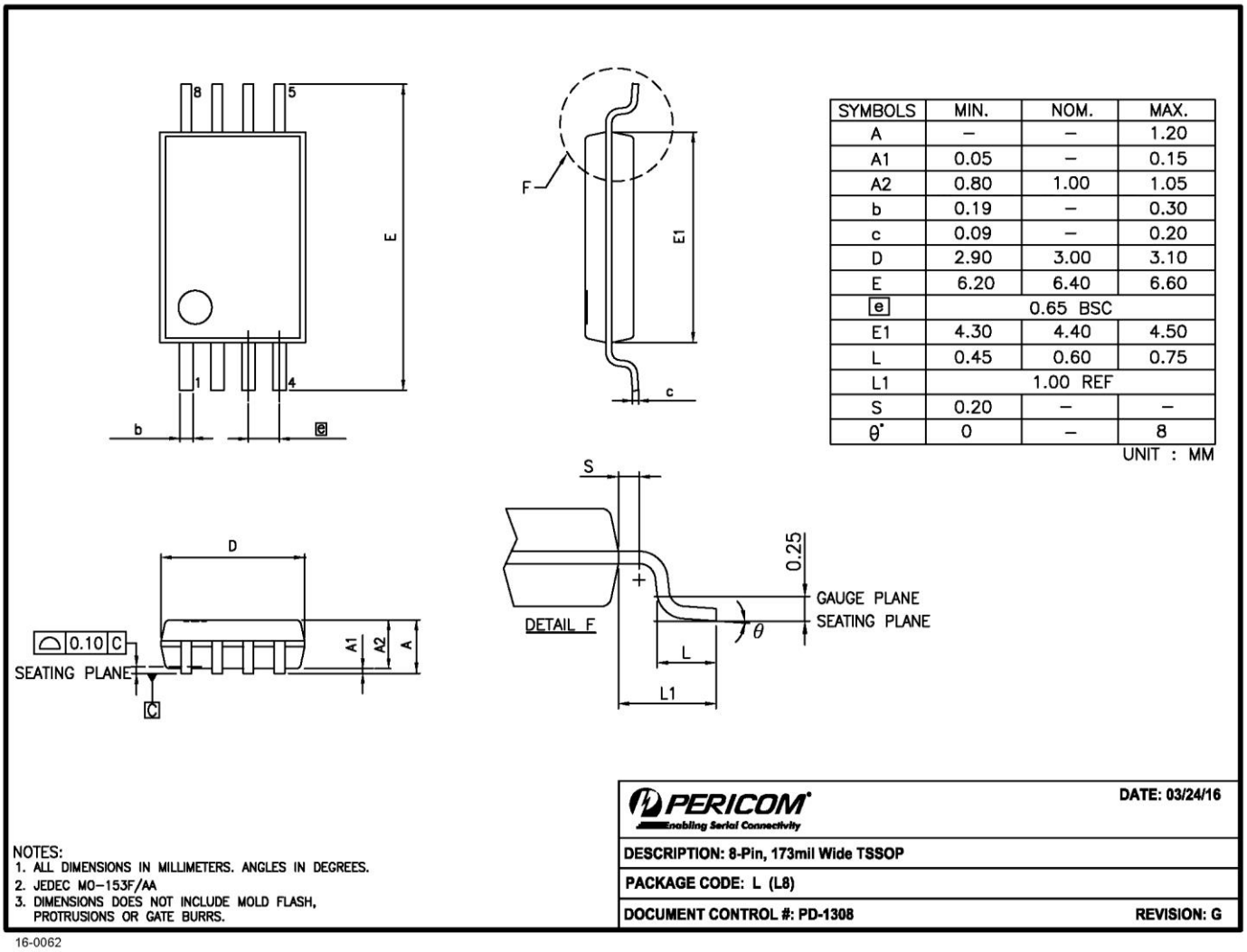
W: Die Rev
A: Year
B: Workweek
J: Assembly Site Code
W: Wafer Fab Site Code

Part Marking (PT7C4372C)

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Packaging Mechanical

8-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E	6.20	6.40	6.60
e		0.65 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	–	–
θ°	0	–	8

UNIT : MM

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F/AA
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/24/16

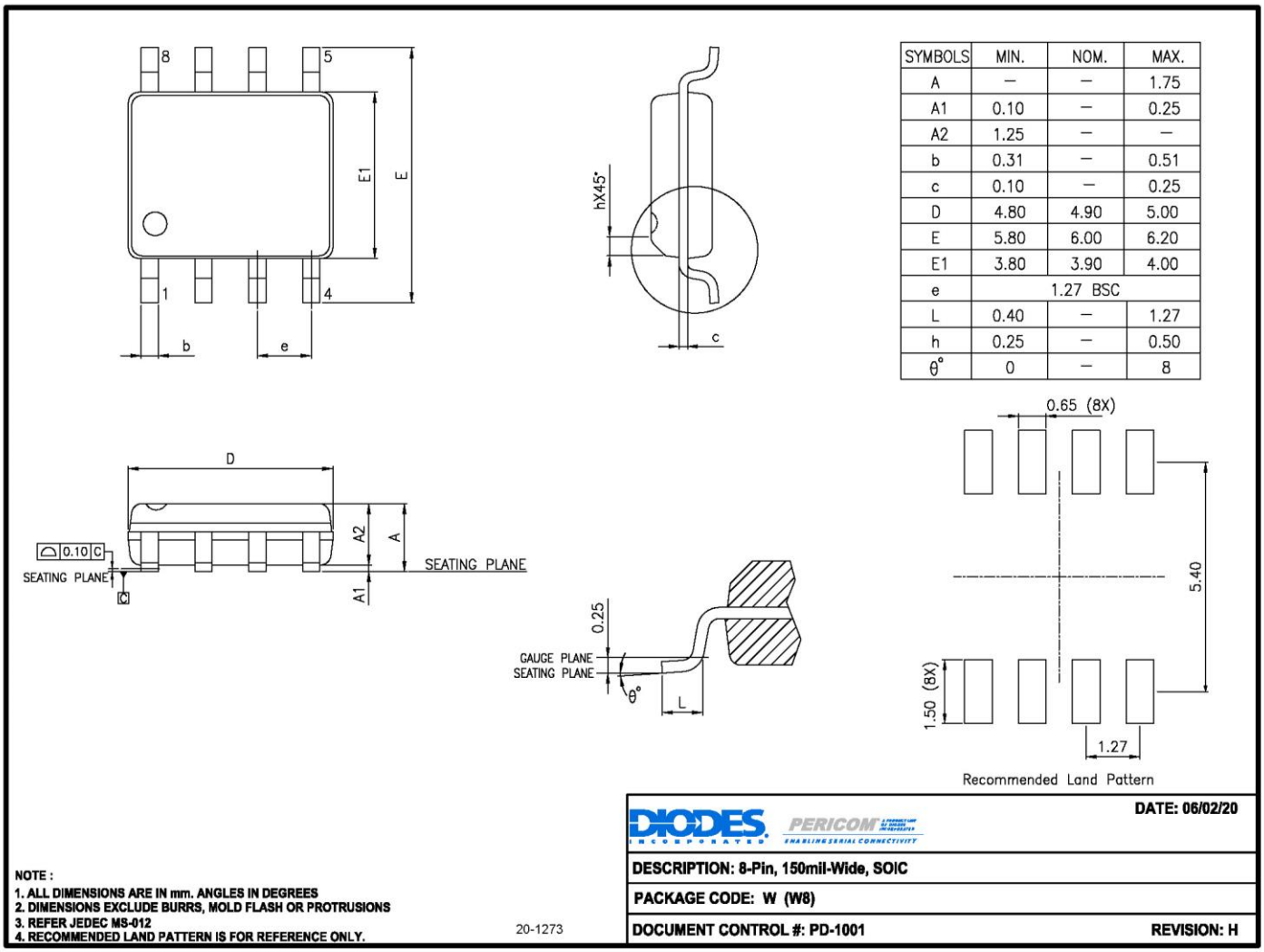
DESCRIPTION: 8-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L8)

DOCUMENT CONTROL #: PD-1308 REVISION: G

16-0062

8-SOIC (W)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Numbers	Package Code	Package Description
PT7C4372ALEX	L	8-Pin, 173mil-Wide (TSSOP)
PT7C4372CLEX	L	8-Pin, 173mil-Wide (TSSOP)
PT7C4372AWEX	W	8-Pin, 150mil-Wide (SOIC)
PT7C4372CWEX	W	8-Pin, 150mil-Wide (SOIC)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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