



**THE DATASHEET OF
PLDC20G10-25PC**





PLDC20G10B/PLDC20G10

CMOS Generic 24-Pin Reprogrammable Logic Device

Features

- **Fast**
 - Commercial: $t_{PD} = 15 \text{ ns}$, $t_{CO} = 10 \text{ ns}$, $t_S = 12 \text{ ns}$
 - Military: $t_{PD} = 20 \text{ ns}$, $t_{CO} = 15 \text{ ns}$, $t_S = 15 \text{ ns}$
- **Low power**
 - $I_{CC} \text{ max.}: 70 \text{ mA}$, commercial
 - $I_{CC} \text{ max.}: 100 \text{ mA}$, military
- **Commercial and military temperature range**
- **User-programmable output cells**
 - Selectable for registered or combinatorial operation
 - Output polarity control
 - Output enable source selectable from pin 13 or product term
- **Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8**
- **Eight product terms and one OE product term per output**

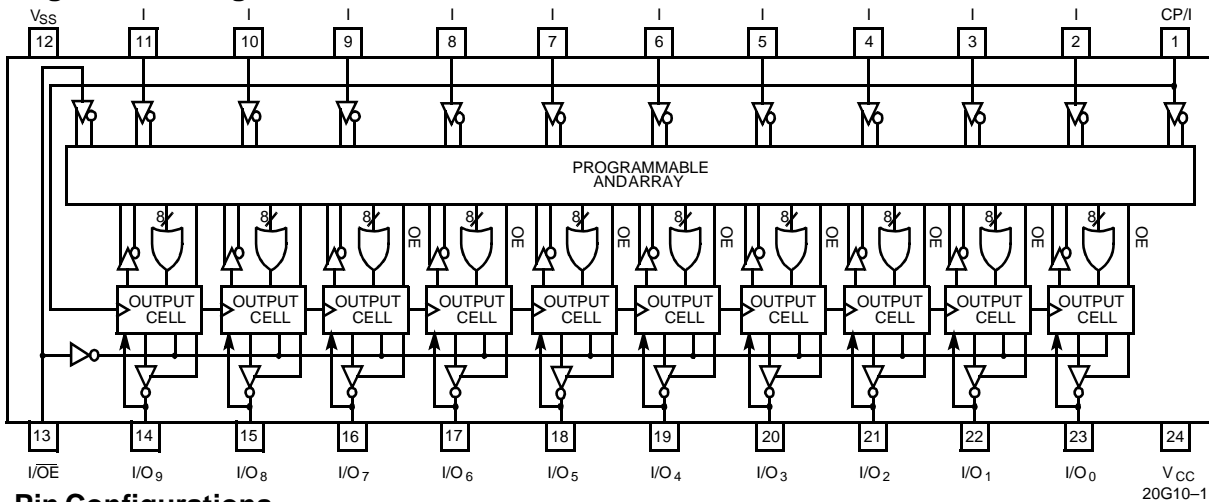
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
 - Uses proven EPROM technology
 - Fully AC and DC tested
 - Security feature prevents logic pattern duplication
 - $\pm 10\%$ power supply voltage and higher noise immunity

Functional Description

Cypress PLD devices are high-speed electrically programmable logic devices. These devices utilize the sum-of-products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

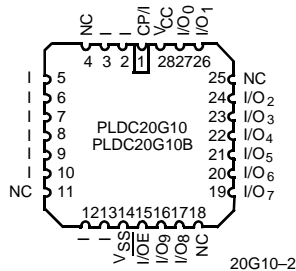
In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

Logic Block Diagram

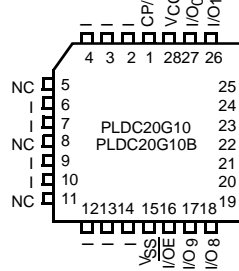


Pin Configurations

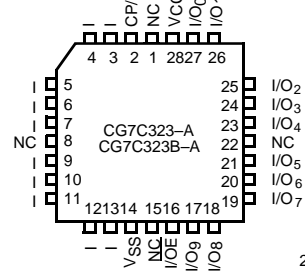
LCC Top View



STD PLCC Top View



JEDEC PLCC [1] Top View



Note:

1. The CG7C323 is the PLDC20G10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The difference is in the location of the "no connect" or NC pins.

Selection Guide

| Generic Part Number | I _{CC} (mA) | | t _{PD} (ns) | | t _S (ns) | | t _{CO} (ns) | |
|---------------------|----------------------|-----|----------------------|-----|---------------------|-----|----------------------|-----|
| | Com/Ind | Mil | Com/Ind | Mil | Com/Ind | Mil | Com/Ind | Mil |
| 20G10B-15 | 70 | | 15 | | 12 | | 10 | |
| 20G10B-20 | 70 | 100 | 20 | 20 | 12 | 15 | 12 | 15 |
| 20G10B-25 | | 100 | | 25 | | 18 | | 15 |
| 20G10-25 | 55 | | 25 | | 15 | | 15 | |
| 20G10-30 | | 80 | | 30 | | 20 | | 20 |
| 20G10-35 | 55 | | 35 | | 30 | | 25 | |
| 20G10-40 | | 80 | | 40 | | 35 | | 25 |

Functional Description (continued)

Cypress PLDC20G10 uses an advanced 0.8-micron CMOS technology and a proven EPROM cell as the programmable element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

20G10 Functional Description

The PLDC20G10 is a generic 24-pin device that can be programmed to logic functions that include but are not limited to: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8. Thus, the PLDC20G10 provides significant design, inventory and programming flexibility over dedicated 24-pin devices. It is executed in a 24-pin 300-mil molded DIP and a 300-mil windowed cerDIP. It provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 20G10 is erased and then can be reprogrammed.

The programmable output cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with registered or combinatorial outputs, active HIGH or active LOW outputs, and product term or Pin 13 generated output enables. Three architecture bits determine the configurations as shown in the Configuration

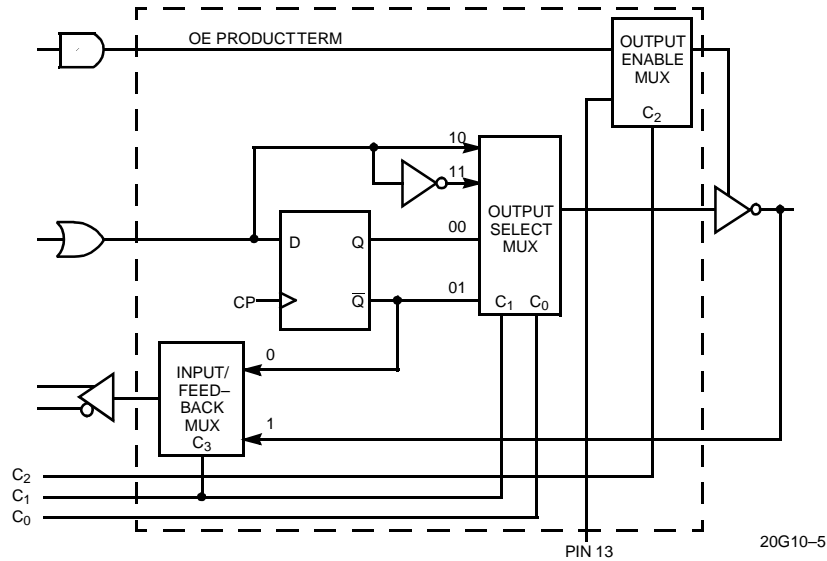
Table and in *Figures 1 through 8*. A total of eight different configurations are possible, with the two most common shown in *Figure 3* and *Figure 5*. The default or unprogrammed state is registered/active/LOW/Pin 11 OE. The entire programmable output cell is shown in the next section.

The architecture bit 'C1' controls the registered/combinatorial option. In either combinatorial or registered configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In either registered or combinatorial configuration, the output of the register is fed back to the array. This allows the creation of control-state machines by providing the next state. The register is clocked by the signal from Pin 1. The register is initialized on power up to Q output LOW and Q output HIGH.

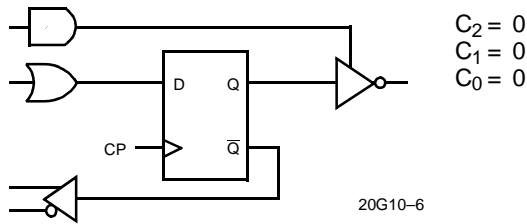
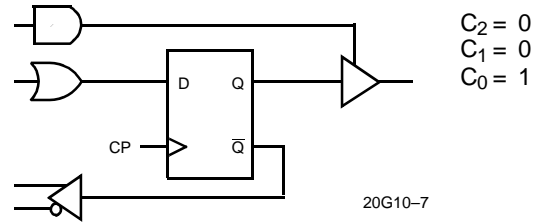
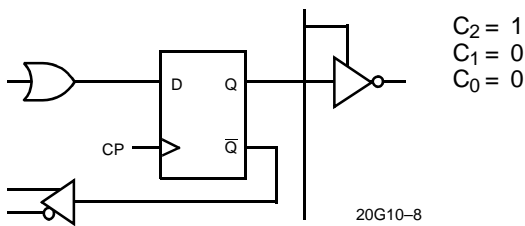
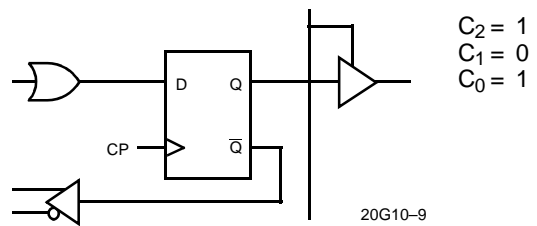
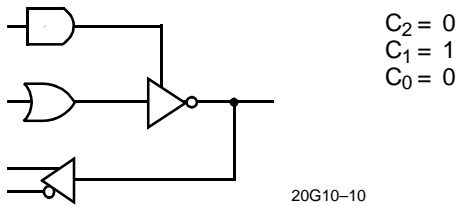
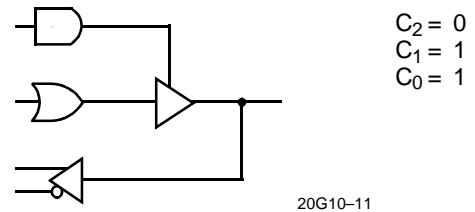
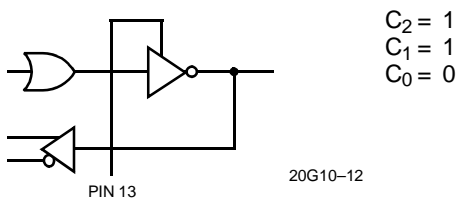
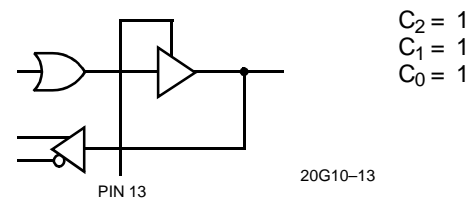
In both the combinatorial and registered configurations, the source of the output enable signal can be individually chosen with architecture bit 'C2'. The OE signal may be generated within the array, or from the external OE (Pin 13). The Pin 13 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for output polarity. The output can be either active HIGH or active LOW. This option is controlled by architecture bit 'C0'.

Along with this increase in functional density, the Cypress PLDC20G10 provides lower-power operation through the use of CMOS technology and increased testability with a register preload feature.

Programmable Output Cell

Configuration Table

| Figure | C ₂ | C ₁ | C ₀ | Configuration |
|--------|----------------|----------------|----------------|---|
| 1 | 0 | 0 | 0 | Product Term OE/Registered/Active LOW |
| 2 | 0 | 0 | 1 | Product Term OE/Registered/Active HIGH |
| 5 | 0 | 1 | 0 | Product Term OE/Combinatorial/Active LOW |
| 6 | 0 | 1 | 1 | Product Term OE/Combinatorial/Active HIGH |
| 3 | 1 | 0 | 0 | Pin 13 OE/Registered/Active LOW |
| 4 | 1 | 0 | 1 | Pin 13 OE/Registered/Active HIGH |
| 7 | 1 | 1 | 0 | Pin 13 OE/Combinatorial/Active LOW |
| 8 | 1 | 1 | 1 | Pin 13 OE/Combinatorial/Active HIGH |

Registered Output Configurations

Figure 1. Product Term OE/Active LOW

Figure 2. Product Term OE/Active HIGH

Figure 3. Pin 13 OE/Active LOW

Figure 4. Pin 13 OE/Active HIGH
Combinatorial Output Configurations^[2]

Figure 5. Product Term OE/Active LOW

Figure 6. Product Term OE/Active HIGH

Figure 7. Pin 13 OE/Active Low

Figure 8. Pin 13 OE/Active HIGH
Note:

2. Bidirectional I/O configurations are possible only when the combinatorial output option is selected



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage to Ground Potential -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State -0.5V to +7.0V
- DC Input Voltage..... -3.0V to +7.0V
- Output Current into Outputs (LOW) 16 mA

- DC Programming Voltage
 PLDC20G10B and CG7C323B-A 13.0V
 PLDC20G10 and CG7C323-A 14.0V
- Latch-Up Current..... >200 mA
- Static Discharge Voltage >500V
 (per MIL-STD-883, Method 8015)

Operating Range

| Range | Ambient Temperature | V _{CC} |
|-------------------------|---------------------|-----------------|
| Commercial | 0°C to +75°C | 5V ±10% |
| Military ^[3] | -55°C to +125°C | 5V ±10% |
| Industrial | -40°C to +85°C | 5V ±10% |

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)^[4]

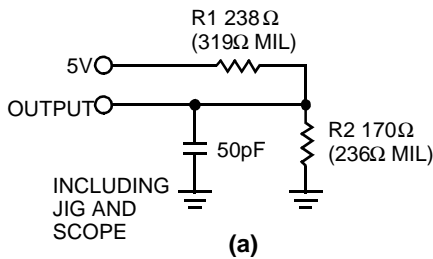
| Parameter | Description | Test Conditions | | Min. | Max. | Unit | |
|-----------------|------------------------------|--|---------------------------|-----------|------|------|----|
| | | | | | | | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} | I _{OH} = -3.2 mA | Com'l/Ind | 2.4 | | |
| | | | I _{OH} = -2 mA | Military | | | |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} | I _{OL} = 24 mA | Com'l/Ind | | 0.5 | |
| | | | I _{OL} = 12 mA | Military | | | |
| V _{IH} | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for All Inputs ^[5] | | 2.0 | | V | |
| V _{IL} | Input LOW Level | Guaranteed Input Logical LOW Voltage for All Inputs ^[5] | | | 0.8 | V | |
| I _{IX} | Input Leakage Current | V _{SS} ≤ V _{IN} ≤ V _{CC} | | -10 | +10 | μA | |
| I _{SC} | Output Short Circuit Current | V _{CC} = Max., V _{OUT} = 0.5V ^[6, 7] | | | -90 | mA | |
| I _{CC} | Power Supply Current | 0 ≤ V _{IN} ≤ V _{CC} V _{CC} = Max., I _{OUT} = 0 mA Unprogrammed Device | Com'l/Ind-15, -20 | | | 70 | mA |
| | | | Com'l/Ind-25, -35 | | | 55 | mA |
| | | | Military-20, -25 | | | 100 | mA |
| | | | Military-30, -40 | | | 80 | mA |
| I _{OZ} | Output Leakage Current | V _{CC} = Max., V _{SS} ≤ V _{OUT} ≤ V _{CC} | | -100 | 100 | μA | |

Capacitance^[7]

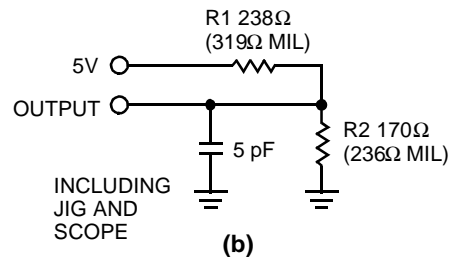
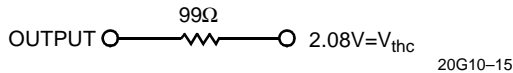
| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz | 10 | pF |
| C _{OUT} | Output Capacitance | V _{IN} = 2.0V, V _{CC} = 5.0V | 10 | pF |

Notes:

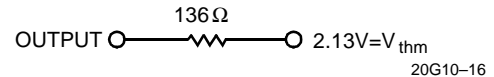
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms (Commercial)


Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military/Industrial)


Switching Characteristics Over Operating Range^[3, 8, 9]

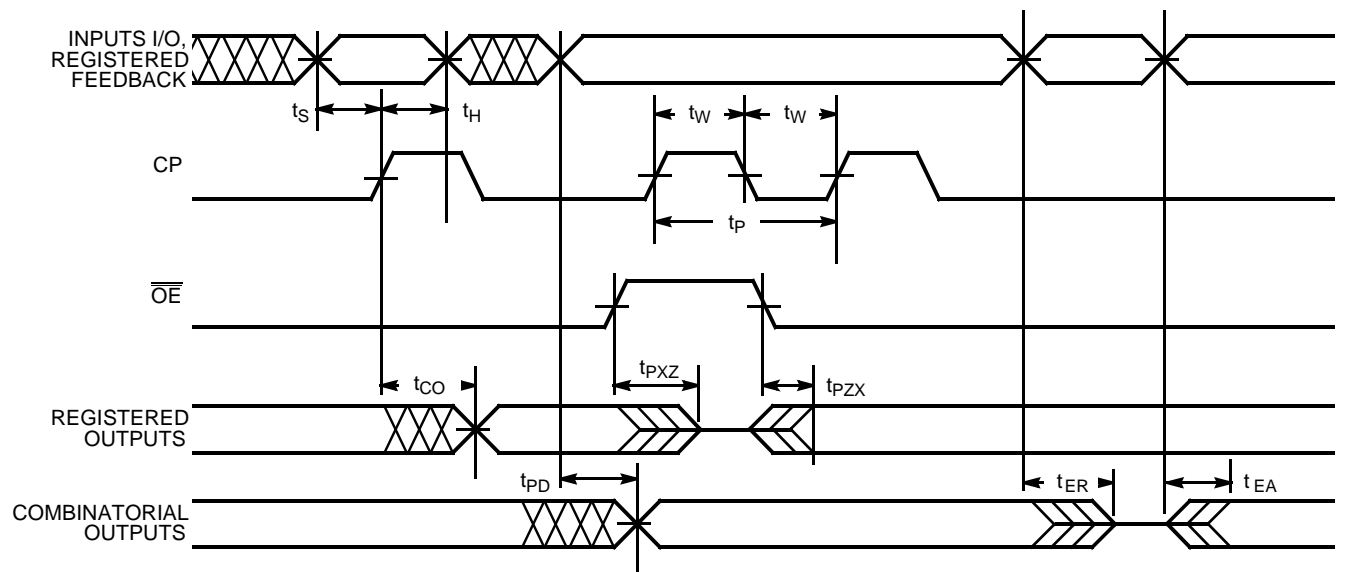
| Parameter | Description | Commercial | | | | | | | | Unit |
|------------------|--|------------|------|------|------|------|------|------|------|------|
| | | B-15 | | B-20 | | -25 | | -35 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{PD} | Input or Feedback to Non-Registered Output | | 15 | | 20 | | 25 | | 35 | ns |
| t_{EA} | Input to Output Enable | | 15 | | 20 | | 25 | | 35 | ns |
| t_{ER} | Input to Output Disable | | 15 | | 20 | | 25 | | 35 | ns |
| t_{PZX} | Pin 11 to Output Enable | | 12 | | 15 | | 20 | | 25 | ns |
| t_{PXZ} | Pin 11 to Output Disable | | 12 | | 15 | | 20 | | 25 | ns |
| t_{CO} | Clock to Output | | 10 | | 12 | | 15 | | 25 | ns |
| t_S | Input or Feedback Set-Up Time | 12 | | 12 | | 15 | | 30 | | ns |
| t_H | Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_P^{[10]}$ | Clock Period | 22 | | 24 | | 30 | | 55 | | ns |
| t_{WH} | Clock High Time | 8 | | 10 | | 12 | | 17 | | ns |
| t_{WL} | Clock Low Time | 8 | | 10 | | 12 | | 17 | | ns |
| $f_{MAX}^{[11]}$ | Maximum Frequency | 45.4 | | 41.6 | | 33.3 | | 18.1 | | MHz |

Notes:

- Part (a) of AC Test Loads and Waveforms used for all parameters except t_{ER} , t_{PZX} , and t_{PXZ} . Part (b) of AC Test Loads and Waveforms used for t_{ER} , t_{PZX} , and t_{PXZ} .
- The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to $V_{OH} - 0.5V$ for an enabled HIGH output or $V_{OL} + 0.5V$ for an enabled LOW input.
- t_P , minimum guaranteed clock period is that guaranteed for state machine operation and is calculated from $t_P = t_S + t_{CO}$. The minimum guaranteed period for registered data path operation (no feedback) can be calculated as the greater of $(t_{WH} + t_{WL})$ or $(t_S + t_H)$.
- f_{MAX} , minimum guaranteed operating frequency, is that guaranteed for state machine operation and is calculated from $f_{MAX} = 1/(t_S + t_{CO})$. The minimum guaranteed f_{MAX} for registered data path operation (no feedback) can be calculated as the lower of $1/(t_{WH} + t_{WL})$ or $1/(t_S + t_H)$.

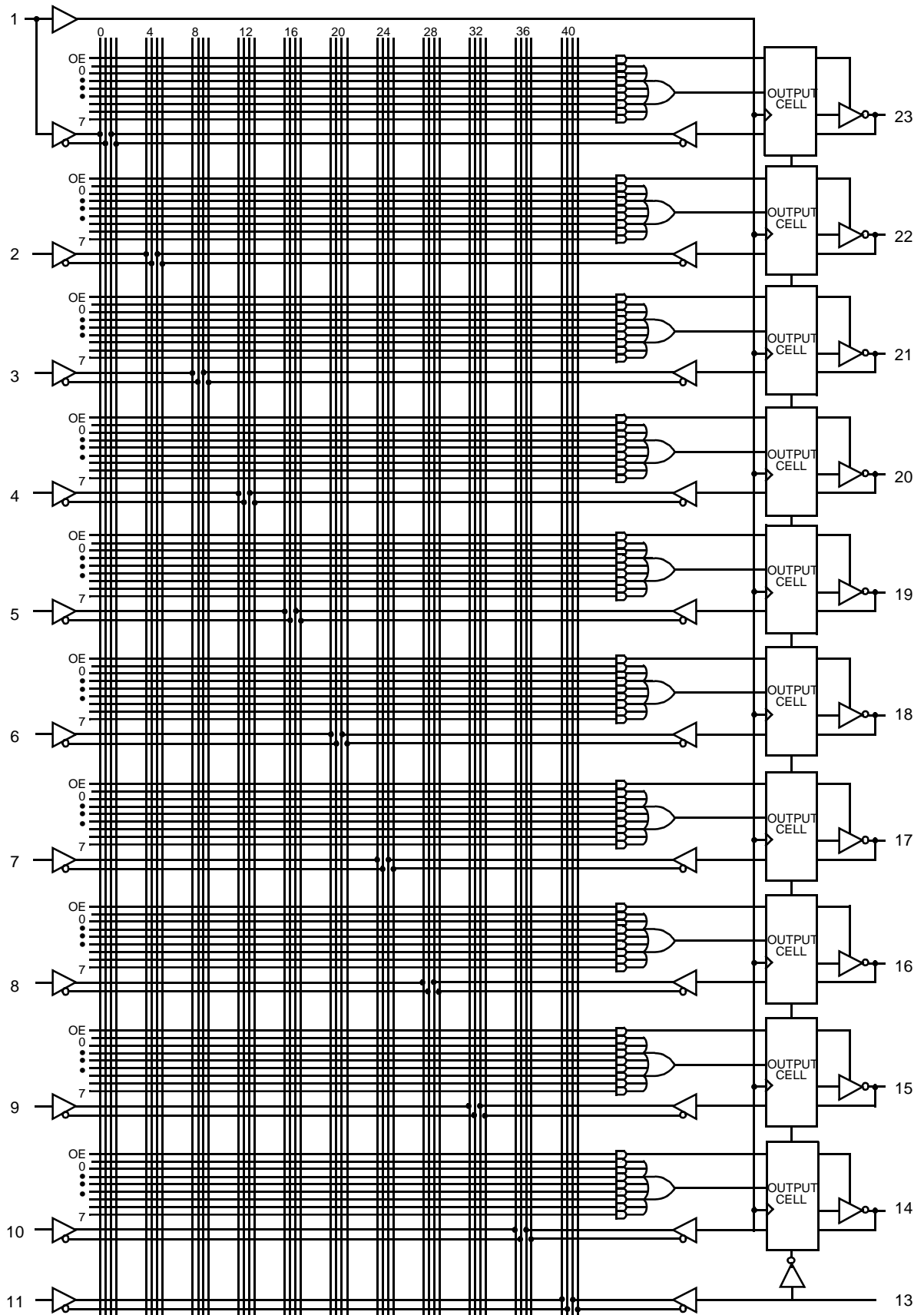
Switching Characteristics Over Operating Range^[3, 8, 9] (continued)

| Parameter | Description | Military/Industrial | | | | | | | | Unit |
|------------------|--|---------------------|------|------|------|------|------|------|------|------|
| | | B-20 | | B-25 | | -30 | | -40 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{PD} | Input or Feedback to Non-Registered Output | | 20 | | 25 | | 30 | | 40 | ns |
| t_{EA} | Input to Output Enable | | 20 | | 25 | | 30 | | 40 | ns |
| t_{ER} | Input to Output Disable | | 20 | | 25 | | 30 | | 40 | ns |
| t_{PZX} | Pin 11 to Output Enable | | 17 | | 20 | | 25 | | 25 | ns |
| t_{PXZ} | Pin 11 to Output Disable | | 17 | | 20 | | 25 | | 25 | ns |
| t_{CO} | Clock to Output | | 15 | | 15 | | 20 | | 25 | ns |
| t_S | Input or Feedback Set-Up Time | 15 | | 18 | | 20 | | 35 | | ns |
| t_H | Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_P^{[10]}$ | Clock Period | 30 | | 33 | | 40 | | 60 | | ns |
| t_{WH} | Clock High Time | 12 | | 14 | | 16 | | 22 | | ns |
| t_{WL} | Clock Low Time | 12 | | 14 | | 16 | | 22 | | ns |
| $f_{MAX}^{[11]}$ | Maximum Frequency | 33.3 | | 30.3 | | 25.0 | | 16.6 | | MHz |

Switching Waveform


20G10-17

Functional Logic Diagram



Ordering Information

| t_{PD} (ns) | t_S (ns) | t_{CO} (ns) | I_{CC} (mA) | Ordering Code | Package Name | Package Type | Operating Range |
|------------------|---------------|------------------|------------------|-------------------|--------------|-------------------------------------|---------------------------|
| 15 | 12 | 10 | 70 | PLDC20G10B-15PC | P13 | 24-Lead (300-Mil) Molded DIP | Commercial |
| | | | | PLDC20G10B-15WC | W14 | 24-Lead (300-Mil) Windowed CerDIP | |
| 20 | 15 | 15 | 100 | PLDC20G10B-20DMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| 25 | 15 | 15 | 55 | PLDC20G10-25JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| | | | | PLDC20G10-25PC/PI | P13 | 24-Lead (300-Mil) Molded DIP | Commercial/ Industrial |
| | | | | PLDC20G10-25WC | W14 | 24-Lead (300-Mil) Windowed CerDIP | Commercial |
| 30 | 20 | 20 | 80 | PLDC20G10-30DMB | D14 | 24-Lead (300-Mil) CerDIP | Military |
| | | | | PLDC20G10-30LMB | L64 | 28-Square Leadless Chip Carrier | |
| | | | | PLDC20G10-30WMB | W14 | 24-Lead (300-Mil) Windowed CerDIP | |
| 35 | 30 | 25 | 55 | PLDC20G10-35JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| | | | | PLDC20G10-35PC | P13 | 24-Lead (300-Mil) Molded DIP | |

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

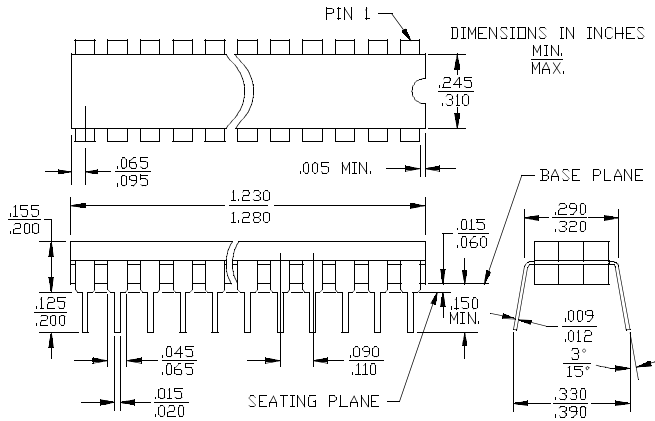
| Parameter | Subgroups |
|-----------|-----------|
| V_{OH} | 1, 2, 3 |
| V_{OL} | 1, 2, 3 |
| V_{IH} | 1, 2, 3 |
| V_{IL} | 1, 2, 3 |
| I_{IX} | 1, 2, 3 |
| I_{OZ} | 1, 2, 3 |
| I_{CC} | 1, 2, 3 |

Switching Characteristics

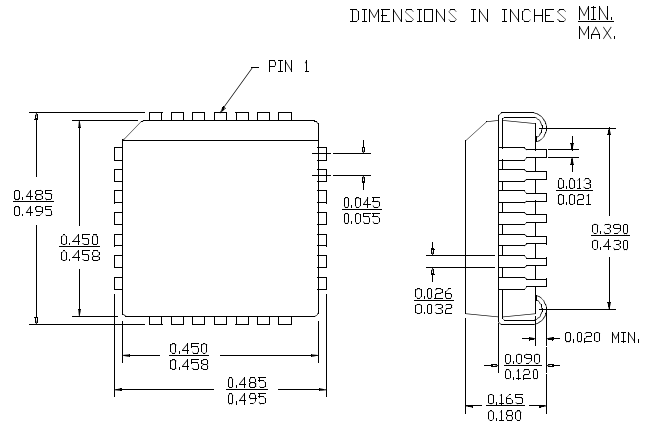
| Parameter | Subgroups |
|-----------|-----------|
| t_{PD} | 9, 10, 11 |
| t_{PZX} | 9, 10, 11 |
| t_{CO} | 9, 10, 11 |
| t_S | 9, 10, 11 |
| t_H | 9, 10, 11 |

Package Diagrams

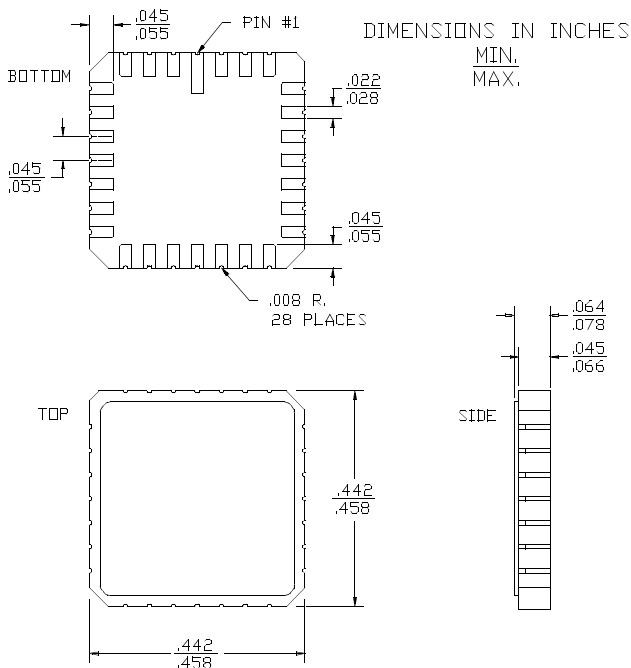
24-Lead (300-Mil) CerDIP D14
MIL-STD-1835 D-9Config.A



28-Lead Plastic Leaded Chip Carrier J64

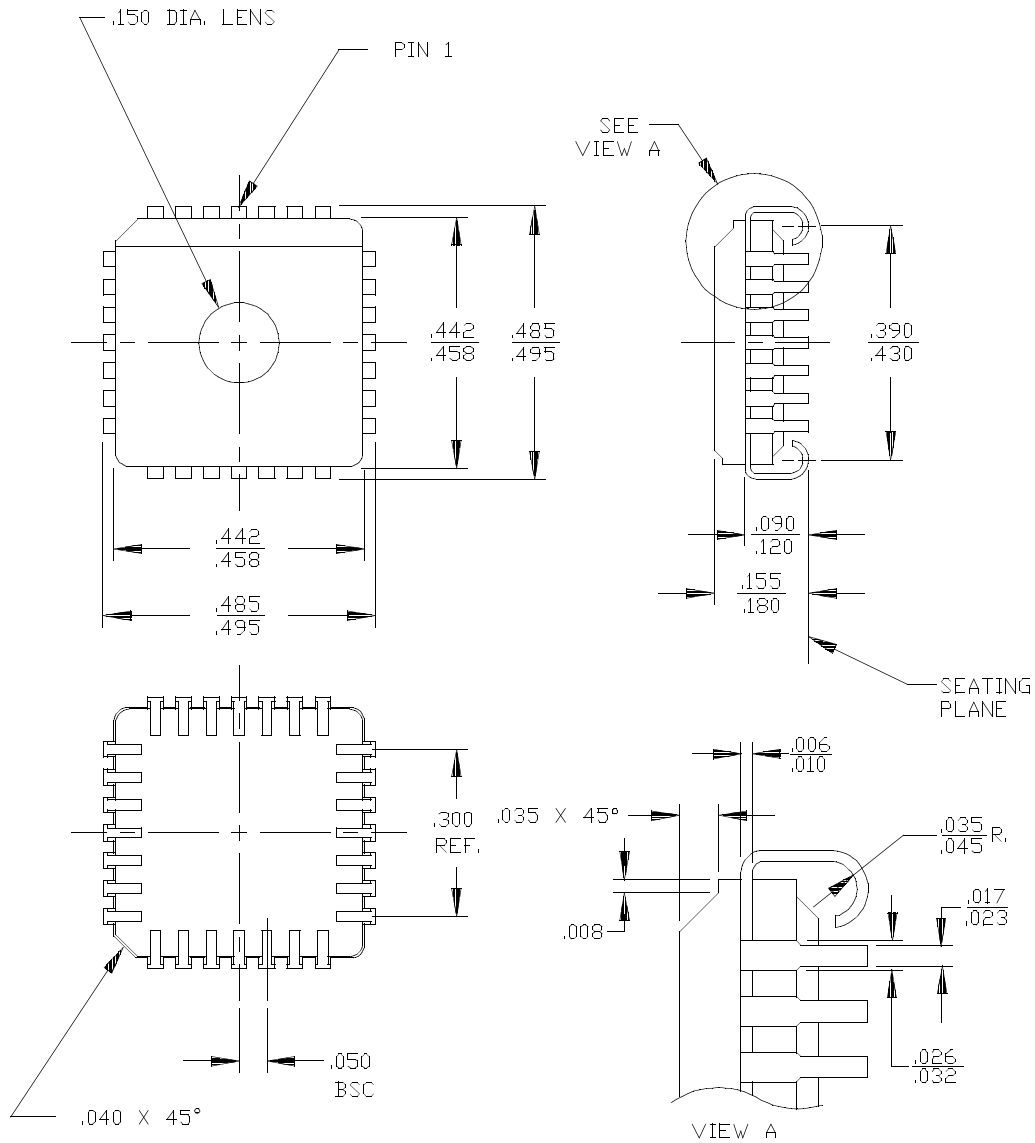


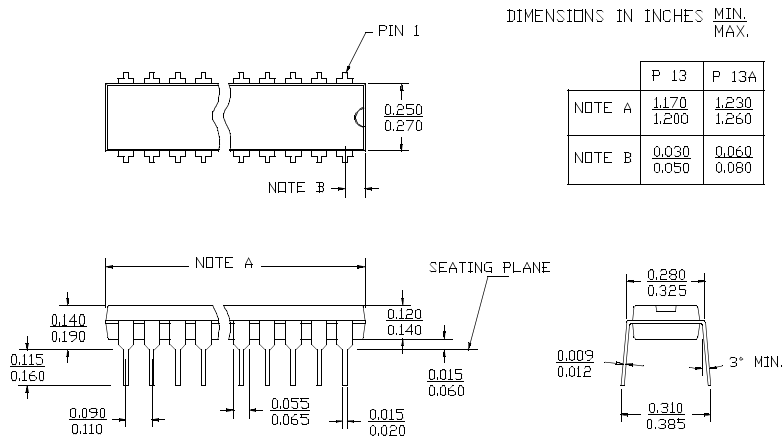
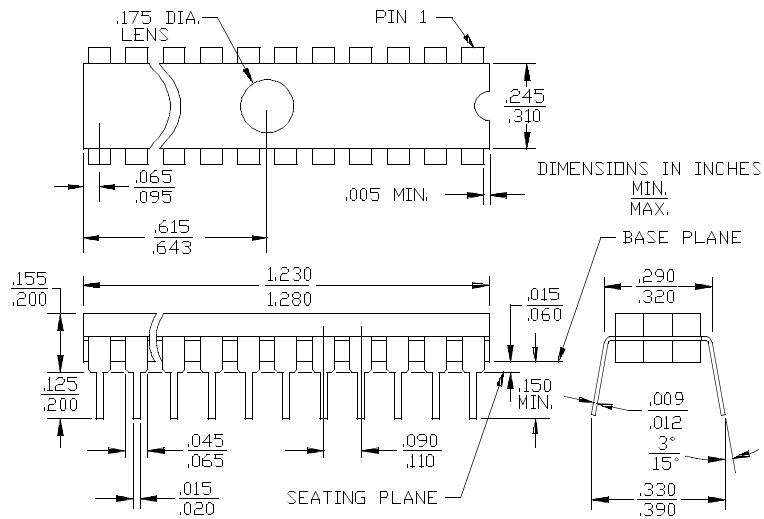
28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4



Package Diagrams (continued)

28-Pin Windowed Leaded Chip Carrier H64




Package Diagrams (continued)
24-Lead (300-Mil) Molded DIP P13/P13A

24-Lead (300-Mil) Windowed CerDIP W14
 MIL-STD-1835 D-9Config.A




| Document Title: PLDC20G10B/PLDC20G10 CMOS Generic 24-Pin Reprogrammable Logic Device Document Number: 38-03010 | | | | |
|---|----------------|-------------------|------------------------|---|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 106292 | 04/25/01 | SZV | Change from Spec number: 38-00019 to 38-03010 |

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