THE DATASHEET OF

PI7C9X762BZHEX

A product Line of
Diodes Incorporated

PI7C9X762

I²C-bus/SPI to UART Bridge Controller w/ 64 bytes of TX/RX FIFOs

Features

- Dual channel full-duplex UART
- Support I²C-bus or SPI interface
- 64 bytes FIFO (transmitter and receiver)
- Fully compatible with industrial standard 16C450 and equivalent
- Baud Rates up to 16Mbit/s in 4X sampling clock rate
- Programmable character formatting
  - 5-bit, 6-bit, 7-bit or 8-bit character
  - Even, odd, or no parity
  - 1, 1.5, or 2 stop bits
- Programmable Receive and Transmit FIFO trigger levels
- Special character detection
- Internal Loopback mode
- Line break generation and detection

Flow control

- Support hardware flow control using RTS/CTS
- Support software flow control with programmable Xon/Xoff characters
- Programmable single or double Xon/Xoff characters

Interface control

- Automatic RS-485 slave address detection
- RS-485 driver direction control via RTS signal
- RS-485 driver direction control inversion
- Built-in IrDA encoder and decoder interface
- Supports IrDA SIR with speeds up to 115.2 kbit/s (optional 1.152Mbps)
- Up to eight user programmable GPIO pins
- Software reset

Others

- Low standby current at 3.3 V
- Wide operation voltage (1.8V, 2.5V or 3.3V)
- Industrial temperature ranges -40 ˚C to 85 ˚C
- Available in TSSOP28 and TQFN32 Packages

I²C interface

- Compliant with I²C-bus fast speed
- Support slave mode only
- Crystal oscillator (up to 24MHz) or external clock (up to 64MHz) input

SPI interface

- PI7C9X762 supports 33 Mbit/s maximum SPI clock speed
- Support SPI mode 0 (slave mode only)

Description

The PI7C9X762 is a I²C-bus/SPI to a dual-channel high performance UART bridge controller. It offers data rates up to 33 Mbps and guarantees low operating and sleeping current. The PI7C9X762 also has up to 8 additional programmable general purpose I/O [GPIO] pins. The device comes in very small TSSOP28 packages, which makes it ideally suitable for cost efficient, handheld, battery operated applications. These UARTs provide a bridge for protocol conversion from I²C -bus or SPI to and RS-232/RS-485 and are fully bidirectional.

The PI7C9X762 supports SPI clock speeds up to 33 Mbps and IrDA SIR up to 1.152 Mbit/s.

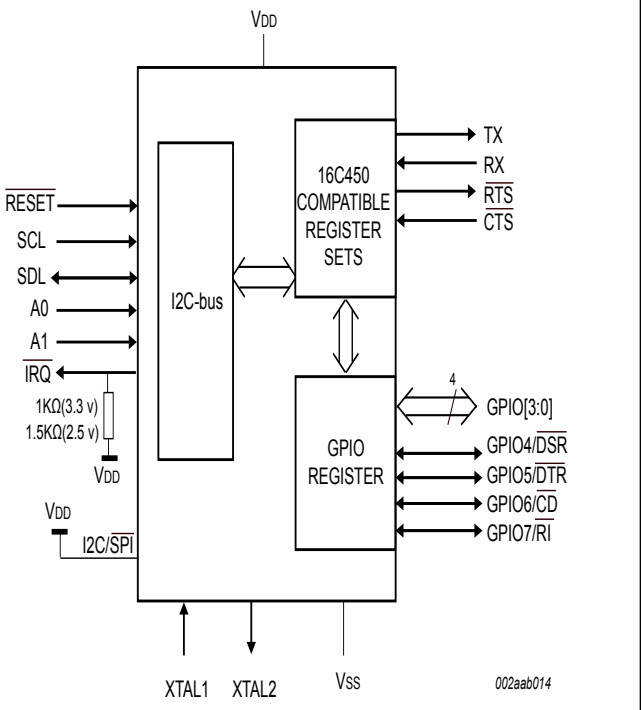
PI7C9X762's internal register set is backward-compatible with the widely used and widely popular 16C450 UART. The PI7C9X762 also provides additional advanced features such as auto hardware and software flow control, automatic RS-485 support, support for fractional baud rates and software reset. This allows the software to reset the UART at any moment, independent of the hardware reset signal.

Application

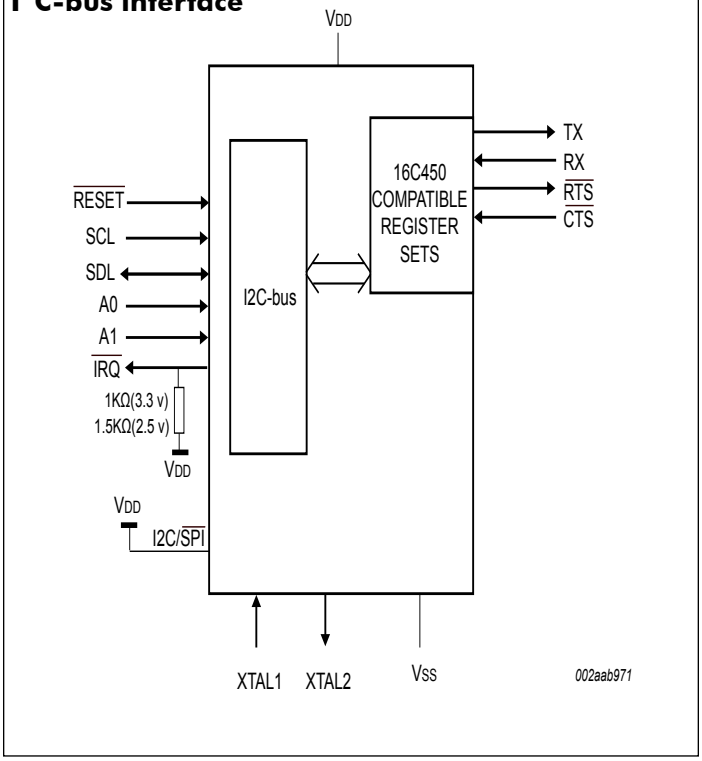
- Industrial computing
- Automation
- Factory process control
- Mobile computing
- Embedded applications
- Battery operated devices
- Networking

Block Diagram

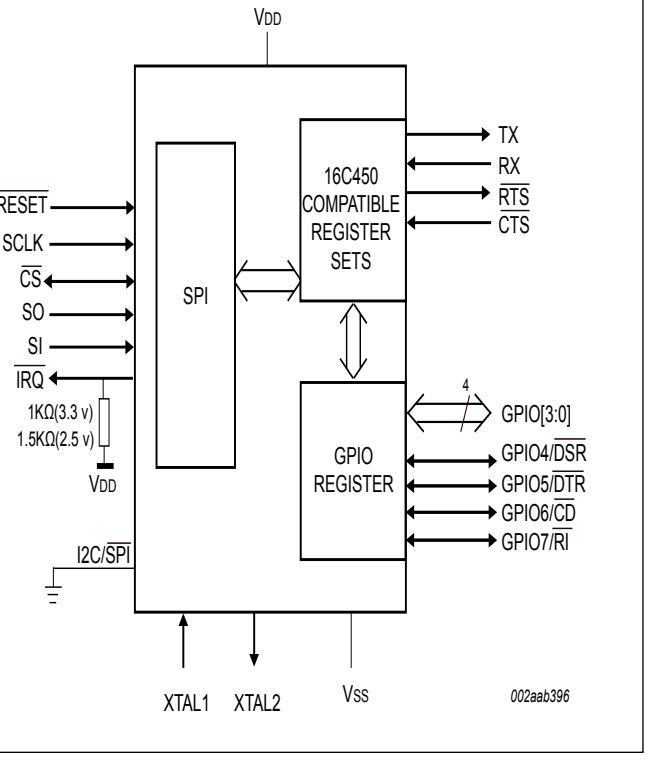
I²C-bus interface



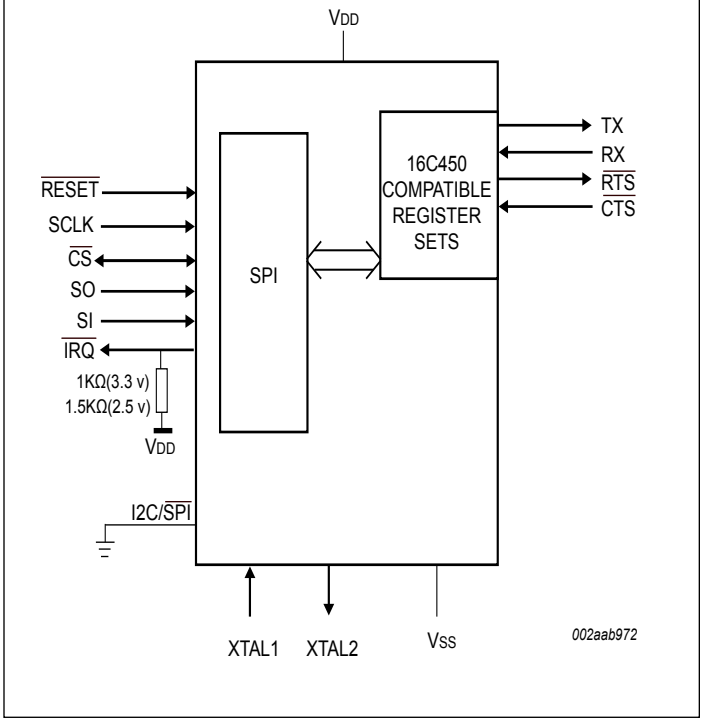
I²C-bus interface



SPI interface

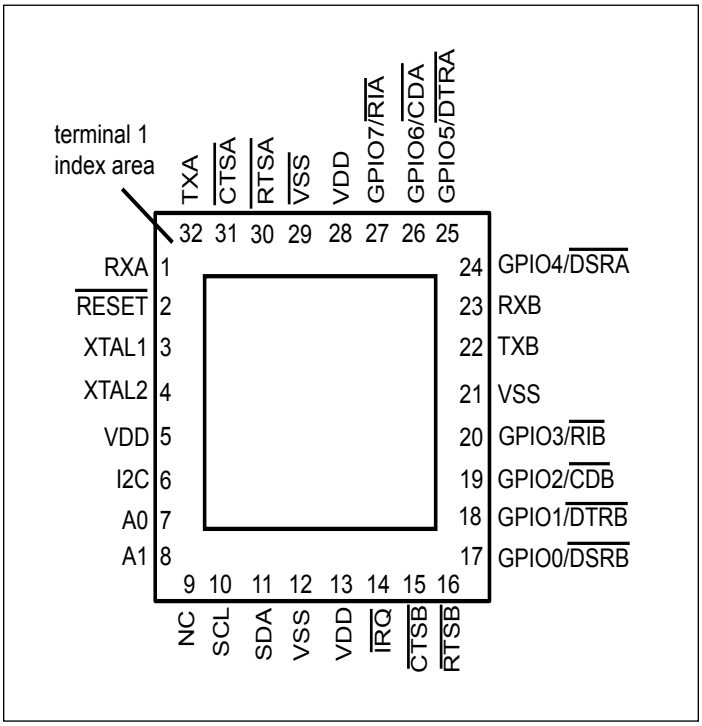


SPI interface

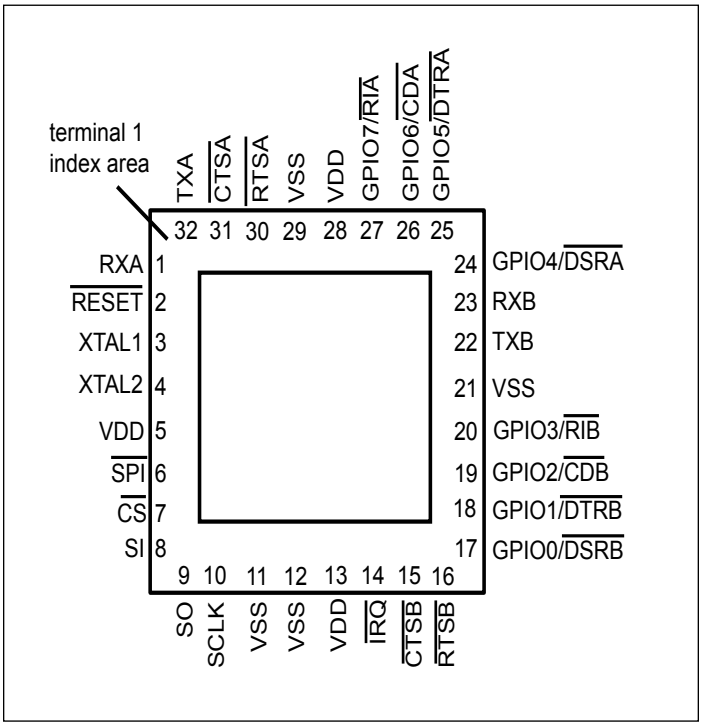


Pin Configuration

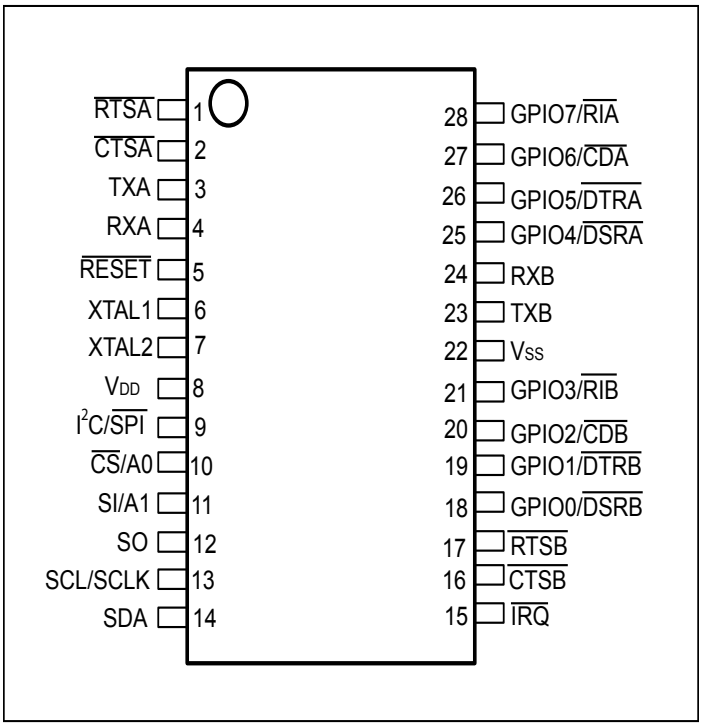
32-Pin TQFN (I²C-Bus Interface)



32-Pin TQFN (SPI Interface)



28-Pin TSSOP



Pin Description

Pin Name	28-TSSOP Pin#	32-TQFN Pin#	Type	Description
I^2C (SPI) INTERFACE				
$\overline{CS}$/A0	10	7	I	SPI chip select or I^2C-bus device address select A0. If SPI confguration is selected by I^2C/SPI Chip select pin (Schmitt-trigger active LOW). If I^2C-BUS configuration is selected by I2C/SPI pin, this pin along with A1 pin allows user to change the device's base address. To select the device address, please refer to table 9.
$\overline{CTSA}$	2	31	I	UART clear to send (active LOW), channel A. Alogic 0 (LOW) on the $\overline{CTSA}$ pin indicates the modem or data set is ready to accept transmit data from the PI7C9X762. Status can be tested by reading MSR(4). This pim only affects the transmit and receive operations when Auto-$\overline{CTS}$ function is enabled via the Enhanced Features Register EFR(7) for hardware flow control operation.
$\overline{CTSB}$	16	15	I	UART clear to send (active LOW), channel B. Alogic 0 on the $\overline{CTSB}$ pin indicates the modem or data set is ready to accept transmit data from the PI7C9X762. Status can be tested by reading MSR(4). This pim only affects the transmit and receive operations when Auto-$\overline{CTS}$ function is enabled via the Enhanced Features Register EFR(7) for hardware flow control operation.
$I^2C/\overline{SPI}$	9	6	I	I^2C-bus or SPI interface select. I^2C-Bus interface is selected if this pin is at logic HIGH. SPI interface is selected if this pin is at logic LOW.
$\overline{IRQ}$	15	14	O	Interrupt (open-drain, active LOW). Interrupt is enabled when interrupt sources are enabled in the Interrupt Enable Register (IER). Interrupt conditions include: change of state of the input pins, receiver errors, available receiver buffer data, availble transmit buffer space, or when a modem status flag is detected. An extemal resistor (1 k-ohm for 3.3 V, 1.5 k-ohm for 2.5 V) must be connected between this pin and V_{DD}.
SI/A1	11	8	I	SPI data input pin or I^2C-bus device address select A1. If SPI configuration is selected by $I^2C/\overline{SPI}$ pin, this is the SPI data input pin. If I^2C-bus configuration is selected by $I^2C/\overline{SPI}$ pin, this pin, this along with the A0 pin allows user to change the slave base address. To select the device address, p;ease refer to Table 9.
SO	12	9	O	SPI data output pin. If SPI configuration is selected by $I^2C/\overline{SPI}$ pin, this is a 3-stateable output pin. If I^2C-bus sonfiguration is selected by the $I^2C/\overline{SPI}$ pin, this pin is undefined and must be left as not connected.
SCL/SCLK	13	10	I	I^2C-bus or SPI input clock.
SDA	14	11	I/O	I^2C-bus data input/output, open-drain if I2C-bus configuration is selected by $I^2C/\overline{SPI}$ pin. If SPI configuration is selected, this is not used and must be connected to V_{SS}.
GPIO0/$\overline{DSRB}$	18	17	I/O	Programmable I/O pin or modem DSRB
GPIO1/$\overline{DTRB}$	19	18	I/O	Programmable I/O pin or modem DTRB
GPIO2/$\overline{CDB}$	20	19	I/O	Programmable I/O pin or modem CDB
GPIO3/$\overline{RIB}$	21	20	I/O	Programmable I/O pin or modem RIB
GPIO4/$\overline{DSRA}$	25	24	I/O	Programmable I/O pin or modem DSRA
GPIO5/$\overline{DTRA}$	26	25	I/O	Programmable I/O pin or modem DTRA

Pin Description Cont.

Pin Name	28-TSSOP Pin#	32-TQFN Pin#	Type	Description
GPIO6/$\overline{\text{CDA}}$	27	26	I/O	Programmable I/O pin or modem CDA
GPIO7/$\overline{\text{RIA}}$	28	27	I/O	Programmable I/O pin or modem RIA
$\overline{\text{RESET}}$	5	2	I	Hardware reset (active LOW)
$\overline{\text{RTSA}}$	1	30	O	UART request to send (active LOW). A logic 0 on the $\overline{\text{RTSA}}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the Modem Control Register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin set to a logic 1. This pin only affects the transmit and receive operations when Auto-$\overline{\text{RTS}}$ function is enabled via the Enhanced Feature Register (EFR[6]) for hardware flow control operation.
$\overline{\text{RTSB}}$	17	16	O	UART request to send (active LOW). A logic 0 on the $\overline{\text{RTSB}}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the Modem Control Register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin set to a logic 1. This pin only affects the transmit and receive operations when Auto-$\overline{\text{RTS}}$ function is enabled via the Enhanced Feature Register (EFR[6]) for hardware flow control operation.
RXA	4	1	I	Channel A receiver input. During the local Loopback mode, the RXA input pin is disabled and TXA data is connected to the UARTA RXA input internally.
RXB	24	23	I	Channel B receiver input. During the local Loopback mode, the RXB input pin is disabled and TXB data is connected to the UARTA RXB input internally.
TXA	3	32	O	Channel A transmitter output. During the local Loopback mode, the TXA input pin is disabled and TXA data is connected to the UARTA RXA input internally.
TXB	23	22	O	Channel B transmitter output. During the local Loopback mode, the TXB input pin is disabled and TXB data is connected to the UARTA RXB input internally.
V_{DD}	8	5, 13, 28		Power supply.
V_{SS}	22	12, 21, 29		Ground
V_{SS}		center pad		The certer pad on the back side of the QFN32 package is metallic aand should be connected to ground on the printed-circuit board.
XTAL1	6	3	I	Crystal input or external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 11). Alternatively, an external clock can be connected to this pin.
XTAL2	7	4	O	Crystal output. (See also XTAL1.) XTAL2 is used as a crystal oscillator output.

Functional Description

The UART will perform serial-to-I^{2}C-bus conversion on data characters received from peripheral devices or modems, and I^{2}C-bus-to-serial conversion on data characters transmitted by the host. The complete status of the UART can be read at any time during functional operation by the host.

The UART can be placed in an alternate mode (FIFO mode) relieving the host of excessive software overhead by buffering received/transmitted characters. Both the receiver and transmitter FIFOs can store up to 64 characters (including three additional bits of error status per character for the receiver FIFO) and have selectable or programmable trigger levels.

The UART has selectable hardware flow control and software flow control. Hardware flow control significantly reduces software overhead and increases system efficiency by automatically controlling serial data flow using the $\overline{RTS}$ output and $\overline{CTS}$ input signals. Software flow control automatically controls data flow by using programmable Xon/Xoff characters.

The UART includes a programmable baud rate generator that can divide the timing reference clock input by a divisor between 1 and (2^{16} - 1).

1. Trigger levels

The UART provides independently selectable and programmable trigger levels for both receiver and transmitter interrupt generation. After reset, both transmitter and receiver FIFOs are disabled and so, in effect, the trigger level is the default value of one character. The selectable trigger levels are available via the FIFO Control Register (FCR). The programmable trigger levels are available via the Trigger Level Register (TLR). If TLR bits are cleared, then selectable trigger level in FCR is used. If TLR bits are not cleared, then programmable trigger level in TLR is used.

2. Hardware flow control

Hardware flow control is comprised of Auto-$\overline{CTS}$ and Auto-RTS (see Figure 1). Auto-$\overline{CTS}$ and Auto-$\overline{RTS}$ can be enabled/disabled independently by programming EFR[7:6].

With Auto-$\overline{CTS}$, $\overline{CTS}$ must be active before the UART can transmit data.

Auto-$\overline{RTS}$ only activates the $\overline{RTS}$ output when there is enough room in the FIFO to receive data and de-activates the $\overline{RTS}$ output when the RX FIFO is sufficiently full. The halt and resume trigger levels in the Transmission Control Register (TCR) determine the levels at which $\overline{RTS}$ is activated/deactivated. If TCR bits are cleared, then selectable trigger levels in FCR are used in place of TCR.

If both Auto-$\overline{CTS}$ and Auto-$\overline{RTS}$ are enabled, when $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receiver FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If not enabled, overrun errors occur if the transmit data rate exceeds the receive FIFO servicing latency.

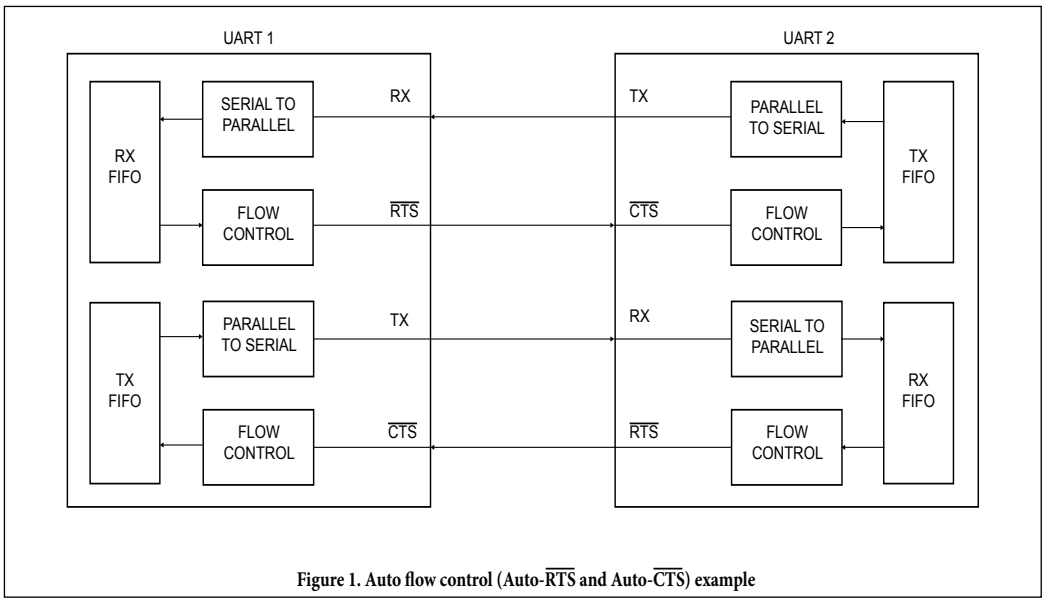
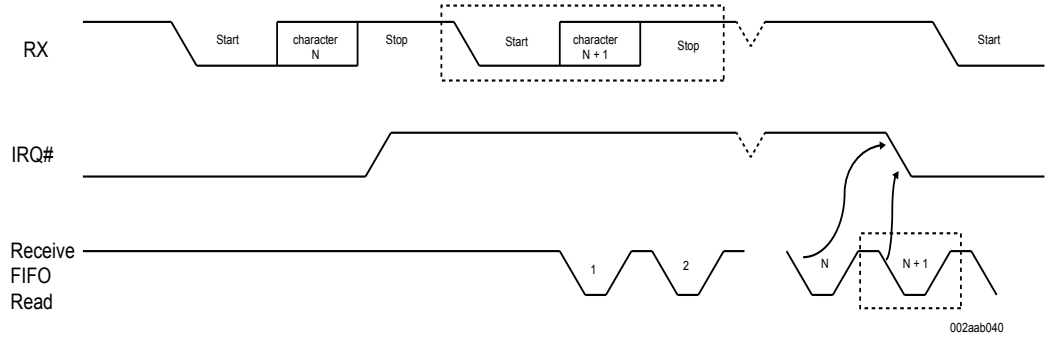


Figure 1. Auto flow control (Auto-$\overline{RTS}$ and Auto-$\overline{CTS}$) example

2.1 Auto-RTS

Figure 2 shows $\overline{RTS}$ functional timing. The receiver FIFO trigger levels used in Auto-$\overline{RTS}$ are stored in the TCR. RTS is active if the RX FIFO level is below the halt trigger level in TCR[3:0]. When the receiver FIFO halt trigger level is reached, RTS is de-asserted. The sending device (for example, another UART) may send an additional character after the trigger level is reached (assuming the sending UART has another character to send) because it may not recognize the de-assertion of $\overline{RTS}$ until it has begun sending the additional character. $\overline{RTS}$ is automatically reasserted once the receiver FIFO reaches the resume trigger level programmed via TCR[7:4]. This re-assertion allows the sending device to resume transmission.

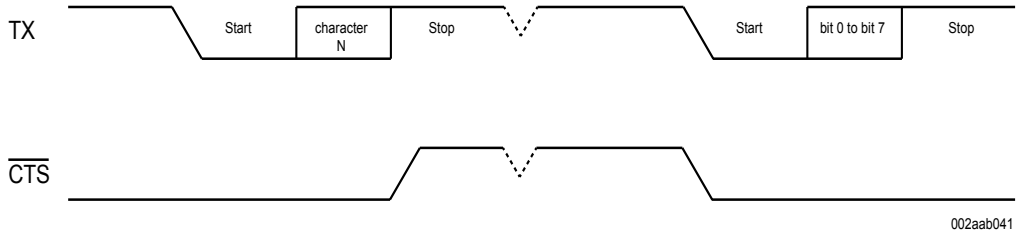


(1) N = receiver FIFO trigger level.
(2) The two blocks in dashed lines cover the case where an additional character is sent.

Figure 2. RTS functional timing

2.2 Auto-CTS

Figure 3 shows $\overline{CTS}$ functional timing. The transmitter circuitry checks $\overline{CTS}$ before sending the next data character. When $\overline{CTS}$ is active, the transmitter sends the next character. To stop the transmitter from sending the following character, $\overline{CTS}$ must be de-asserted before the middle of the last stop bit that is currently being sent. The Auto-$\overline{CTS}$ function reduces interrupts to the host system. When flow control is enabled, $\overline{CTS}$ level changes do not trigger host interrupts because the device automatically controls its own transmitter. Without Auto-$\overline{CTS}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error may result.



(1) When $\overline{CTS}$ is LOW, the transmitter keeps sending serial data out.
(2) When $\overline{CTS}$ goes HIGH before the middle of the last stop bit of the current character, the transmitter finishes sending the current
character, but it does not send the next character.
(3) When $\overline{CTS}$ goes from HIGH to LOW, the transmitter begins sending data again.

Figure 3. $\overline{CTS}$ functional timing

3 Software flow control

Software flow control is enabled through the Enhanced Features Register and the Modem Control Register. Different combinations of software flow control can be enabled by setting different combinations of EFR[3:0]. Table 1 shows software flow control options.

Table 1. Software flow control options (EFR[3:0])

EFR[3]	EFR[2]	EFR[1]	EFR[0]	TX, RX software flow control
0	0	x	x	no transmit flow control
1	0	x	x	transmit Xon1, Xoff1
0	1	x	x	transmit Xon2, Xoff2
1	1	x	x	transmit Xon1 and Xon2, Xoff1 and Xoff2
x	x	0	0	no receive flow control
x	x	1	0	receiver compares Xon1, Xoff1
x	x	0	1	receiver compares Xon2, Xoff2
1	0	1	1	transmit Xon1, Xoff1 receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	transmit Xon2, Xoff2 receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	transmit Xon1 and Xon2, Xoff1 and Xoff2 receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	0	1	1	no transmit flow control receiver compares Xon1 and Xon2, Xoff1 and Xoff2

There are two other enhanced features relating to software flow control:

• Xon Any function (MCR[5]): Receiving any character will resume operation after recognizing the Xoff character. It is possible that an Xon1 character is recognized as an Xon Any character, which could cause an Xon2 character to be written to the RX FIFO.

• Special character (EFR[5]): Incoming data is compared to Xoff2. Detection of the special character sets the Xoff interrupt (IIR[4]) but does not halt transmission. The Xoff interrupt is cleared by a read of the Interrupt Identification Register (IIR). The special character is transferred to the RX FIFO.

3.1 Receive flow control

When software flow control operation is enabled, UART will compare incoming data with Xoff1/Xoff2 programmed characters (in certain cases, Xoff1 and Xoff2 must be received sequentially). When the correct Xoff characters are received, transmission is halted after completing transmission of the current character. Xoff detection also sets IIR[4] (if enabled via IER[5]) and causes $\overline{\text{IRQ}}$ to go LOW.

To resume transmission, an Xon1/Xon2 character must be received (in certain cases Xon1 and Xon2 must be received sequentially). When the correct Xon characters are received, IIR[4] is cleared, and the Xoff interrupt disappears.

3.2 Transmit flow control

Xoff1/Xoff2 character is transmitted when the RX FIFO has passed the halt trigger level programmed in TCR[3:0], or the selectable trigger level in FCR[7:6].

Xon1/Xon2 character is transmitted when the RX FIFO reaches the resume trigger level programmed in TCR[7:4], or falls below the lower selectable trigger level in FCR[7:6].

The transmission of Xoff/Xon(s) follows the exact same protocol as transmission of an ordinary character from the FIFO. This means that even if the word length is set to be 5, 6, or 7 bits, then the 5, 6, or 7 least significant bits of Xoff1/Xoff2, Xon1/Xon2 will be transmitted. (Note that the transmission of 5, 6, or 7 bits of a character is seldom done, but this functionality is included to maintain compatibility with earlier designs.)

It is assumed that software flow control and hardware flow control will never be enabled simultaneously. Figure 4 shows an example of software flow control.

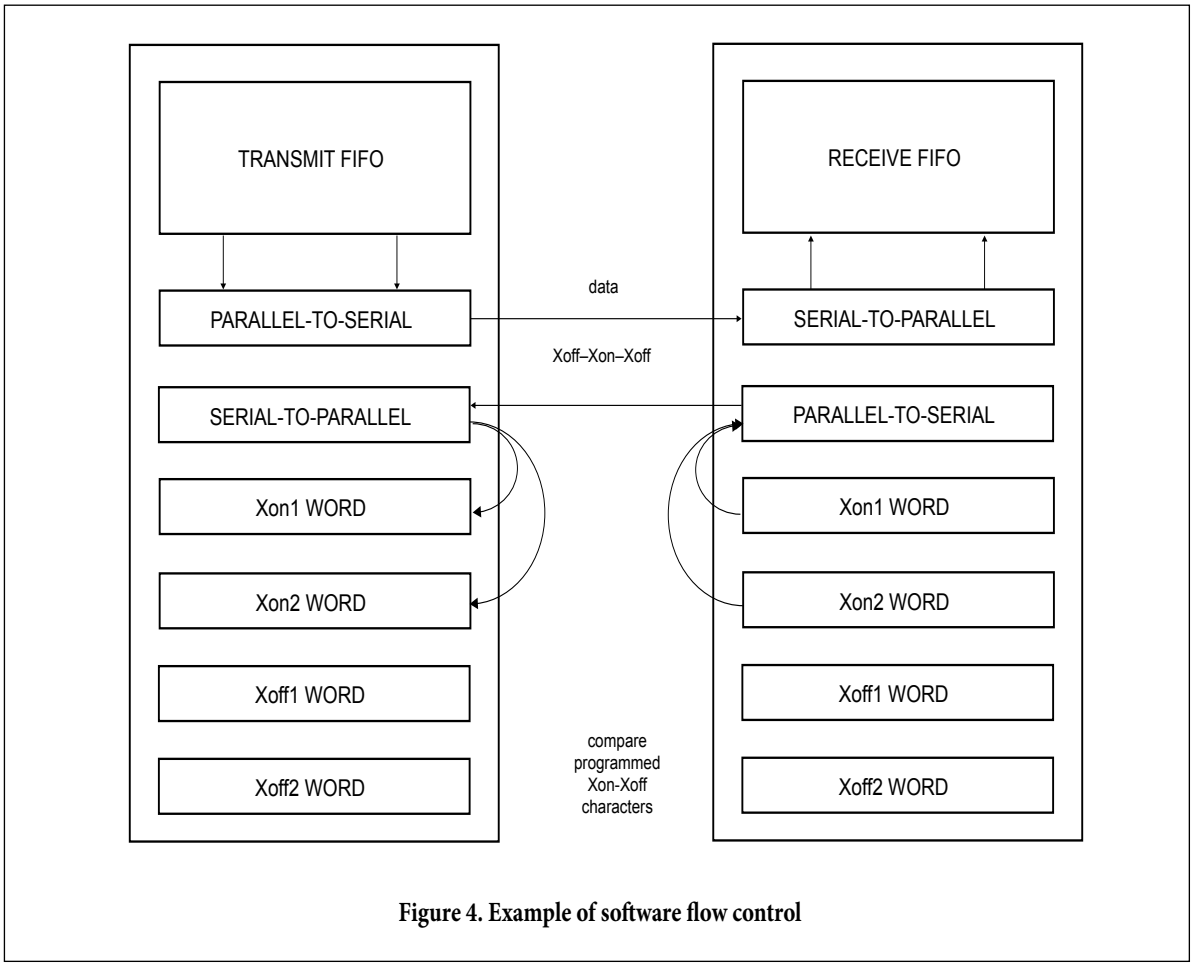


Figure 4. Example of software flow control

4. Hardware Reset, Power-On Reset (POR) and Software Reset

These three reset methods are identical and will reset the internal registers as indicated in Table 4.

Table 2 summarizes the state of register after reset.

Table 2. Register reset

Register	Reset state
Interrupt Enable Register	all bits cleared
Interrupt Identification Register	bit 0 is set; all other bits cleared
FIFO Control Register	all bits cleared
Line Control Register	reset to 0001 1101 (0x1D)
Modem Control Register	all bits cleared
Line Status Register	bit 5 and bit 6 set; all other bits cleared
Modem Status Register	bits 3:0 cleared; bits 7:4 input signals
Enhanced Features Register	all bits cleared
Receive Holding Register	pointer logic cleared
Transmit Holding Register	pointer logic cleared
Transmission Control Register	all bits cleared
Trigger Level Register	all bits cleared
Transmit FIFO level	reset to 0100 0000 (0x40)
Receive FIFO level	all bits cleared
I/O direction	all bits cleared
I/O interrupt enable	all bits cleared
I/O control	all bits cleared
Extra Features Control Register	all bits cleared

Remark: Registers DLL, DLH, SPR, XON1, XON2, XOFF1, XOFF2 are not reset by the top-level reset signal RESET, Software Reset, that is, they hold their initialization values during reset.

Table 3 summarizes the state of output signals after reset.

Table 3. Output signals after reset

Signal	Reset state
TX	HIGH
$\overline{\text{RTS}}$	HIGH
I/Os	inputs
$\overline{\text{IRQ}}$	HIGH by external pull-up

5 Interrupts

The UART has interrupt generation and prioritization (seven prioritized levels of interrupts) capability. The interrupt enable registers (IER and IOIntEna) enable each of the seven types of interrupts and the IRQ signal in response to an interrupt generation. When an interrupt is generated, the IIR indicates that an interrupt is pending and provides the type of interrupt through IIR[5:0]. Table 4 summarizes the interrupt control functions.

Table 4. Interrupt Source and Priority Level

IIR[5:0]	Priority level	Interrupt type	Interrupt source
00 0001	none	none	None
00 0110	1	receiver line status	Overrun Error (OE), Framing Error (FE), Parity Error (PE), or Break Interrupt (BI) errors occur in characters in the RX FIFO
00 1100	2	RX time-out	Stale data in RX FIFO
00 0100	2	RHR interrupt	Receive data ready (FIFO disable) or RX FIFO above trigger level (FIFO enable)
00 0010	3	THR interrupt	Transmit FIFO empty (FIFO disable) or TX FIFO passes above trigger level (FIFO enable)
00 0000	4	modem status	Change of state of modem input pins
11 0000	5	I/O pins	Input pins change of state
01 0000	6	Xoff interrupt	Receive Xoff character(s)/special character
10 0000	7	$\overline{\text{CTS}}$, $\overline{\text{RTS}}$	$\overline{\text{RTS}}$ pin or $\overline{\text{CTS}}$ pin change state from active (LOW) to inactive (HIGH)

It is important to note that for the framing error, parity error, and break conditions, Line Status Register bit 7 (LSR[7]) generates the interrupt. LSR[7] is set when there is an error anywhere in the RX FIFO, and is cleared only when there are no more errors remaining in the FIFO. LSR[4:2] always represent the error status for the received character at the top of the RX FIFO. Reading the RX FIFO updates LSR[4:2] to the appropriate status for the new character at the top of the FIFO. If the RX FIFO is empty, then LSR[4:2] are all zeros.

For the Xoff interrupt, if an Xoff flow character detection caused the interrupt, the interrupt is cleared by an Xon flow character detection. If a special character detection caused the interrupt, the interrupt is cleared by a read of the IIR.

5.1 Interrupt mode operation

In Interrupt mode (if any bit of IER[3:0] is 1) the host is informed of the status of the receiver and transmitter by an interrupt signal, $\overline{IRQ}$. Therefore, it is not necessary to continuously poll the Line Status Register (LSR) to see if any interrupt needs to be serviced. Figure 5 shows Interrupt mode operation.

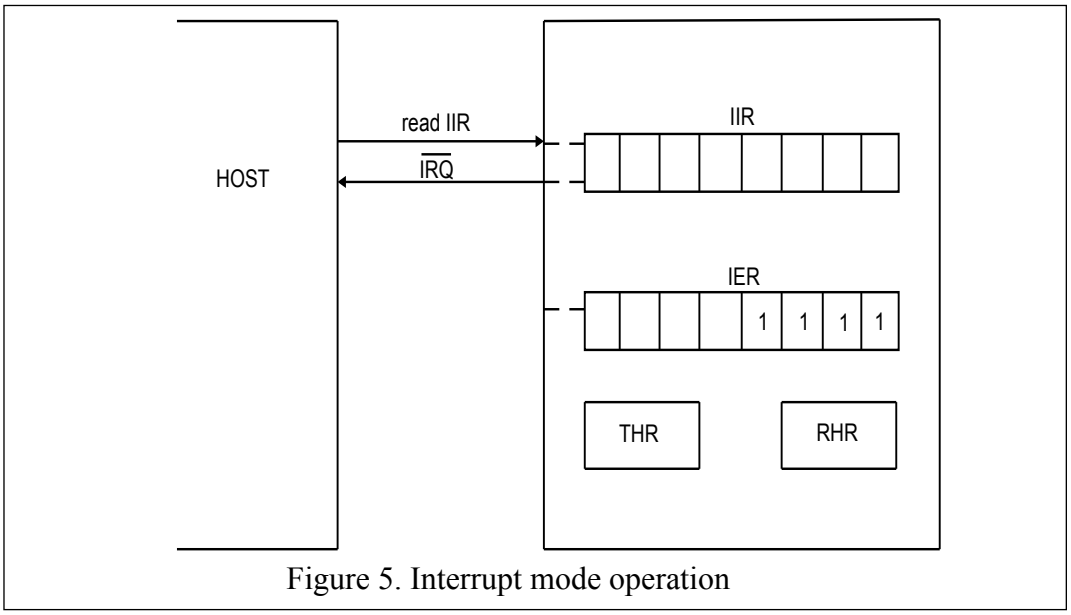


Figure 5. Interrupt mode operation

5.2 Polled mode operation

In Polled mode (IER[3:0] = 0000) the status of the receiver and transmitter can be checked by polling the Line Status Register (LSR). This mode is an alternative to the FIFO Interrupt mode of operation where the status of the receiver and transmitter is automatically known by means of interrupts sent to the CPU. Figure 6 shows FIFO Polled mode operation.

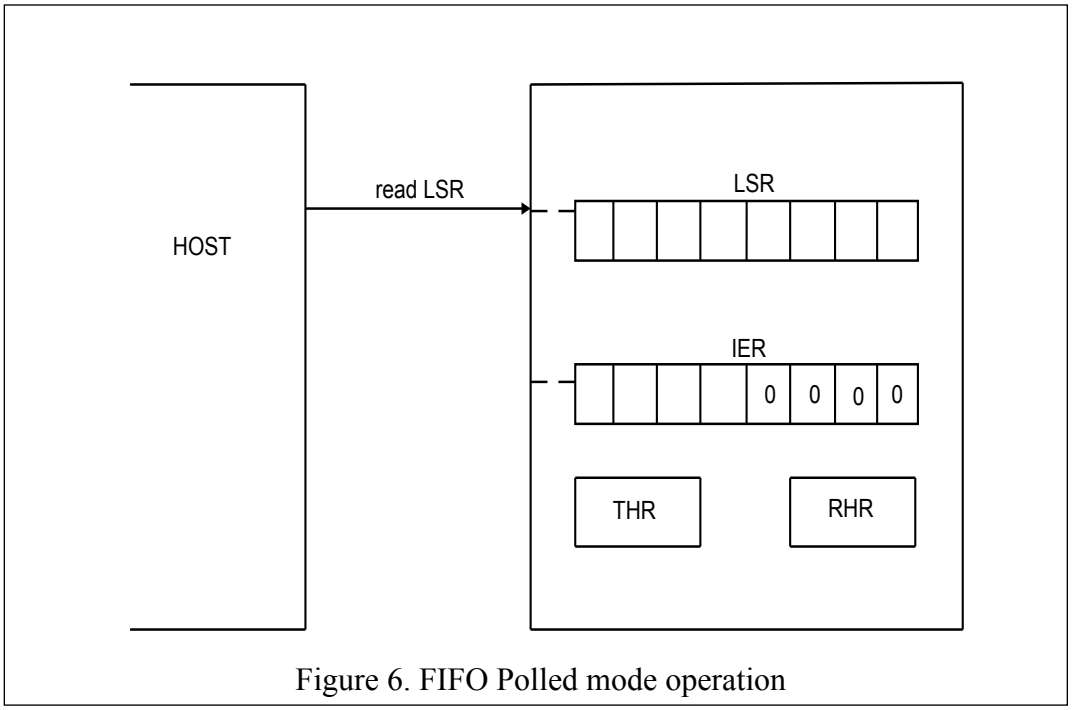


Figure 6. FIFO Polled mode operation

6 Sleep mode

Sleep mode is an enhanced feature of the UART. It is enabled when EFR[4], the enhanced functions bit, is set and when IER[4] is set. Sleep mode is entered when:

- The serial data input line, RX, is idle (see Section 7 “Break and time-out conditions”).
- The TX FIFO and TX shift register are empty.
- There are no interrupts pending except THR.

Remark: Sleep mode will not be entered if there is data in the RX FIFO.

In Sleep mode, the clock to the UART is stopped. Since most registers are clocked using these clocks, the power consumption is greatly reduced. The UART will wake up when any change is detected on the RX line, when there is any change in the state of the

modem input pins, or if data is written to the TX FIFO.

Remark: Writing to the divisor latches DLL and DLH to set the baud clock must not be done during Sleep mode. Therefore, it is advisable to disable Sleep mode using IER[4] before writing to DLL or DLH.

7 Break and time-out conditions

When the UART receives a number of characters and these data are not enough to set off the receive interrupt (because they do not reach the receive trigger level), the UART will generate a time-out interrupt instead, 4 character times after the last character is received. The time-out counter will be reset at the center of each stop bit received or each time the receive FIFO is read.

A break condition is detected when the RX pin is pulled LOW for a duration longer than the time it takes to send a complete character plus start, stop and parity bits. A break condition can be sent by setting LCR[6], when this happens the TX pin will be pulled LOW until LSR[6] is cleared by the software.

8 Programmable baud rate generator

The UART contains a programmable baud rate generator that takes any clock input and divides it by a divisor in the range between 1 and (2^{16} - 1). An additional divide-by-4 prescaler is also available and can be selected by MCR[7], as shown in Figure 7. The formula for the baud rate is:

$$\text{Baud rate} = \frac{\left(\frac{\text{XTAL1 crystal input frequency}}{\text{prescaler}}\right)}{\text{divisor x sample rate}}$$

where:

prescaler = 1, when MCR[7] is set to logic 0 after reset (divide-by-1 clock selected)

prescaler = 4, when MCR[7] is set to logic 1 after reset (divide-by-4 clock selected).

Divisor = {DLH, DLL}

Sample rate = 16 - SCR + CPRN

Remark: The default value of prescaler after reset is divide-by-1.

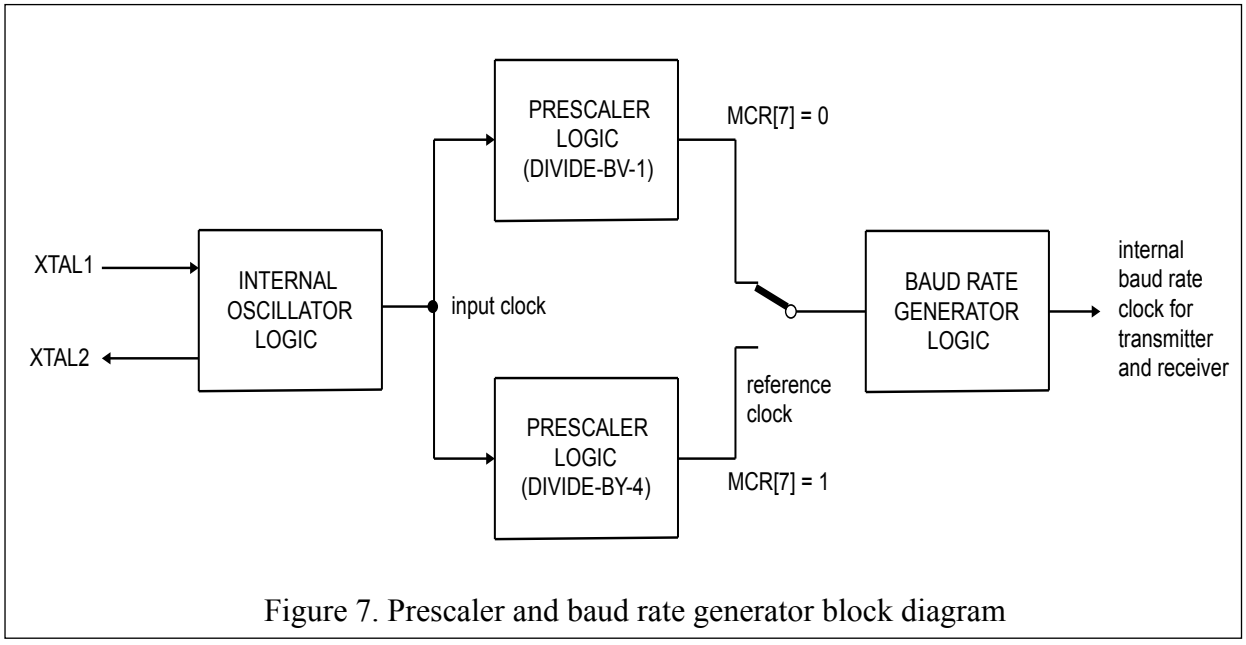


Figure 7. Prescaler and baud rate generator block diagram

DLL and DLH must be written to in order to program the baud rate. DLL and DLH are the least significant and most significant byte of the baud rate divisor. If DLL and DLH are both zero, the UART is effectively disabled, as no baud clock will be generated.

Remark: The programmable baud rate generator is provided to select both the transmit and receive clock rates.

Table 5 to 8 show the baud rate and divisor correlation for crystal with frequency 1.8432 MHz, 3.072 MHz, 14.74926 MHz, and 24MHz respectively.

Figure 8 shows the crystal clock circuit reference.

Table 5. Baud rates using a 1.8432 MHz crystal

Desired baud rate (bit/s)	Divisor used to generate 16x clock	Sample rate	Percent error difference between desired and actual
50	2304	16	0
75	1536	16	0
110	1047	16	0.026
134.5	857	16	0.058
150	768	16	0
300	384	16	0
600	192	16	0
1200	96	16	0
1800	64	16	0
2000	46	20	0.617
2400	48	16	0
3600	32	16	0
4800	24	16	0
7200	16	16	0
9600	12	16	0
19200	6	16	0
38400	3	16	0
56000	2	16	2.86

Table 6. Baud rates using a 3.072 MHz crystal

Desired baud rate (bit/s)	Divisor used to generate 16x clock	Sample rate	Percent error difference between desired and actual
50	2304	16	0
75	2560	16	0
110	1745	16	0.026
134.5	1428	16	0.034
150	1280	16	0
300	640	16	0
600	320	16	0
1200	160	16	0
1800	90	19	0.195
2000	96	16	0
2400	80	16	0
3600	45	19	0.195
4800	40	16	0
7200	25	17	0.392
9600	20	16	0
19200	10	16	0
38400	5	16	0

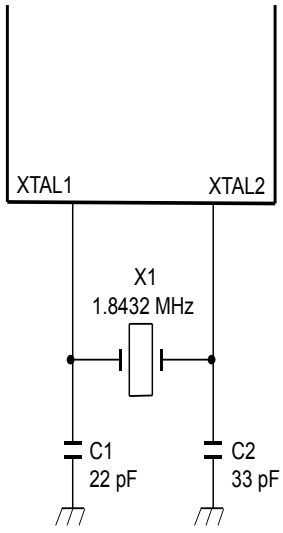


Figure 8. Crystal oscillator circuit reference

Table 7. Baud rates using a 14.74926 MHz crystal

Desired baud rate (bit/s)	Divisor used to generate 16x clock	Sample rate	Percent error difference between desired and actual
38400	24	16	0.025
56000	11	24	0.235
57600	16	16	0.025
115200	8	16	0.025
153600	6	16	0.025
921600	1	16	0.025

Table 8. Baud rates using a 24 MHz crystal

Desired baud rate (bit/s)	Divisor used to generate 16x clock	Sample rate	Percent error difference between desired and actual
4800	250	20	0
7200	159	21	0.17
25000	48	20	0
38400	25	25	0
57600	22	19	0.32
115200	8	26	0.16
225000	6	18	1.2
400000	3	20	0
921600	1	26	0.16
1000000	1	24	0

9. RS-485 features

9.1 Auto RS-485 RTS control

Normally the $\overline{RTS}$ pin is controlled by MCR bit 1, or if hardware flow control is enabled, the logic state of the $\overline{RTS}$ pin is controlled by the hardware flow control circuitry. EFCR register bit 4 will take the precedence over the other two modes; once this bit is set, the transmitter will control the state of the $\overline{RTS}$ pin. The transmitter automatically asserts the $\overline{RTS}$ pin (logic 0) once the host writes data to the transmit FIFO, and de-asserts $\overline{RTS}$ pin (logic 1) once the last bit of the data has been transmitted.

To use the auto RS-485 $\overline{RTS}$ mode the software would have to disable the hardware flow control function.

9.2 RS-485 RTS output inversion

EFCR bit 5 reverses the polarity of the $\overline{RTS}$ pin if the UART is in auto RS-485 $\overline{RTS}$ mode. When the transmitter has data to be sent it de-asserts the $\overline{RTS}$ pin (logic 1), and when the last bit of the data has been sent out the transmitter asserts the $\overline{RTS}$ pin (logic 0).

9.3 Auto RS-485

EFCR bit 0 is used to enable the RS-485 mode (multidrop or 9-bit mode). In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' stations. The slave stations examine the received data and interrupt the controller if the received character is an address character (parity bit = 1).

To use the auto RS-485 RTS mode the software would have to disable the hardware flow control function.

9.3.1 Normal multidrop mode

The 9-bit mode in EFCR (bit 0) is enabled, but not Special Character Detect (EFR bit 5). The receiver is set to Force Parity 0 (LCR[5:3] = 111) in order to detect address bytes.

With the receiver initially disabled, it ignores all the data bytes (parity bit = 0) until an address byte is received (parity bit = 1). This address byte will cause the UART to set the parity error. The UART will generate a line status interrupt (IER bit 2 must be set to '1' at this time), and at the same time puts this address byte in the RX FIFO. After the controller examines the byte it must make a decision whether or not to enable the receiver; it should enable the receiver if the address byte addresses its ID address, and must not enable the receiver if the address byte does not address its ID address.

If the controller enables the receiver, the receiver will receive the subsequent data until being disabled by the controller after the controller has received a complete message from the 'master' station. If the controller does not disable the receiver after receiving a message from the 'master' station, the receiver will generate a parity error upon receiving another address byte. The controller then determines if the address byte addresses its ID address, if it is not, the controller then can disable the receiver. If the address byte addresses the 'slave' ID address, the controller take no further action; the receiver will receive the subsequent data.

9.3.2 Auto address detection

If Special Character Detect is enabled (EFR[5] is set and XOFF2 contains the address byte) the receiver will try to detect an address byte that matches the programmed character in XOFF2. If the received byte is a data byte or an address byte that does not match the programmed character in XOFF2, the receiver will discard these data. Upon receiving an address byte that matches the XOFF2 character, the receiver will be automatically enabled if not already enabled, and the address character is pushed into the RX FIFO along with the parity bit (in place of the parity error bit). The receiver also generates a line status interrupt (IER bit 2 must be set to 1 at this time). The receiver will then receive the subsequent data from the 'master' station until being disabled by the controller after having received a message from the 'master' station.

If another address byte is received and this address byte does not match XOFF2 character, the receiver will be automatically disabled and the address byte is ignored. If the address byte matches XOFF2 character, the receiver will put this byte in the RX FIFO along with the parity bit in the parity error bit (LSR[2]).

10. I²C-bus Interface

The I²C-bus interface is compliant with the Standard-mode and Fast-mode I²C-bus specifications. The I²C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the Standard-mode, the serial clock and serial data can go up to 100 kbps and in the Fast-mode, the serial clock and serial data can go up to 400 kbps. The first byte sent by an I²C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The UART responds to each write with an acknowledge (SDA driven LOW by UART for one clock cycle when SCL is HIGH). If the TX FIFO is full, the UART will respond with a negative acknowledge (SDA driven HIGH by UART for one clock cycle when SCL is HIGH) when the CPU tries to write to the TX FIFO. The last byte sent by an I²C-bus master is a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See Figures 8 - 10 below. For complete details, see the I²C-bus specifications.

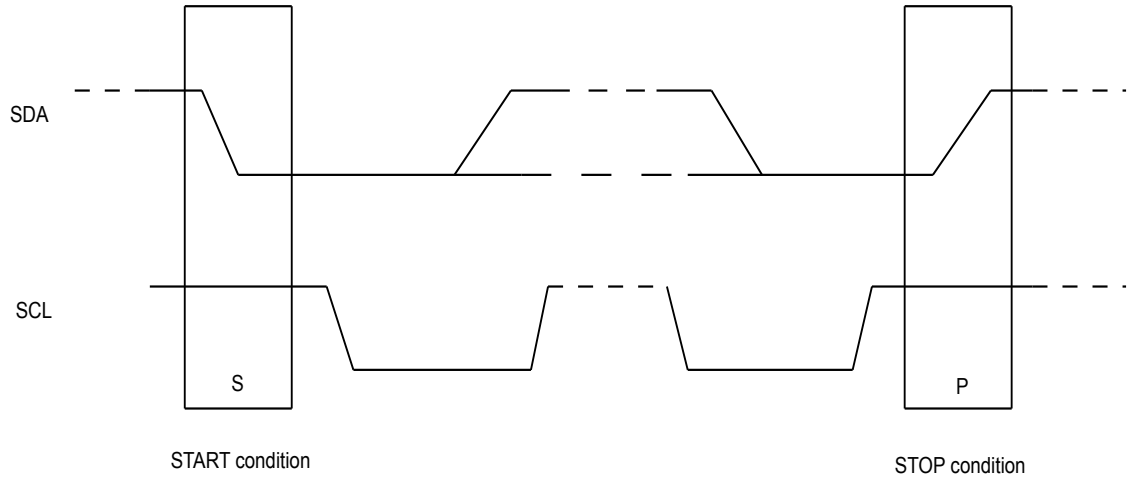
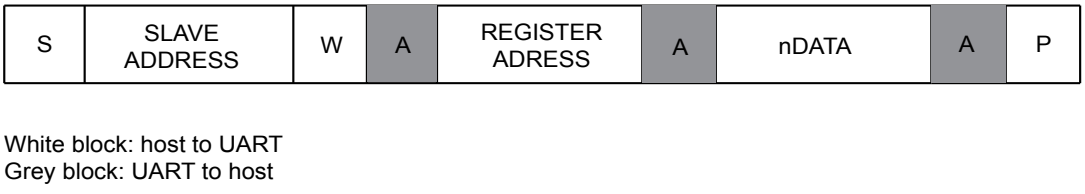
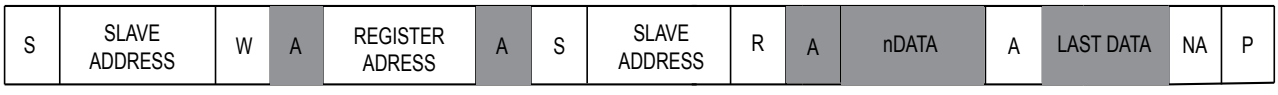


Figure 9. I²C Start and Stop Conditions



White block: host to UART
Grey block: UART to host

Figure 10. Master writes to slave (UART)



White block: host to UART
Grey block: UART to host

Figure 11. Master reads from slave (UART)

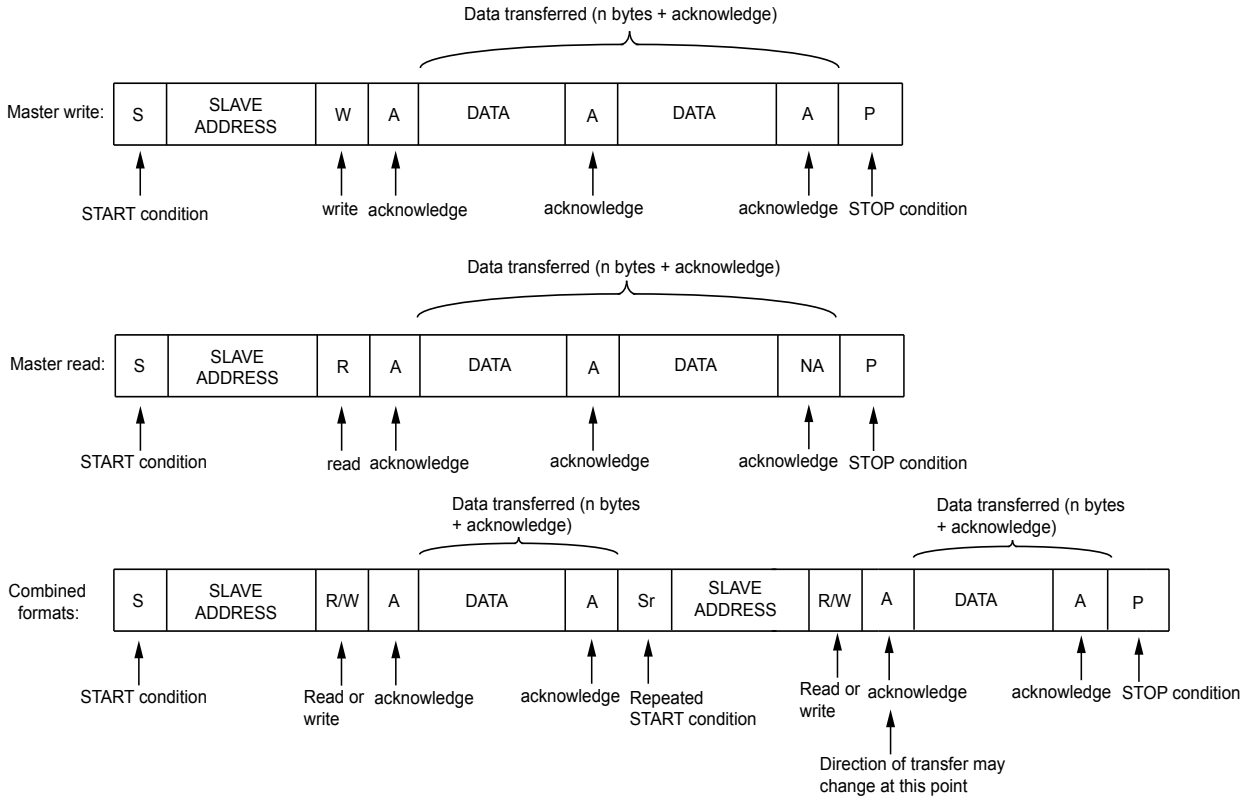


Figure 12. I^2C data formats

10.1 I²C-bus Addressing

There could be many devices on the I²C-bus. To distinguish itself from the other devices on the I²C-bus, there are eight possible slave addresses that can be selected for the UART using the A1 and A0 address lines. Table 9 below shows the different addresses that can be selected. Note that there are two different ways to select each I2C address.

Table 9: I²C Address Map

A1	A0	I²C ADDRESS
V_{DD}	V_{DD}	0x90 (1001 000X)
V_{DD}	V_{SS}	0x92 (1001 001X)
V_{DD}	SCL	0x94 (1001 010X)
V_{DD}	SDA	0x96 (1001 011X)
V_{SS}	V_{DD}	0x98 (1001 100X)
V_{SS}	V_{SS}	0x9A (1001 101X)
V_{SS}	SCL	0x9C (1001 110X)
V_{SS}	SDA	0x9E (1001 111X)
SCL	V_{DD}	0xA0 (1010 000X)
SCL	V_{SS}	0xA2 (1010 001X)
SCL	SCL	0xA4 (1010 010X)
SCL	SDA	0xA6 (1010 011X)
SDA	V_{DD}	0xA8 (1010 100X)
SDA	V_{SS}	0xAA (1010 101X)
SDA	SCL	0xAC (1010 110X)
SDA	SDA	0xAE (1010 111X)

An I²C sub-address is sent by the I²C master following the slave address. The sub-address contains the UART register address being accessed. A read or write transaction is determined by bit-0 of the slave address (HIGH = Read, LOW = Write). Table 10 below lists the functions of the bits in the I²C sub-address.

Table 10: I²C Sub-Address (Register Address)

Bit	Function
7	Reserved
6:3	UART Internal Register Address A3:A0
2:1	UART Channel Select '00' = UART Channel A '01' = UART Channel B other values are reserved
0	Reserved

After the last read or write transaction, the I²C-bus master will set the SCL signal back to its idle state (HIGH).

11. SPI Bus Interface

The SPI interface consists of four lines: serial clock (SCL), chip select (CS#), slave output (SO) and slave input (SI). The serial clock, slave output and slave input can be as fast as 33 MHz at 3.3V. To access the device in the SPI mode, the CS# signal for the UART is asserted by the SPI master, then the SPI master starts toggling the SCL signal with the appropriate transaction information. The first bit sent by the SPI master includes whether it is a read or write transaction and the UART register being accessed. See Table 11 below.

Table 11: SPI First Byte Format

Bit	Function
7	Read/Write# Logic 1 = Read Logic 0 = Write
6:3	UART Internal Register Address A3:A0
2:1	UART Channel Select '00' = UART Channel A '01' = UART Channel B Other values are reserved
0	Reserved

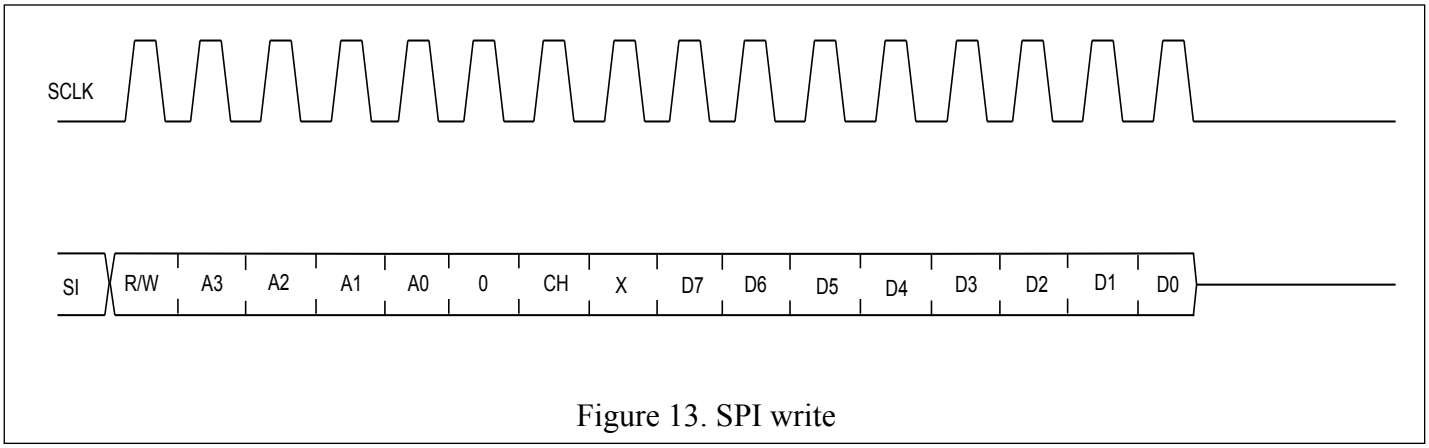


Figure 13. SPI write

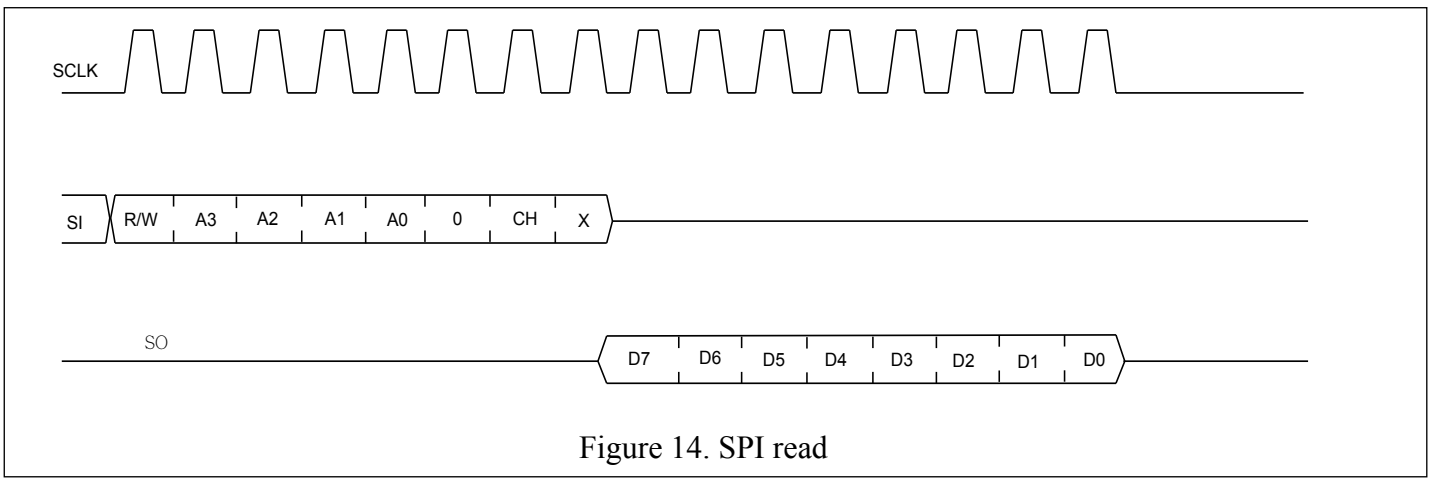


Figure 14. SPI read

The 64 byte TX FIFO can be loaded with data or 64 byte RX FIFO data can be unloaded in one SPI write or read sequence.

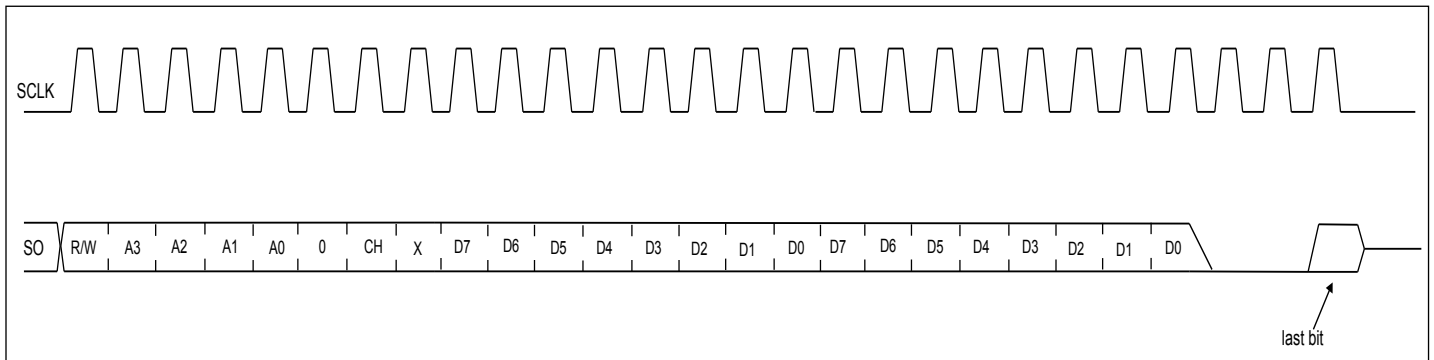


Figure 15. SPI FIFO write

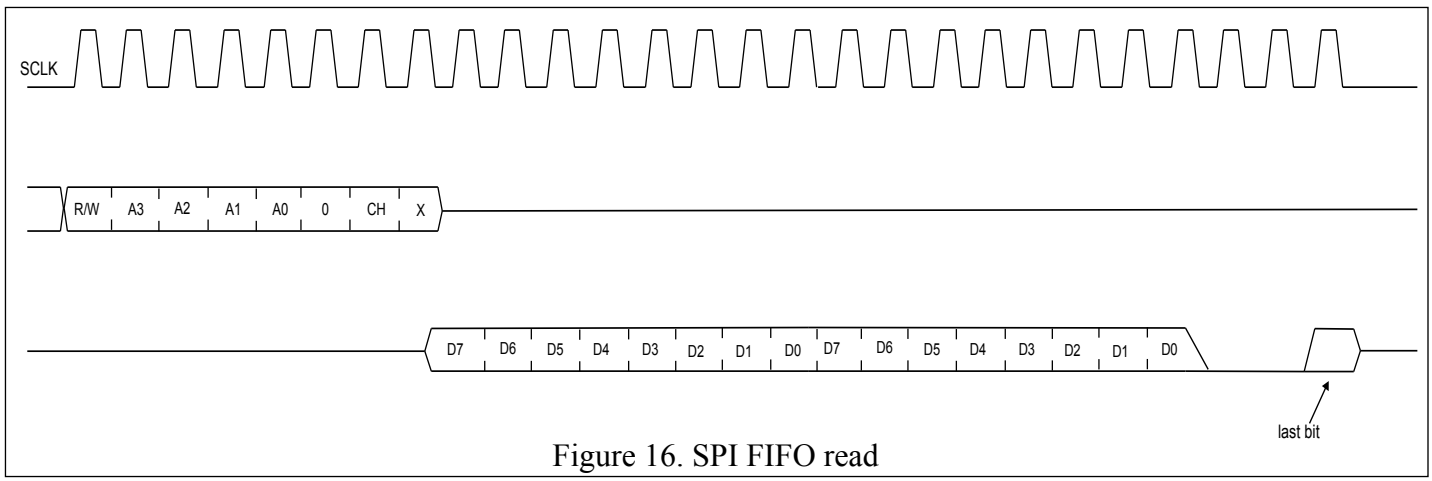


Figure 16. SPI FIFO read

After the last read or write transaction, the SPI master will set the SCL signal back to its idle state (LOW).

12 Infrared Mode

The UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0 and 1.1. The IrDA 1.0 standard that stipulates the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream with a data rate up to 115.2 Kbps. For the IrDA 1.1 standard, the infrared encoder sends out a 1/4 of a bit time wide HIGH-pulse for each "0" bit in the transmit data stream with a data rate up to 1.152 Mbps. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 17 below.

The infrared encoder and decoder are enabled by setting MCR register bit-6 to a ‘1’. With this bit enabled, the infrared encoder and decoder is compatible to the IrDA 1.0 standard. For the infrared encoder and decoder to be compatible to the IrDA 1.1 standard, EFCR bit-7 will also need to be set to a ’1’. When the infrared feature is enabled, the transmit data output, TX, idles LOW. Likewise, the RX input also idles LOW, see Figure 17.

The wireless infrared decoder receives the input pulse from the infrared sensing diode on the RX pin. Each time it senses a light pulse, it returns a logic 1 to the data bit stream.

The UART can be in the infrared mode upon power-up if the ENIR# pin is LOW. After power-up, the infrared mode can be controlled via MCR bit-6.

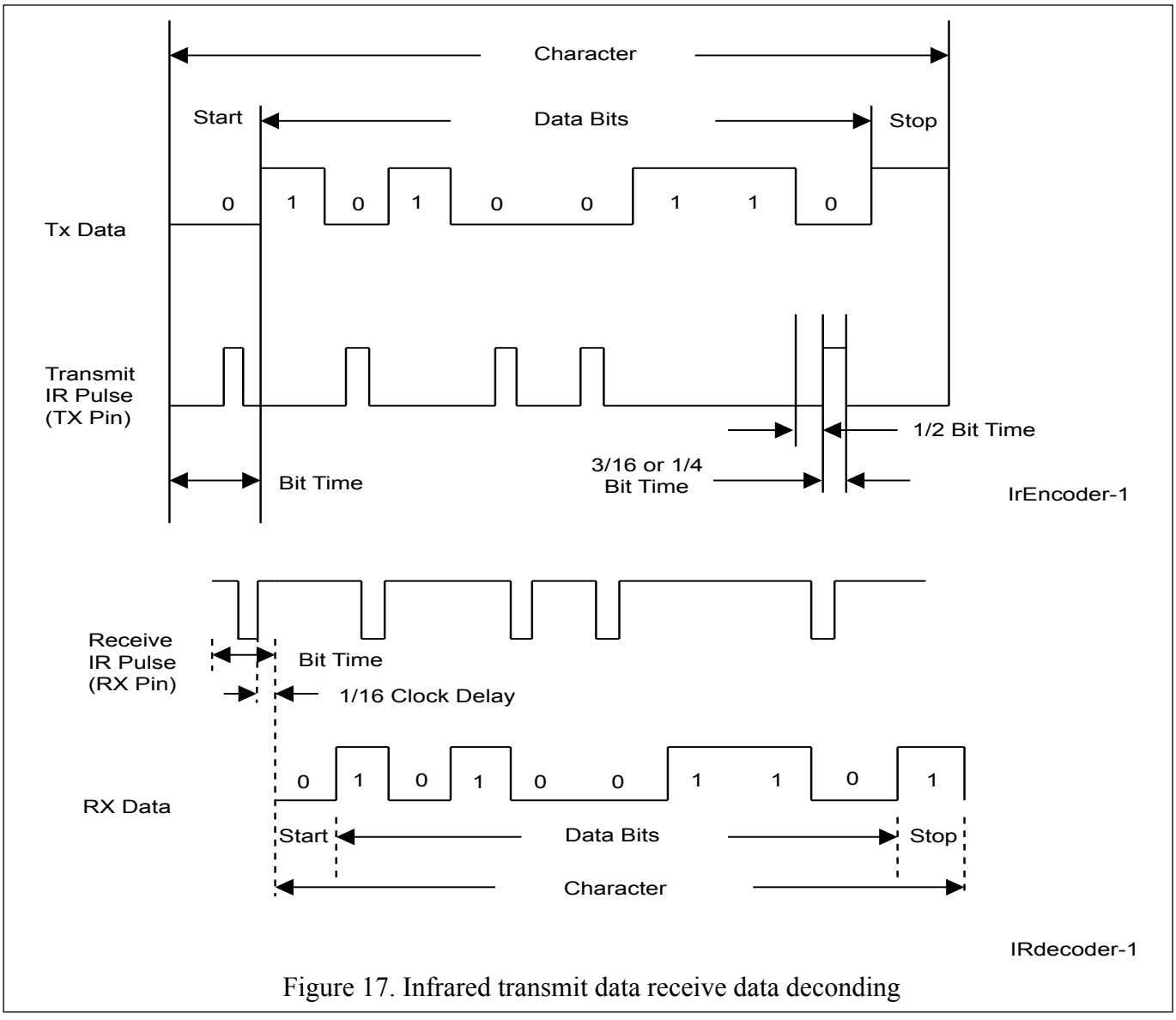


Figure 17. Infrared transmit data receive data deconding

Configuration Registers

Offset 00H: Receiver Holding Register (RHR). Accessable when LCR[7]=0. Default=00		
Bit	**Type**	**Description**
[7:0]	RO	Rx Holding - When data are read from the RHR,they are removed from the top of the receiver's FIFO. Data read from the RHR when FIFO is empty are invalid. The Line Status Register(LSR) indicates the full or empty status of the FIFOs.
Offset 00H: Transmitter Holding Register (THR). Accessable when LCR[7]=0. Default=00		
Bit	**Type**	**Description**
[7:0]	WO	Tx Holding - When data are written to the THR,they are written to the bottom of the transmitter's FIFO. Data written to the THR when FIFO is full are lost. The Line Status Register(LSR) indicates the full or empty status of the FIFOs.
Offset 00H: Divisor Latch LSB(DLL). Accessable when LCR[7]=1 and LCR!=0xBF. Default=01		
Bit	**Type**	**Description**
[7:0]	WO	LSB bits of divisor for baud rate generator. Note: It is reset only when Power-On-Reset.
Offset 01H: Interrupt Enable Register (IER). Accessable when LCR[7]=0. Default=00		
Bit	**Type**	**Description**
7	RW	CTS interrupt - "1": Enable CTS/DSR interrupt
6	RW	RTS interrupt - "1": Enable RTS/DTR interrupt
5	RW	Xoff/Special charatcter interrupt - "1": Enable the Software Flow Control interrupt
4	RW	Sleep mode - "1" : Enable sleep mode (It requires EFR[4] = 1). The Uart may enter sleep mode when all conditions met: - no interrupts pending - modem inputs are not toggled - RX input pin is idling HIGH - TX/RX FIFO are empty It will exit from sleep mode when any below condition met: - modem inputs are toggling - RX input pin changed to LOW -a data byte is loaded to the TX FIFO In sleep mode, Crystal is stopped and no Uart clock
3	RW	Modem Status interrupt - "1": Enable Modem Status interrupt
2	RW	Receiver Line Status interrupt - "1": Enable Receiver Line Status interrupt
1	RW	Tx Ready interrupt - "1": Enable THR Ready interrupt 1 = Interrupt is issued whenever the THR becomes empty in non-FIFO mode or when spaces in the FIFO is above the trigger level in the FIFO mode.
0	RW	Rx Data Ready interrupt - "1": enable Data Ready interrupt

Note: IER[7:4] can only be modified if EFR[4]=1.

Configuration Registers cont.

Offset 01H: Divisor Latch MSB(DLH). Accessable when LCR[7]=1 and LCR!=0xBF. Default=00

Bit	Type	Description
[7:0]	RW	MSB bits of divisor for baud rate generator. Note: It is reset only when Power-On-Reset.

Offset 02H: Interrupt Identification Register (IIR). Accessable when LCR[7]=0. Default=01

Bit	Type	Description
[7:6]	RO	Mirror the content of FCR[0]
[5:1]	RO	5-bit encoded interrupt.
0	RO	Interrupt status. "1": No interrupt is pending. "0": An interrupt is pending.

Priority Level	IIR[5]	IIR[4]	IIR[3]	IIR[2]	IIR[1]	IIR[0]	Source of Interrupt
1	0	0	0	1	1	0	Receive Line Status Error
2	0	0	1	1	0	0	Receiver timeout
2	0	0	0	1	0	0	RHR interrupt
3	0	0	0	0	1	0	THR interrupt
4	0	0	0	0	0	0	Modem interrupt
5	1	1	0	0	0	0	Input pin change of state
6	0	1	0	0	0	0	Rx Xoff signal/special character
7	1	0	0	0	0	0	CTS,RTS change from active to inactiove

Note: IIR[4] is cleared by Xon detection if the interrupt is caused by Xoff detection, or cleared by a read of the IIR if it is caused by special char detection.

Offset 02H: FIFO Control Register (FCR). Accessable when LCR[7]=0. Default=00

Bit	Type	Description
[7:6]	WO	RX trigger. Sets the trigger level for the RX FIFO 00 = 8 characters 01 = 16 characters 10 = 56 characters 11 = 60 characters
[5:4]	WO	TX trigger. Sets the trigger level for the TX FIFO 00 = 8 spaces 01 = 16 spaces 10 = 32 spaces 11 = 56 spaces
3	RO	Reserved
2	WOS	Reset TX FIFO. 0 = No FIFO transmit reset 1 = Clears the contents of Tx FIFO and resets the FIFO level logic. TSR is not cleared. This bit will return to logic 0 after clearing the FIFO
1	WOS	Reset RX FIFO. 0 = No FIFO receive reset 1 = Clears the contents of Rx FIFO and resets the FIFO level logic. RSR is not cleared. This bit will return to logic 0 after clearing the FIFO

Configuration Registers cont.

0	WO	FIFO enable 0 = Disable the transmit and receive FIFO, and TX/RX can only hold one character at a time. Other FCR bits are not programmable, and the trigger level is set to one character. 1 = enable the transmit and receive FIFO. and TX/RX FIFO can hold 64 characters. Note: FCR[5:4] can only be modified and enabled if EFR[4]=1.

Offset 02H: Enhanced Feature Register (EFR). Accessable when LCR=0xBF and SFR[2]=0. Default=00

Bit	Type	Description
7	RW	Auto CTS Flow Control Enable 0 = Automatic CTS flow control is disabled. 1 = Automatic CTS flow control is enabled.
6	RW	Auto RTS Flow Control Enable 0 = Automatic RTS flow control is disabled. 1 = Automatic RTS flow control is enabled.
5	RW	Special character detect 0 = Special character detect is disabled. 1 = Special character detect is enabled. If received data matchs Xoff2 data, the received data is transferred to RX FIFO and IIR[4] is set to high to indicate a special character detection. However,if flow control is set for comparing Xoff2, then flow control works normally and Xoff2 will not go to the FIFO and will generate an Xoff interrupt and a special character interrupt.
4	RW	Enhanced Function Bits Enable This bit enables IER[7:4],IIR[5:4],FCR[5:4],MCR[7:5],TCR and TLP to be modified, and enables the sleep mode.
[3:0]	RW	Software Flow Control Select: 00xx = No TX flow control 10xx = Transmit Xon1,Xoff1 01xx = Transmit Xon2,Xoff2 11xx = Transmit Xon1 and Xon2,Xoff1 and Xoff2 xx00 = No RX flow control xx10 = Receiver compares Xon1,Xoff1 xx01 = Receiver compares Xon2,Xoff2 1011 = Transmit Xon1,Xoff1; Receiver compares Xon1 or Xon2,Xoff1 or Xoff2 0111 = Transmit Xon2,Xoff2; Receiver compares Xon1 or Xon2,Xoff1 or Xoff2 1111 = Transmit Xon1 and Xon2,Xoff1 and Xoff2; Receiver compares Xon1 and Xon2,Xoff1 and Xoff2 0011 = No transmit flow control; Receiver compares Xon1 and Xon2,Xoff1 and Xoff2

Offset 03H: Line Control Register (LCR). Default=1D

Bit	Type	Description
7	RW	Divisor latch enabled when set
6	RW	Break control bit. 0 = no TX break condition 1 = forces TX to logic 0 to alert a line break condition

Configuration Registers cont.

5	RW	Set forced parity format(if LCR[3]=1) 0 = parity is not forced. 1 = parity bit is forced to high if LCR[4]=0,or low if LCR[4]=1.
4	RW	Parity type select. 0 = odd parity is generated(if LCR[3]=1) 1 = even parity is generated(if LCR[3]=1)
3	RW	Parity enable when set
2	RW	Number of Stop bits 0 = 1 stop bit. 1 = 1.5 stop bits for word length=5, or 2 stop bits for word length=6,7,8
1:0	RW	Word length bits: 00 = 5 bits. 01 = 6 bits 10 = 7 bits. 11 = 8 bits
Offset 04H: Modem Control Register (MCR). Accessable when LCR[7]=0. Default=00		
Bit	Type	Description
7	RW	Clock pre-scaler select. 0 = divide-by-1 clock input 1 = divide-by-4 clock input
6	RW	IrDA mode enable when set.
5	RW	When set, Xon Any function is enabled and receiving any character will resume transmit operation. the RX character will be loaded into the RX FIFO. unless the RX character is an Xon/Xoff character and receiver software flow control is enabled.
4	RW	When set, internal loopback mode is enabled and TX output is looped back to the RX input internally, and MCR[1:0] signals are looped back into MSR[4:5]
3	RW	OP2. It is not available as an output pin but can be controlled in Internal Loopback Mode(MCR[4]=1) and is outputed to DCD internally.
2	RW	OP1/TCR and TLR enable. In Internal Loopback Mode(MCR[4]=1), it is outputed to RI internally. otherwise it is used to select between the MSR and TCR registers at offset 0x6 and the SPR and TLR registers at offset 0x7.
1	RW	RTS pin control. 0 = force RTS pin High 1 = force RTS pin Low When IN internal loopback mode, it controls MSR[4]. If Auto-RTS is enabled, the RTS pin is controlled by hardware flow control .
0	RW	DTR pin control if GPIO5 or GPIO1 is selected as DTR modem pin through IOControl register bit 1 or bit 2: 0 = force DTR pin High 1 = force DTR pin Low When internal loopback mode, it controls MSR[5].

Note: MCR[7:5],MCR[3:2] can only be modified if EFR[4]=1.

Configuration Registers cont.

Offset 04H: XON1 character Register (XON1). Accessable when LCR=0xBF and SFR[2]=0. Default=00		
Bit	**Type**	**Description**
[7:0]	RW	XON1 character Note: It is reset only when Power-On-Reset.
Offset 05H: Line Status Register (LSR). Accessable when LCR[7]=0. Default=60		
Bit	Type	Description
7	RO	Receiver FIFO Data Error Flag. 0 = No FIFO Error 1 = a flag for the sum of all error bits (parity error, framing error, or break) in the RX FIFO. this bit clears when there is no more error in any of the bytes in the RX FIFO.
6	RO	THR and TSR Empty Flag This bit is set whenever the transmitter goes idle, it clears whenever either the THR or TSR contains a data character.
5	RO	THR Empty Flag This bit is set when the last data byte is transferred from THR to TSR.
4	RO	Receiver Break Error Flag 0 = No Break Error 1 = break condition occurred in data to be read from RX FIFO(RX was LOW for at least one character frame time).
3	RO	Receiver Data Framing Error Flag 0 = No Data Framing Error 1 = framing error occurred in data to be read from RX FIFO (The receive character did not have a valid stop bits).
2	RO	Receiver Data Parity Error Flag 0 = No Data Parity Error 1 = parity error in data to be read from RX FIFO
1	RO	Receiver Overrun Error 0 = No verrun Error 1 = additional data received while the RX FIFO is full. This data should not be transferred into FIFO.
0	RO	Receiver Data Ready Indicator 0 = No data in received in RX FIFO 1 = Data has been received and saved in the RX FIFO
Offset 05H: XON2 character Register (XON2). Accessable when LCR=0xBF and SFR[2]=0. Default=00		
Bit	**Type**	**Description**
[7:0]	RW	XON2 character Note: It is reset only when Power-On-Reset.
Offset 06H: Modem Status Register (MSR). Accessable when LCR[7]=0 and MCR[2]=0 and SFR[2]=0. Default=00		
Bit	Type	Description
7	RO	CD input satus Normally this bit is the complement of the CD# input. In the loopback mode this bit is equivalent to MCR[3].

Configuration Registers cont.

6	RO	RI input satus Normally this bit is the complement of the RI# input. In the loopback mode this bit is equivalent to MCR[2].
5	RO	DSR input satus Normally this bit is the complement of the DSR# input. In the loopback mode this bit is equivalent to MCR[0].
4	RO	CTS input satus Normally this bit is the complement of the CTS# input. In the loopback mode this bit is equivalent to MCR[1].
3	RO	Delta CD# input flag 0 = No change on CD# input 1 = The CD# input has changed state. A modem status interrupt will be generated if MSR interrupt is enabled.
2	RO	Delta RI# input flag 0 = No change on RI# input 1 = The RI# input has changed from a LOW to HIGH. A modem status interrupt will be generated if MSR interrupt is enabled.
1	RO	Delta DSR# input flag 0 = No change on DSR# input 1 = The DSR# input has changed state. A modem status interrupt will be generated if MSR interrupt is enabled.
0	RO	Delta CTS# input flag 0 = No change on CTS# input 1 = The CTS# input has changed state. A modem status interrupt will be generated if MSR interrupt is enabled.

Offset 06H: Transmission Control Register (TCR). Accessable when EFR[4]=1 and MCR[2]=1 and SFR[2]=0. Default=00

Bit	Type	Description
[7:4]	RW	RX FIFO Resume level. When the RX FIFO is less than or equal to the value (decimal value of TCR[7:4] multiplied by 4), the RTS# output will be re-asserted if Auto RTS flow is used or XON character will be transmitted if Auto XON/XOFF flow control is used. It is recommended that this value is less than the RX Trigger Level.
[3:0]	RW	RX FIFO Halt level. When the RX FIFO is greater than or equal to the value (decimal value of TCR[3:0] multiplied by 4), the RTS# output will be de-asserted if Auto RTS flow is used or XOFF character will be transmitted if Auto XON/XOFF flow control is used. It is recommended that this value is greater than the RX Trigger Level.

Offset 06H: XOFF1 character Register (XOFF1). Accessable when LCR=0xBF and SFR[2]=0. Default=00

Bit	Type	Description
[7:0]	RW	XOFF1 character Note: It is reset only when Power-On-Reset.

Configuration Registers cont.

Offset 07H: Scratch Pad Register (SPR). Accessable when LCR[7]=0 and MCR[2]=0. Default=FF		
Bit	**Type**	**Description**
[7:0]	RW	This is 8-bit general purpose register for the user to store temporary data. the content is preserved during sleep mode. Note: It is reset only when Power-On-Reset.
Offset 07H: Trigger Level Register (TLR). Accessable when EFR[4]=1 and MCR[2]=1. Default=00		
Bit	**Type**	**Description**
[7:4]	RW	RX FIFO Trigger level. When the number of characters received in RX FIFO is greater than or equal to the value (decimal value of TLR[7:4] multiplied by 4), a Receive Data Ready interrupt is generated. If TLR[7:4]=0x0, then the RX FIFO Trigger Level is the value selected by FCR[7:6]
[3:0]	RW	TX FIFO Trigger level. When the number of available space in TX FIFO is greater than or equal to the value (decimal value of TLR[3:0] multiplied by 4), a Transmit Ready interrupt is generated. If TLR[3:0]=0x0, then the TX FIFO Trigger Level is the value selected by FCR[5:4]
Offset 07H: XOFF2 character Register (XOFF2). Accessable when LCR=0xBF and SFREN!=0x5A. Default=00		
Bit	**Type**	**Description**
[7:0]	RW	XOFF2 character Note: It is reset only when Power-On-Reset.
Offset 08H: Transmit FIFO Level Register (TXLVL). Accessable when SFR[2]=0. Default=40		
Bit	**Type**	**Description**
[7:0]	RO	This register reports the number of spaces available in the TX FIFO.
Offset 09H: Receiver FIFO Level Register (RXLVL). Accessable when SFR[2]=0. Default=00		
Bit	**Type**	**Description**
[7:0]	RO	This register reports the number of character available in the RX FIFO.
Offset 0AH: GPIO Direction Register (IODir). Default=00		
Bit	**Type**	**Description**
[7:0]	RW	This register program the direction of the GPIO pins. 0 = set GPIO pin as input 1 = set GPIO pin as output
Offset 0BH: GPIO State Register (IOState). Default=FF		
Bit	**Type**	**Description**
[7:0]	RW	This register reports the state of all GPIO pins during read and writes to any GPIO that is an output 0 = set output pin LOW 1 = set output pin HIGH

Configuration Registers cont.

Offset 0CH: GPIO Interrupt Enable Register (IOIntEna). Default=00		
Bit	**Type**	**Description**
[7:0]	RW	This register enable the interrupt for GPIO pins. If GPIO[7:4] or GPIO[3:0] are programmed as modem pins, IOIntEna will have no effect on GPIO[7:4] or GPIO[3:0]. 0 = disabled 1 = enabled
Offset 0EH: GPIO Control Register (IOControl). Default=00		
Bit	**Type**	**Description**
[7:4]	RO	Reserved
3	RW	Uart Software Reset. Writing a logic 1 to this bit will reset the device. This bit is automatically be reset after device is reset.
2	RW	GPIO[3:0] or Modem IO Select(CH B) 0 = GPIO[3:0] behave as GPIO pins 1 = GPIO[3:0] behave as RIB#,CDB#,DTRB#,DSRB#
1	RW	GPIO[7:4] or Modem IO Select(CH A) 0 = GPIO[7:4] behave as GPIO pins 1 = GPIO[7:4] behave as RIA#,CDA#,DTRA#,DSRA#
0	RW	This bit enable GPIO inputs latching 0 = GPIO input values are not latched. If the input goes back to its initial logic state before the input register is read, then the interrupt is cleared. 1 = GPIO input values are latched. If the input goes back to its initial logic state before the input register is read, then the interrupt is not cleared and the corresponding bit of IOState register keeps the logic value that generated the interrupt.
Offset 0FH: Extra Features Control Register (EFCR). Accessable when SFR[2]=0, Default=00		
Bit	Type	Description
7	RW	IrDA mode. 0 = IrDA version 1.0, 3/16 pulse ratio,data rate up to 115.2 Kbps 1 = IrDA version 1.1, 1/4 pulse ratio,data rate up to 1.152 Mbps
6	RO	Reserved
5	RW	Auto RS-485 Polarity Inversion This bit changes the polarity of the Auto RS-485 Direction Control output(RTS#). it will only affect the behavior of RTS# if EFCR[4]=1 0 = RTS# output is LOW when transmitting and HIGH when receiving 1 = RTS# output is HIGH when transmitting and LOW when receiving
4	RW	Auto RS-485 direction control This bit enables the transmitter to control RTS# pin 0 = transmitter does not control RTS# pin 1 = transmitter controls RTS# pin
3	RO	Reserved

Notes: GPIO registers(0AH-0EH) are channel independent. For example, setting software reset will reset all channels.

Configuration Registers cont.

2	RW	Transmitter Disable 0 = transmitter is enabled 1 = transmitter is disabled,Uart does not send serial data out on the TX output pin after current data in the TSR is send.
1	RW	Receiver Disable 0 = Receiver is enabled 1 = Receiver is disabled
0	RW	9-bit or Multidrop Mode Enable 0 = Normal 8-bit mode 1 = Enable 9-bit mode (addition bit defines data or address byte)

Offset 0DH: Special Features Enable Control Register (SFREN). Accessable when LCR==8'hBF. Default=00

Bit	Type	Description
[7:0]	RW	Set 8'h5A to enable SFR register access

Offset 02H: Advance Status Register (ASR). Accessable when LCR=0xBF and SFR[2]=1. Default=00

Bit	Type	Description
[7:6]	RO	Reserved
[5:4]	RO	Xon/Xoff flow state 00 = idle state 01 = Xoff received 10 = TX off 11 = Xon received
[3:2]	RO	Reserved
1	RO	Remote TX disabled 1 = TX has sent XOFF message or RTS message
0	RO	Transmitter terminate condition 1 = This TX has disabled by remote termiate.

Offset 04H: Clock Prescale Register (CPR). Accessable when LCR=0xBF and SFR[2]=1. Default=10

Bit	Type	Description
[7:4]	RW	CPRM - M number in calculating the prescaler,which is used to generate Baud Rate,it is recommended to be set to "01h" or "02h"
[3:0]	RW	CPRN - N number in calculating the prescaler,which is used to generate Baud Rate.

Offset 05H: Received FIFO Data counter Register (RFD). Accessable when LCR=0xBF and SFR[2]=1, SFR[6]=0. Default=00

Bit	Type	Description
[7:0]	RO	Indicated the amount of data in RX FIFO

Offset 05H: Received Line Error Status counter Register (RLS). Accessable when LCR=0xBF and SFR[2]=1, SFR[6]=1. Default=00

Bit	Type	Description
[7:0]	RO	Indicated the amount of data byte with error in RX FIFO

Configuration Registers cont.

Offset 06H: Transmitter FIFO Data counter Register (TFD). Accessable when LCR=0xBF and SFR[2]=1. Default=00		
Bit	**Type**	**Description**
[7:0]	RO	Indicated the amount of data in TX FIFO
Offset 07H: Special Function Register(SFR). Accessable when LCR=0xBF and SFREN==0x5A. Default=00		
Bit	Type	Description
7	RW	If set, Crystal feedback resistor disable
6	RW	RFD/LSR counter select 0 = Receive FIFO Data Counter is selected 1 = Line Status Error Counter is selected
5	RW	Reserved
4	RW	Registers burst R/W enable if set
3	RW	enable the loopback from RX to TX internally
2	RW	Special Register Access Enable when set, registers(CPR,ISCR,TIDLE,TRCTL) are accessable.
1	RW	Auto DSR and DTR Flow Control enable 0 = Auto DSR and DTR Flow Control is disabled 1 = Auto DSR and DTR Flow Control is enabled
0	RW	If set, forces transmitter to always to transmit data
Offset 08H: Transmit Idle Time Count Register (TIDLE). Accessable when LCR=0xBF and SFR[2]=1. Default=00		
Bit	**Type**	**Description**
[7:0]	RW	Transmit Idle Time control.
Offset 09H: TX/RX Control Register (SCR/TRCTL). Accessable when LCR=0xBF and SFR[2]=1. Default=06		
Bit	**Type**	**Description**
[7:4]	RW	SCR - Sample Clock value used in the Baud Rate Generator. Baud Rate = XIN / (DL * 2 ** (M+2*MCR[7]-1) * (16-SCR+N))
3	RW	Transmit In-band Xon enable
2	RW	TX Empty Interrupt enable
1	RW	RX Timeout enable
0	RW	TX Idle insertion enable

Note: When IrDA mode is enabled, the setting in register SCR(bit 7-3 of 09H) and N(bit 3-0 of CPR should meet: SCR=N or (16-SCR+N) > 1.

Configuration Registers cont.

Offset 0FH: Interrupt Status and Clear Register (ISCR). Accessable when LCR=0xBF and SFR[2]=1. Default=00		
Bit	Type	Description
7	RW	1 = CTS/RTS change Interrupt is active
6	RW	1 = Rx Xoff signal/special character Interrupt is active
5	RW	1 = Modem Interrupt is active
4	RW	1 = THR Interrupt is active
3	RW	1 = Receiver Timeout Interrupt is active
2	RW	1 = RHR Interrupt is active
1	RW	1 = Receive Line Error Interrupt is active
0	RW	CLSTATUS, when set, the Interrupt Status registers are cleared. This bit returns to zero after write.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Power Supply Range	3.8V
Voltage at IO Pins	GND-0.3V to 5.5V
Storage Temperature	–65°C to +150°C
Package Dissipation	500 mW
Junction Temperature (Tj)	125°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

(TA = -40° to + 85°C, V_{DD} = 1.62V - 3.63V)

Symbol	Parameter	V_{DD} = 1.8V ± 10%		V_{DD} = 2.5V ± 10%		V_{DD} = 3.3V ± 10%		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{ILCK}	Clock input low level	-0.3	0.3	-0.3	0.6	-0.3	0.6	V	
V_{IHCK}	Clock input high level	1.4	VDD	1.8	VDD	2.4	VDD	V	
V_{IL}	Input low voltage	-0.3	0.2	-0.3	0.5	-0.3	0.8	V	
V_{IH}	Input high voltage	1.4	5.5	1.8	5.5	2.0	5.5	V	
V_{OL}	Output low voltage		0.4		0.4		0.4	V V V	I_{OL} = 4 mA I_{OL} = 2 mA I_{OL} = 1.5 mA
V_{OH}	Output high voltage	1.4		1.8		2.0		V V V	I_{OH} = -1 mA I_{OH} = -400 uA I_{OH} = -200 uA
I_{IL}	Input low leakage current		10		10		10	uA	
I_{IH}	Input high leakage current		10		10		10	uA	
C_{IN}	Input pin capacitance		5		5		5	pF	
I_{CC}	Power supply current		3		3		6	mA	XTAL1 = 14.75 MHz
I_{SLEEP}	Sleep current		15		20		30	uA	

Note: 5.5V steady voltage tolerance on inputs and outputs is valid only when the supply voltage is present.

AC Electrical Characteristics - UART Clock

(TA = -40° to + 85°C, V_{DD} = 1.62V - 3.63V)

Symbol	Parameter	VDD = 1.8V ± 5%		V_{DD} = 1.8V ± 10%		V_{DD} = 2.5V ± 10%		V_{DD} = 3.3V ± 10%		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
XTAL1	UART Crystal Oscillator		24		24		24		24	MHz
ECLK	UART External Clock		32		24		250		64	MHz
T_{ECLK}	External Clock Time Period	1/ECLK		1/ECLK		1/ECLK		1/ECLK		ns

AC Electrical Characteristic - I2C-Bus Timing Specifications

(Unless otherwise noted: TA = -40° to +85°C, V_{DD} = 1.62 - 3.63V)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	Operating frequency	0	100	0	400	kHz
T_{BUF}	Bus free time between STOP and START	4.7		1.3		µs
$T_{HD;STA}$	START condition hold time	4.0		0.6		µs
$T_{SU;STA}$	START condition setup time	4.7		0.6		µs
$T_{HD;DAT}$	Data hold time	0		0		ns
$T_{VD;ACK}$	Data valid acknowledge		0.6		0.6	µs
$T_{VD;DAT}$	SCL LOW to data out valid		0.6		0.6	µs
$T_{SU;DAT}$	Data setup time	250		150		ns
T_{LOW}	Clock LOW period	4.7		1.3		µs
T_{HIGH}	Clock HIGH period	4.0		0.6		µs
T_F	Clock/data fall time		300		300	ns
T_R	Clock/data rise time		1000		300	ns
T_{SP}	Pulse width of spikes tolerance		100		100	ns
T_{D1}	I^2C-bus GPIO output valid	0.2		0.2		µs
T_{D2}	I^2C-bus modem input interrupt valid	0.2		0.2		µs
T_{D3}	I^2C-bus modem input interrupt clear	0.2		0.2		µs
T_{D4}	I^2C input pin interrupt valid	0.2		0.2		µs
T_{D5}	I^2C input pin interrupt clear	0.2		0.2		µs
T_{D6}	I^2C-bus receive interrupt valid	0.2		0.2		µs
T_{D7}	I^2C-bus receive interrupt clear	0.2		0.2		µs
T_{D8}	I^2C-bus transmit interrupt clear	1.0		0.5		µs
T_{D15}	SCL delay after reset	3		3		µs

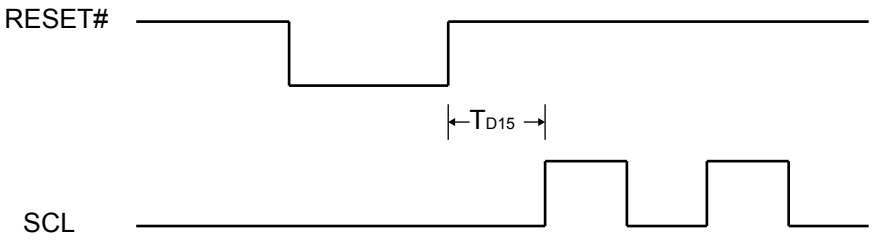


Figure 1. SCL Delay After Reset

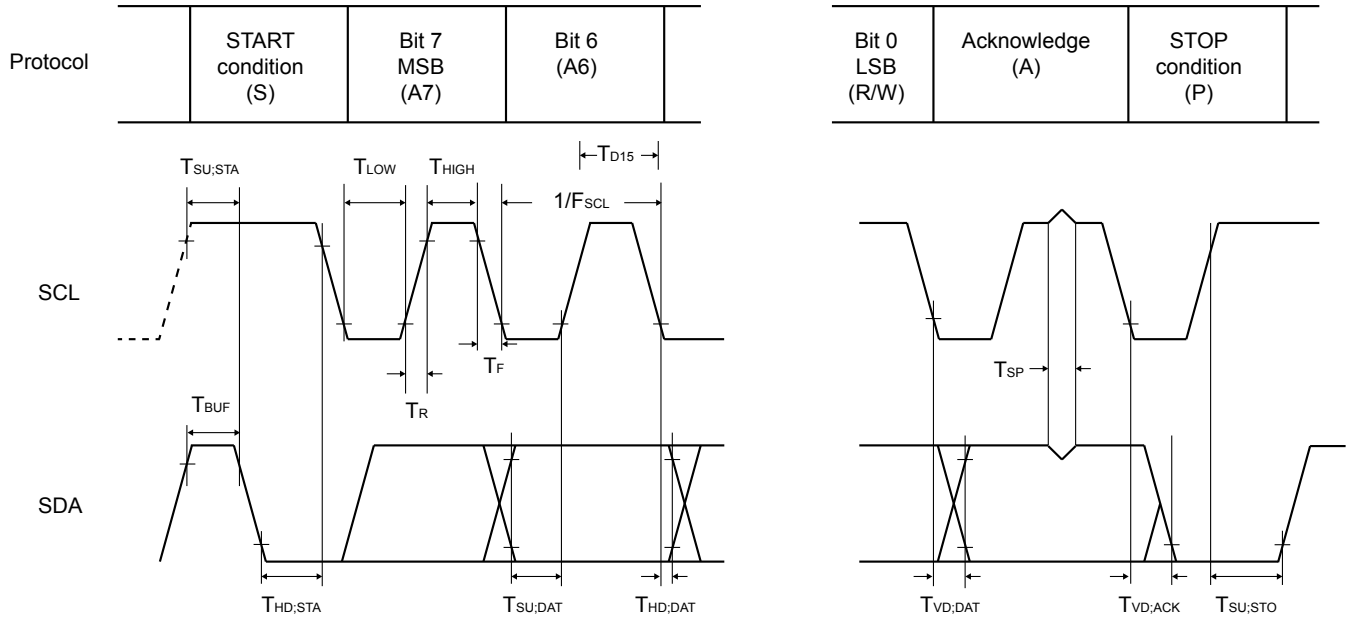


Figure 2. I²C-Bus Timing Diagram

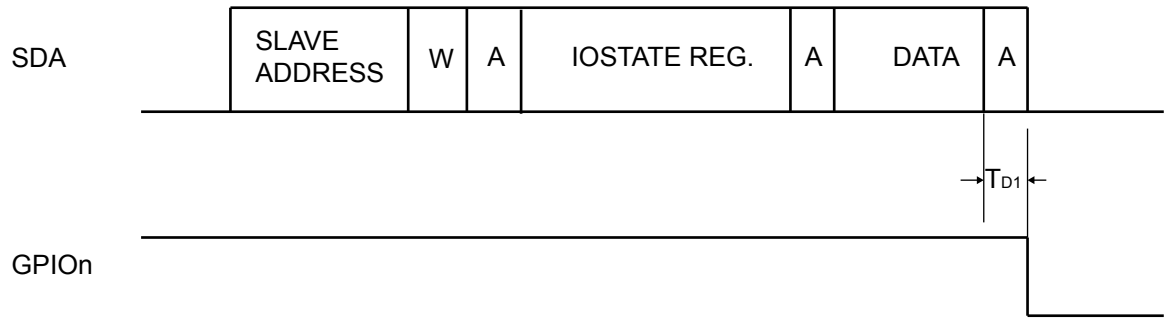


Figure 3. Write To Output

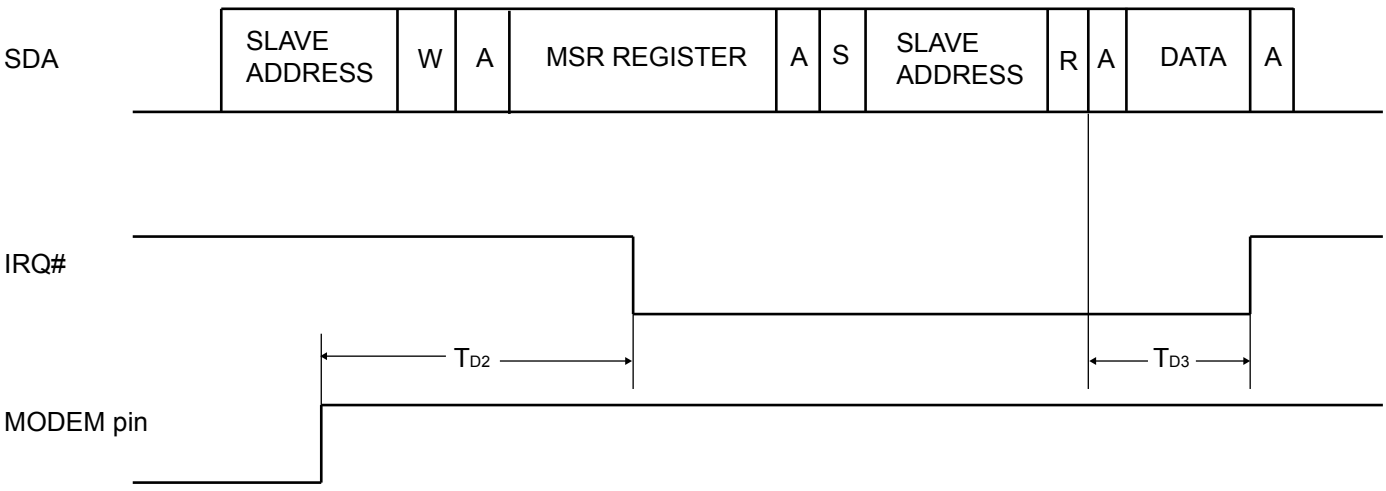


Figure 4. Modem Input Pin Interrupt

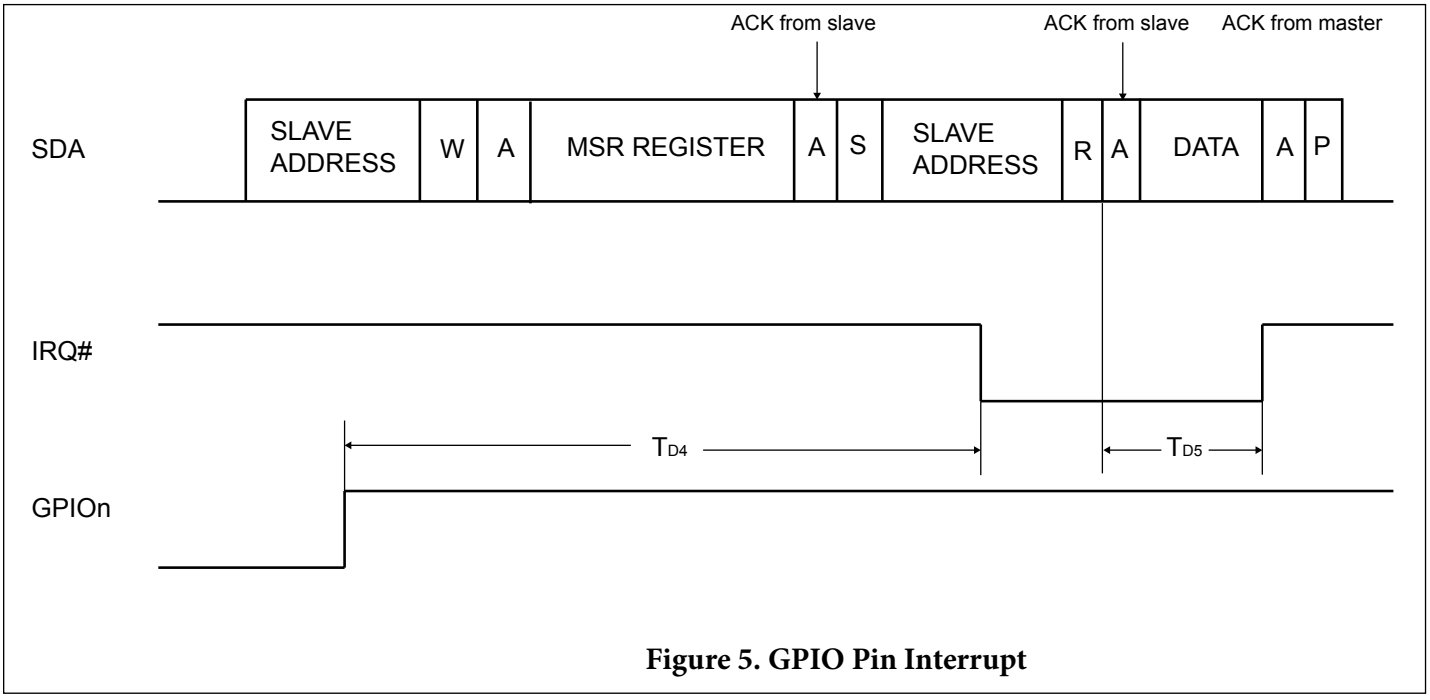


Figure 5. GPIO Pin Interrupt

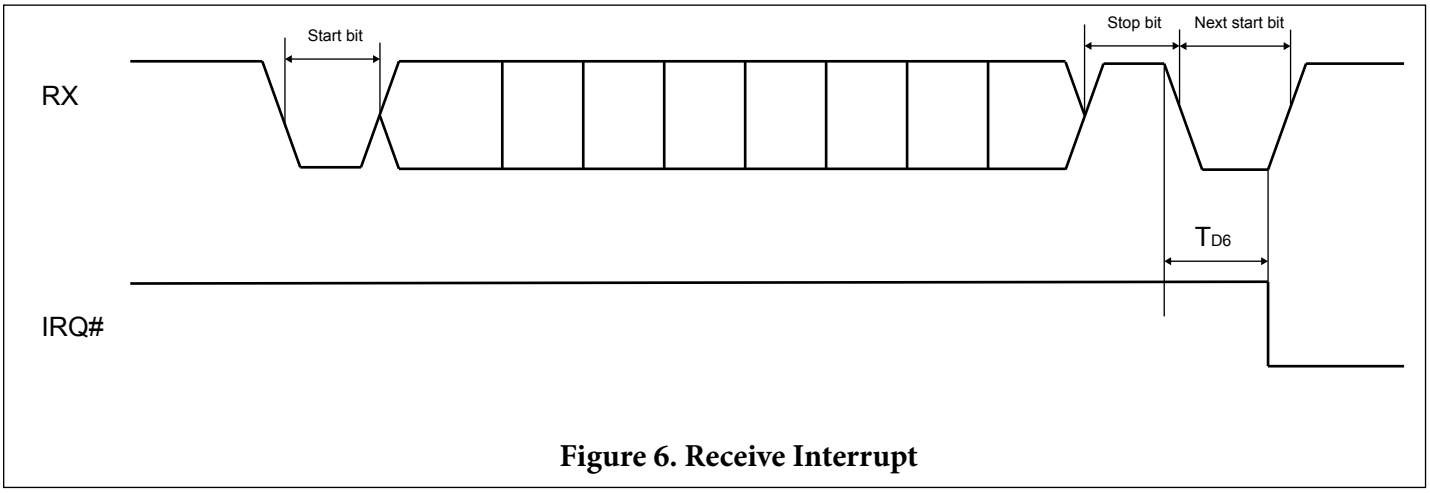


Figure 6. Receive Interrupt

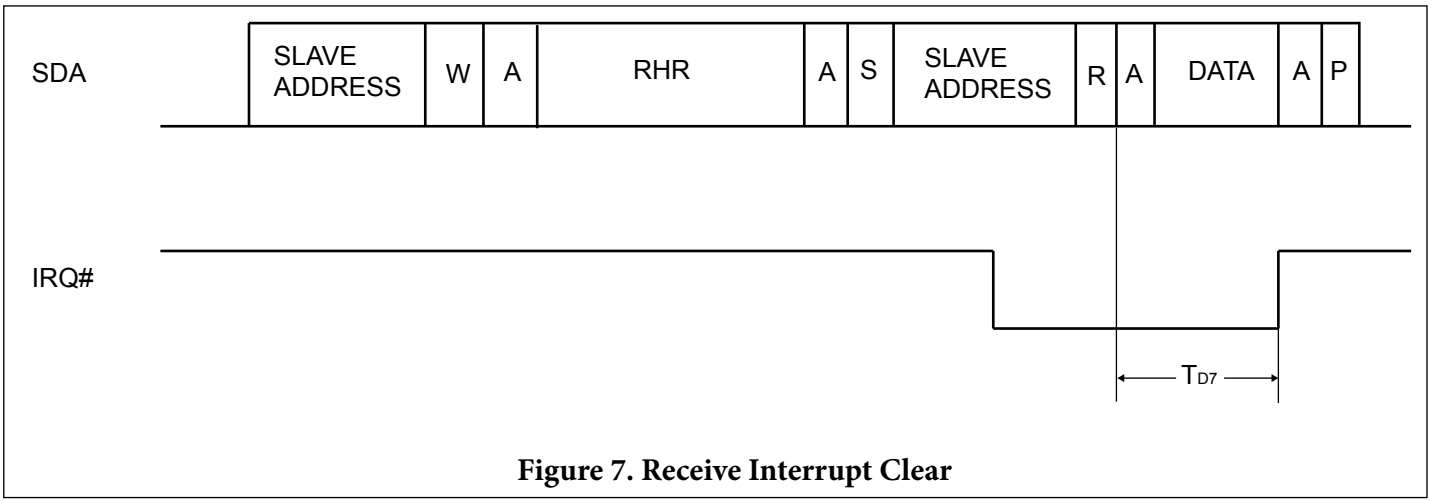


Figure 7. Receive Interrupt Clear

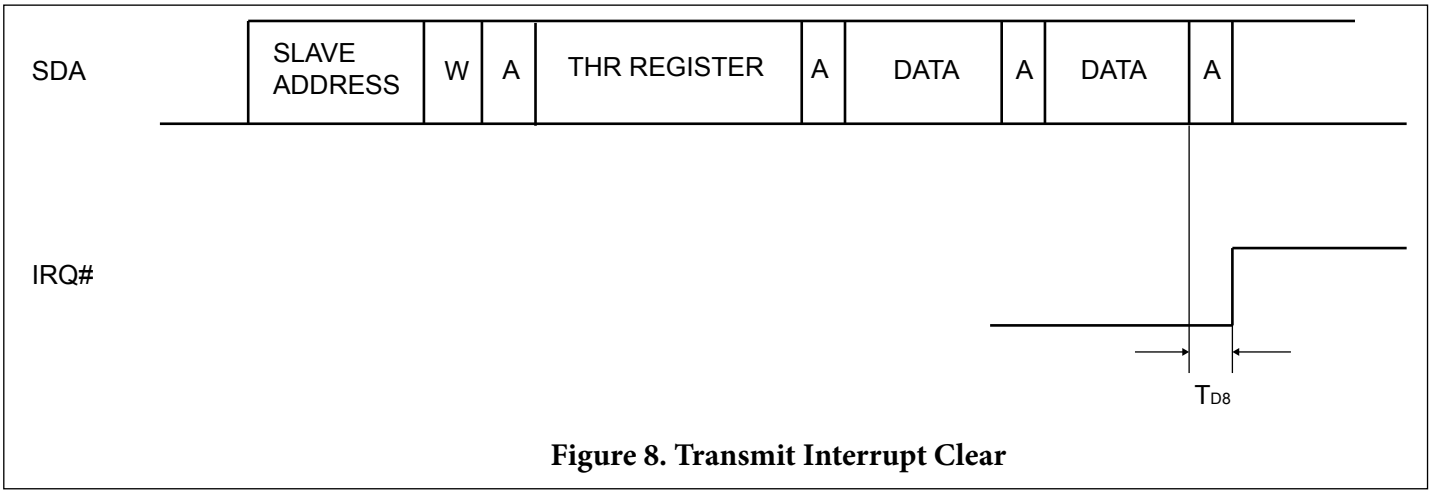


Figure 8. Transmit Interrupt Clear

AC Electrical Characteristic - SPI-Bus Timing Specifications

(Unless otherwise noted: TA = -40o to +85oC, VDD = 1.62 - 3.63V)

Symbol	Parameter	V_{DD} = 1.8V±10%		V_{DD} = 2.5V±10%		V_{DD} = 3.3V±10%		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{SCL}	SPI clock frequency		18		27		33	MHz	
T_{TR}	CS# HIGH to SO three-state time		100		100		100	ns	C_L = 70 pF
T_{CSS}	CS# to SCL setup time	100		100		100		ns	
T_{CSH}	CS# to SCL hold time	20		20		20		ns	
T_{DO}	SCL fall to SO valid time		22		13		11	ns	C_L = 70 pF
T_{DS}	SI to SCL setup time	6.0		5.0		4.0		ns	
T_{DH}	SI to SCL hold time	0		0		0		ns	
T_{CP}	SCL period time	56		36		30		ns	$T_{CH} + T_{CL}$
T_{CH}	SCL HIGH time	28		18		15		ns	
T_{CL}	SCL LOW time	28		18		15		ns	
T_{CSW}	CS# HIGH pulse width	200		200		200		ns	
T_{D9}	SPI output data valid	200		200		200		ns	
T_{D10}	SPI modem output data valid	200		200		200		ns	
T_{D11}	SPI transmit interrupt clear	200		200		200		ns	
T_{D12}	SPI modem input interrupt clear	200		200		200		ns	
T_{D13}	SPI input pin interrupt clear	200		200		200		ns	
T_{D14}	SPI receive interrupt clear	200		200		200		ns	

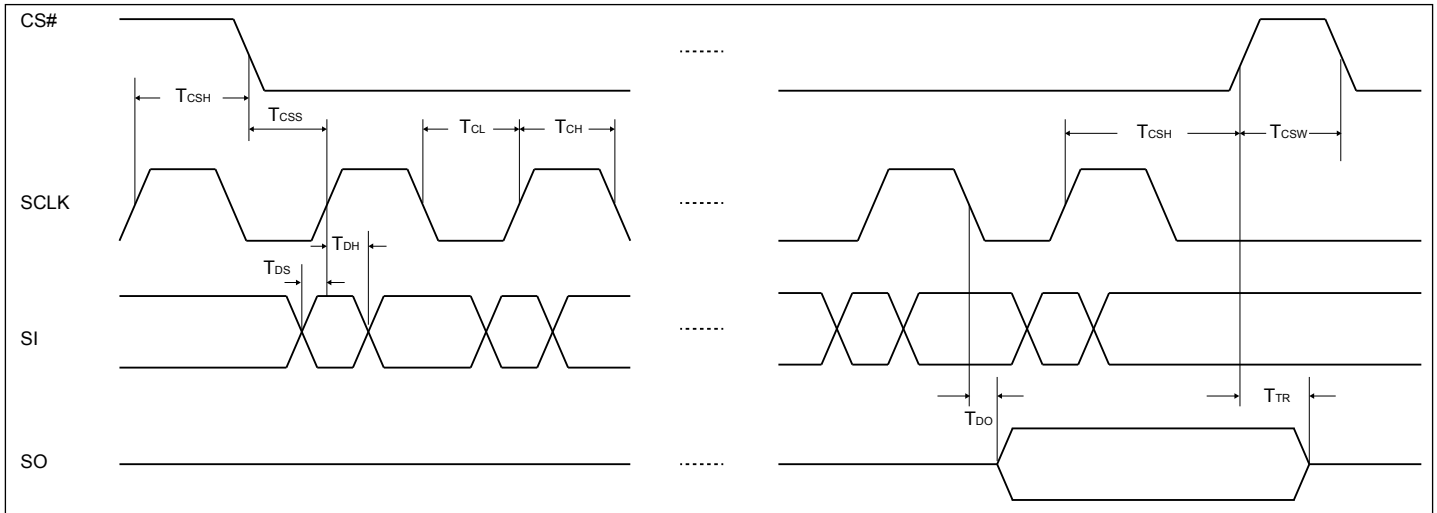


Figure 9. SPI-bus Timing

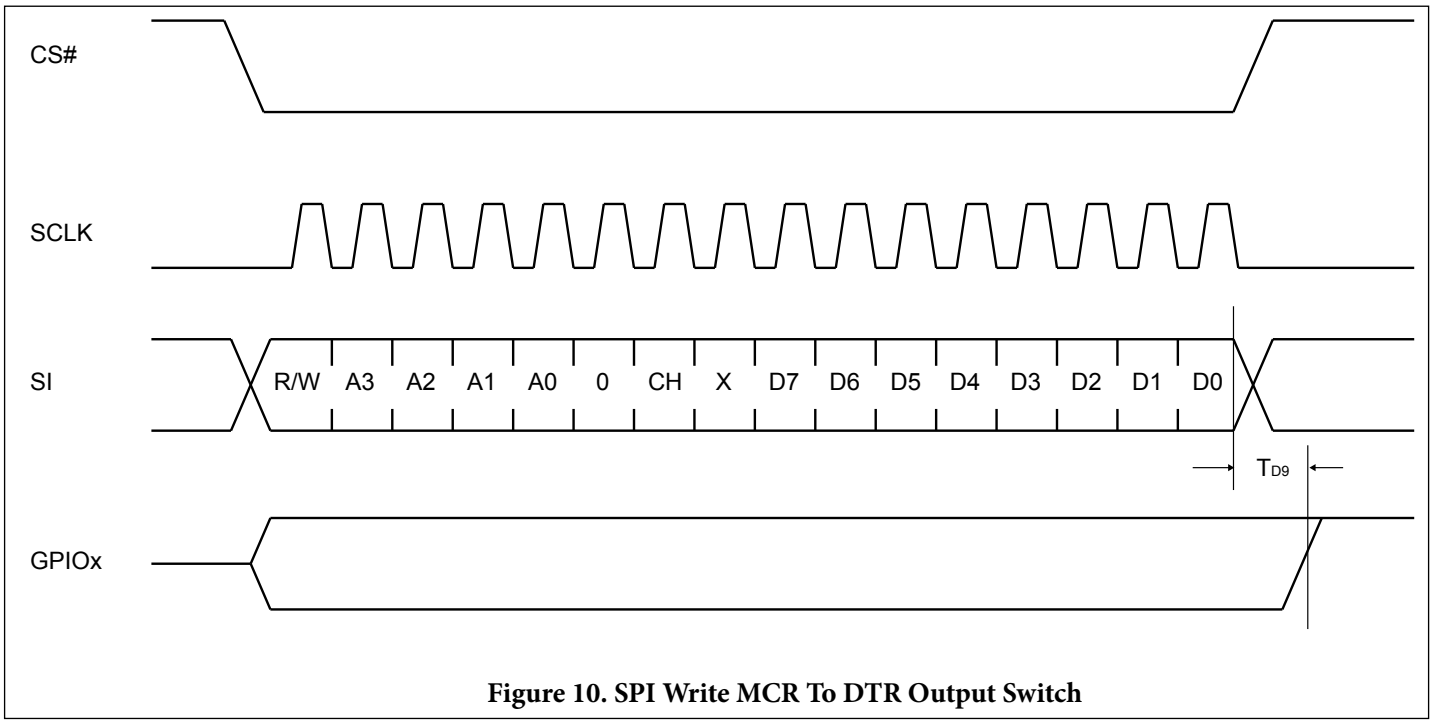


Figure 10. SPI Write MCR To DTR Output Switch

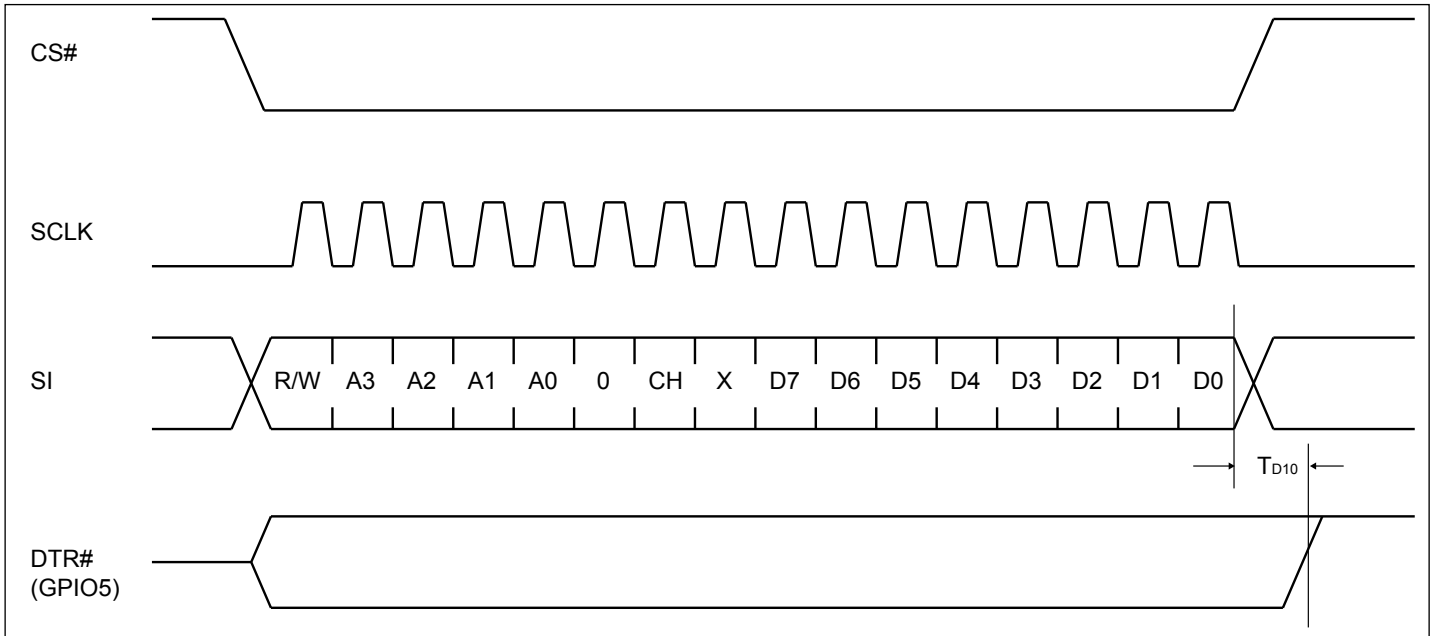


Figure 11. SPI Write MCR To DTR Output Switch

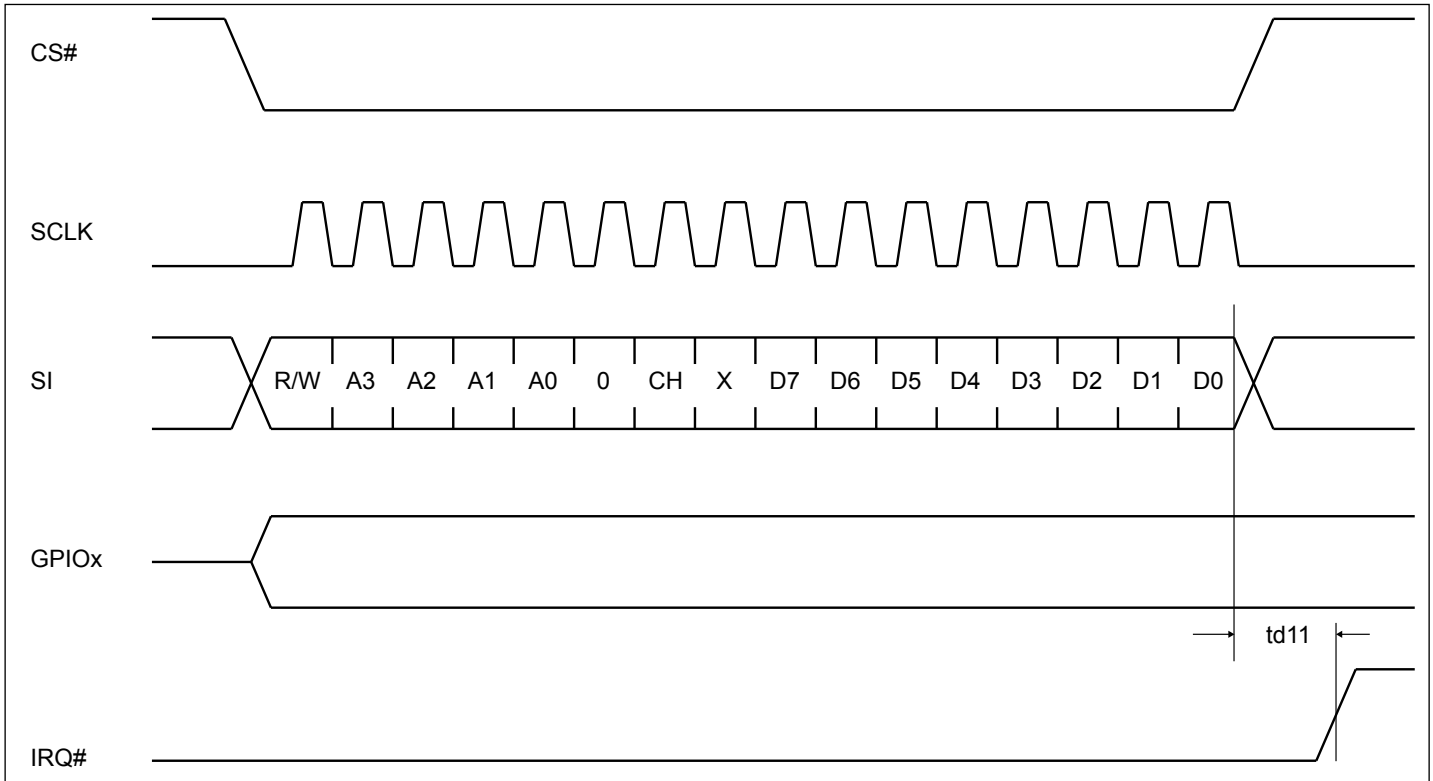


Figure 12. SPI Write THR To Clear TX INT

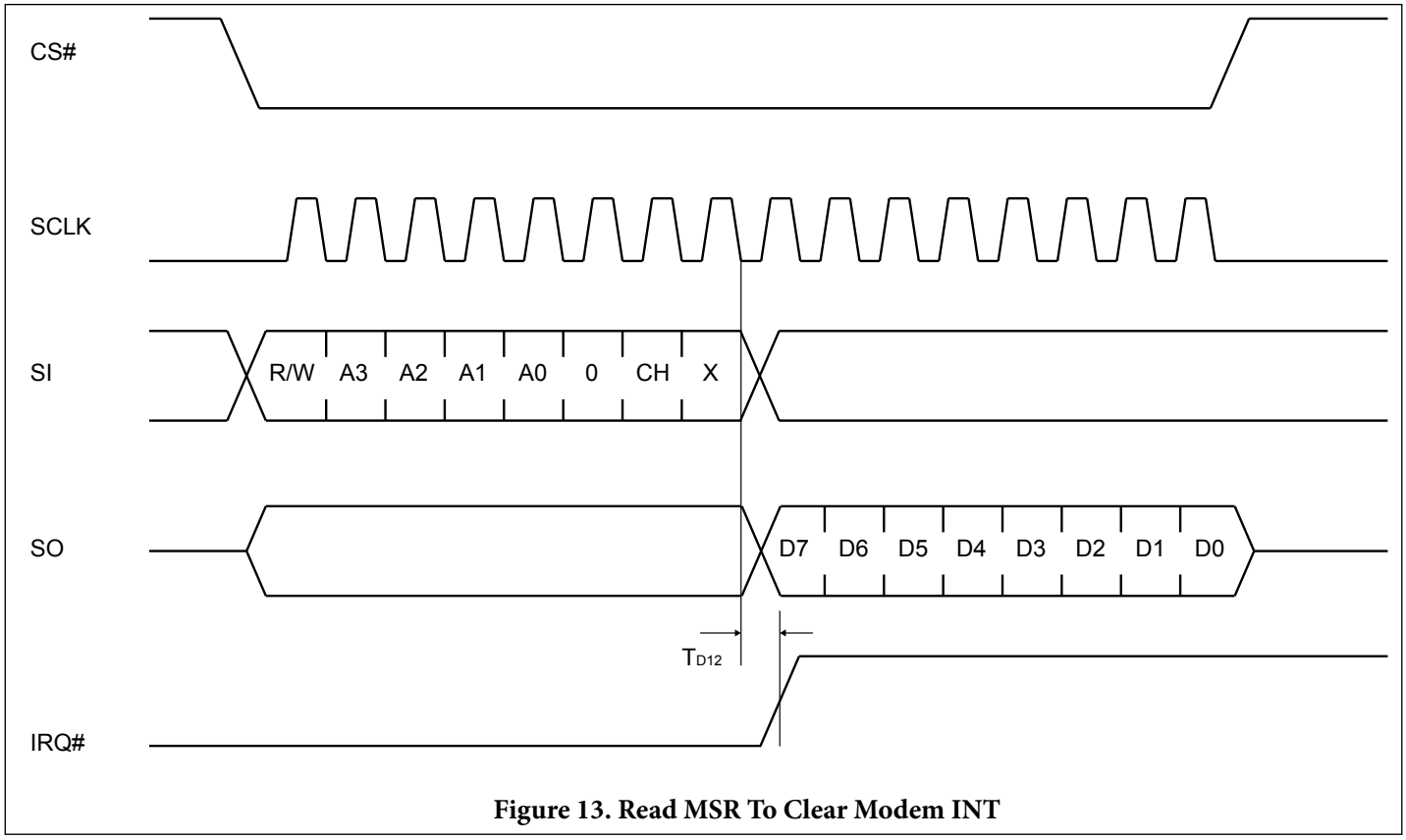


Figure 13. Read MSR To Clear Modem INT

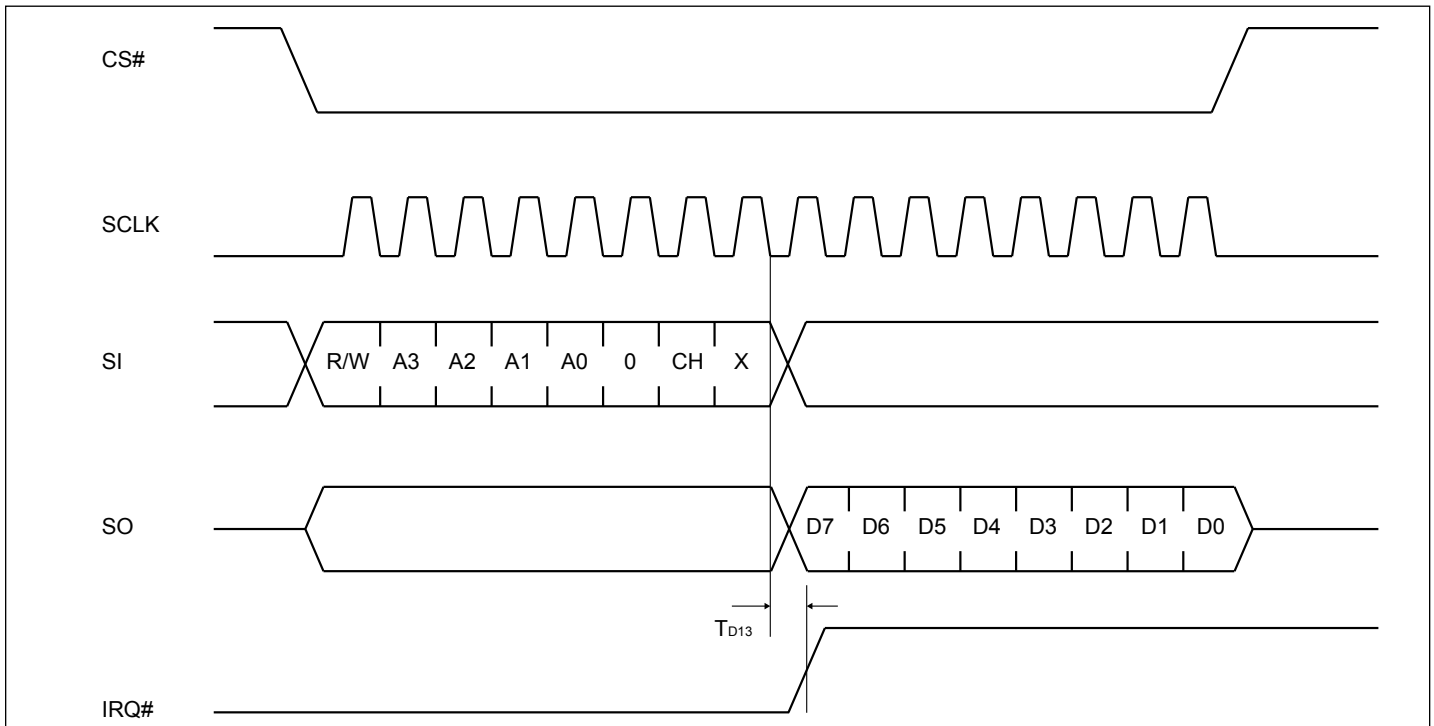


Figure 14. Read IOState To Clear GPIO INT

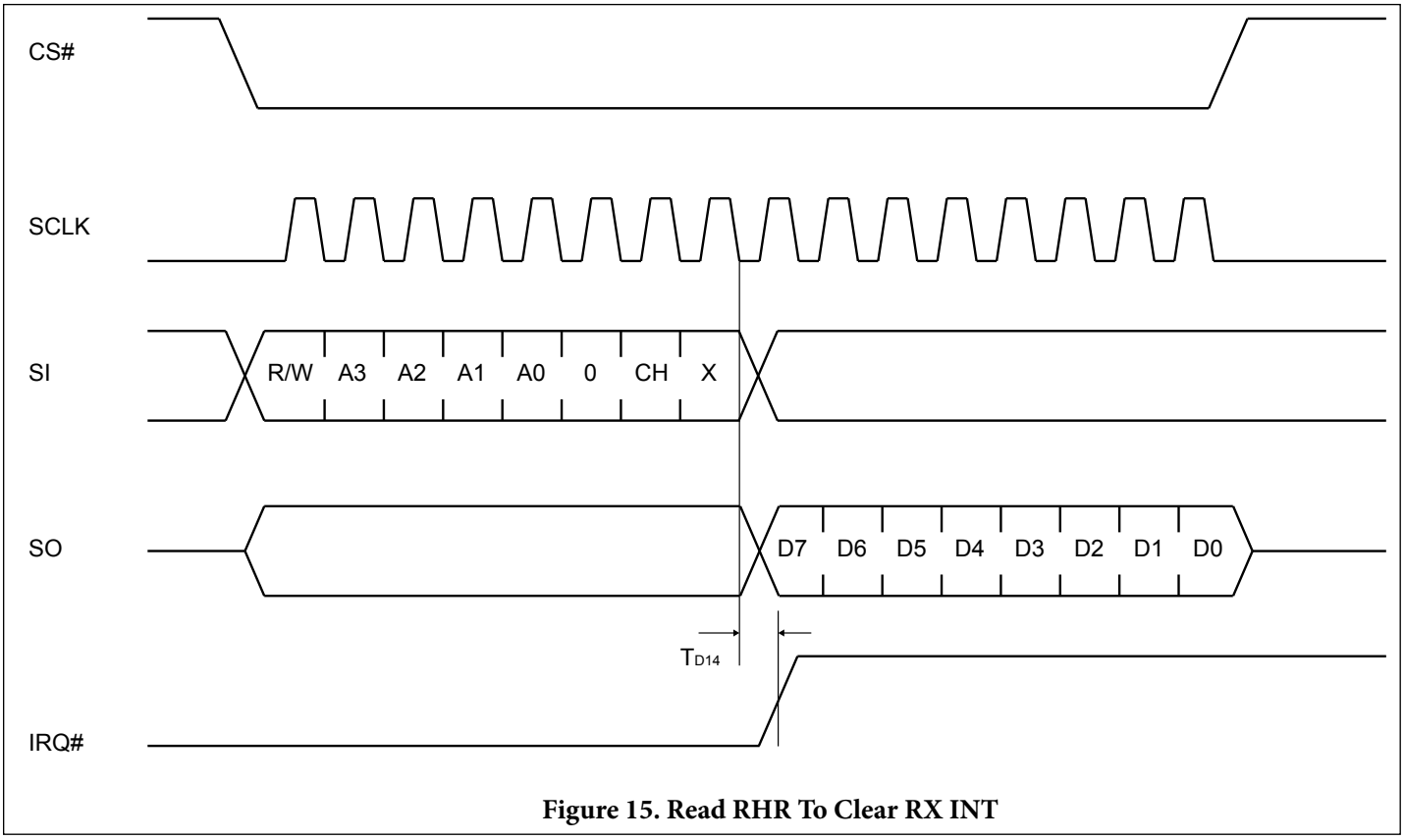


Figure 15. Read RHR To Clear RX INT

Part Marking

L Package

PI7C9X762CLE

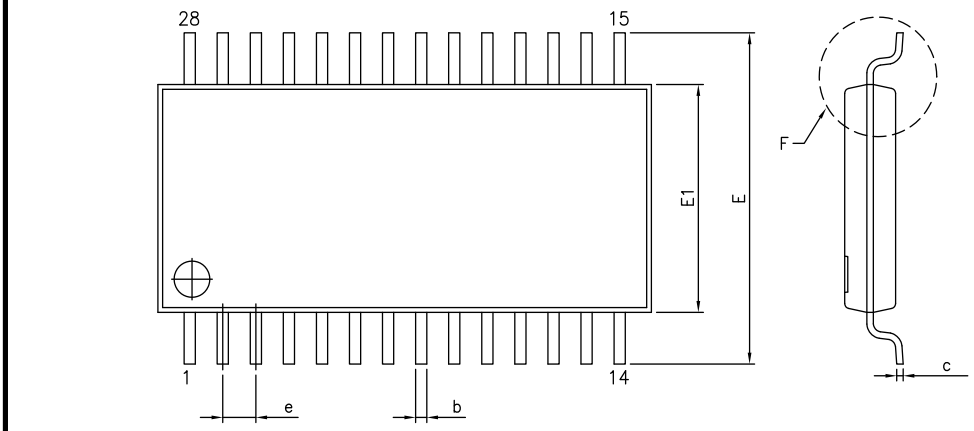
YYWW: Year & Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code

ZH Package

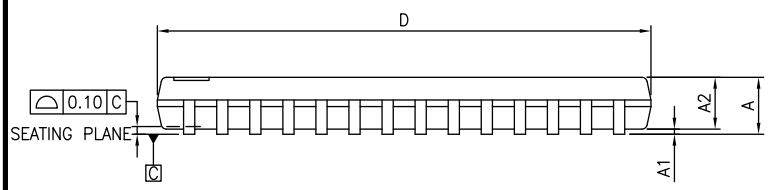
PI7C9X762CZHE

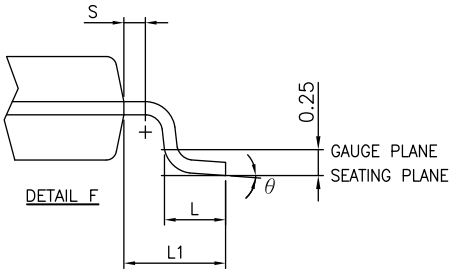
YYWW: Year & Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code

Packaging Mechanical: 28-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO–153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/31/16

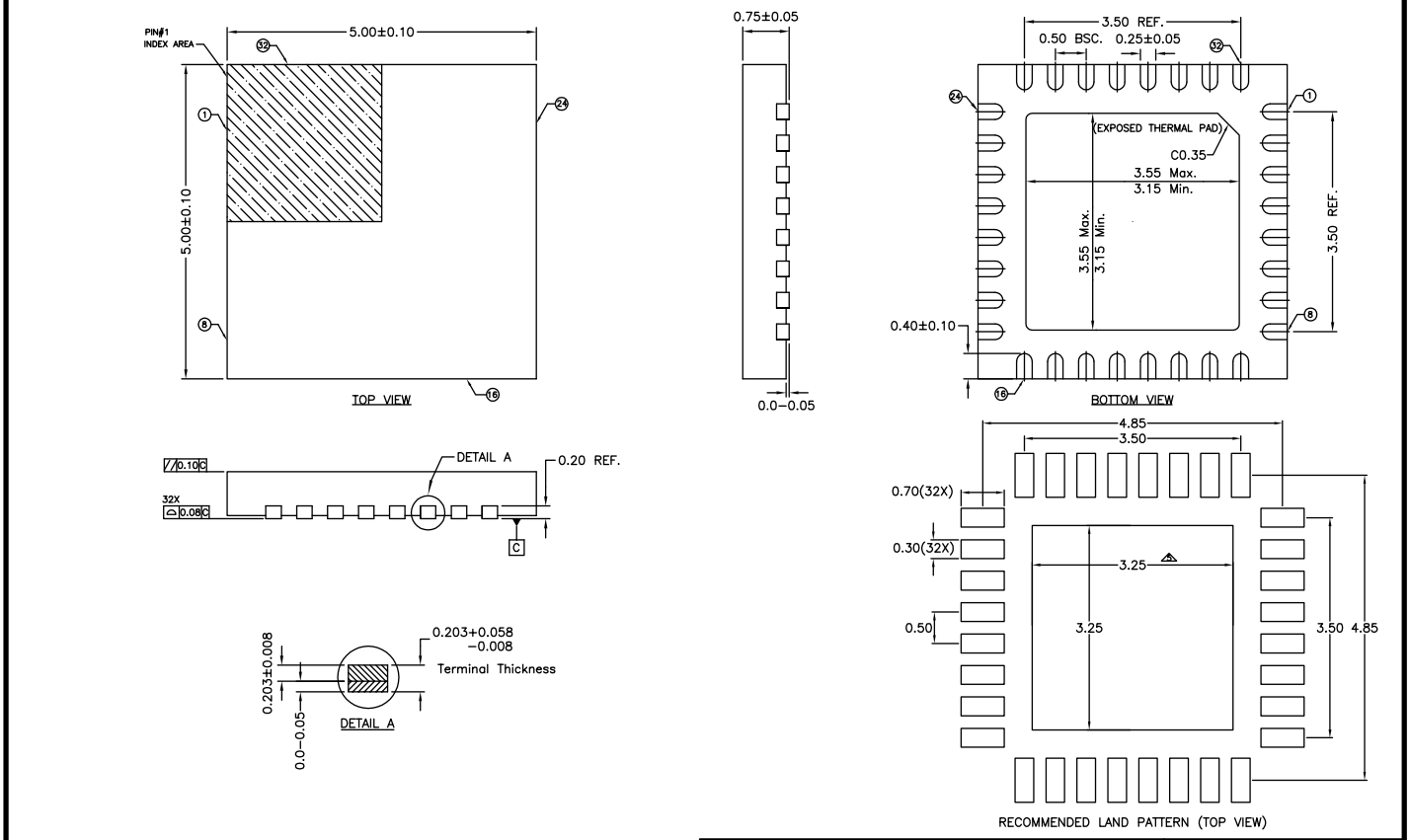
DESCRIPTION: 28-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L28)

DOCUMENT CONTROL #: PD-1313 **REVISION: F**

16-0076

Packaging Mechanical: 32-TQFN (ZH)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

17-0570

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI7C9X762CLEX	L	28-Contact, 173mil wide (TSSOP)
PI7C9X762CZHEX	ZH	32-Contact, Thin Quad Flat No-Lead (TQFN)

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com

Revision History

Date	Revision	Description
8/14/2014	0.1	First Release
10/21/2014	0.1	Updated the AC Electrical Characteristic - I2C-Bus Timing Specifications Updated the SPI Bus Interface Updated the Feature Updated the Description Updated Configuration Register
05/13/2015	1.0	Updated the Maximum Rating Updated the Ordering Information
05/25/2016	1.1	Updated the Packaging Mechanical
12/14/2016	1.2	Chnage the revision to C Updated the Maximum Ratings
06/05/2017	1.3	Remove C from part numbers except ordering information
10/20/2017	2	Revision numbering system changed to whole number
04/27/2018	3	Updated the Pin Configuration 32-Pin TQFN (I2C-Bus Interface) Diagram Updated the Ordering Information Added Part Marking
05/09/2018	4	Updated Configuration Registers

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View PI7C9X762BZHEX on WIN SOURCE
- Diodes Incorporated Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management