THE DATASHEET OF

P3041NSN1PNB

QorIQ Communications Platforms

P3 Series

P3041 optimized quad-core processor

Overview

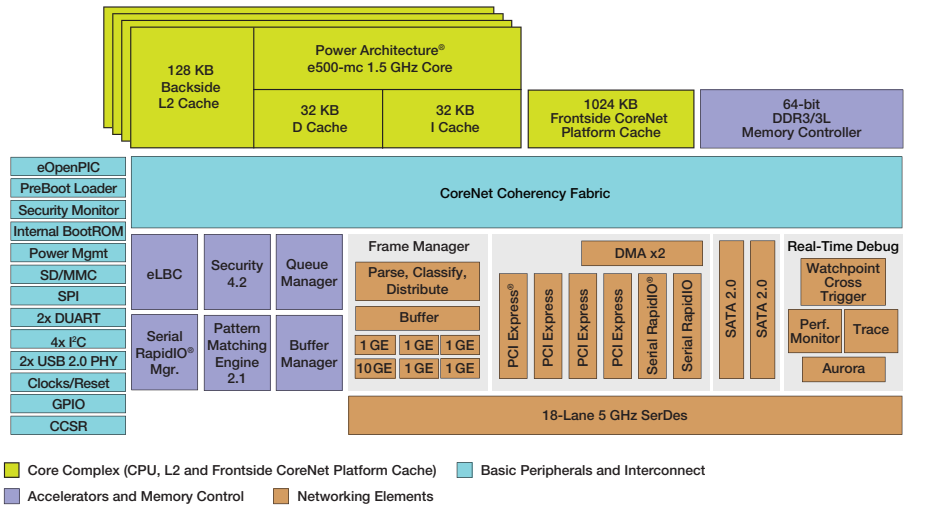
The QorIQ P3041 processor is an optimized, quad-core device that leverages architectural features pioneered in the P4 platform. Built on Power Architecture® technology, the P3041 fits into many of the same applications as the P4 platform processors, yet is designed to offer a more power- and cost-efficient solution.

The P3041 includes P4 platform features such as the three-level cache hierarchy for low latencies, hardware hypervisor for robust virtualization support, data path acceleration architecture (DPAA) for offloading packet handling tasks from the core and the CoreNet switch fabric which eliminates internal bottlenecks. This enables architectural compatibility from the P3041 to the P4 platform and also to the P5 platform, which uses the same architecture.

The P3041 processor uses the same 37.5 mm x 37.5 mm 1295-pin package as the P4 and P5 processors, resulting in pin-compatibility across a broad range of performance levels. Between the architectural similarity and the pin-compatible package, developers can leverage the same software and printed circuit board (PCB) across many applications with a variety of requirements:

- Low-power, mid-range mixed control and data plane (P3 platform)
- High-performance data path performance (P4 platform)
- High-performance control plane application (P5 platform)

P3041 Block Diagram



Key Architectural Features

- Three-level cache hierarchy: The low-latency 32 KB L1 instruction and data caches are augmented by a unified 128 KB private backside L2 cache per core. The L2 is 8-way set associative and is ECC protected. When instructions are locked in the L2, the per-packet “hot” code is always readily available, improving application performance. A shared 1 MB CoreNet platform cache (L3) facilitates core-to-core communications and minimizes accesses to main memory.
- Hardware hypervisor: The e500mc supports a hardware hypervisor that is designed to enable each core to run its own operating system completely independent of the other core. The hypervisor facilitates resource sharing and partitioning in a multicore environment, and provides protection in the event that a core, driven by malicious or improperly programmed code, tries to access memory does not have permission to read or write. It also allows the sharing and partitioning of various I/Os across the cores and it helps ensure that incoming memory mapped transactions are written only into appropriate ranges of the memory map.
- DPAA: This offloads the cores from the need to perform common packet-handling tasks. For instance, the DPAA will extract headers from incoming packets, police them, classify them and manage their data buffers. The work is assigned to cores with a three-level scheduling hierarchy, which can also facilitate sharing of packet workload over multiple cores.
- CoreNet switch fabric: The fabric-based interface provides scalable on-chip, point-to-point connectivity supporting concurrent traffic to and from multiple resources connected to the fabric, eliminating single-point bottlenecks for non-competing resources. This is designed to eliminate bus contention and latency issues associated with scaling shared bus architectures that are common in other multicore approaches.

Target Applications

The P3 family is targeted at mixed control plane and data plane applications, where in previous generations separate devices would implement each function. Typically, one or two cores would implement the control plane, while the remaining cores implement the data plane. The hardware hypervisor facilitates this, with its capability to safely provision flexible core allocations into groups running SMP, one core running alone, separate cores running in parallel or a core running end-user applications. There are many applications that look similar to this, including:

- Integrated access router (IAD). Dual SATA ports provide high-speed, cost-effective storage options for statistics or large databases. Compared to SGMII, 2.5 Gb/s Ethernet enables the next step in performance connectivity to switches.
- Base station network interface card (NIC): Dual Serial RapidIO ports (up to 5 GHz) can be used for redundancy or multiple connections, both to the backplane or to the DSP farm. With improved Type 11 messaging and new support for Type 9 data streaming, the Serial RapidIO interconnect can now be used not only as a control plane interface, but can also achieve its intended potential as a highly efficient data path.

Features

Four e500mc cores, built on Power Architecture technology

- Up to 1.5 GHz
- Each with 128 KB backside L2 cache

Memory controller

- DDR3, 3L up to 1.3 GHz
- 32/64-bit data bus w/ECC

High-speed interconnects

- 18 x 5 GHz SerDes lanes
- 4 x PCI Express® 2.0 controllers at 5 GHz
- 2 x Serial RapidIO 1.3/2.1 controllers at 5 GHz
- 2 x SATA 2.0 at 3 Gbps
- 2 x USB 2.0 with PHY

CoreNet switch fabric

- 1 MB shared CoreNet platform cache (L3) with ECC

Ethernet

- 5 x 10/100/1000 Ethernet controllers
- 1 x 10 Gigabit Ethernet controllers
- All with classification, hardware queueing, policing, buffer management, checksum offload, QoS, lossless flow control, IEEE® 1588
- Up to 1 x XAUI, 4 x SGMII or 2.5 Gbps SGMII, 2 x RGMII

Data path acceleration

- SEC 4.2: public key accelerator, DES, AES, message digest accelerator, random number generator, ARC4, SNOW 3G F8 and F9, CRC, Kasumi
- PME 2.1: searches for 128 byte text strings in 32 KB patterns in 128 M sessions
- RapidIO messaging: Type 9 and 11

Device

- 45 nm SOI process technology
- 1295-pin FCPBGA package, 37.5 mm x 37.5 mm

Enablement

- Enea®: Real-time operating system support
- Green Hills®: Complete portfolio of software and hardware development tools, trace tools and real-time operating systems
- Mentor Graphics®: Commercial grade Linux® solution
- CodeSourcery: Tool chain support for new core technology
- Wind River®: Simics® model
- Development System: Four PCI Express slots, one Serial RapidIO slot, one XAUI slot, one SGMII slot, SATA disk, Aurora debug port

For more information, please visit freescale.com/QorIQ

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