THE DATASHEET OF

NRF24AP2-1CHQ32-R7

www.win-source.net 0086-755-83957316

nRF24AP2

nRF24AP2-1CH, nRF24AP2-8CH

Single-chip ANT™ ultra-low power wireless network solution

Product Specification v1.2

Key Features

- Second generation single chip ANT solution
- nRF24AP2-1CH supports 1 ANT (logic) channel – ideal for sensors
- nRF24AP2-8CH supports up to eight ANT (logic) channels – ideal for hubs
- World wide 2.4 GHz ISM band operation
- Fully embedded, enhanced ANT protocol stack
- True ultra-low power operation
- Typically years of battery lifetime on a coin cell
- Built-in device search and pairing
- Built-in timing and power management
- Built-in interference handling
- Configurable channel period 5.2 ms - 2 s
- Broadcast, Acknowledged and Burst communication modes
- Burst data rate up to 20 kbps
- Simple to complex network topologies: Peer-to-peer, star, tree and practical mesh
- Supports public, private and managed networks
- Support for ANT+ device profile implementations enabling multivendor interoperability
- Fully interoperable with nRF24AP1 and Dynastream ANT chipset / module based products and other nRF24AP2 variants
- Simple asynchronous/ synchronous host interface
- Single 1.9 - 3.6V power supply
- RoHS compliant 5×5 mm 32-pin QFN package
- Low cost external 16 MHz crystal
- Optional on-chip 32.768 kHz crystal oscillator

Applications

- Sports
- Wellness
- Home health monitoring
- Home/industrial automation
- Environmental sensor networks
- Active RFID
- Logistics/goods tracking
- Audience-response systems

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June 2010

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Datasheet status	
Objective product specification	This product specification contains target specifications for Nordic Semiconductor's product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Revision History

Date	Version	Description
April 2010	1.1	Updated schematics. Added section 2.4.1 on page 12, updated sections 8.1 on page 43 and 8.2 on page 46.
June 2010	1.2	Updated sections 2.1 on page 8 and 2.4 on page 11, Table 4. on page 22, section 4.2.2 on page 16, section 8.1 on page 43, and chapter 11 on page 49.

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1 Introduction

nRF24AP2 is a member of Nordic Semiconductor's low-cost, high-performance family of 2.4 GHz ISM single-chip connectivity devices with the ANT protocol stack embedded. nRF24AP2 offers the market's most efficient, single chip, transceiver solution for Ultra Low Power (ULP) networks, through the integration of the extremely power efficient ANT protocol stack, the world leading Nordic Semiconductor 2.4 GHz RF technology as well as critical low-power oscillator and timing features.

This document covers the two products:

- nRF24AP2-1CH
- nRF24AP2-8CH

1.1 Prerequisites

In order to fully understand the product specification, a good knowledge of electronics and software engineering is necessary. Please also refer to the document *ANT Message Protocol and Usage* when reading this product specification. You can download the document from Nordic's web site www.nordicsemi.com or from www.thisisant.com.

1.2 Writing conventions

This product specification follows a set of typographic rules to ensure that the document is consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in **`Courier New`**.
- Pin names and pin signal conditions are written in **`Courier New bold`**.
- Cross references are underlined and highlighted in blue.

2 Product overview

ANT is a demonstrably superior Wireless Sensor Network (WSN) RF protocol for almost all practical ultra-low power networking applications – from simple point-to-point links to complex networks. Embedded in nRF24AP2 devices, it is paired up with Nordic Semiconductor's market leading 2.4 GHz radio technology. The combination gives you high performance, ultra-low-power network connectivity to applications, and requires minimal resources in the application's microcontroller. Less than 1 kB of code space, and an Asynchronous or Synchronous serial interface are all it takes to enable ANT connectivity in your application.

The nRF24AP2 variants meet the specific requirements of end nodes and central nodes in a network. nRF24AP2-1CH offers one logic communication channel (ANT channel) for end nodes like sensors to connect to data collectors. nRF24AP2-8CH can manage up to eight ANT channels to collect data from multiple sensors.

Figure 1. shows a network in which a network node with nRF24AP2-8CH embedded, communicates with ANT nodes with nRF24AP2-1CH devices embedded. An example might be a sports watch collecting data from several sensors (like heart rate-, speed- and distance sensors). Of course, the 8-channel node can also set up ANT channels with other central nodes (gym equipment, for instance). These central nodes are in turn connected to additional sensors.

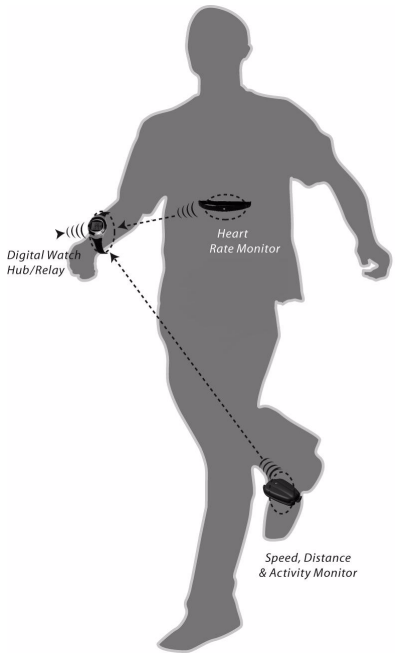


Figure 1. Simple setup with nRF24AP2

See Figure 10. on page 21 for more complex ANT-network topologies.

2.1 Features

Features of the 1-channel nRF24AP2-1CH and 8-channel nRF24AP2-8CH include:

- Ultra low power 2.4 GHz transceiver
  - World wide 2.4 GHz ISM band operation
  - Based on nRF24L01+ transceiver
  - GFSK modulation
  - 1 Mbps on-air data rate
  - 1 MHz frequency resolution
  - 78 RF channels
  - -85 dBm sensitivity
  - Up to 0 dBm output power
- ANT protocol stack
  - Full implementation of the physical, data link, network- and transport OSI layers
  - Packet-based communication – 8 byte payload per packet
  - Optimized for ultra-low power operation
- ANT channels
  - Logic communication channel between ANT nodes
  - nRF24AP2-1CH supports 1 channel – ideal for sensors
  - nRF24AP2-8CH support up to 8 channels – ideal for hubs
  - Built-in timing and power management
  - Built-in interference handling
  - Configurable channel period 5.2 ms - 2 s
  - Broadcast, acknowledged and burst communication modes
  - Burst data rate up to 20 kbps
- Device search and pairing
  - Wild-card searches
  - Proximity searches
  - Specific searches
  - Automatic link establishment if correct device is found
  - Automatic re-link attempt if link is lost
  - Configurable search timeout
- Network topologies
  - Point-to- point and star networks using independent ANT channels
  - Shared networks: Polled data collection (N:1) by using ANT shared channel option
  - Broadcast networks: Mass distribution of data (1:N)
- Network management / ANT+
  - Supports public and private (managed) networks
  - Support for ANT+ system implementations enabling multi-vendor interoperability
- ANT core stack enhancements
  - Background scanning channel
  - Continuous scanning mode
  - High density node support
  - Improved channel search
  - Channel ID management
  - Improved transmission power control on a per channel basis
  - Frequency agility
  - Proximity search
- Power Management
  - Fully controlled by ANT protocol stack
  - On-chip voltage regulator
  - Single DC supply operation
  - 1.9 to 3.6V supply range
- Ultra low power operation
  - Up to 50% lower average compared to nRF24AP1
  - Up to 40% lower peak current compared to nRF24AP1
  - 20 µA average current consumption at 1 Hz broadcast
  - 71 µA average current consumption at 4 Hz broadcast
- On-chip oscillators and clock inputs
  - 16 MHz crystal oscillator supporting low-cost crystals
  - 16 MHz clock input
  - Ultra low power 32.768 kHz crystal oscillator
  - 32.768 kHz clock input
- Host interface
  - Supports asynchronous and synchronous modes
  - 5-pins for asynchronous
  - 6-pins for synchronous

2.2 Block diagram

nRF24AP2 is composed of five main blocks as shown in Figure 2. The blocks indicate the interface, power management, the ANT protocol engine, on-chip oscillators and the RF transceiver.

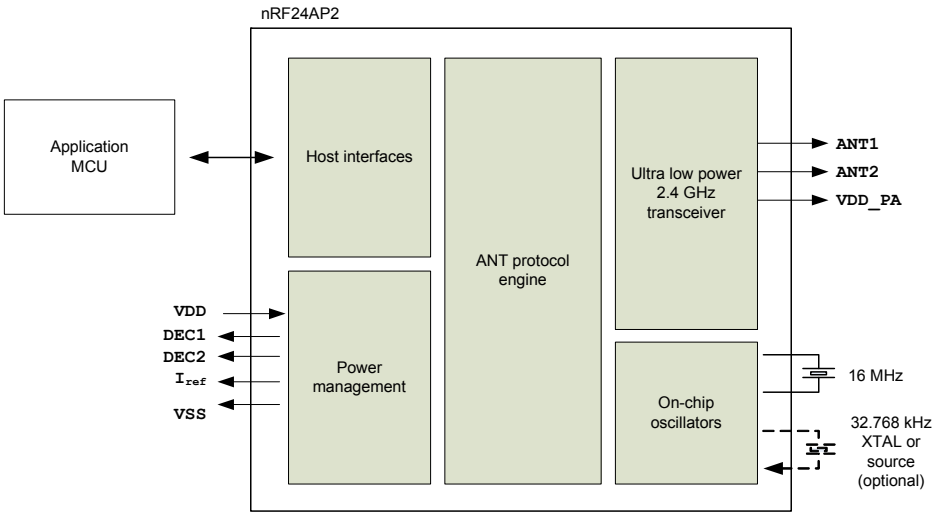


Figure 2. Block diagram of nRF24AP2 solution

To find more information about each block in the diagram, see Table 1.

Name	Reference
RF Transceiver	Chapter 3 on page 13
ANT protocol engine	Chapter 4 on page 15
Host interfaces	Chapter 5 on page 23
On-chip oscillators	Chapter 6 on page 34
Power management	Chapter 8 on page 40

Table 1. Block diagram cross references

2.3 Pin Assignments

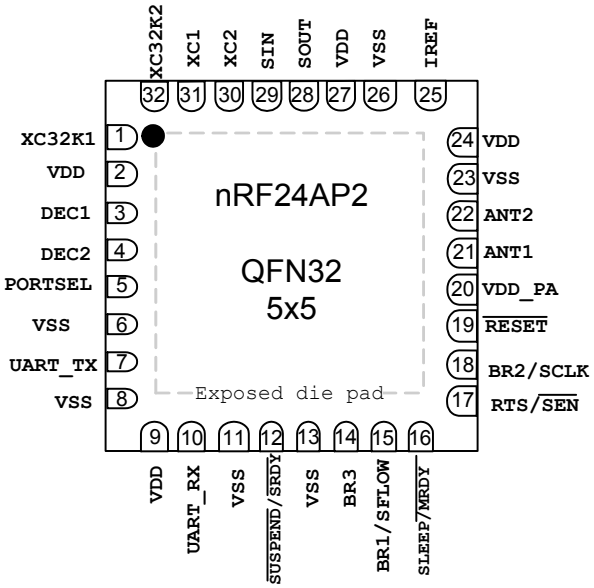


Figure 3. nRF24AP2 pin assignment (top view) for a QFN32 5×5 mm package

2.4 Pin Functions

Pin	Pin name	Pin functions	Description
1	XC32K1	Analog input	Crystal connection for 32.768 kHz crystal oscillator, optionally a synthesized or external 32.768 kHz clock can be used as described in chapter 6 on page 34
2	VDD	Power	Power Supply (1.9-3.6V DC)
3	DEC1	Power	Power supply outputs for de-coupling purposes (100nF)
4	DEC2	Power	Power supply outputs for de-coupling purposes (33nF)
5	PORTSEL	Digital input	Port Select Asynchronous serial interface: Tie to VSS Synchronous serial interface: Tie to VDD
6	VSS	Power	Ground (0V)
7	UART_TX	Digital IO	Asynchronous mode: Transmit data signal Synchronous mode: Tie to VSS or VDD.
8	VSS	Power	Ground (0V)
9	VDD	Power	Power Supply (1.9-3.6V DC)
10	UART_RX	Digital input	Asynchronous mode: Receive data signal Synchronous mode: Tie to VDD
11	VSS	Power	Ground (0V)
12	$\overline{\text{SUSPEND}}$/$\overline{\text{SRDY}}$	Digital input	Asynchronous mode: Suspend control Synchronous mode: Serial port ready
13	VSS	Power	Ground (0V)
14	BR3	Digital input	Asynchronous mode: Baud rate selection Synchronous mode: Tie to VSS
15	BR1/SFLOW	Digital input	Asynchronous mode: Suspend Control Synchronous mode: Bit or Byte flow control select (Bit: Tie to VDD, Byte: Tie to VSS)
16	SLEEP/$\overline{\text{MRDY}}$	Digital input	Asynchronous mode: Sleep mode enable Synchronous mode: Message ready indication
17	$\overline{\text{RTS}}$/$\overline{\text{SEN}}$	Digital output	Asynchronous mode: Request to send Synchronous mode: Serial enable signal
18	BR2 / SCLK	Digital IO	Asynchronous mode: Baud rate selection Synchronous mode: Clock output signal
19	$\overline{\text{RESET}}$	Digital input	Reset, active low. Internal pull up. Leave unconnected if not used.
20	VDD_PA	Power output	Power supply output (+1.8V) for on-chip RF Power amplifier
21	ANT1	RF	Differential antenna connection (TX and RX)
22	ANT2	RF	Differential antenna connection (TX and RX)
23	VSS	Power	Ground (0V)
24	VDD	Power	Power Supply (1.9-3.6V DC)
25	IREF	Analog output	Device reference current output. To be connected to reference resistor on PCB.
26	VSS	Power	Ground (0V)
27	VDD	Power	Power Supply (1.9-3.6V DC)
28	SOUT	Digital IO	Asynchronous mode: Tie to VSS or VDD. Synchronous mode: Data output
29	SIN	Digital input	Asynchronous mode: Tie to VDD Synchronous mode: Data input
30	XC2	Analog output	Crystal connection for 16 MHz crystal oscillator

Pin	Pin name	Pin functions	Description
31	**XC1**	Analog Input	Crystal connection for 16 MHz crystal oscillator
32	**XC32K2**	Analog output	Crystal connection for 32.768 kHz crystal oscillator, optionally a synthesized or external 32.768 kHz clock can be used as described in chapter 6 on page 34
Exposed die pad	**VSS**	Power	Connects the die pad to **VSS**

Table 2. nRF24AP2 pin functions

2.4.1 Reset pin

The **RESET** pin provides an optional reset when the nRF24AP2 is placed in a system that has a master reset source. This pin is not needed for normal application. Pull **RESET** pin low for minimum 0.2 µs and return to high, this will reset the nRF24AP2 to the default state. Leave unconnected if not used in the application.

3 RF Transceiver

All transceiver operations are controlled solely by the ANT protocol stack. Configuration of the ANT protocol stack occurs through a serial interface by issuing ANT commands to nRF24AP2.

3.1 Features

Features of the RF transceiver include:

- General
  - Worldwide 2.4 GHz ISM band operation
  - Common antenna interface in transmit and receive
  - GFSK modulation
  - 1 Mbps on air data rate
- Transmitter
  - Programmable output power: 0, -6, -12 or -18 dBm
- Receiver
  - Integrated channel filters
  - -85 dBm sensitivity
- RF Synthesizer
  - Fully integrated synthesizer
  - 1 MHz frequency programming resolution
  - 78 RF channels in the 2.4 GHz ISM band
  - Accepts low cost ± 50 ppm 16 MHz crystal
  - 1 MHz non-overlapping channel spacing

3.2 Block diagram

Figure 4. shows a block diagram of the RF transceiver in nRF24AP2.

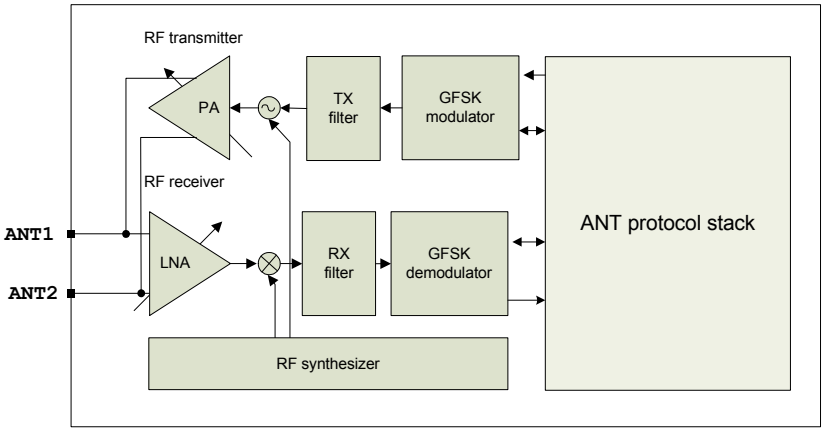


Figure 4. Internal circuitry of RF transceiver relative to ANT

4 ANT overview

The ANT protocol has been engineered for simplicity and efficiency. In operation, this results in ultra-low power consumption, maximized battery life, a minimal burden on system resources, simpler network designs and lower implementation costs.

4.1 Block diagram

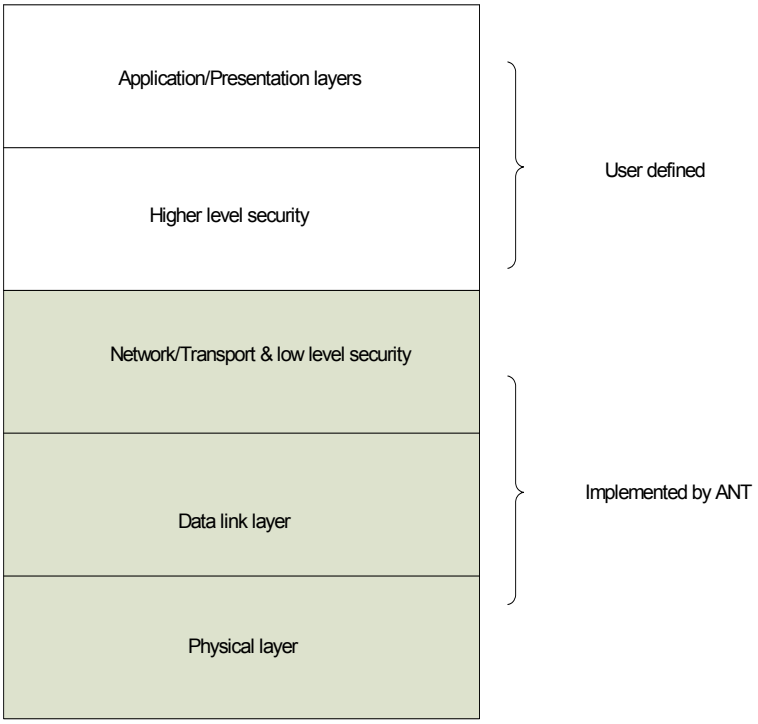


Figure 5. OSI layer model of ANT protocol stack

ANT provides carefree handling of the Physical, Data Link, Network, and Transport OSI layers. See Figure 5. In addition, it incorporates key, low-level security features that form the foundation for user-defined, sophisticated, network-security implementations. ANT ensures adequate user control while considerably easing the computational burden, by providing a simple yet effective wireless networking solution.

4.2 Functional description

A brief overview of the ANT concept is presented here for convenience. A complete description of the ANT protocol is found in the *ANT Message Protocol and Usage* document available at www.nordicsemi.com or www.thisisant.com.

4.2.1 ANT nodes

All ANT networks are built up of nodes. See the ANT node represented in Figure 6. on page 16. A node can be anything from a simple sensor to a complex, collection unit like a watch or computer. Common to all

nodes is that they contain an ANT engine (nRF24AP2) handling all connectivity to other nodes and a host processor handling the application features. nRF24AP2 interfaces to the host processor through a serial interface, and all configuration and control are performed using a simple command library.

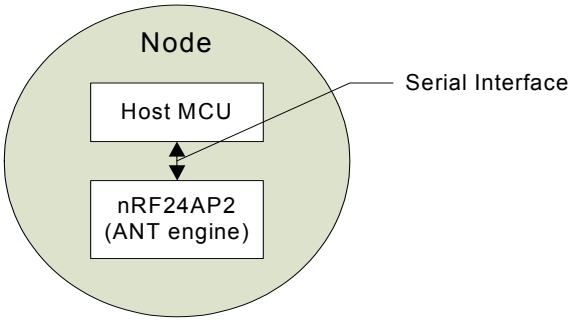


Figure 6. The ANT node

4.2.2 ANT channels

nRF24AP2 can establish one or up to eight logic channels, called ANT channels, to other ANT nodes. The number of ANT channels available depends on the nRF24AP2 variant being used.

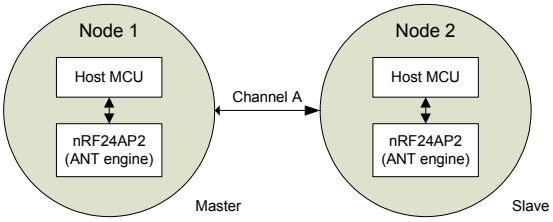


Figure 7. ANT nodes and the channel between them

The simplest ANT channel is called an independent channel and consists of two nodes, one acting as master, the other as slave for this channel. For each ANT channel opened, nRF24AP2 will set up and manage a synchronous wireless link, exchanging data packets with other ANT nodes at preset time intervals called channel periods. See Figure 8. on page 17. The master controls the timing of a channel, that is to say, it will always initiate communication between the nodes. The slave locks on to the timing set by the master, receives the transmissions from the master and can then (if configured so) send acknowledge and/or data (if any) back to the master.

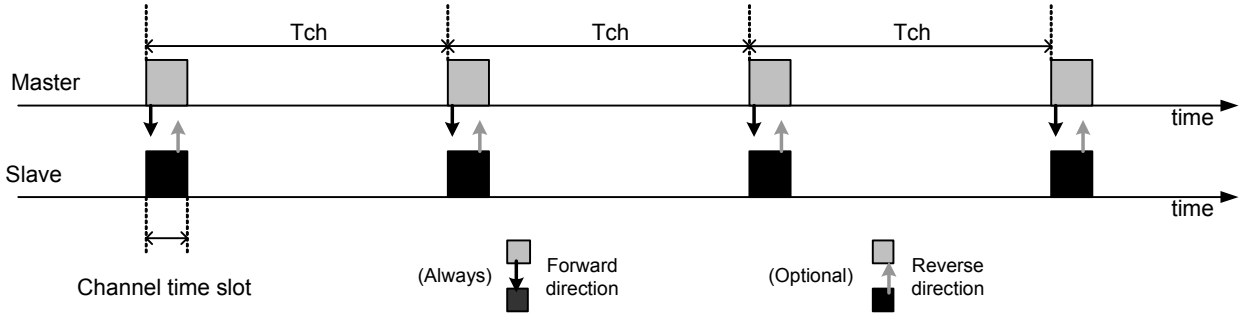


Figure 8. Channel communication showing forward and reverse directions. Not to scale

At each time slot an ANT channel can transfer user data (8 bytes) both ways as simple broadcasts, broadcast with acknowledgement from the receiver, or transfer data as bursts (this will extend the time slot used) to accommodate transfer of larger blocks of user data. The total available payload bandwidth in an ANT node is shared between active ANT channels through a Time Division Multiple Access (TDMA) scheme. If a channel time slot comes up, but there is no new data from the master. The master will still send the last packet to keep the timing of the channel and enable the slave to send data back if needed.

Each ANT channel available in the nRF24AP2 can for example be configured as a simple, uni-directional (broadcast) or bi-directional independent channel; or as a more complex, shared channel where a master interfaces to multiple slaves (1:N topologies). Please see the *ANT Message Protocol and Usage* document for further details on shared ANT channels.

4.2.3 ANT channel configuration

Unique to ANT is that the setup of each ANT channel is independent from all the other ANT channels in the network, including other channels in the same node. This means that one ANT node can act as master on one ANT channel while being a slave to another. Since there is no overall ‘network master’ present in ANT networks, ANT allows you to configure and run each ANT channel solely based on the needs of the nodes on that channel. Search- and pairing algorithms in ANT let you easily set up and shut down ANT channels in an ad-hoc fashion. This gives you ultimate flexibility in adjusting ANT channel parameters like data rate and latency versus power consumption. Moreover, you only make the network as complex as it needs to be at any given time. In order for two ANT nodes to set up an ANT channel, they must share a common channel configuration and channel ID. The necessary configuration parameters are summarized in Table 3. on page 18.

Parameter	Comment
Channel configuration	
Channel period	Time interval between data exchanges on this channel (5.2 ms - 2 s)
RF frequencies	Which of the 78 available RF frequencies is used by this channel
Channel type	Bi-directional slave, bi-directional master, shared bi-directional slave, Slave Receive only
Network type	Decides if this ANT channel is going to be generally accessible (public) to all ANT nodes, or if it shall limit its connectivity to devices belonging to a managed or private network
Channel ID	
Transmission type	1 byte – Identifying characteristics of the transmission, can for instance contain codes on how payload is to be interpreted
Device type	1 byte - ID to identify the device type of the channel master (Ex: heart rate belt, temperature sensor etc.)
Device number	2 byte - Unique ID for this channel

Table 3. ANT channel ID

The channel configuration parameters are static, system parameters that must match in the master and slave, and the channel ID is included in all transmissions identifying the two nodes for each other. For in-depth details on each parameter please refer to *ANT Message Protocol and Usage*.

Network

In addition to setting the content of the channel ID, which is the primary ID of an ANT node, ANT nodes can limit their connectivity to a selection of other ANT nodes by defining a network for each ANT channel. The limited access to certain networks is managed through unique network keys

The defined ANT networks are:

1. **Public networks:** These are open ANT networks with no limitation on connectivity. All ANT nodes sharing the same channel configuration (by design or by accident) will be able to connect. This is the default setting in nRF24AP2.
2. **Managed networks:** These are ANT networks managed by special interest groups or alliances. An example is the ANT+ alliance for sport and wellness products. To join the ANT+ alliance, visit www.thisisant.com. By joining the ANT+ alliance and complying with the ANT+ device profiles set by the alliance, you achieve two goals:
   - Limited connectivity: Only other ANT+ compliant devices can connect to this channel.
   - Interoperability: Your node can connect to ANT+ compliant products from other vendors.
3. **Private networks:** Your own protected networks, and no other devices, will be able to connect to your ANT nodes unless you share the network key with someone outside the network. Please note that this requires purchase of a unique network key from ANT, see www.thisisant.com.

Since the network parameter can be chosen independently for each ANT channel, one ANT node (1 nRF24AP2-8CH) can have up to eight ANT channels, operating on different networks at the same time.

Note: The network parameter has no impact on the network topologies you can build. It is merely a tool to protect your ANT network and prevent accidental or deliberate access from other ANT nodes.

Channel ID, search and pairing

The primary parameters which two ANT nodes use to identify each other make up the **channel ID**. Once an ANT channel is established, the **channel ID parameters** must of course match; but they don't have to be known by both nodes (pre-configured) to be able to establish an ANT channel.

When an nRF24AP2 configured as a master (set in channel type) opens an ANT channel, it will broadcast its entire **channel ID**. Hence you must configure all three **channel ID parameters** before opening an ANT channel as a master.

On the other hand, in a slave you can configure nRF24AP2 to search for and connect with both known and unknown masters. To connect with a known master you must configure the **Transmission type**, **Device type** and **Device number** in nRF24AP2 before opening the ANT channel.

You can also configure the nRF24AP2 to conduct wild-card searches on one or more of the three parameters in the **channel ID** to enable it to pair up with unknown masters. You can for instance set only the **Device type** of the masters you want to link up with, and set wild cards on the **Transmission type** and **Device number**. If a new master with a matching **Device type** is found, the slave device will connect and store the unknown parts of the **channel ID**. The new parts of the **channel ID** can then be stored in the host MCU to enable specific searches for this master later.

4.2.4 Proximity search

When using the basic search and pairing algorithm a slave will automatically identify and connect to the first master it finds matching the search criteria. In areas where you either have a high density of similar master nodes or high density of independent ANT networks, there is always the chance that multiple masters are found within the coverage area. This presents the risk that it is not the master you wanted to connect to that is found first. The proximity search feature in ANT designates 'bins' of proximity from 1 (closest) to 10 (furthest) as shown in Figure 9.

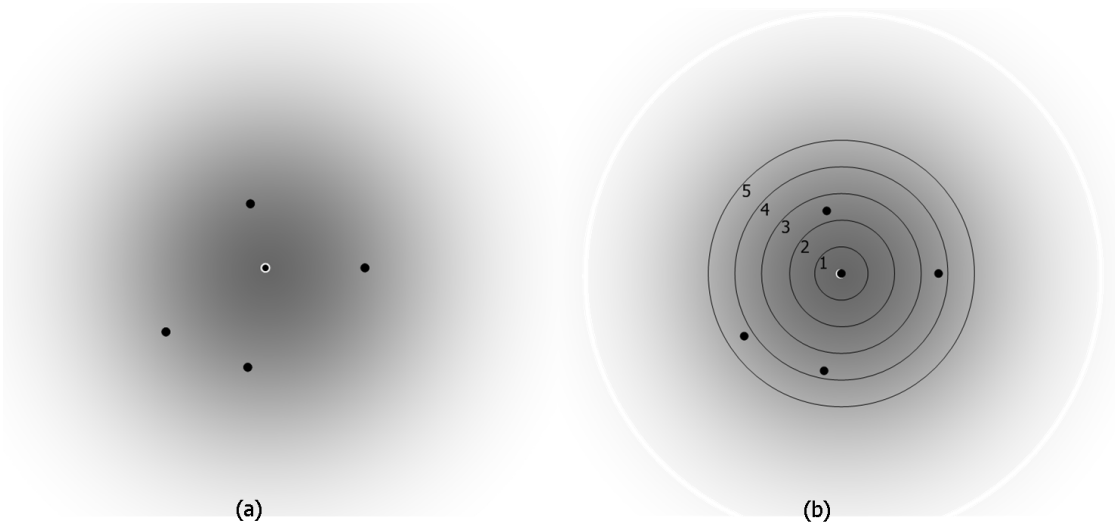


Figure 9. Standard search (a), Proximity search (b), showing bins 1-5 (of maximum 10)

This 'binning' enables you to further control your search by for instance only accepting the master that is closest (only accept masters that fall in bin 1-2). This makes it easy for a user to pair up network nodes and prevent accidental connection to nodes possibly belonging to another network close by.

4.2.5 Continuous scanning mode

Continuous scanning mode allows for fully asynchronous communication between an ANT node using continuous scanning mode, and any other ANT node using a standard master channel. This has two main advantages over only using standard ANT channels. The first is that the latency to initiate communication with the scanning node is reduced to zero and every message sent by a master channel in proximity will be received by the scanning device. Secondly, the requirement to maintain communication for the purpose of synchronization while in proximity is removed. This means that it is possible for nodes to come and go very quickly or to turn off for long periods of time in between communication events. This saves power on the transmitting node.

The disadvantage of continuous scanning mode is that it consumes much more power than standard ANT channels and will therefore only typically be used on devices that are plugged in and not mobile such as a computer (USB dongle). Another disadvantage is that a node in scanning mode can no longer be configured to have discoverable master channels because scanning mode disables standard ANT channel functionality. It is worth noting that two ANT nodes in scanning mode cannot communicate with one another because neither will be able to spontaneously generate communication.

Standard ANT channels are recommended over scanning channels, even in dynamic systems where devices are coming and going. This is because scanning channels are not recommended for mobile networks which is the primary area of application for ANT. Scanning channels will typically be used in statically located networks where the scanning channel node is plugged in and not mobile.

4.2.6 ANT network topologies

By combining ANT channels with different features depending on local needs, you can build anything from very simple peer-to-peer links and star networks to complex networks as shown in Figure 10. on page 21.

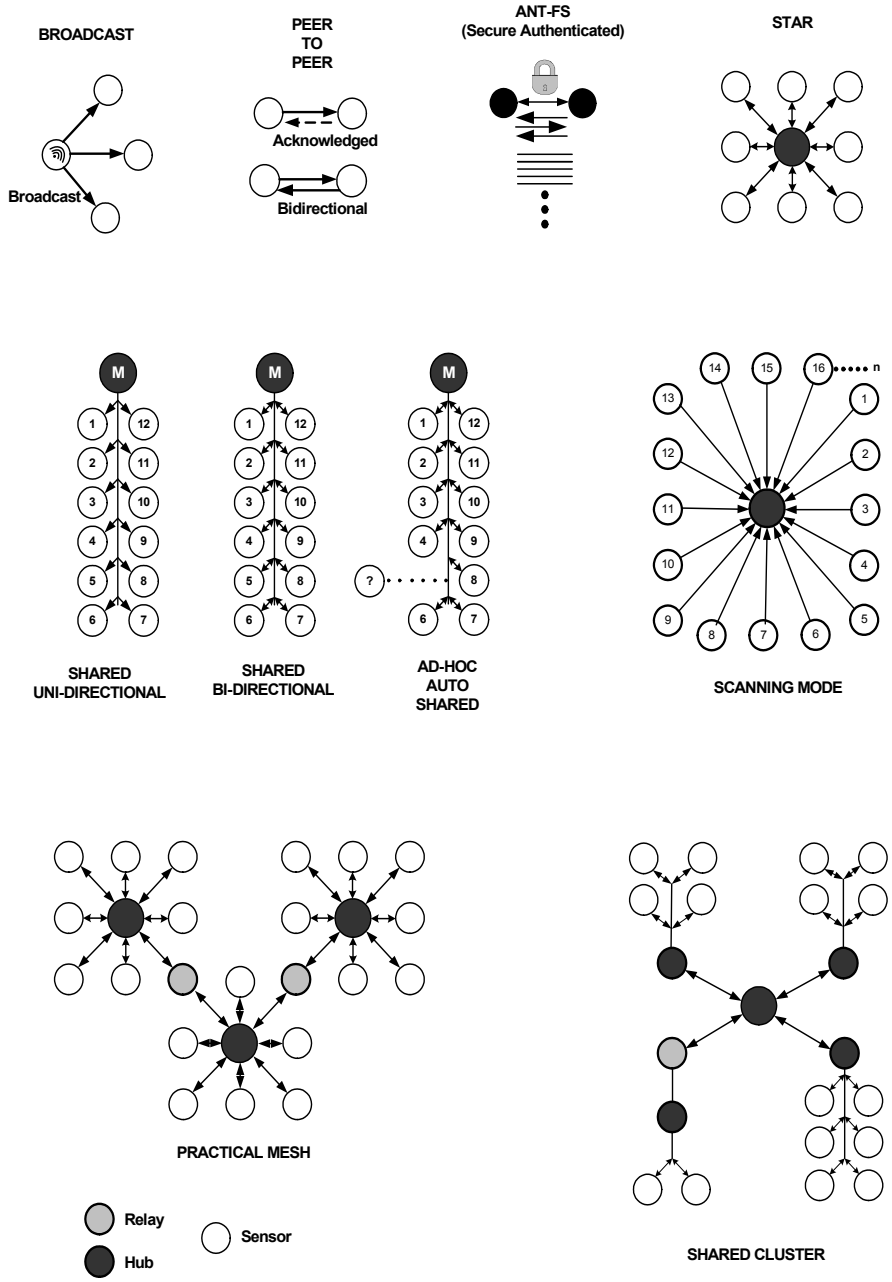


Figure 10. Network topology examples supported by ANT

4.2.7 ANT message protocol

All the configuration and control of the various ANT node and channel parameters in nRF24AP2 are handled by the host microcontroller over a simple serial interface by using the command library. See the document *ANT Message Protocol and Usage* for further details on the command library.

Class	Type	Commands in ANT command library	Reply	From
Config. messages	Unassign Channel	ANT_UnassignChannel()	Yes	Host
	Assign Channel	ANT_AssignChannel()	Yes	Host
	Channel ID	ANT_SetChannelId()	Yes	Host
	Channel Period	ANT_SetChannelPeriod()	Yes	Host
	Search Timeout	ANT_SetChannelSearchTimeout()	Yes	Host
	Channel RF Frequency	ANT_SetChannelRFFreq()	Yes	Host
	Set Network	ANT_SetNetworkKey()	Yes	Host
	Transmit Power	ANT_SetTransmitPower()	Yes	Host
	ID List Add	ANT_AddChannelID()[a]	Yes	Host
	ID List Config	ANT_ConfigList()[a]	Yes	Host
	Channel Transmit Power	ANT_SetChannelTxPower()	Yes	Host
	Low Priority Search Timeout	ANT_SetLowPriorityChannelSearchTimeout()	Yes	Host
	Enable Ext RX Mesgs	ANT_RxExtMesgsEnable()	Yes	Host
	Crystal Enable	ANT_CrystalEnable()	Yes	Host
	Frequency Agility	ANT_ConfigFrequencyAgility()	Yes	Host
	Proximity Search	ANT_SetProximitySearch()	Yes	Host
Notifications	Startup Message	→ ResponseFunc(-, 0x6F)	-	ANT
Control Messages	SystemReset	ANT_ResetSystem()	No	Host
	Open Channel	ANT_OpenChannel()	Yes	Host
	Close Channel	ANT_CloseChannel()	Yes	Host
	Open Rx Scan Mode	ANT_OpenRxScanMode()[a]	Yes	Host
	Request Message	ANT_RequestMessage()	Yes	Host
	Sleep Message	ANT_SleepMessage()	No	Host
Data Messages	Broadcast Data	ANT_SendBroadcastData() → ChannelEventFunc(Chan,EV)	No	Host/ANT
	Acknowledge Data	ANT_SendAcknowledgedData() → ChannelEventFunc(Chan, EV)	No	Host/ANT
	Burst Transfer Data	ANT_SendBurstTransferPacket() → ChannelEventFunc(Chan, EV)	No	Host/ANT
Channel Event Messages	Channel Response/ Event	→ ChannelEventFunc(Chan, MessageCode) or → ResponseFunc(Chan, MsgID)	-	ANT
Requested Response Messages	Channel Status	→ ResponseFunc(Chan, 0x52)	-	ANT
	Channel ID	→ ResponseFunc(Chan, 0x51)	-	ANT
	ANT Version	→ ResponseFunc(Chan, 0x51)	-	ANT
	Capabilities	→ ResponseFunc(-, 0x3E)	-	ANT
Test Mode	CW Init	ANT InitCWTestMode()	Yes	Host
	CW Test	ANT SetCWTestMode()	Yes	Host
Ext Data messages	Extended Broadcast Data	ANT SendExtBroadcastData()[b] → ChannelEventFunc(Chan, EV)	No	Host
	Extended Ack. Data	ANT SendExtAcknowledgedData()[b] → ChannelEventFunc(Chan, EV)	No	Host
	Extended Burst Data	ANT SendExtBurstTransferPacket()[b] → ChannelEventFunc(Chan, EV)	No	Host

a. This is only supported by the nRF24AP2-8CH.
b. nRF24AP2 does not send these ChannelEventFunctions() to the host. nRF24AP2 will send extended messages by appending the additional bytes to standard broadcast, acknowledged and burst data.

Table 4. ANT message summary supported by nRF24AP2

5 Host interface

The host microcontroller can configure and control all of the nRF24AP2 features through a simple serial interface. Three interface options are available, enabling both high and low end microcontrollers to be used.

5.1 Features

Serial interfaces supported by nRF24AP2:

- Asynchronous (UART)
  - Interface requires 5 pins to host microcontroller
  - Configurable baud rate from 4800 to 57600 baud
- Synchronous
  - Bit or byte flow
  - Interface requires 6 pins to host microcontroller

5.2 Asynchronous serial interface

The host MCU and nRF24AP2 may communicate using the asynchronous mode of the serial interface. Asynchronous mode is selected by the PORTSEL input being tied low.

5.2.1 Block diagram

The asynchronous serial interface between nRF24AP2 and the host MCU is shown in Figure 11.

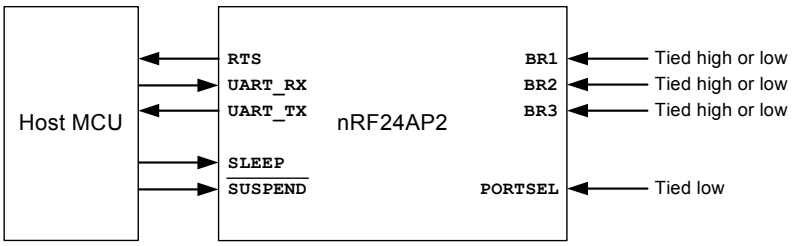


Figure 11. Asynchronous mode connections

The **UART** communication is for one start bit, one stop bit, 8 bits of data and no parity. Data is sent and received LSBit first.

5.2.2 Baud rate

The baud rate of the asynchronous communication between the host and ANT is controlled by the speed select signals **BR1**, **BR2** and **BR3**. Table 5. shows the relationship between the states of the speed select signals and the corresponding baud rates.

BR3	BR2	BR1	Baud rate
0	0	0	4800
0	1	0	19200
0	0	1	38400
0	1	1	50000
1	0	0	1200
1	1	0	2400
1	0	1	9600
1	1	1	57600

Table 5. Relationship between states of speed-select signals and corresponding baud rates

Note: The baud rate may have a significant impact on system current consumption. Refer to section 8.2 on page 46 for application-specific current consumption figures.

5.2.3 Asynchronous Port Control (RTS)

When nRF24AP2 is configured in asynchronous mode, a full duplex asynchronous serial port is provided with flow control for data transmission from the host to ANT. The flow control is performed by the **RTS** signal, which conforms to standard hardware flow control CMOS signal levels. The signal may therefore be attached to a computer serial port (with use of an RS-232 level shifter), or to any other RS-232 device. The RTS signal is de-asserted for approximately 50 µs after each correctly formatted message has been received. This **RTS** signal duration is independent of the baud rate. Incorrect messages or partial messages are not acknowledged.

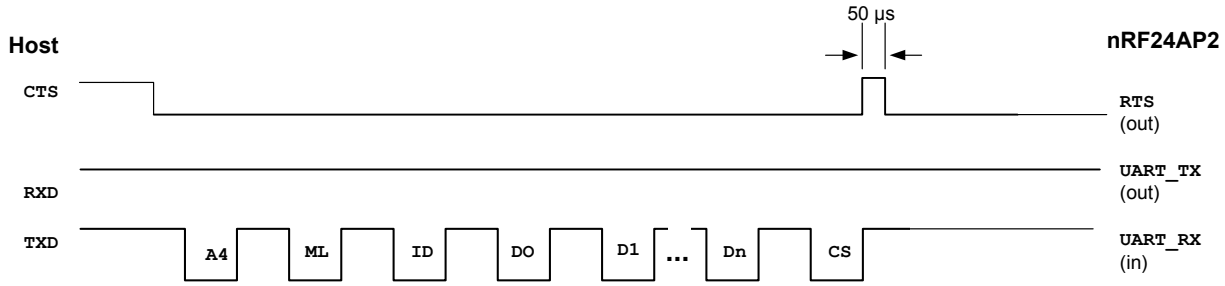


Figure 12. RTS signal following a serial host -> nRF24AP2 transfer

When nRF24AP2 raises the **RTS** signal high, the host MCU may not send any more data until the **RTS** signal is lowered again. There is no flow control for data being transmitted from nRF24AP2 to the host controller, and therefore the host controller must be able to receive data at any time. **RTS** is toggled following a reset.

The **RTS** signal is raised by nRF24AP2 after the last byte of a message has been received, and nRF24AP2 will therefore lose any bytes that were sent, or in the process of being sent, before the **RTS** signal is acted upon by the host MCU, and the transmission is halted. To avoid this problem, either the messages need to be spaced apart by the host MCU or 0-pad bytes need to be added to the end of each message being transmitted to handle whatever byte pipeline is in place. For example, when considering computer

communication, two 0-bytes must be appended to every message, since computers interpret CTS at the driver- rather than the hardware level.

nRF24AP2 will discard 0-pad bytes received. This issue usually occurs only when using burst transfers from the host to nRF24AP2 and high data rates are expected.

5.2.4 Sleep enable (SLEEP)

The **SLEEP** input signal allows nRF24AP2 to sleep when the serial port is not required. The signal is essential for conserving power when using the asynchrnous serial interface. This control mechanism is illustrated in Figure 13.

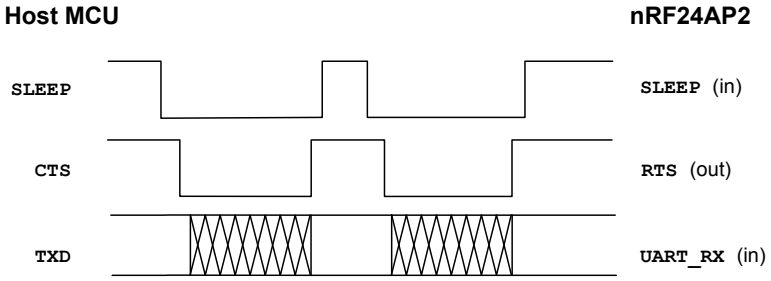


Figure 13. nRF24AP2 sleep control

If the **SLEEP** signal is not used, then it must be tied low. In this configuration, the nRF24AP2 will never sleep and will always be ready to receive data. The **SUSPEND** functionality cannot be used if the **SLEEP** signal is not used.

The **SLEEP** and **RTS** signals only affect the data being transferred from the host MCU to nRF24AP2. nRF24AP2 will send data to the host, when available, regardless of the state of these two signals.

5.2.5 Suspend mode control ($\overline{\text{SUSPEND}}$)

When using the asynchronous serial interface, you also have a $\overline{\text{SUSPEND}}$ signal available.The assertion of the $\overline{\text{SUSPEND}}$ signal will cause nRF24AP2 to terminate all RF and serial port activity and power down. This will happen immediately, regardless of the state of the nRF24AP2 system. This signal provides support for use in USB applications, where USB devices are required to quickly enter a low-power state through hardware control.

Entering and exiting from the suspend mode require the use of the **SLEEP** signal, in addition to the $\overline{\text{SUSPEND}}$ signal. The assertion of $\overline{\text{SUSPEND}}$ is only recognized if **SLEEP** is also asserted at the time. De-assertion of the **SLEEP** signal is the only method for exiting from suspend mode, as shown in Figure 14. on

page 26. Following exit, all previous transactions and configurations will be lost – nRF24AP2 will be in its power-up state.

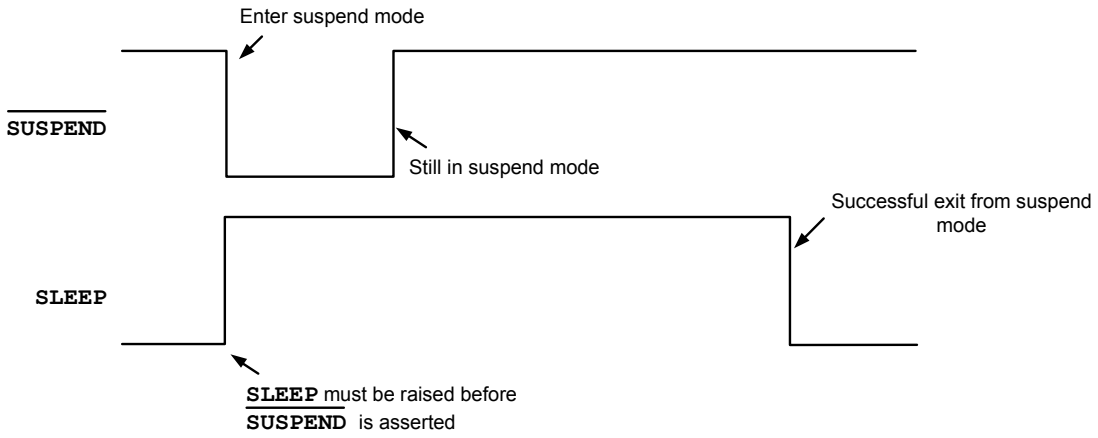


Figure 14. SUSPEND signal use

5.3 Synchronous serial interface

This section explains in detail the synchronous serial interface between nRF24AP2 and a host MCU. This mode is selected by connecting the **PORTSEL** input high.

When operating in synchronous mode, careful attention to reset behavior is required to prevent inadvertent deadlock conditions between nRF24AP2 and the host MCU.

In synchronous mode, nRF24AP2 uses a half-duplex synchronous master serial interface with message flow control. The host must be configured as a synchronous slave. The interface is meant to accommodate either a hardware synchronous slave port or a simple I/O control on the host MCU. The host MCU retains full control of the message flow and can halt incoming messages as required.

5.3.1 Block diagram

The synchronous serial interface between nRF24AP2 and the host MCU is shown in Figure 15. The **PORTSEL** signal should be connected to logic high for synchronous serial mode.

Figure 15. Synchronous mode connections

5.3.2 Flow Control Select (SFLOW)

The Flow Control Select signal is used to configure the synchronous serial port for either Byte or Bit flow control.

SFLOW	Flow control
0	Byte flow control
1	Bit flow control

Please note that Byte flow control assumes that the host contains synchronous communication hardware which can be configured for synchronous slave communication. Bit flow control can be used by all microcontrollers. It is especially useful for microcontrollers that offer no hardware serial interface, and which require the serial interface to be emulated in software on the host MCU. The differences between byte and bit flow control are detailed in the remaining sections of this chapter.

5.3.3 Synchronous interface handshaking

A basic description of the communications mechanism follows.

- The synchronous serial port provided by nRF24AP2 is a half-duplex synchronous master.
- Two handshake signals (**SEN**, **MRDY**) are used to set up communication.
- Being a master, the nRF24AP2 will forward all incoming radio messages to the host as they become available.
- The host must request the use of the serial port and get acknowledge from nRF24AP2 before a transaction can take place.
- **SRDY** enables flow control in both directions.
- The first byte in each message is always sent from the nRF24AP2 and indicates the direction of this message.

The steps needed to initiate synchronous message transfers in both directions are shown in Figure 16. on page 27.

5.3.3.1 Synchronization

In order for the host MCU to guarantee synchronization with nRF24AP2 in startup conditions, a reset sequence must be applied to nRF24AP2. This only applies to synchronous mode communication.

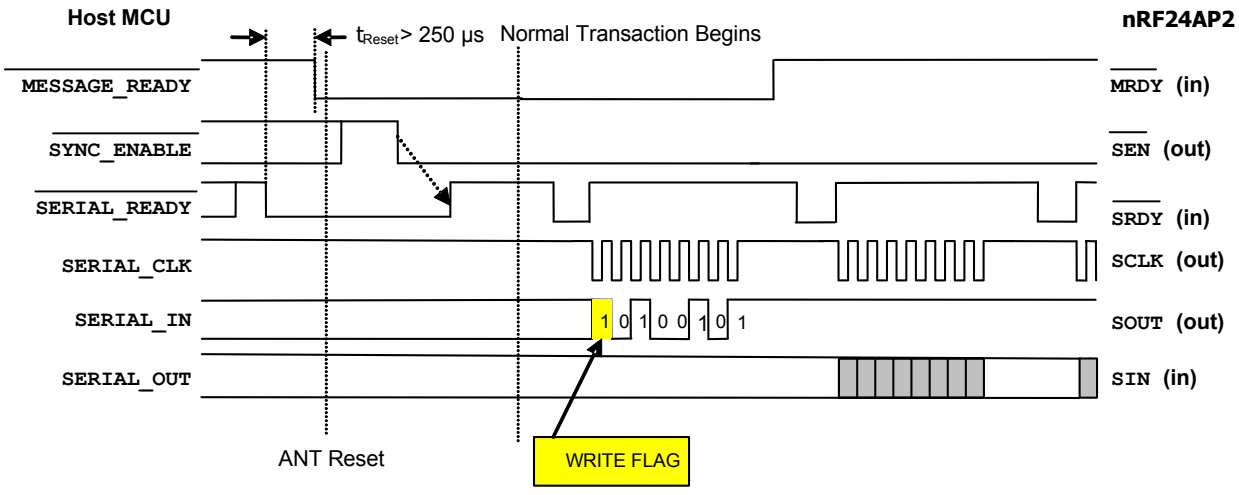


Figure 16. Synchronization with nRF24AP2 upon startup

5.3.3.2 Power up/power down

nRF24AP2 will automatically place itself into idle mode when all radio channels are closed and there is no activity on the **MRDY** input signal. The host MCU should ensure these conditions during times that the nRF24AP2 radio is not required in order to maximize product battery life. Upon every power up, the host must apply the Synchronous Reset sequence.

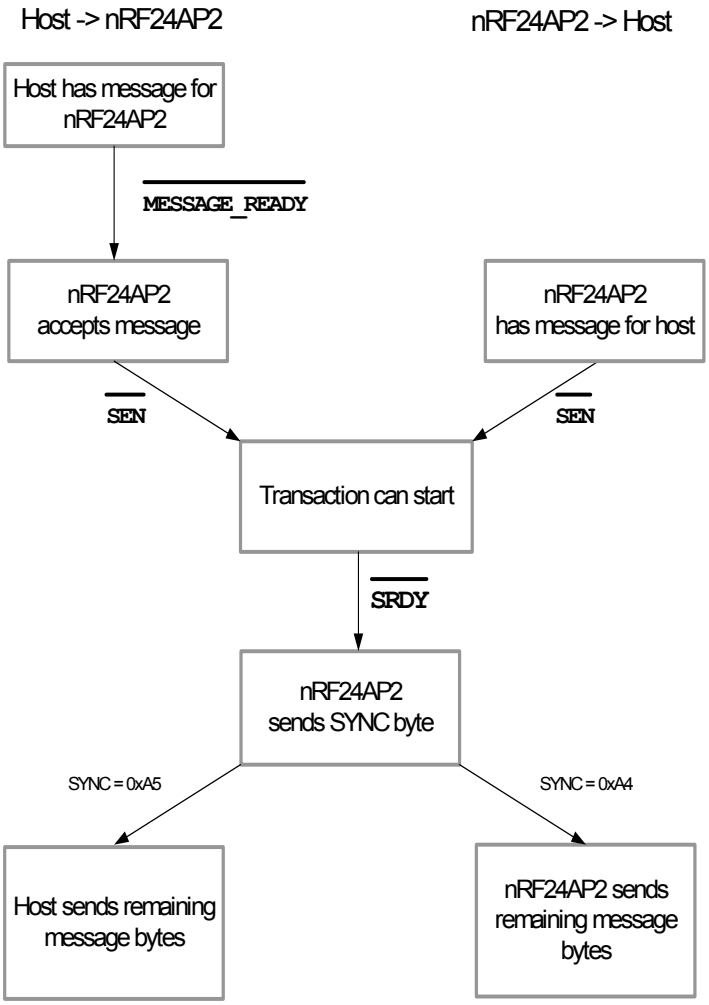


Figure 17. Synchronous serial communication

Figure 17. on page 28 and timing diagrams in Figure 18. on page 29 and Figure 19. on page 30 illustrate the basic, message transaction sequence:

For a message from host->nRF24AP2:

- The host will assert the **MRDY** signal indicating it has a message for the nRF24AP2.

For messages in either direction:

1. nRF24AP2 will assert **SEN** to indicate the start of a message transfer.
2. After **SEN** has been asserted, the host will assert **SRDY** to indicate it is ready for communication.
3. After **SEN** and **SRDY** are both asserted, nRF24AP2 **always** transmits the first (for example SYNC) byte. This is output from **SOUT**, and clocked with **SCLK** (see chapter 8 on page 40 for details of clock frequency). The LSB of the **SYNC** byte indicates the direction of the remaining message bytes (0 : Message Receive, nRF24AP2 → host; 1: Message Transmit, host → nRF24AP2).
4. If the **SYNC** byte indicates a message receive (nRF24AP2->host), the additional message bytes will be transmitted the same way as the **SYNC** byte.
5. If the **SYNC** byte indicates a message transmit (host->nRF24AP2), the host must output its data to nRF24AP2 **SIN** at the clock rate provided by nRF24AP2 **SCLK**.

Data is transmitted least-significant-bit (LSB) first.

5.3.4 Synchronous messaging with byte flow control

Byte flow-control mode is used when a synchronous hardware serial port is available.

The host MCU flow-control signal **SRDY** must be toggled for each byte and can either be implemented with a software controlled I/O line, or in some cases may be controlled by the host's hardware serial port. Data bits change state on the falling edge of **SCLK** and are read on the rising edge of **SCLK**. This is true for transactions in either direction.

The first byte in the transaction sequence is always sent from nRF24AP2 to the host MCU. The first bit of the first byte dictates the direction for the remaining bytes in the transaction.

Figure 18. on page 29 and Figure 19. on page 30 show transactions between the host and nRF24AP2 in byte synchronous mode.

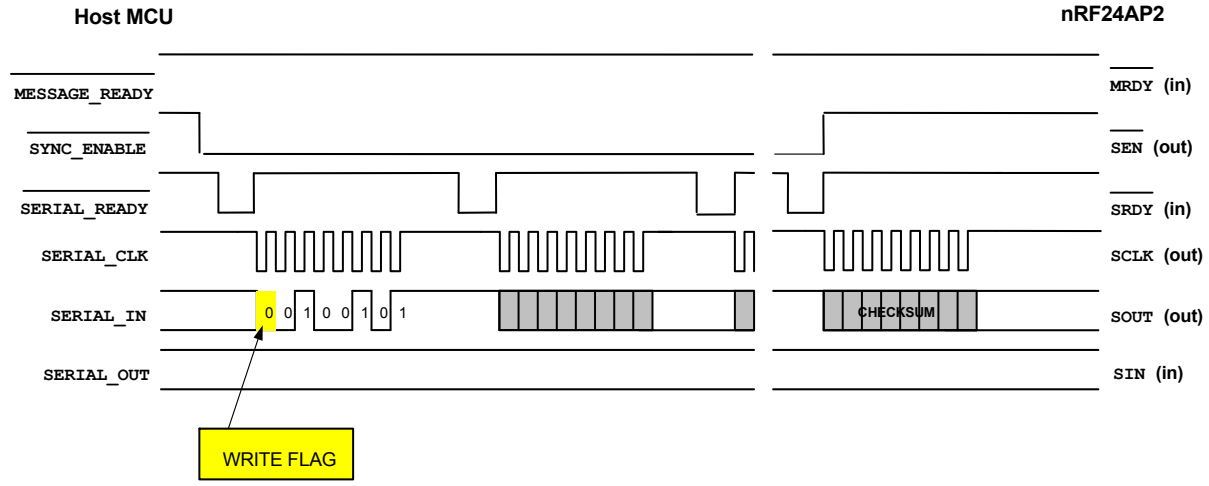


Figure 18. nRF24AP2 → host transaction

The nRF24AP2 asserts **SEN** and waits for the host to assert **SRDY** . Once both **SEN** and **SRDY** have been asserted, nRF24AP2 will send the SYNC byte from **SOUT**.

For hardware **SRDY** , this signal will be de-asserted on the first **SCLK** transition, if a software controlled I/O line is used for **SRDY**, it only needs to stay asserted for 2.5 µs minimum before the host can de-assert it again. The LSB of the SYNC byte will notify the host of the message direction (that is to say,

nRF24AP2 -> host), and once ready, the host will once again assert **SRDY** to receive the next message byte from nRF24AP2. After the last message byte, **SRDY** must remain de-asserted until the next message transaction is requested.

The process for nRF24AP2 to host transactions with software **SRDY** (Figure 21.) is very similar as for hardware **SRDY** . The sole difference is that the host can just pulse **SRDY** and does not have to wait until the first SCLK transition.

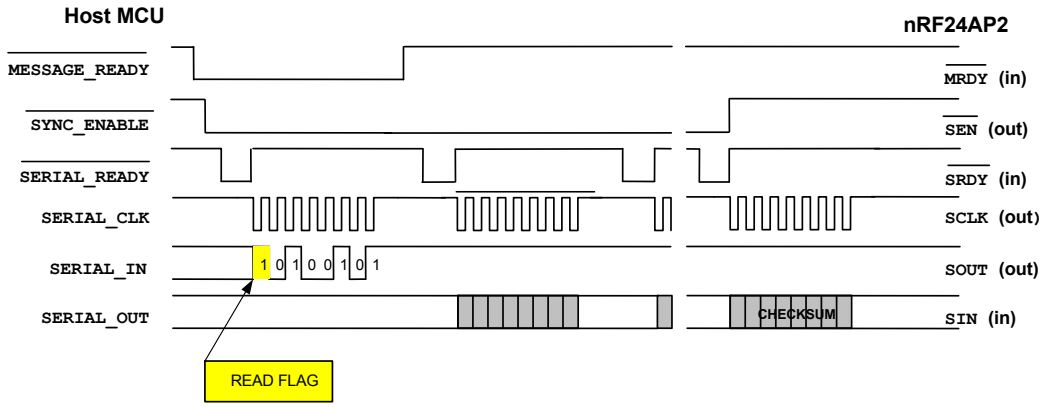


Figure 19. Host → nRF24AP2 transaction

For host to nRF24AP2 transactions with hardware **SRDY** (See Figure 19.) the process is very similar. The main difference is that the host first asserts **MRDY** to inform nRF24AP2 that it wished to send a message. nRF24AP2 will respond by asserting **SEN** and then waiting for the host to assert **SRDY** . Once both **SEN** and **SRDY** have been asserted, nRF24AP2 will the send the SYNC byte. For hardware **SRDY** , this signal will be de-asserted on the first **SCLK** transition. The first bit of the SYNC byte will notify the host of the message direction (meaning host-> nRF24AP2), and the host will once again assert **SRDY** and then send the next message byte to nRF24AP2 on host **SOUT** at the rate of **SCLK**. Again, the hardware **SRDY** will de-assert on the first **SCLK** transition and re-assert after each byte until the entire message has been transferred. After the last message byte, **SRDY** will remain de-asserted until the next message transaction is requested.

The process for host to nRF24AP2 transactions with software **SRDY** (See Figure 19.) is very similar as for hardware **SRDY** . The only difference is that the host can pulse **SRDY** and does not have to wait until the first **SCLK** transition.

5.3.5 Synchronous timing with byte flow control

Synchronous mode with byte flow is compatible with a host microcontroller, hardware SPI slave, configured as mode 3 and polarity 1. In Figure 20. signals to the left indicate pins on the host MCU. Signals on the right-hand side indicate pins on nRF24AP2. Shaded areas indicate “don’t care” values.

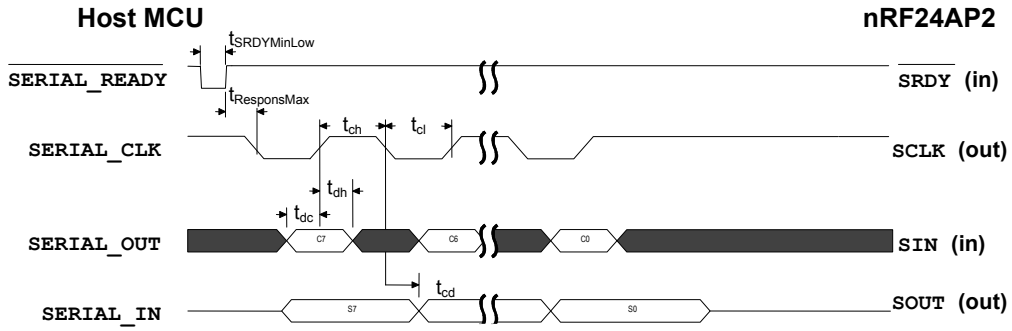


Figure 20. Synchronous byte flow timing

Symbol	Parameter (condition)	Notes	Min	Typ	Max	Units
$SCLK_{frequency}$	Synchronous clock frequency (byte mode)			500		kHz
t_{dc}	Data to SCK Setup (byte mode)		100			ns
t_{dh}	SCK to Data Hold (byte mode)		20			ns
t_{cd}	SCK to Data Valid (byte mode)				60	ns
t_{cl}	SCK Low Time (byte mode)		900	1000		ns
t_{ch}	SCK High Time (byte mode)		900	1000		ns
$t_{SRDY\ MinLow}$	Minimum $\overline{SRDY}$ low time		2.5			µs
t_{Reset}	Synchronous reset. $\overline{SRDY}$ falling edge to $\overline{MRDY}$ falling edge		250			µs
t_{POR}	Power on reset time (supply rise time not included)	a			2.0	ms
$t_{SoftReset}$	Software reset (synchronous reset suspend reset and reset command)	a			1.5	ms
$t_{ResponseMax}$	Time the nRF24AP2 will take to respond to input signal				1.0	ms

a. Defines the time before the host MCU can start to configure the nRF24AP2 after a reset.

Table 6. Synchronous serial timing

5.3.6 Synchronous messaging with bit flow control

If no hardware serial port is available on the host MCU, nRF24AP2 can still be controlled using bit flow control. Using this method, the serial lines are implemented with software controlled I/O lines. All of the signaling at the message transaction level remains the same as above. However, instead of pulsing after every byte, $\overline{SRDY}$ is pulsed for each bit of the message as shown below in Figure 21. on page 32.

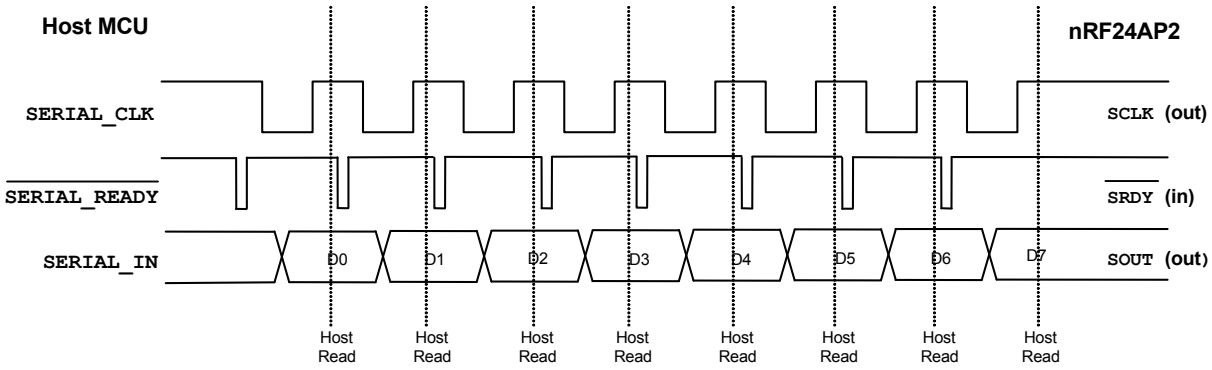


Figure 21. nRF24AP2 → host transaction

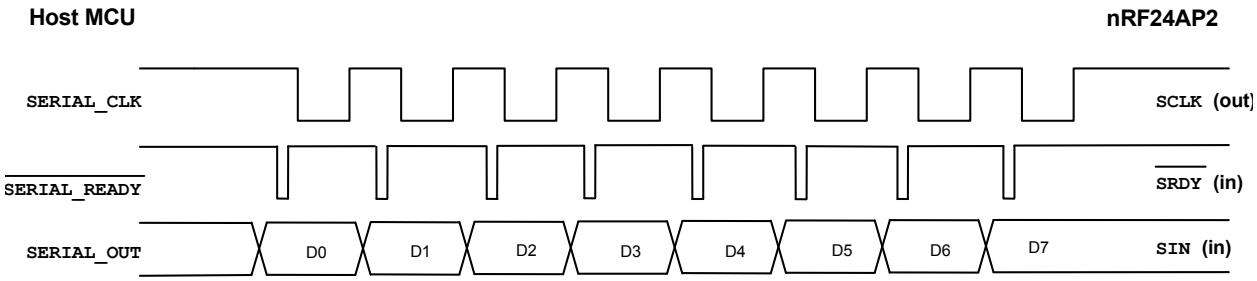


Figure 22. Host → nRF24AP2 transaction

It is important to note that the host MCU will do all bit processing on the rising edge of the **SCLK** signal, with the exception being when the byte is being transmitted from the host MCU to nRF24AP2, where the first data bit will need to be asserted prior to the first clock edge. The final rising edge of the byte transaction will be the event to drive byte processing.

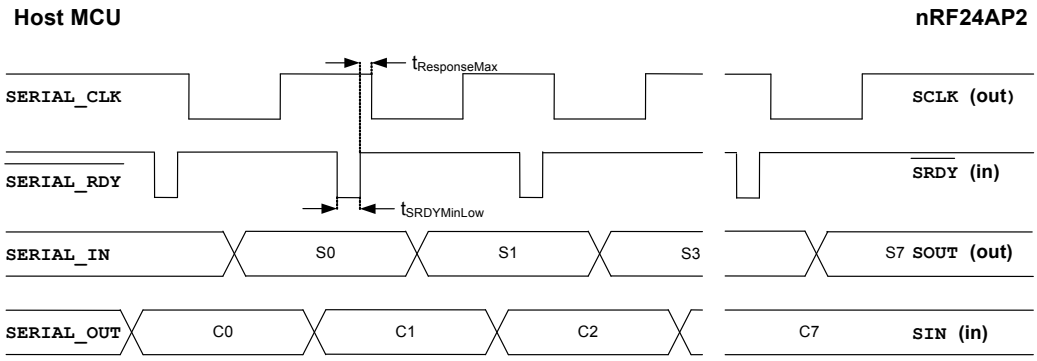


Figure 23. Synchronous bit flow timing

5.3.7 Serial enable control

The $\overline{\text{SEN}}$ signal will be asserted by nRF24AP2 prior to all message transmissions. It can therefore be used as a serial port enable signal, which is useful in cases where the host serial port requires hardware activation.

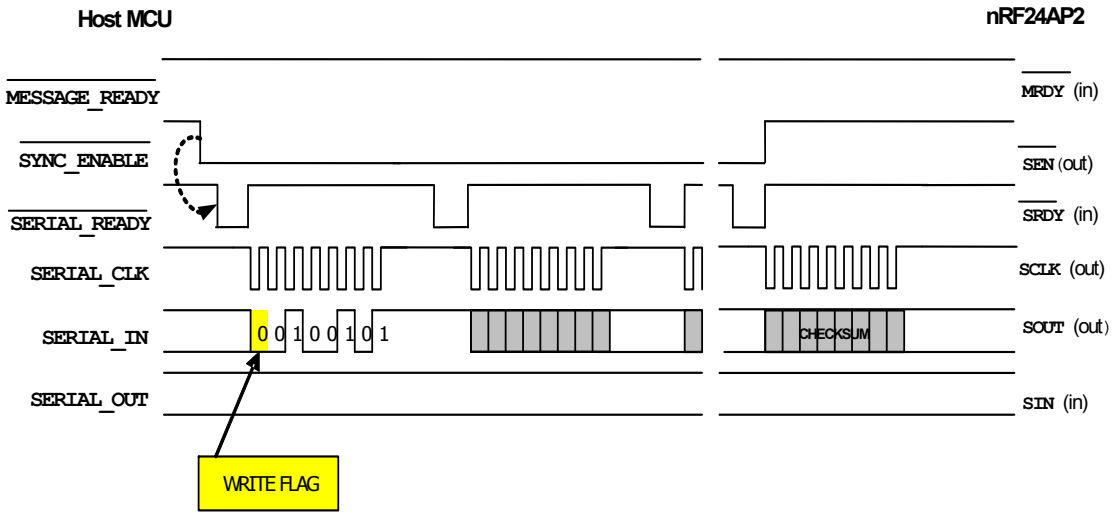


Figure 24. Serial enable control using nRF24AP2

6 On-chip oscillator

In order to provide the necessary clocks for the ANT protocol stack, nRF24AP2 contains one high frequency oscillator used by the RF transceiver. and two optional low frequency oscillators for ANT protocol timing. The mandatory, high frequency clock source must be a 16 MHz crystal oscillator. The low frequency clock source can be generated by a 32.768 kHz crystal oscillator or synthesized 32.768 kHz from the 16 MHz crystal oscillator clock. External 16 MHz and 32.768 kHz clocks may also be used instead of the on-chip oscillators of nRF24AP2. For ultra low-power applications, we recommend you use the 32.768 kHz crystal oscillator or provide a 32.768 kHz clock signal, to achieve the lowest possible current consumption.

6.1 Features

- Low-power, amplitude regulated 16 MHz crystal oscillator
- Ultra low-power amplitude regulated 32.768 kHz crystal oscillator
- Low power, synthesized 32.768 kHz clock from the 16 MHz crystal oscillator

6.2 Block diagrams

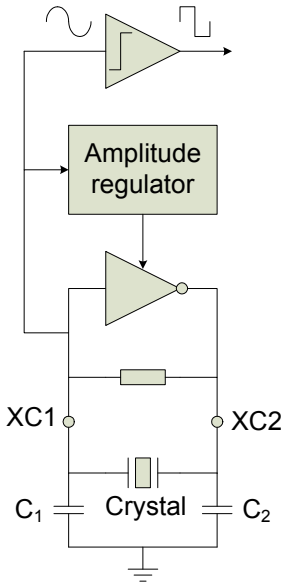


Figure 25. Block diagram of 16 MHz crystal oscillator

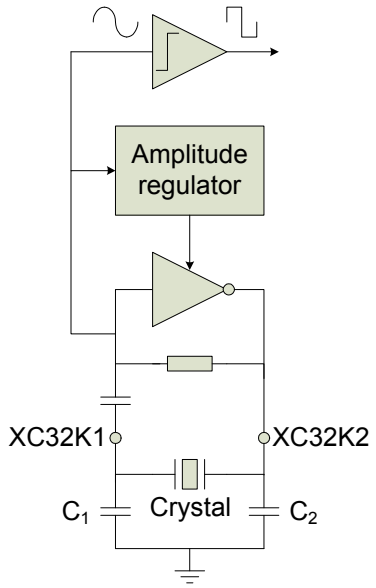


Figure 26. Block diagram of 32.768 kHz crystal oscillator

6.3 Functional description

6.3.1 16 MHz crystal oscillator

The 16 MHz crystal oscillator is designed to be used with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency it is very important that the load capacitance matches the specification in the crystal datasheet. The load capacitance is the total capacitance from the perspective of the crystal across its terminals:

$$C_{LOAD} = \frac{C_1' \cdot C_2'}{C_1' + C_2'}$$

$$C_1' = C_1 + C_{PCB1} + C_{PIN}$$

$$C_2' = C_2 + C_{PCB2} + C_{PIN}$$

C_1 and C_2 are ceramic SMD capacitors connected between each crystal terminal and VSS, C_{PCB1} and C_{PCB2} are stray capacitances on the PCB, while C_{PIN} is the input capacitance on the **XC1** and **XC2** pins of nRF24AP2 (typically 1pF). C_1 and C_2 should be of the same value, or as close as possible.

To ensure a functional radio link the frequency accuracy must be ± 50 ppm or better. The initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance must all be taken into account. For reliable operation the crystal load capacitance, shunt capacitance, equivalent series resistance (ESR) and drive level must comply with the specifications in Table 9. on page 42. It is recommended to use a crystal with lower than maximum ESR if the load capacitance and/or shunt capacitance is high. This will give faster start-up and lower current consumption.

The start-up time is typically about 1 ms for a crystal with 9pF load capacitance and an ESR specification of 60Ω max. This value is valid for crystals in a 3.2×2.5 mm can. If you use the smallest crystal cans (like 2.0×2.5 mm), pay particular attention to the start-up time of the crystal. These crystals have a longer start

up than crystals in larger cans. To make sure the start-up time is <1.24 ms use a crystal for load capacitance of 6pF. A low load capacitance will reduce both start-up time and current consumption.

For more details regarding how to measure the start up of a specific crystal, please see the nAN24-13 application note. This application note describes measurements on the nRF24LE1, which has an equal crystal oscillator. The start-up time must be measured to <1.5 ms in this setup since it includes a debounce time of 256 µs.

6.3.2 External 16 MHz clock

nRF24AP2 may be used with an external 16 MHz clock applied to the **XC1** pin. The input signal must be analog, coming from the crystal oscillator of a microcontroller, for example. An input amplitude of 0.8V peak-to-peak or higher is recommended to achieve low current consumption and a good signal-to-noise ratio. The DC level is not important as long as the applied signal never rises above VDD or drops below VSS. The **XC1** pin will load the microcontroller's crystal with approximately 1pF in addition to PCB routing. **XC2** shall not be connected.

Note: A frequency accuracy of ±50 ppm or better is required to achieve device performance as outlined in chapter 8 on page 40.

6.3.3 32.768 kHz crystal oscillator

The crystal must be connected between port pins **XC32K2** and **XC32K1**. To achieve correct oscillation frequency it is important that the load capacitance matches the specification in the crystal datasheet. The load capacitance is the total capacitance seen by the crystal across its terminals:

$$C_{LOAD} = \frac{C_1^{'} \cdot C_2^{'}}{C_1^{'} + C_2^{'}}$$

$$C_1^{'} = C_1 + C_{PCB1} + C_{PIN}$$

$$C_2^{'} = C_2 + C_{PCB2} + C_{PIN}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and VSS, CPCB1 and CPCB2 are stray capacitances on the PCB, while CPIN is the input capacitance on the **XC32K2** and **XC32K1** pins of nRF24AP2. C1 and C2 should be of the same value, or as close as possible. The oscillator uses an amplitude regulated design similar to the 16 MHz crystal oscillator. For reliable operation the crystal load capacitance, shunt capacitance, equivalent series resistance (ESR) and drive level must comply with the specifications in Table 9. on page 42.

It is recommended to use a crystal with lower than maximum ESR if the load capacitance and/or shunt capacitance is high. This will give faster start-up and lower current consumption.

Note: A frequency accuracy of ± 50 ppm or better is required to get reliable ANT functionality. The ANT_CrystalEnable() must be executed in order to enable external, crystal oscillator.

6.3.4 Synthesized 32.768 kHz clock

The low frequency clock can also be synthesized from the 16 MHz crystal oscillator clock. This saves the cost of a crystal but increases average power consumption. The synthesized clock is enabled by connecting **XC32K1** to VSS and leaving **XC32K2** unconnected.

6.3.5 External 32.768 kHz clock

nRF24AP2 may be used with an external 32.768 kHz clock applied to the **XC32K1** port pin. The external clock must be a rail-to-rail digital signal. **XC32K2** must not be connected.

Note: A frequency accuracy of ±50 ppm or better is required to get reliable ANT functionality. The ANT_CrystalEnable() must be executed in order to enable external, clock.

7 Operating conditions

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage		1.9	3.0	3.6	V
t_{R_VDD}	Supply rise time (0V to 1.9V)	a	1 µs		50 ms	
T_A	Operating temperature		-40		+85	°C

a. The power-on reset circuitry may not function properly for rise times outside the specified interval.

Table 7. Operating conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Unit
	16 MHz crystal					
f_{NOM}	Nominal frequency (parallel resonant)			16.000		MHz
f_{TOL}	Frequency tolerance	a			±50	ppm
C_L	Load capacitance			9	16	pF
C_0	Shunt capacitance			3	7	pF
ESR	Equivalent series resistance			50	100	Ω
P_D	Drive level				100	µW
T_{START}	Required 16 MHz oscillator startup time	b			1.24	ms
	Bias resistor (IREF pin to GND)					
Rref	Resistance			22		kΩ
Rrefacc	Tolerance				1	%
	32.768 kHz crystal					
f_{TOL}	Frequency tolerance				±50	ppm
f_{NOM}	Crystal frequency (parallel resonant)			32.768		kHz
C_L	Load capacitance			9	12.5	pF
C_0	Shunt capacitance			1	2	pF
ESR	Equivalent series resistance			50	80	kΩ
P_D	Drive level				1	µW

a. Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance.
b. Crystal oscillator start up time must not exceed 1.24 ms. Please see section 6.3 on page 35.

Table 8. External circuitry specification

8 Electrical specifications

This section contains electrical and timing specifications.

Conditions: VDD = 3.0V, T_A = –40ºC to +85ºC (unless otherwise noted)

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	General RF conditions					
f_{OP}	Operating frequency	a	2400	2403-2480	2483.5	MHz
PLL_{res}	PLL Programming resolution			1		MHz
f_{XTAL}	Crystal frequency			16		MHz
Δf	Frequency deviation			±160		kHz
R_{GFSK}	Air data rate	b		1000		kbps
$F_{CHANNEL}$	Non-overlapping channel spacing	c		1		MHz
	Transmitter operation					
P_{RF}	Maximum output power	d		0	+4	dBm
P_{RFC}	RF power control range		16	18	20	dB
P_{RFCR}	RF power accuracy				±4	dB
P_{BW1}	20dB bandwidth for modulated carrier			950	1100	kHz
$P_{RF1.1}$	1^{st} Adjacent Channel Transmit Power 1 MHz				-20	dBc
$P_{RF2.1}$	2^{nd} Adjacent Channel Transmit Power 2 MHz				-40	dBc
	Receiver operation					
RX_{MAX}	Maximum received signal at < 0.1% BER			0		dBm
RX_{SENS}	Sensitivity (0.1% BER)			-85		dBm
RX selectivity according to ETSI EN 300 440-1 V1.3.1 (2001-09) page 27						
C/I_{CO}	C/I co-channel			9		dBc
C/I_{1ST}	1^{st} ACS, C/I 1 MHz			8		dBc
C/I_{2ND}	2^{nd} ACS, C/I 2 MHz			-20		dBc
C/I_{3RD}	3^{rd} ACS, C/I 3 MHz			-30		dBc
C/I_{Nth}	N^{th} ACS, C/I f_i > 6 MHz			-40		dBc
C/I_{Nth}	N^{th} ACS, C/I f_i > 25 MHz			-47		dBc
RX selectivity with nRF24AP2 equal modulation on interfering signal (Pin = -67dBm for wanted signal)						
C/I_{CO}	C/I co-channel			12		dBc
C/I_{1ST}	1^{st} ACS, C/I 1 MHz			8		dBc
C/I_{2ND}	2^{nd} ACS, C/I 2 MHz			-21		dBc
C/I_{3RD}	3^{rd} ACS, C/I 3 MHz			-30		dBc
C/I_{Nth}	N^{th} ACS, C/I f_i > 6 MHz			-40		dBc
C/I_{Nth}	N^{th} ACS, C/I f_i > 25 MHz			-50		dBc
RX intermodulation performance in line with *Bluetooth* specification version 2.0, 4^{th} November 2004, page 42						
P_IM(3)	Input power of IM interferers at 3 and 6 MHz distance from wanted signal	e		-36		dBm
P_IM(4)	Input power of IM interferers at 4 and 8 MHz distance from wanted signal	g		-36		dBm
P_IM(5)	Input power of IM interferers at 5 and 10 MHz distance from wanted signal	g		-36		dBm

a. Usable band is determined by local regulations.
b. Data rate in each burst on-air.

c. The minimum channel spacing is 1 MHz.
d. Antenna load impedance = 15 Ω + j88 Ω.
e. Wanted signal level at Pin=64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is unmodulated, the other interferer is modulated equal to the wanted signal. The input power of interferers where the sensitivity equals BER=0.1% is presented.

Table 9. Transceiver characteristics

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		0.7×VDD		VDD	V
V_{IL}	Input low voltage		VSS		0.3×VDD	V
V_{OH}	Output high voltage (I_{OH}=0.5mA)		VDD-0.3		VDD	V
V_{OL}	Output low voltage (I_{OH}=0.5mA)		VSS		0.3	V

Table 10. Digital inputs/outputs

8.1 Current consumption

The power nRF24AP2 consumes depends on the configuration of nRF24AP2, in specific what you use in the way of serial interface, channel period, master-slave operation and broadcast-, acknowledge- or burst data.

Table 11. shows peak- and base current consumption for typical applications.

Conditions: VDD = 3.0V, TA = +25ºC

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
$I_{DeepSleep}$	Deep Sleep Command			0.5		µA
I_{Idle}	No active channels—no communications			2.0		µA
$I_{Suspend}$	Asynchronous suspend activated			2.0		µA
I_{Base_32kXO}	Base active current (32.768 kHz crystal oscillator or 32.768 kHz external clock source)			3.0		µA
$I_{Base_32kSynt}$	Base active current (synthesized 32.768 kHz from 16 MHz)			87		µA
I_{Search}	Search current			2.8		mA
I_{PeakRX}	Peak RX Current	a b		17		mA
I_{PeakTX}	Peak TX Current at 0 dBm	b c		15		mA
$I_{PeakTX-6}$	Peak TX Current at -6 dBm	b c		13		mA
$I_{PeakTX-12}$	Peak TX Current at -12 dBm	b c		12		mA
$I_{PeakTX-18}$	Peak TX Current at -18 dBm	b c		11		mA

a. Time of Maximum Current consumption in RX is typical 500 µs and maximum 1 ms.
b. Peak value is typically 1mA higher in asynchronous mode at 57600 baud.
c. Time of maximum TX Only Current is typical 300 µs and maximum 350 µs.

Table 11. Peak- and base current consumption for nRF24AP2

Table 12. shows average current consumption for typical applications and interfaces.

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
$I_{Msq_Rx_ByteSync}$	Average current per Rx message in byte sync mode			21		µA
$I_{Msq_Rx_BitSync}$	Average current per Rx message in bit sync mode			30		µA
$I_{Msg_Rx_57600}$	Average current per Rx message in async mode at 57600 baud			22		µA
$I_{Msg_Rx_50000}$	Average current per Rx message in async mode at 50000 baud			25		µA
$I_{Msg_Rx_38400}$	Average current per Rx message in async mode at 38400 baud			31		µA
$I_{Msg_Rx_19200}$	Average current per Rx message in async mode at 19200 baud			40		µA
$I_{Msg_Rx_9600}$	Average current per Rx message in async mode at 9600 baud			65		µA
$I_{Msg_Rx_4800}$	Average current per Rx message in async mode at 4800 baud			115		µA

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
$I_{Msg_TxAck_ByteSync}$	Average current per Acknowledged Tx message in byte sync mode			35		µA
$I_{Msg_TxAck_BitSync}$	Average current per Acknowledged Tx message in bit sync mode			48		µA
$I_{Msg_TxAck_57600}$	Average current per Acknowledged Tx message at 57600 baud			54		µA
$I_{Msg_TxAck_50000}$	Average current per Acknowledged Tx message at 50000 baud			52		µA
$I_{Msg_TxAck_38400}$	Average current per Acknowledged Tx message at 38400 baud			58		µA
$I_{Msg_TxAck_19200}$	Average current per Acknowledged Tx message at 19200 baud			72		µA
$I_{Msg_TxAck_9600}$	Average current per Acknowledged Tx message at 9600 baud			112		µA
$I_{Msg_TxAck_4800}$	Average current/Acknowledged Tx message at 4800 baud			192		µA
$I_{Msg_RxAck_ByteSync}$	Average current/Acknowledged Rx message in byte sync mode			26		µA
$I_{Msg_RxAck_BitSync}$	Average current/Acknowledged Rx message in bit sync mode			36		µA
$I_{Msg_RxAck_57600}$	Average current/Acknowledged Rx message at 57600 baud			28		µA
$I_{Msg_RxAck_50000}$	Average current/Acknowledged Rx message at 50000 baud			29		µA
$I_{Msg_RxAck_38400}$	Average current/Acknowledged Rx message at 38400 baud			35		µA
$I_{Msg_RxAck_19200}$	Average current/Acknowledged Rx message at 19200 baud			44		µA
$I_{Msg_RxAck_9600}$	Average current/Acknowledged Rx message at 9600 baud			69		µA
$I_{Msg_RxAck_4800}$	Average current/Acknowledged Rx message at 4800 baud			120		µA
$I_{Msg_Tx_ByteSync}$	Average current/Tx-only message in byte sync mode	a		17		µA
$I_{Msg_Tx_BitSync}$	Average current/Tx-only message in bit sync mode	a		32		µA
$I_{Msg_Tx_57600}$	Average current/Tx-only message in async mode at 57600 baud	a		32		µA
$I_{Msg_Tx_50000}$	Average current/Tx-only message in async mode at 50000 baud	a		28		µA
$I_{Msg_Tx_38400}$	Average current/Tx-only message in async mode at 38400 baud	a		34		µA
$I_{Msg_Tx_19200}$	Average current/Tx-only message in async mode at 19200 baud	a		50		µA
$I_{Msg_Tx_9600}$	Average current/Tx-only message in async mode at 9600 baud	a		90		µA
$I_{Msg_Tx_4800}$	Average current/Tx-only message in async mode at 4800 baud	a		170		µA

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
$I_{Msg_TR_ByteSync}$	Average current/Tx message in byte sync mode			27		µA
$I_{Msg_TR_BitSync}$	Average current/Tx message in bit sync mode			42		µA
$I_{Msg_TR_57600}$	Average current/Tx message in async mode at 57600 baud			42		µA
$I_{Msg_TR_50000}$	Average current/Tx message in async mode at 50000 baud			40		µA
$I_{Msg_TR_38400}$	Average current/Tx message in async mode at 38400 baud			45		µA
$I_{Msg_TR_19200}$	Average current/Tx message in async mode at 19200 baud			60		µA
$I_{Msg_TR_9600}$	Average current/Tx message in async mode at 9600 baud			100		µA
$I_{Msg_TR_4800}$	Average current/Tx message in async mode at 4800 baud			180		µA
I_{Ave}	Broadcast Tx at 0.5 Hz in byte sync mode	b		14		µA
I_{Ave}	Broadcast Tx at 2 Hz in byte sync mode	b		54		µA
I_{Ave}	Broadcast Rx at 0.5 Hz in byte sync mode	b		11		µA
I_{Ave}	Broadcast Rx at 2 Hz in byte sync mode	b		42		µA
I_{Ave}	Acknowledged TX at 0.5 Hz in byte sync mode	b		18		µA
I_{Ave}	Acknowledged TX at 2 Hz in byte sync mode	b		70		µA
I_{Ave}	Acknowledged RX at 0.5 Hz in byte sync mode	b		13		µA
I_{Ave}	Acknowledged RX at 2 Hz in byte sync mode	b		52		µA
I_{Ave}	Burst continuous at 20 kbps in byte sync mode			5.9		mA
I_{Ave}	Burst continuous at 7.5 kbps in bit sync mode			6.1		mA
I_{Ave}	Burst continuous at 20 kbps in async mode at 57600 baud			6.3		mA
I_{Ave}	Burst continuous at 20 kbps in async mode at 50000 baud			5.9		mA
I_{Ave}	Burst continuous at 13.8 kbps in async mode at 38400 baud			5.7		mA

a. Transmit only operation provides no ANT channel management across the air and is not recommended for normal operation.
b. Does not include base current. See I_{Ave} examples below.

Table 12. Average current consumption for typical applications and interfaces

8.2 Current calculations examples

By using the values in Table 12. on page 45 together with the formulas presented in this section, you can calculate the current consumption for a specific application setup. Channel period is defined as the number of data packets received or transmitted each second.

1. Master channel with Broadcast data at 0.5 Hz with a byte synchronous serial interface using a 32.768 kHz external clock source.

$$\begin{aligned} I_{Ave} &= (I_{Msg_TxByteSync} \times Message_Rate) + I_{Base_32kXO} \\ &= (\frac{17\,\mu A}{message} \times 0.5\,message) + 3\,\mu A \\ &= 12\,\mu A \end{aligned}$$

2. Receive channel with Acknowledged data at 2 Hz with an asynchronous serial interface at 57600 baud using a 32.768 kHz external clock source.

$$\begin{aligned} I_{Ave} &= (I_{Msg_RxAck_57600} \times Message_Rate) + I_{Base_32kXO} \\ &= (\frac{28\,\mu A}{message} \times 2\,messages) + 3\,\mu A \\ &= 59\,\mu A \end{aligned}$$

3. Transmit channel at 2 Hz with an asynchronous serial interface at 50000 baud using the internal clock source .

$$\begin{aligned} I_{Ave} &= (I_{Msg_TR_50000} \times Message_Rate) + I_{Base_32kSynt} \\ &= (\frac{40\,\mu A}{message} \times 2\,messages) + 87\,\mu A \\ &= 167\,\mu A \end{aligned}$$

9 Absolute maximum ratings

Maximum ratings are the extreme limits to which nRF24AP2 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Note: For operating conditions see Table 7. on page 38.

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	+3.6	V
VSS		0	V
I/O pin voltage			
V_{IO}	-0.3	VDD +0.3, max 3.6	V
Temperatures			
Operating temperature	-40	+85	°C
Storage temperature[a]	-40	+85	°C

a. The device can withstand up to 125°C for short periods without damage. Recommended long-time storage temperature <65°C.

Table 13. Absolute maximum ratings

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Attention!

Observe precaution for handling Electrostatic Sensitive Device.

HBM (Human Body Model): Class 1C

10 Mechanical specification

nRF24AP2 is packaged in the following QFN-package:

- QFN32 5 x 5 x 0.85 mm, 0.5 mm pitch.

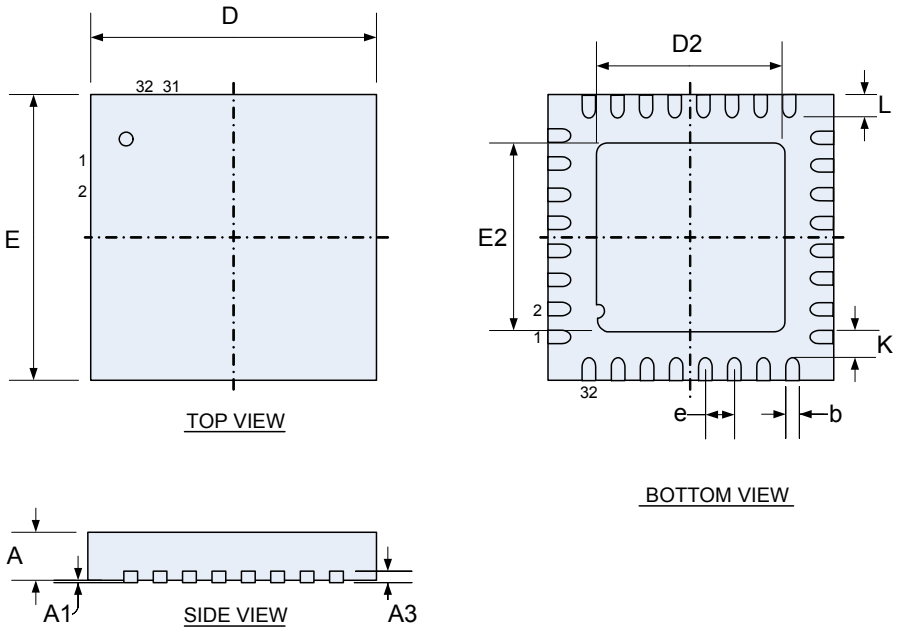


Figure 27. QFN32 pin 5x5mm

Package	A	A1	A3	b	D, E	D2, E2	e	K	L	
QFN32	0.80	0.00		0.18	4.9	3.50		0.20	0.35	Min
	0.85	0.02	0.20	0.25	5.0	3.60	0.5		0.40	Typ
	0.90	0.05		0.30	5.1	3.70			0.45	Max

Table 14. QFN32 dimensions in mm

11 Reference circuitry

To ensure optimal performance it is essential that you follow the schematics- and layout references closely. Especially in the case of the antenna matching circuitry (components between device pins **ANT1**, **ANT2**, **VDD_PA** and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50Ω single end antenna.

11.1 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality. A fully qualified RF-layout for the nRF24AP2 and its surrounding components, including matching networks, can be downloaded from www.nordicsemi.com.

A PCB with a minimum of two layers including a ground plane is recommended for optimal performance. The nRF24AP2 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics in Chapter 11 on page 49 for recommended decoupling capacitor values. The nRF24AP2 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long, power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF24AP2 I/C. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have Via holes as close as possible to the VSS pads. A minimum of one Via hole should be used for each VSS pin.

Full-swing digital data or control signals should not be routed close to the crystal or the power supply lines.

11.2 Synchronous (bit) mode schematics

Figure 28. shows that all interface signals are connected directly to I/O pins on the microcontroller. **SCLK** and **SEN** need to be on interrupt-capable I/O pins on the microcontroller. **RESET** allows optional control of the **RESET** signal by a microcontroller I/O pin.

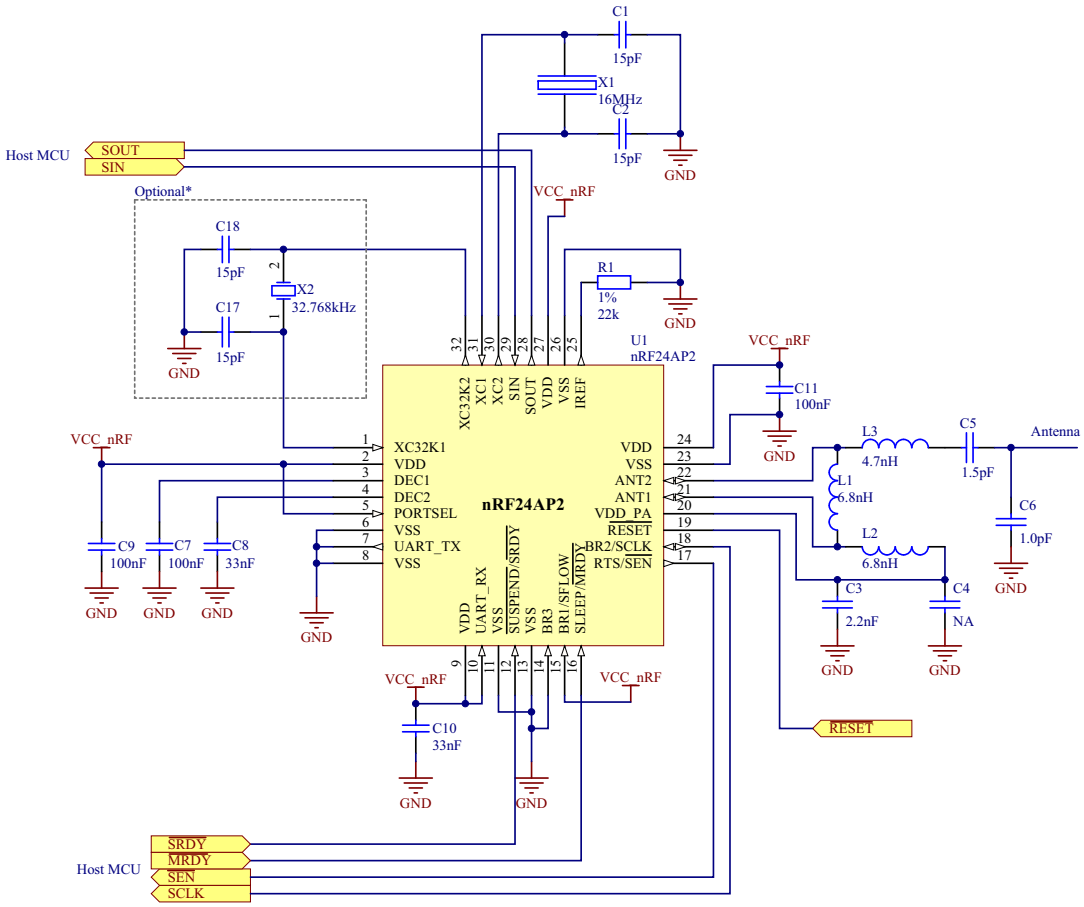
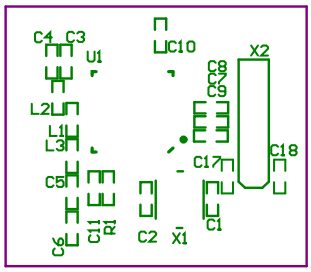


Figure 28. Synchronous (bit) mode schematic

*) For low-frequency oscillator options, refer to chapter 6 on page 34.

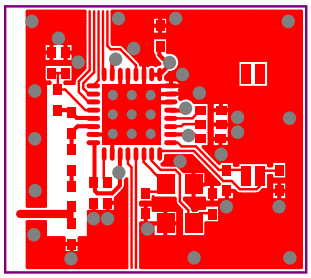
11.3 Layout



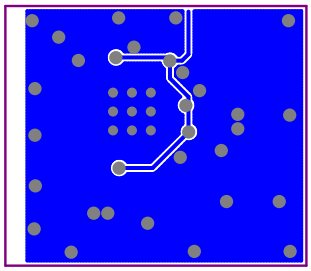
Top silk screen

No components

in bottom layer



Top view



Bottom view

Figure 29. Synchronous (bit) mode layout

11.4 Synchronous (byte) mode schematics

Figure 30. shows how the pins **SOUT** and **SIN** are connected directly to hardware **USART** (SPI) of the microcontroller. **SCLK** and **SEN** need to be on interrupt-capable I/O pins on the microcontroller. **RESET** allows optional control of the module **RESET** signal by a microcontroll I/O pin.

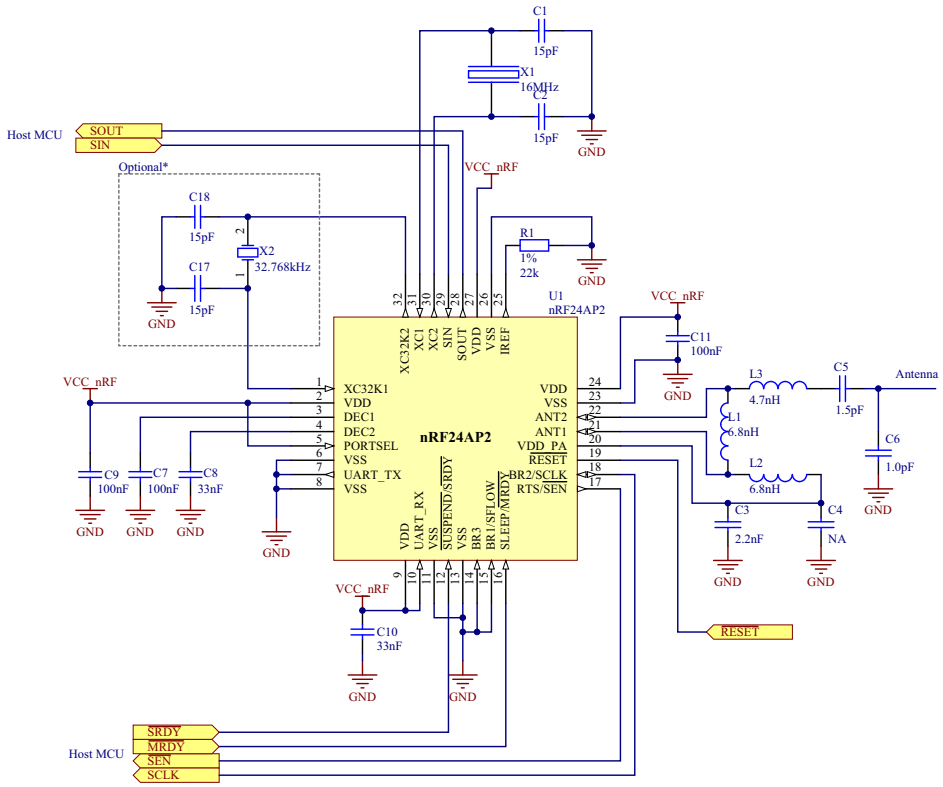
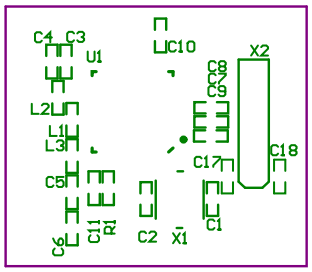


Figure 30. Synchronous (byte) mode schematic

*) For low-frequency oscillator options, refer to chapter 6 on page 34.

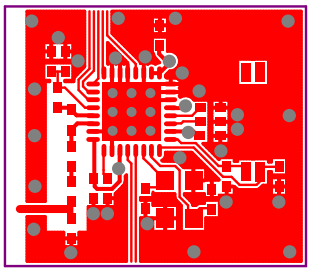
11.5 Layout



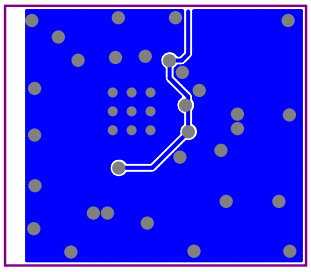
Top silk screen

No components

in bottom layer



Top view



Bottom view

Figure 31. Synchronous (byte) mode layout

11.6 Asynchronous mode schematics

Figure 32. shows that pins **UART_TX** and **UART_RX** are directly connected to hardware **USART** (UART) of the microcontroller. The illustrated baud rate selection pins (**BR1**, **BR2**, and **BR3**) define **UART** baud rate. The Baud rate selection pins may be connected directly to the logic level of interest. **RESET** allows optional control of the **RESET** signal by a microcontroller I/O pin.

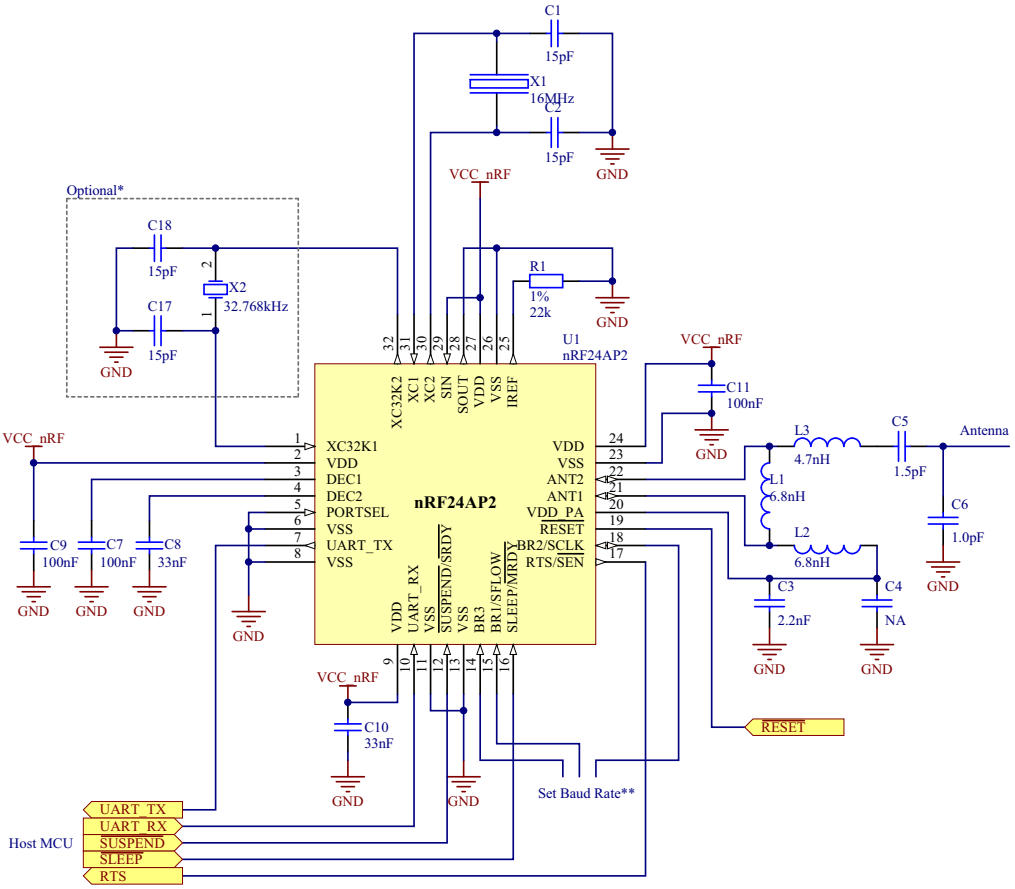
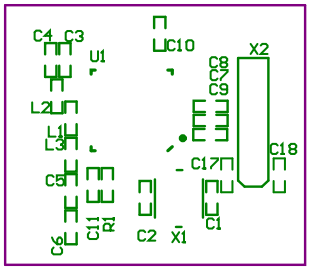


Figure 32. Asynchronous mode schematic

*) For low-frequency oscillation options, refer to chapter 6 on page 34.
**) Refer to Table 5 on page 24 for selectable baud rates.

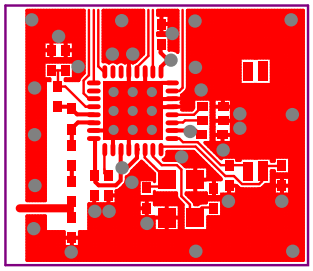
11.7 Layout

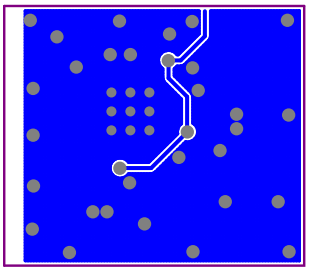


No components

in bottom layer

Top silk screen





Top view

Bottom view

Figure 33. Asynchronous mode layout

11.8 Bill Of Materials (BOM)

Please refer to the next table to see Bill of Materials for the schematics and layout presented in this document.

Designator	Value	Footprint	Comment
C1, C2, C17, C18	15pF	0402	NP0 ± 2%
C3	2.2nF	0402	X7R ± 10%
C4	Not mounted	0402	
C5	1.5pF	0402	NP0 ± 0.1pF
C6	1.0pF	0402	NP0 ± 0.1pF
C7, C9, C11	100nF	0402	X7R ± 10%
C8, C10	33nF	0402	X7R ± 10%
L1, L2	6.8nH	0402	High frequency chip inductor ± 5%
L3	4.7nH	0402	High frequency chip inductor ± 5%
R1	22 kΩ	0402	1%
U1	nRF24AP2	QFN32	QFN32 5×5 mm package
X1	16 MHz	3.2 × 2.5	SMD-3225, 16 MHz, CL=9pF, ±50 ppm
X2	32.768 kHz	7.0 × 1.5	32.768 kHz CL=9pF, ±50 ppm
PCB substrate	FR4 laminate	17.5 × 16	2-layer, 1.6 mm thickness

Table 15. Bill Of Materials

12 Ordering information

12.1 Package marking

N	R	F		B	X
2	4	A	P	2	Z
Y	Y	W	W	L	L

12.1.1 Abbreviations

Abbreviation	Definition
B	Build Code variable, that is, unique code for production sites, package type and test platform
X	"X" grade, that is, Engineering Samples (optional)
Z	Product identifier: O = nRF24AP2-1CH, E = nRF24AP2-8CH
YY	Two-digit year number
WW	Two-digit week number
LL	Two-letter wafer-lot number code

Table 16. Abbreviations

12.2 Product options

12.2.1 RF silicon

Ordering code	Product	Package	Container	MOQ
nRF24AP2-1CHQ32-T	nRF24AP2-1CH Single chip ANT solution with 1 ANT channel	5×5mm 32-pin QFN	Tray	490
nRF24AP2-1CHQ32-R7	nRF24AP2-1CH Single chip ANT solution with 1 ANT channel	5×5mm 32-pin QFN	Tape-and-reel	1500
nRF24AP2-1CHQ32-R	nRF24AP2-1CH Single chip ANT solution with 1 ANT channel	5×5mm 32-pin QFN	Tape-and-reel	4000
nRF24AP2-1CHQ32-S	nRF24AP2-1CH Single chip ANT solution with 1 ANT channel	5×5mm 32-pin QFN	Sample box	5
nRF24AP2-8CHQ32-T	nRF24AP2-8CH Single chip ANT solution with 8 ANT channels	5×5mm 32-pin QFN	Tray	490
nRF24AP2-8CHQ32-R7	nRF24AP2-8CH Single chip ANT solution with 8 ANT channels	5×5mm 32-pin QFN	Tape-and-reel	1500
nRF24AP2-8CHQ32-R	nRF24AP2-8CH Single chip ANT solution with 8 ANT channels	5×5mm 32-pin QFN	Tape-and-reel	4000
nRF24AP2-8CHQ32-S	nRF24AP2-8CH Single chip ANT solution with 8 ANT channels	5×5mm 32-pin QFN	Sample box	5

Table 17. nRF24AP2 RF silicon options

12.2.2 Development tools

Type Number	Description
nRF24AP1-DK3	ANT Development Kit[a]
nRF24AP2-UPGRADE	ANT upgrade kit with two nRF24AP2 modules (requires an nRF24AP1-DK3 kit)
nRF24AP2-DK1	Complete ANT Devleopment Kit with two other nRF24AP2 modules

a. The ANT Development Kit does not contain modules with nRF24AP2. Upgrade kit must be purchased separately.

Table 18. nRF24AP2 solution options

13 Glossary

Term	Description
ANT™	Ultra-low power network protocol stack from Dynastream Innovations Inc.
ANT+	Alliance of companies making ANT based products. The ANT+ alliance develops and maintain device profiles for sports and wellness applications, enabling interoperability between products from the alliance members.
BER	Bit Error Rate
GFSK	Gaussian Frequency-Shift Keying
Independent channel	An ANT channel between two ANT devices that has a unique setup of RF frequency, timing and channel configuration
ISM	Industrial-Scientific-Medical
MCU	MicroController Unit
MOQ	Minimum Order Quantity
OSI	Open Systems Interconnection
PA	Power Amplifier
PCB	Printed Circuit Board
QFN	Quad Flat package. No leads
RFID	Radio Frequency Identification
Shared channel	ANT channel between 2 or more ANT devices that share RF frequency, timing and channel configuration
TDMA	Time Division Multiple Access
USB	Universal Serial Bus

Table 19. Glossary

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View NRF24AP2-1CHQ32-R7 on WIN SOURCE
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- Shortage Management
- Alternative Solution
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