THE DATASHEET OF

NCL30060B3DR2G

NCL30060

High PF Offline Single Stage LED Driver with High Voltage Startup

The NCL30060 is a switch mode power supply controller intended for low to medium power single stage power factor (PF) corrected LED Drivers. It employs a constant on−time control method to ensure near unity power factor across a wide range of input voltages and output power. It can be used for isolated flyback as well as buck topologies. The device offers a suite of robust protection features to ensure safe operation under a range of fault conditions.

Version NCL30060B2 is intended for constant voltage (CV) regulated output drivers where a DC−DC converter or linear regulator in the second stage controls the current to the LEDs so the output short circuit protection detector function has been disabled. Version NCL30060B3 is intended for applications not requiring Brown Out protection or output short circuit protection as typical with low standby operation. The NCL30060B4 removes on−time modulation for solutions not needing this feature.

Features

- Built−In High Voltage Start−up Circuit
- Direct Opto−coupler Feedback Connection
- Constant On−Time PWM Control
- Quasi−Resonant Switching
- Low Operating Current (1.6 mA typical)
- Source 250 mA / Sink 400 mA Totem Pole Gate Driver
- Integrated 12 V (typ) Gate Drive Clamp
- Frequency Dithering for Reduced EMI Profile
- Enable/Disable Function
- Dynamic Self−Supply (DSS) Operation
- Operating T_J from −40°C to 105°C
- Maximum On Time Protection
- Integrated Brown−out
- Overvoltage Protection
- Cycle−by−Cycle Overcurrent Protection
- Output Winding Short−Circuit Protection
- Thermal Shutdown
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- LED Lighting

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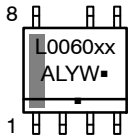
SOIC−7
CASE 751U

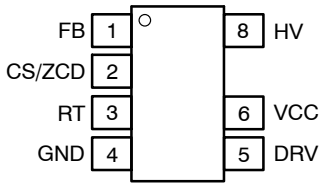
MARKING DIAGRAM



L0060xx = Specific Device Code
xx = A, B, B1, B2, B3, B4
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

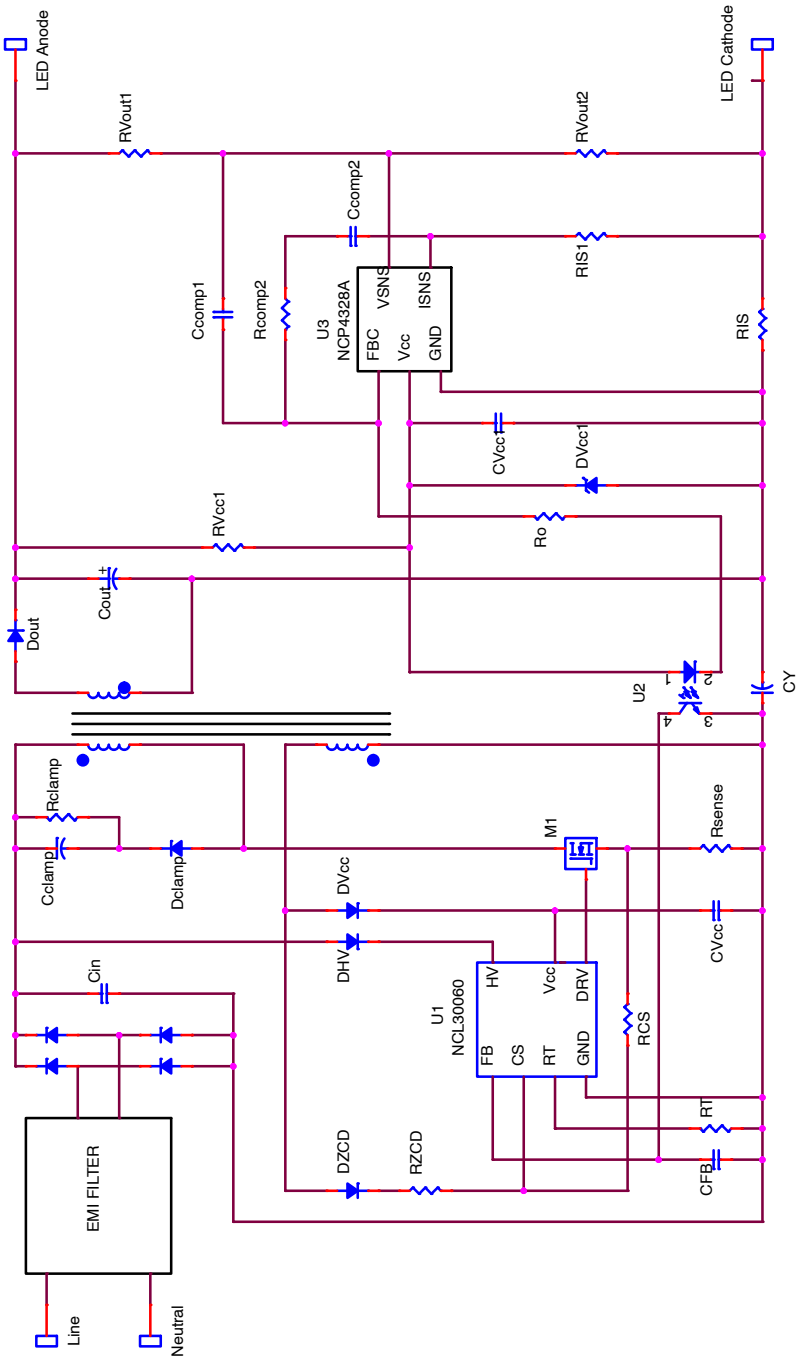


Figure 1. NCL30060 Typical Application Diagram

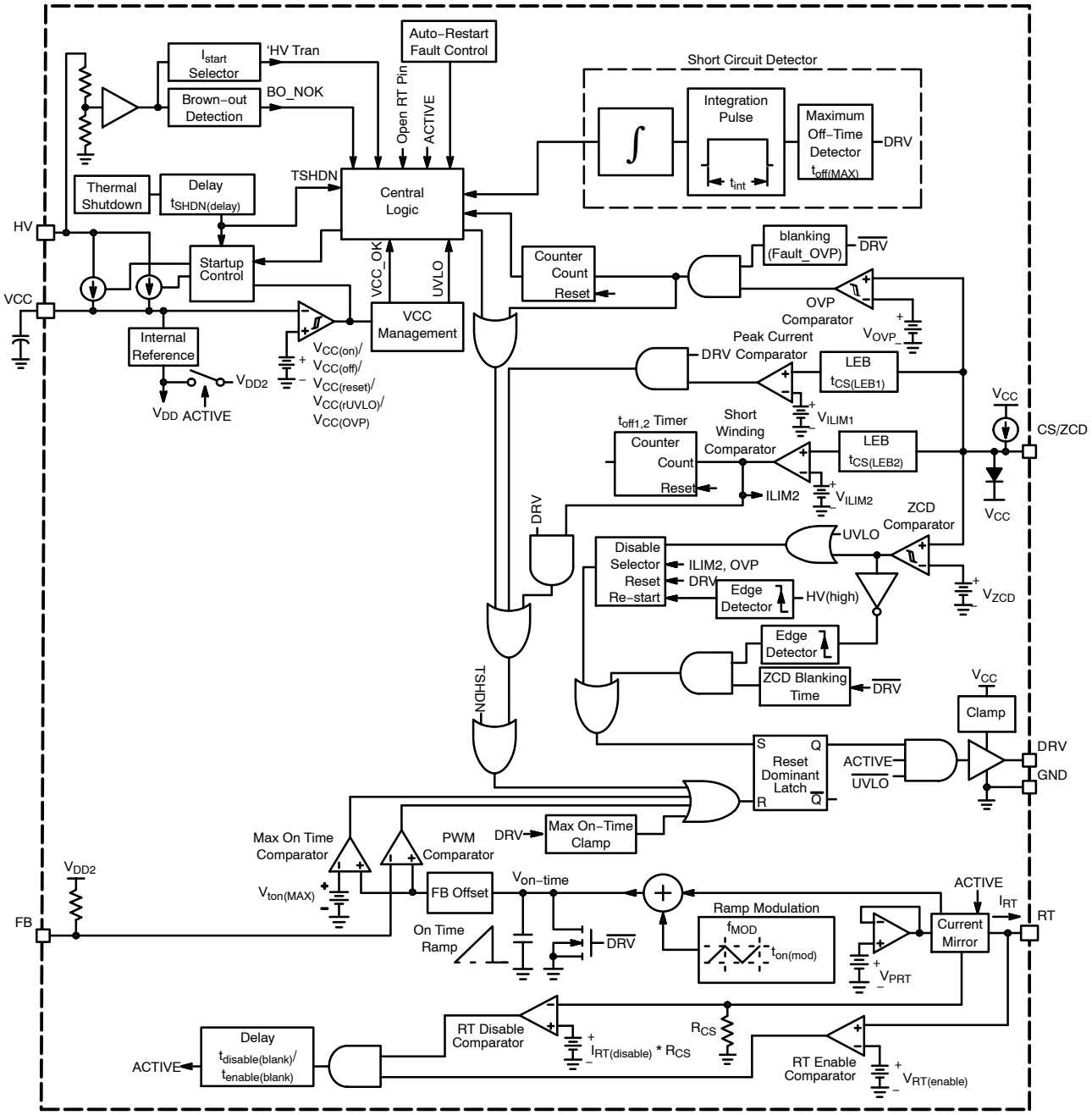


Figure 2. NCL30060 Internal Functional Block Diagram

Table 1. NCL30060 PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Pin Description
1	FB	Feedback Input. The FB pin is the control input to the PWM comparator. A voltage level controlled by the feedback loop on this pin is compared to the internal ramp establishing power switch on time.
2	CS/ZCD	Current sense and zero current detection. The CS input is used to sense the instantaneous switch current in the external power switch during switch on time. A fast−responding high threshold level for short circuit detection is provided along with a longer blanking time at lower level for overload conditions. During switch off time, this pin monitors the bias winding to detect transformer demagnetization. When stored energy is depleted the gate drive turns on the power switch initiating the next cycle. This pin also detects overvoltage conditions through the bias winding. A blanking time prevents false overvoltage triggering due to noise.
3	RT	Maximum on−time adjust. The RT pin establishes the ramp charging current. The PWM comparator establishes the switch on time from the ramp and FB signal. Pulling the RT pin below the disable threshold forces the controller in the Armed mode where all switching functions cease.
4	GND	Ground. This is the ground reference for the controller. All bypassing and control components should be connected to the GND pin with a short trace length to minimize noise.
5	DRV	Drive. The high current capability of the totem pole gate drive makes it suitable to directly control high gate charge power MOSFETs. The driver stage provides both passive and active pull−down circuits which force the MOSFET gate off when VCC is below normal operating levels.
6	VCC	IC Supply. This is the positive supply of the controller and source for powering external circuits. Internal bias will be disabled when external power is sufficient to maintain operation.
7	NC	No−connect. This missing pin provides creepage distance.
8	HV	High−voltage input. Monitors input voltage for brown−out detection and power to operate controller.

Table 2. MAXIMUM RATINGS (Notes 1, 2, 3 and 4)

Rating	Symbol	Value	Unit
FB Voltage	V_{FB}	−0.3 to 10	V
FB Current	I_{FB}	±10	mA
CS/ZCD Voltage	$V_{CS/ZCD}$	−0.9 to 12.4	V
CS/ZCD Current	$I_{CS/ZCD}$	−2 / +5	mA
RT Voltage	V_{RT}	−0.3 to 5	V
RT Current	I_{RT}	±10	mA
DRV Voltage (Note 2)	V_{DRV}	−0.3 to $V_{DRV(high)}$	V
DRV Sink Current	$I_{DRV(sink)}$	400	mA
DRV Source Current	$I_{DRV(source)}$	250	mA
Supply Voltage	V_{CC}	−0.3 to 30	V
Supply Voltage Rate of Change	dV_{CC}/dt	1	V/μs
Supply Current	I_{CC}	20	mA
HV Voltage	V_{HV}	−0.3 to 700	V
HV Current	I_{HV}	20	mA
Thermal Resistance, Junction to Ambient 1 Oz Cu Printed Circuit Copper Clad)	$R_{\theta JA}$	125	°C/W
ESD Capability Human Body Model per JEDEC Standard JESD22−A114E. (Note 5) Machine Model per JEDEC Standard JESD22−A114E. Charge Device Model per JEDEC Standard JESD22−C101E.		 5000 200 1500	V
Operating Temperature Range While Biased	T_J	−40 to 105	°C
Maximum Junction Temperature	T_{JMax}	150	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
Lead Temperature (Soldering, 10 s)	T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $V_{CS/ZCD(MAX)}$ is the maximum voltage of the pin shown in the electrical table. When the voltage on this pin exceeds 7.4 V, the pin sinks a current equal to [($V_{CS/ZCD}$ − 7.4 V) / 1 kΩ]. A $V_{CS/ZCD}$ of 9 V generates a sink current of approximately 1.6 mA.
2. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.
3. This device contains Latch−Up protection and has been tested per JEDEC Standard JESD78D, Class I and exceeds ±100 mA.
4. Low Conductivity Board. As mounted on 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper trances and heat spreading area. As specified for a JEDEC51−1 conductivity test PCB. Test conditions were under natural convection of zero air flow.
5. Pin 8 HV pin is ESD rated to 1200 V.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, V_{HV} = 120 V, V_{FB} = 4 V, $V_{CS/ZCD}$ = 0 V, C_{DRV} = 1 nF, R_T = 20 kΩ, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 105°C, unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	1 V/ms, V_{CC} increasing	$V_{CC(on)}$	11.75	12.5	13.75	
Minimum Operating Voltage	1 V/ms, V_{CC} decreasing	$V_{CC(MIN)}$	10.7	11.5	12.8	
Operating Hysteresis	$V_{CC(on)}$ − $V_{CC(MIN)}$	$V_{CC(HYS1)}$	0.9	–	–	
Undervoltage Lockout	V_{CC} decreasing	$V_{CC(UVLO)}$	8.2	8.8	9.4	
Hysteresis Between $V_{CC(MIN)}$ and $V_{CC(UVLO)}$	1 V/ms, $V_{CC(min)}$ − $V_{CC(UVLO)}$	$V_{CC(HYS2)}$	2.0	–	–	
Internal Latch/Logic Reset Level	V_{CC} decreasing	$V_{CC(reset)}$	4.5	5.5	7.5	
Transition from I_{start1} to I_{start2}	V_{CC} increasing	$V_{CC(inhibit)}$	0.35	0.7	0.95	
Supply Current						μA
In Fault Mode		I_{CC1}	140	190	240	
In Disable Modes	V_{RT} = 0 V	I_{CC2}	300	335	450	
Active Mode Without C_{DRV}, f_{SW} = 60 kHz	C_{DRV} = open	I_{CC4}	800	870	975	
Active Mode With C_{DRV}, f_{SW} = 60 kHz	C_{DRV} = 1nF	I_{CC5}	1490	1600	1700	
Startup Current	V_{CC} = 0 V to $V_{inhibit}$	I_{start1}	0.31	0.77	1.23	mA
		I_{start2}	9	14	19	
	V_{HV} = 400V	I_{start3}	3.5	5.25	7.00	
V_{CC} Overvoltage Protection Threshold		$V_{CC(OVP)}$	27	28	29	V
V_{CC} Overvoltage Protection Delay		$t_{delay(VCC\_OVP)}$	15	30	50	μs
Startup Circuit Off−State Leakage Current	V_{HV} = 400 V, V_{CC} = $V_{CC(on)}$ to $V_{CC(MAX)}$	$I_{HV(off)}$	–	24	30	μA
Minimum Startup Voltage	I_{start2} = 1 mA	$V_{HV(MIN)}$	–	–	40	V
Startup Current Transition Voltage Threshold	I_{start3} = 5.25 mA	$V_{HV(tran)}$	160	175	190	V
GATE DRIVE						
Rise Time (10−90%)	V_{DRV} from 10 to 90% of V_{DRV}	$t_{PDRV(rise)}$	–	80	180	ns
Fall Time (90−10%)	V_{DRV} from 90 to 10% of V_{DRV}	$t_{PDRV(fall)}$	–	40	80	ns
Current Capability						mA
Source	V_{DRV} = 2 V	$I_{DRV(SRC)}$	–	250	–	
Sink	V_{DRV} = 10 V	$I_{DRV(SNK)}$	–	400	–	
High State Voltage	V_{CC} = $V_{CC(UVLO)}$ + 0.2 V, R_{DRV} = 10 kΩ	$V_{DRV(highuvlo)}$	–	–	0.25	V
	V_{CC} = $V_{CC(OVP)}$ − 0.5 V , R_{DRV} = 10 kΩ	$V_{DRV(high)}$	10	12	14	V
Low State Voltage	I_{DRV} = 100μA	$V_{DRV(low)}$	–	–	0.25	V
FEEDBACK						
Feedback Open Voltage	V_{FB} = open	$V_{FB(open)}$	6.0	6.3	6.6	V
Minimum FB Voltage to Generate Drive Pulses	V_{FB} decreasing	$V_{FB(offset)}$	0.60	0.70	0.80	V
Feedback Bias Resistor		$R_{FB(bias)}$	20	25.8	29.6	kΩ
CONSTANT ON TIME GENERATOR						
On Time	R_T = 20 kΩ, V_{FB} = $V_{FB(open)}$	t_{on1}	4.75	5.0	5.25	μs
	R_T = 10 kΩ, V_{FB} = $V_{FB(open)}$	t_{on2}	2.37	2.50	2.63	
	R_T = 80 kΩ, V_{FB} = $V_{FB(open)}$	t_{on3}	18.4	19.5	20.7	
	R_T = 80 kΩ, V_{FB} = 4.45 V	t_{on4}	13.6	14.5	15.5	
	R_T = 80 kΩ, V_{FB} = 3.2 V	t_{on5}	9.0	9.56	10.1	
Maximum On Time	R_T = 110 kΩ to open, V_{FB} = $V_{FB(open)}$	$t_{on(MAX)}$	22.0	27.5	33.0	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, V_{HV} = 120 V, V_{FB} = 4 V, $V_{CS/ZCD}$ = 0 V, C_{DRV} = 1 nF, R_T = 20 kΩ, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 105°C, unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
CONSTANT ON TIME GENERATOR						
Maximum On−Time Feedback Voltage	V_{FB} increasing	$V_{FB(tonMAX)}$	5.415	5.70	5.985	V
RT Pin Regulation Voltage		$V_{RT(REG)}$	–	2.0	–	V
On−Time Modulation Frequency (Note 6)		f_{MOD}	254	292	325	Hz
On Time Modulation (Note 6)		$t_{on(MOD)}$	±4	±6	±8	%
DISABLE FUNCTION						
RT Disable Current Threshold	I_{RT} Decreasing	$I_{RT(disable)}$	250	325	400	μA
RT Enable Threshold	V_{RT} increasing	$V_{RT(enable)}$	380	400	420	mV
RT Pull−Up Current In Disable Mode		$I_{RT(dis)}$	45	50	55	μA
Disable Blanking	I_{RT} increasing or $V_{Disable}$ decreasing	$t_{disable(blank)}$	6.8	8	9.8	μs
ZERO CURRENT DETECTION						
ZCD Arming Threshold	$V_{CS/ZCD}$ Increasing	$V_{ZCD(ARM)}$	225	250	275	mV
ZCD Trigger Threshold	$V_{CS/ZCD}$ Decreasing	$V_{ZCD(TRIG)}$	35	55	90	mV
ZCD Arming Blanking Duration		$t_{ARM(blank)}$	1.7	2.05	2.35	μs
ZCD Propagation Delay	$V_{CS/ZCD}$ stepping from 2.0 V to 0 V, dV/dt = 20 V/μs, $V_{CS/ZCD}$ = $V_{ZCD(TRIG)}$ to V_{DRV} = 10%	$t_{ZCD(PROP)}$	–	150	170	ns
Input Voltage Excursion Upper Clamp Negative Clamp	 V_{CC} = 14V, $I_{CS/ZCD}$ = 5 mA V_{CC} = 14V, $I_{CS/ZCD}$ = −2 mA	 $V_{CS/ZCD(MAX)}$ $V_{CS/ZCD(MIN)}$	 – −0.9	 12.4 −0.7	 – 0	V
CS/ZCD Open Voltage		$V_{ZCD(open)}$	6.5	–	–	V
Pull−up Current Source		$I_{CS/ZCD}$	0.7	1.0	1.3	μA
Timeout After Last Demagnetization Detection	$V_{CS/ZCD}$ > V_{ILIM2}	t_{off1} t_{off2}	100 1000	200 1250	300 1700	μs
Minimum ZCD Pulse Width	Between $V_{ZCD(rising)}$ and $V_{ZCD(falling)}$ to DRV	t_{SYNC}	–	70	200	ns
CURRENT SENSE						
Current Sense Voltage Threshold	T_J = 25°C T_J = −40°C to 125°C	V_{ILIM1}	242.5 238	250 250	257.5 262	mV
Propagation Delay	Step $V_{CS/ZCD}$ 0 V to V_{ILIM1} + 0.1 V to DRV falling edge,	t_{ILIM1}	–	100	200	ns
Leading Edge Blanking Duration	Step $V_{CS/ZCD}$ 0 V to V_{ILIM1} + 0.1 V to DRV falling edge,	$t_{CS(LEB1)}$	250	325	400	ns
Abnormal Overcurrent Fault Threshold		V_{ILIM2}	475	500	525	mV
Fault Propagation Delay	Step $V_{CS/ZCD}$ 0 V to V_{ILIM2} + 0.1 V to DRV falling edge,	t_{ILIM2}	–	125	175	ns
Fault Leading Edge Blanking Duration	Step $V_{CS/ZCD}$ 0 V to V_{ILIM2} + 0.1 V to DRV falling edge,	$t_{CS(LEB2)}$	90	120	150	ns
Leading Edge Blanking Duration Ratio	$t_{LEB(LEB2)}/t_{LEB1}$	$t_{LEB(ratio)}$	–	0.37	–	–
Number of Consecutive Abnormal Current Events to Enter Fault Mode (Latch mode available on customer request)		n_{ILIM2}	–	4	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, V_{HV} = 120 V, V_{FB} = 4 V, $V_{CS/ZCD}$ = 0 V, C_{DRV} = 1 nF, R_T = 20 kΩ, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 105°C, unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
OUTPUT SHORT CIRCUIT AND OVERVOLTAGE PROTECTION						
Output Short Off−Time Detector Threshold (Note 7)	Detected during DRV low	$t_{off(OS)}$	43	50	55	μs
Output Short Detection Integration Weighting Ratio (Note 7)	$N_{INTratio(OS)}$= Charging speed(Output Short detected) / Discharging speed (normal operation)	$N_{INTratio(OS)}$		20		
Output Short Detection Integration Time for Continuous Integration pulses (Note 7)		$t_{INTCON(OS)}$	36.7	40	45.7	ms
Overvoltage Threshold	DRV is low	V_{OVP}	5.8	6.0	6.2	V
Overvoltage Propagation Delay	$V_{CS/ZCD}$ = 0 V to 7 V ramp, dV/dt = 1 V/μs, $V_{CS/ZCD}$ = V_{OVP} to DRV low	$t_{OVP(PROP)}$	–	–	2.5	μs
Overvoltage Blanking		$t_{OVP(blank)}$	1.5	2.0	2.5	μs
Number of Consecutive Overvoltage Events to Enter Fault Mode Mode (Latch mode available on customer request)		n_{OVP}	–	4	–	
Auto−recovery Timer Duration		$t_{autorecovery}$	0.8	1.0	1.2	s
BROWN−OUT PROTECTION (does not apply to B1 and B3 options)						
System Startup Threshold		$V_{BO(start)}$	102	111	120	V
System Shutdown Threshold		$V_{BO(stop)}$	88	96	104	V
Brown−out Detection Blanking Time	V_{HV} decreasing, delay from $V_{BO(stop)}$ to drive disable	$t_{BO(stop)}$	43	54	65	ms
THERMAL PROTECTION						
Thermal Shutdown	Temperature increasing	T_{SHDN}	–	160	–	°C
Thermal Shutdown Hysteresis	Temperature decreasing	$T_{SHDN(HYS)}$	–	50	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Parameter does not apply to B4 option.
7. Parameter does not apply to B2, B3 and B4 options.

DETAILED OPERATING DESCRIPTION

HIGH VOLTAGE STARTUP CIRCUIT

The NCL30060 integrates a 700 V startup regulator eliminating the need of external startup components. The startup regulator consists of a constant current source that supplies current from the high voltage input terminal (HV) to the supply capacitor on the VCC pin (C_{CC}). The startup circuit current (I_{start2}) and (I_{start3}) are disabled if the VCC pin is below $V_{CC(inhibit)}$. In this condition, the startup current is reduced to I_{start1}, typically 0.77 mA. In addition, this regulator reduces no load power and increases the system efficiency as it uses negligible power in the normal operation mode.

After VCC pin is higher than $V_{CC(inhibit)}$ threshold, the startup circuit uses I_{start3} to charge the V_{CC} capacitor during the initial charging. I_{start3} has a typical value of 5.25 mA.

Once C_{CC} is charged to the startup threshold, $V_{CC(on)}$, typically 12.5 V, the startup regulator is disabled and the controller is enabled. The initial charging on V_{CC} capacitor is done. The controller is then biased by the V_{CC} capacitor.

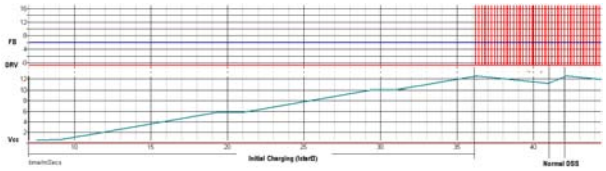


Figure 3. Initial Charging of V_{CC} and Normal DSS

The startup regulator is enabled once V_{CC} falls below its minimum operating threshold, $V_{CC(MIN)}$, typically 11.5 V. The driver continues operation while V_{CC} is charged by the startup circuit. This operating mode is known as dynamic self supply or DSS. During normal DSS operation, the startup circuit uses I_{start2} to charge the V_{CC} capacitor when the line voltage is below $V_{HV(tran)}$, and the startup circuit uses I_{start3} when the line voltage is higher than $V_{HV(tran)}$. $V_{HV(tran)}$ has a typical value of 175 V. Figure 3 shows the initial charging of V_{CC} capacitor and normal DSS.

The startup circuit continues to charge V_{CC} until the convertor bias winding is able to provide power to the V_{CC} capacitor. As long as the bias winding can maintain the V_{CC} voltage higher than $V_{CC(MIN)}$, the startup circuit will not be enabled. The startup circuit enters DSS mode if the V_{CC} voltage is lower than $V_{CC(MIN)}$.

The increase in current consumption due to external gate charge is calculated using Equation 1.

$$I_{CC(gate\ charge)} = f \cdot Q_G \qquad \text{(eq. 1)}$$

where f is the operating frequency and Q_G is the gate charge of the external MOSFETs. The additional gate charge current should not exceed the startup circuit. Otherwise, V_{CC} will not charge to $V_{CC(on)}$ and may stay at an undetermined voltage while dissipating excessive power. The controller and the startup circuit are disabled if the junction temperature of the device exceeds the thermal shutdown threshold, T_{SHDN}, typically 160°C. The controller is disabled if V_{CC} falls below the undervoltage lockout (UVLO) threshold, $VCC_{(UVLO)}$, typically 8.8 V. A noise filter, t_{UVLO}, 25 μs maximum, blanks the UVLO fault before disabling the controller.

FEEDBACK INPUT

A signal proportional to the output error is applied to the FB pin by means of an optocoupler or other means such as an Op Amp. The PWM Comparator compares the feedback or error signal to a level shifted voltage ramp to control the power switch on−time. The feedback voltage is directly proportional to the output power. An internal pull up resistor, R_{FB}, drives this pin to provide more linear response from the optocoupler transistor. The voltage reference biasing R_{FB} is typically 6.3 V .

The minimum on−time, $t_{on(MIN)}$, is determined by the propagation delay of the PWM Comparator and control logic. It is limited below 200 ns. The minimum on−time is achieved when V_{FB} is right on the voltage offset of the On−time Ramp, $V_{FB(offset)}$. A V_{FB} below $V_{FB(offset)}$ results in no drive pulses or “zero” on−time.

The maximum on−time is limited by the Maximum On−time comparator. The comparator is enabled once the feedback voltage, V_{FB}, exceeds $V_{FB(tonMAX)}$. This establishes the point where the LED driver transitions from constant current feedback (if so configured) to primary power control.

MAXIMUM ON−TIME

The PWM Comparator controls the on−time by comparing an internal voltage ramp, $V_{on-time}$, to the feedback voltage. The internal ramp is generated by charging an internal capacitor with a fixed current source. The slope of the ramp is adjusted by the user using an external timing resistor, R_T, between the R_T and GND pins. The architecture of the on−time control circuitry is shown in Figure 4.

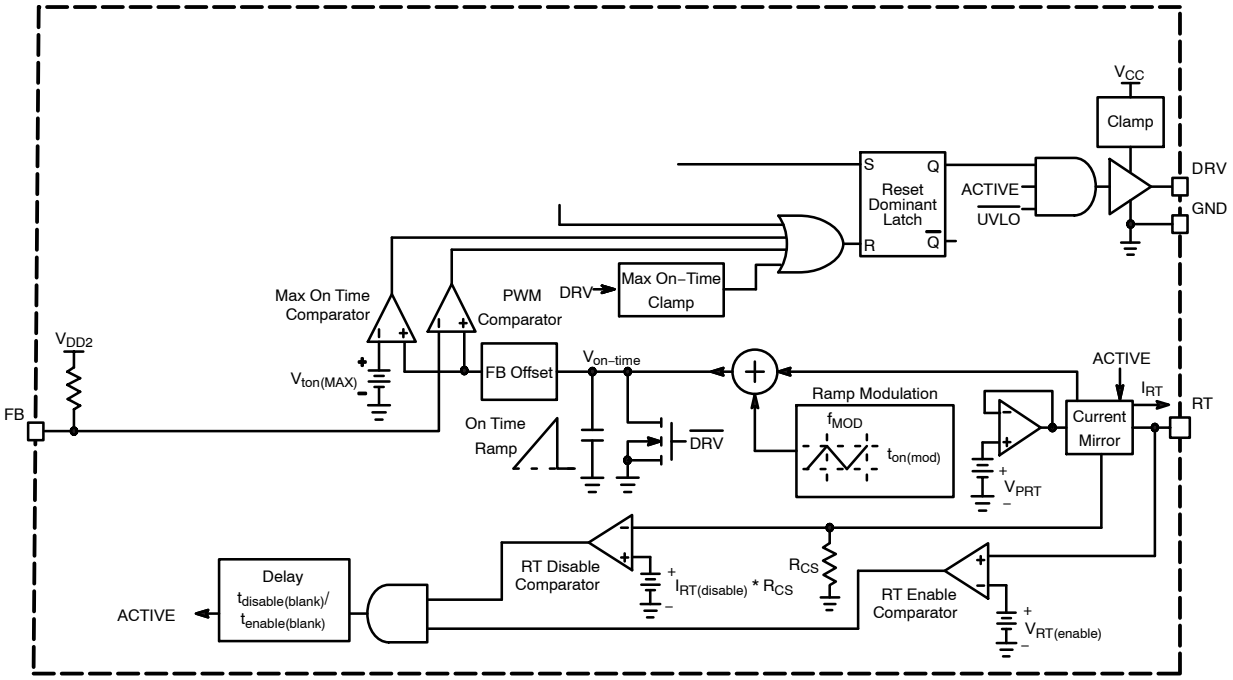


Figure 4. On−Time Control Architecture

The on−time is internally modulated to reduce the EMI signature of the controller. The modulation is accomplished by modulating the charge current using an internal triangle wave oscillator. The charge current is adjusted ±6% from the nominal value. The EMI signature of the controller is spread over a wide range of frequencies eliminating high peaks during an average reading. Version NCL30060B4 can be selected for some applications not requiring modulation of the control loop or output short circuit protection.

The absolute maximum on−time determines the maximum power of the system. The NCL30060 accurately controls the maximum on−time of the system by the Max On−time Clamp circuits. It ensures that On−time can't exceed $t_{on(MAX)}$, typically 27.5 μs, when the R_T resister value is above 110 kΩ. There is also a fixed voltage reference, $V_{ton(MAX)}$, which defines the maximum effective V_{FB} voltage. Given a certain R_T value between 10 kΩ and 110 kΩ, the Maximum On−time Comparator controls the on−time when primary side regulation is required. This could occur during an overload condition or during startup when the feedback signal is not present. The relationship between R_T and $t_{on(MAX)}$ is given by Equation 2 and Figure 5.

$$t_{on(MAX)} = 0.25 \cdot R_T \qquad \text{(eq. 2)}$$

Where $t_{on(MAX)}$ is in μs and R_T is in kΩ.

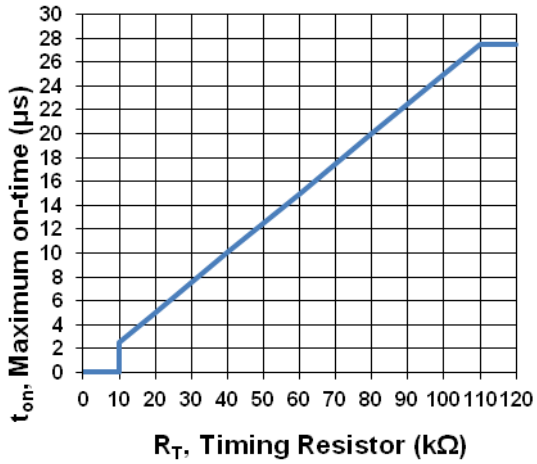


Figure 5. Maximum On−Time vs R_T

The RT pin has a threshold output current of $I_{RT(disable)}$ which has a maximum value of 400 μA. The maximum on−time is limited to 27.5 μs if the pin is left open or the Rt is higher than 110 kΩ. If the resistance between RT pin and GND is small enough to make the RT pin current higher than $I_{RT(disable)}$, the device is disabled after the blanking delay $t_{disable(blank)}$ and the RT pin output current is switched to $I_{RT(dis)}$ which has 50 μA typical value. After the device is disabled, the integrated HV source maintains V_{CC} above

$V_{CC(min)}$. The IC is activated when the voltage of the RT pin is higher than the $V_{RT(enable)}$, which has typical value of 400 mV. And the RT pin output current is switched back to normal operation, and the RT voltage is regulated to $V_{RT(REG)}$,which has a typical value of 2 V.

The timing resistor should be placed as close as possible to the RT and GND pins with short trace lengths. Care should be taken to keep switching nodes (high dv/dt) away from R_T to reduce noise pickup.

CURRENT SENSE, ZERO CURRENT AND OVERVOLTAGE DETECTION

The NCL30060 uses a novel architecture combining the current sense, the zero current detector (ZCD), output overvoltage and shorted output detector functions in a single terminal. Figure 6 shows the circuit schematic of the current sense and ZCD detectors.

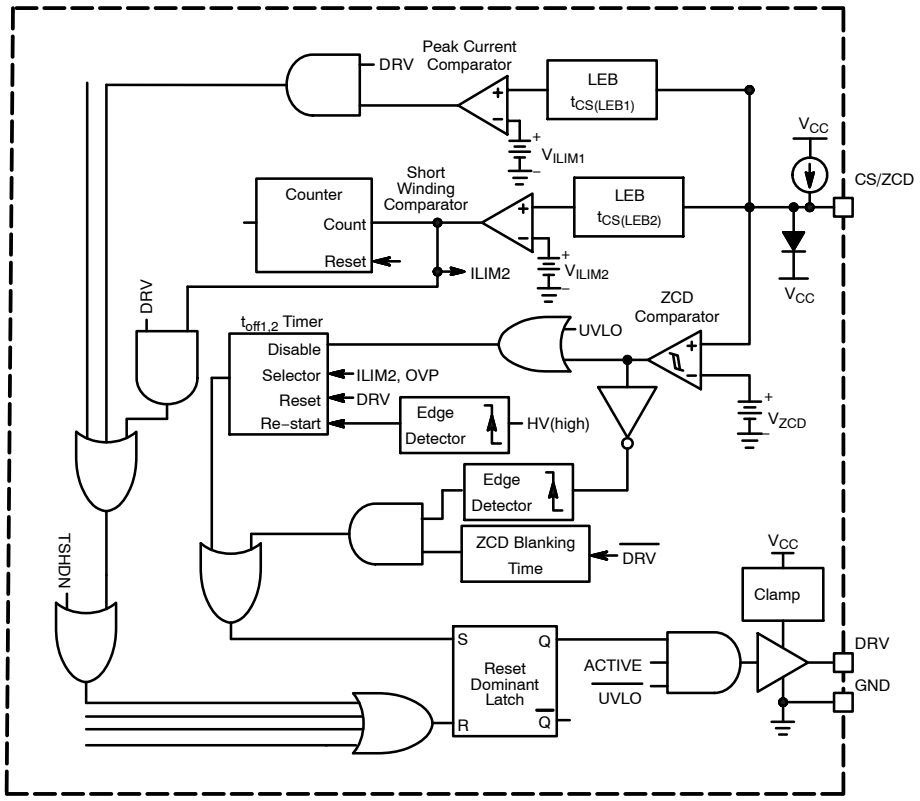


Figure 6. Current Sense and ZCD Detectors Schematic

CURRENT SENSE

The Switch current is sensed across a sense resistor, R_{sense}, and the resulting voltage ramp is applied to the CS/ZCD pin. The current signal is blanked by a leading edge blanking (LEB) circuit. The blanking period eliminates the leading edge spike and high frequency noise during the switch turn−on event. The LEB period, $t_{CS(LEB1)}$, is typically 325 ns. The Current Limit Comparator disables the driver once the current sense signal exceeds the current sense reference, V_{ILIM1}, typically 0.25 V. The next switching cycle is initiated by the ZCD or watchdog timer.

A severe overload fault like a secondary side winding short circuit causes the switch current to increase very rapidly during the on−time. The current sense signal significantly exceeds V_{ILIM1}. But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the current could damage the system.

The NCL30060 protects against this fault by adding an additional comparator, Short Circuit Comparator. The current sense signal is blanked with a shorter LEB duration, $t_{CS(LEB2)}$, typically 125 ns, before applying it to the Short Circuit Comparator. The voltage threshold of the comparator, V_{ILIM2}, typically 0.5 V, is set twice the level of V_{ILIM1}, to avoid interference with normal operation. Four consecutive faults detected by the Short Circuit Comparator causes the controller to enter a fault mode. The NCL30060B will auto−recover from the fault state if the short is removed. The count to 4 provides noise immunity during surge testing. The counter is reset each time a DRV pulse occurs without activating the Short Circuit Comparator.

The watchdog timer duration (t_{off2}) is increased to 1.25 ms independent of the PFC ZCD state.

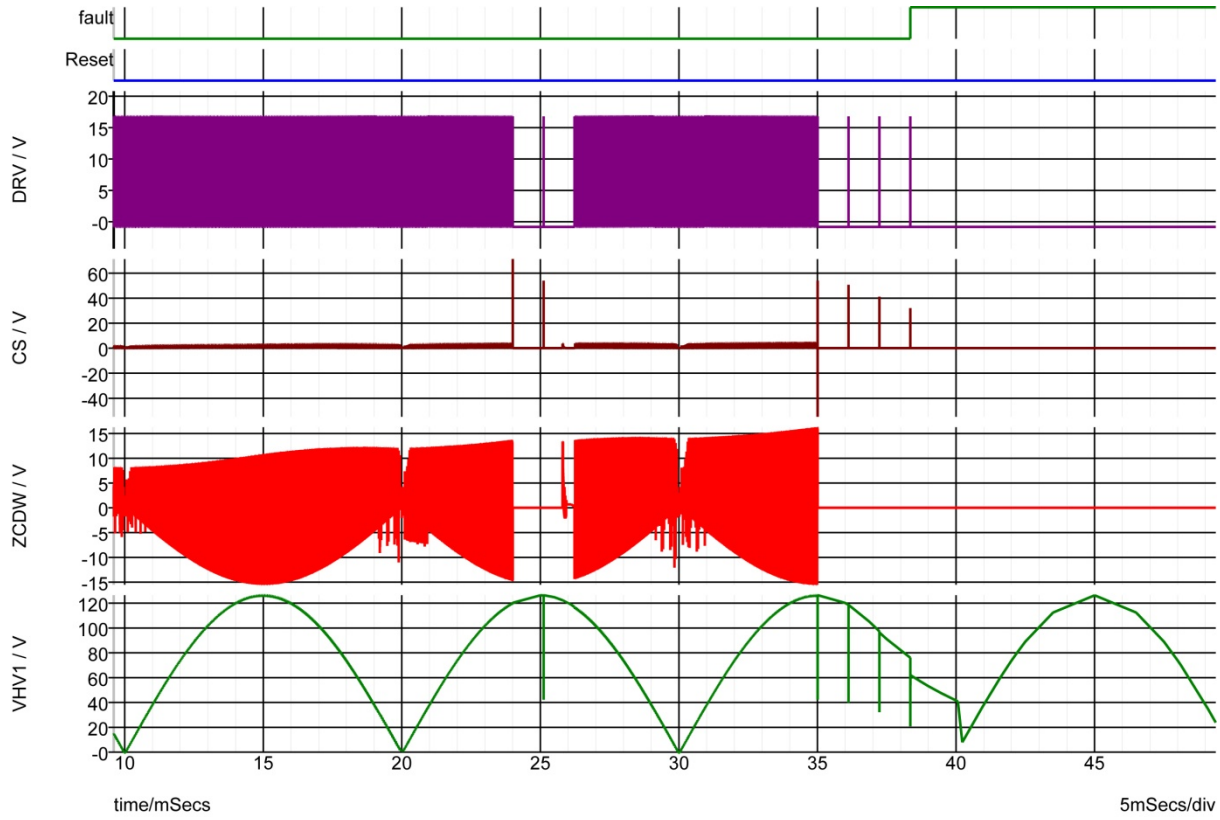


Figure 7. Secondary Side Winding Short−Circuit Waveforms

Figure 7 shows simulation results for an output winding short. The simulation waveforms are described below:

- DRV/V is gate drive signal for the PFC switch.
- VCS/V is the signal on the CS/ZCD pin.
- ZCDW/V is the voltage across the ZCD winding.
- VHV1/V is the voltage on the HV pin.

The converter is operating normally and a momentary fault is applied at 24 ms. Once the fault is applied, the watchdog timer duration increases to t_{off2}. The fault is removed after two faults overcurrent events are detected. The fault is re−applied at 35 ms. After four consecutive overcurrent conditions are detected, the fault signal goes high.

ZERO CURRENT DETECTION

The off−time in a CrM topology varies with the instantaneous line voltage and it is adjusted every cycle to allow the inductor current to reach zero before the next switch cycle begins. The inductor is demagnetized once its current reaches zero. Once the inductor is demagnetized the drain voltage of the switch begins to fall. The inductor demagnetization is detected by sensing the voltage across the inductor using an auxiliary winding. This winding is commonly known as a zero crossing detector (ZCD) winding. This winding provides a scaled version of the drain voltage. Figure 8 shows the ZCD winding arrangement.

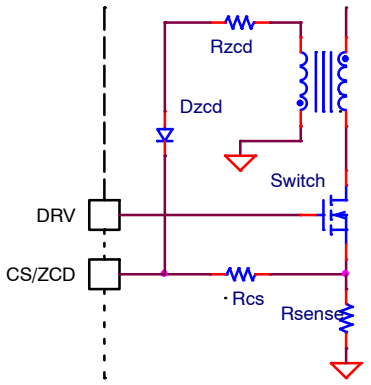


Figure 8. ZCD Winding Implementation

The ZCD voltage, $V_{CS/ZCD}$, is positive while the Switch is off and current flows on the secondary side. $V_{CS/ZCD}$ drops to and rings around zero volts once the transformer is demagnetized. The next switch cycle commences once a negative going transition is detected in the CS/ZCD pin. A positive transition (corresponding to the switch turn off) arms the ZCD detector to prevent false triggering. The arming of the ZCD detector, $V_{ZCD(ARM)}$, is typically 250 mV ($V_{CS/ZCD}$ increasing). The trigger threshold, $V_{ZCD(TRIG)}$, is typically 55 mV ($V_{CS/ZCD}$ decreasing).

The NCL30060 incorporates a minimum off−time delay, $t_{ARM(blank)}$.,typically 2.0 μs . This delay blanks the ringing which may be present on the bias winding during start up or if the output of the converter is shorted. The next DRV pulse is initiated once $t_{ARM(blank)}$ expires if a ZCD transition is detected prior to the delay expiring. Otherwise, it will initiate on the ZCD transition after $t_{ARM(blank)}$ expires. In the absence of a ZCD transition, the watchdog timer initiates the next drive pulse.

The CS/ZCD pin is internally clamped to V_{CC} thru an internal diode. A 7.4 V Zener diode with a 1 kΩ resistor to GND also clamp the pin. A resistor in series with the CS/ZCD pin is required to limit the current into pin. The Zener diode also prevents the voltage from going below ground. Figure 9 shows typical ZCD waveforms.

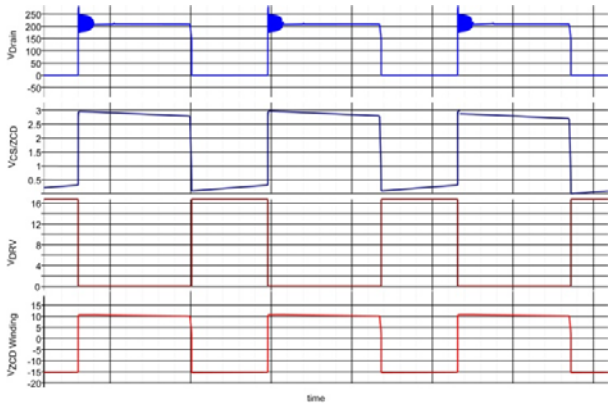


Figure 9. ZCD Winding Waveforms

During startup there are no ZCD transitions to set the PWM Latch and generate a DRV pulse. A watchdog timer, t_{off1}, starts the drive pulses in the absence of ZCD transitions. Its duration is typically 200 μs. The timer is also useful during startup and while operating at light load because the amplitude of the ZCD signal may be very small to cross the ZCD thresholds. The watchdog timer is reset at the beginning of a drive pulse. It is disabled if the CS/ZCD pin is above the ZCD arming threshold.

The watchdog timer duration increases to t_{off2}, typically 1.25 ms, when a V_{ILIM2} fault is detected.

OVERVOLTAGE PROTECTION

Output overvoltage protection (OVP) is provided by monitoring the CS/ZCD pin during the off−time. A dedicated comparator compares the voltage on CS/ZCD pin to an internal reference, V_{OVP}, typically 6 V. If 4 consecutive OVP events are detected the controller enters a fault mode. A 2 μs blanking delay, $t_{OVP(blank)}$, blanks the signal CS/ZCD signal after the drive turns off to blank ringing generated by system parasitics. The blanking provides protection during power up and steady state operation. Figure 10 shows the controller shutting down after an overvoltage condition is detected.

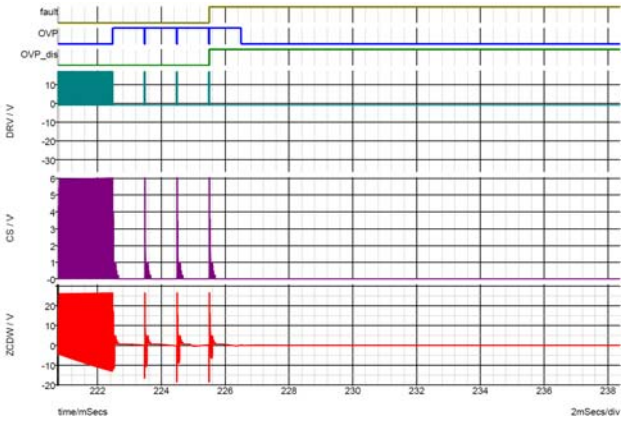


Figure 10. Overvoltage Detection Operating Waveforms

OUTPUT SHORT CIRCUIT DETECTION

When the converter is operating with low output voltage, the off−time is extended in CrM operation. In Figure 11 of the output short detection function block, the maximum off−time detector signals when the off time is longer than 50 μs. This 50 μs off time detection triggers a 150 μs pulse to feed the integrator. The integrator has a weighted integration feature, which makes the charging 20 times faster than the discharging. A continuous stream of 150 μs pulses will reach the integrator threshold in 40ms. Periods of time without triggering the 150 μs timer will extend the time to reach the threshold. The integrator discharges as the relative number of 150 μs pulses over time decreases.

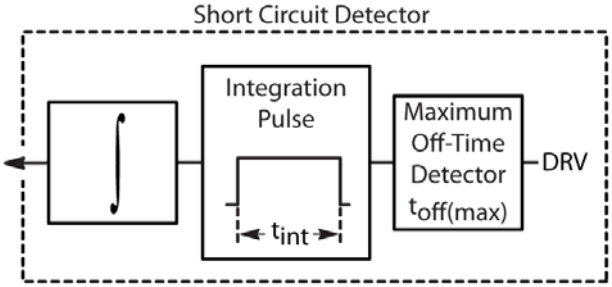


Figure 11. Output Short−Circuit Detector

When the threshold is reached, the system will determine there is an output short event. The system enters into fault mode. The NCL30060B will try to auto−recover after a 1 sec typical delay. This minimizes system power consumption due to the output short event. Figure 12 shows auto−restart operating waveforms.

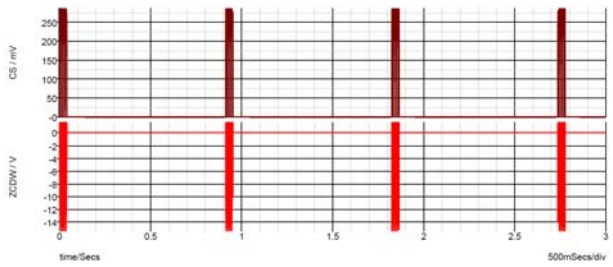


Figure 12. Output Short Detection and Protection Waveform

Versions NCL30060B2 and NCL30060B4 are intended for constant voltage (CV) regulated output drivers where a DC−DC converter or linear regulator in the second stage controls the current to the LEDs so the output short circuit protection detector function has been disabled. Version NCL30060B3 is useful in applications where the Brown Out function is not required and light load operation may trigger the output short circuit protection function. Ensure proper operation in fault modes.

BROWN OUT DETECTION

The NCL30060 includes brown out protection providing a defined shutdown for low input voltage. This feature is enabled after a V_{CC} reset event and does not allow the controller to enter Active mode until the input voltage is above the startup threshold, typically 111 V.

If the input voltage remains below the system shutdown threshold, typically 96 V, longer than the brown out detection blanking time, typically 54 ms, a shutdown flag is set. Gate drive pulses will continue to be issued until the input voltage is near the ac line voltage zero crossing. When a zero crossing is detected and the flag is set, gate drive pulses cease thereby stopping power delivery to the LED load. The brown out flag remains set and switching is suspended until the input voltage rises above the startup threshold.

Delaying termination of gate drive pulses until the zero crossing ensures the system is at a low power state before shutting down. This approach avoids a situation where energy stored in the input filter may artificially force the sensed voltage to cross the startup threshold if switching is abruptly terminated. A false startup level would be followed by crossing the shutdown threshold again. Such cycling on and off near the brown out threshold would result in LED flicker. Allowing the energy to discharge naturally near the zero crossing provides a clean brown out shutdown.

MOSFET DRIVER

The NCL30060 maximum supply voltage, $V_{CC(OVP)}$, is 28 V. Typical high voltage MOSFETs have a maximum gate voltage rating of 20 V. The driver incorporates an active voltage clamp to limit the gate voltage on the external MOSFET. The voltage clamp, $V_{DRV(high)}$, is typically 12 V with a maximum limit of 14 V.

AUTO−RECOVERY

The controller is disabled and enters a fault mode if V_{CC} drops below $V_{CC(UVLO)}$ or a non−latching fault is detected. The controller auto−restarts after the auto−recovery timer $t_{autorecovery}$, expires, typically 1 s.

THERMAL SHUTDOWN

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller including the startup circuit is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN}, typically 150 °C. Once a thermal shutdown condition is validated, the startup circuit is disabled. The startup circuit is enabled once V_{CC} falls below $V_{CC(reset)}$, charging V_{CC} up to $V_{CC(on)}$. The controller remains disabled if the thermal shutdown is present upon reaching $V_{CC(on)}$. The controller restarts at the next $V_{CC(on)}$ once the IC temperature drops below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 40°C.

LAYOUT CONSIDERATIONS

The GND pin is the reference point for the controller. Unless specified otherwise, all measurements are made relative to this pin. Both power and control circuits use this reference. It is recommended to have short traces between this pin and control components to reduce parasitic inductance.

ORDERING INFORMATION

Ordering Part No.	OCP	Brown Out	Output Short Detection	On−Time Modulation	Package	Shipping†
NCL30060ADR2G*	Latched	Enabled	Enabled	Enabled	SOIC−7 (Pb−Free)	2500 / Tape & Reel
NCL30060BDR2G	Auto−recoverable	Enabled	Enabled	Enabled		
NCL30060B1DR2G*	Auto−recoverable	Disabled	Enabled	Enabled		
NCL30060B2DR2G	Auto−recoverable	Enabled	Disabled	Enabled		
NCL30060B3DR2G	Auto−recoverable	Disabled	Disabled	Enabled		
NCL30060B4DR2G	Auto−recoverable	Enabled	Disabled	Disabled		

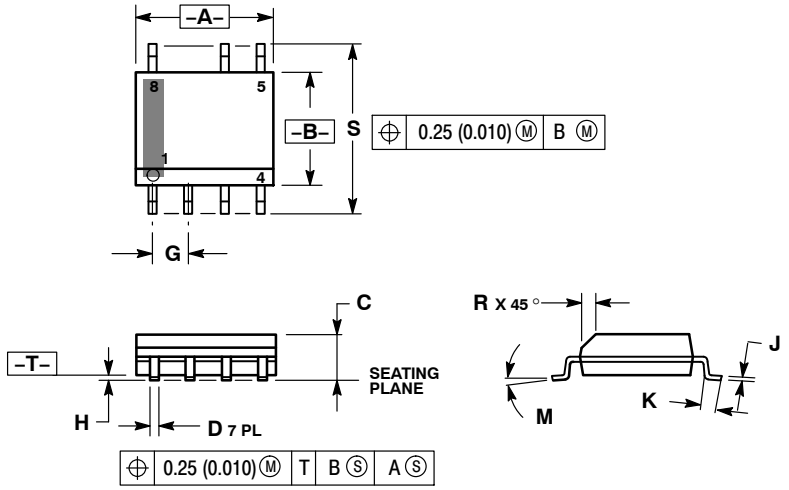
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Version available only by customer request.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−7
CASE 751U
ISSUE E

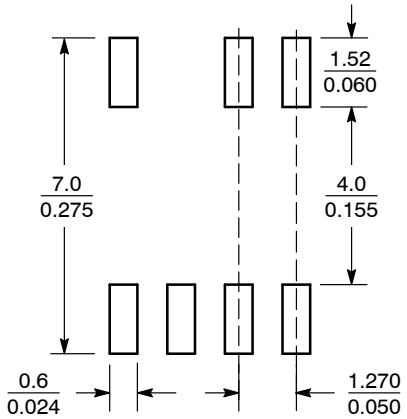
DATE 20 OCT 2009



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

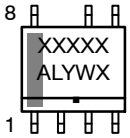
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98AON12199D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−7**		**PAGE 1 OF 2**

SOIC−7
CASE 751U
ISSUE E

DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

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