



**THE DATASHEET OF
MR2A16ATS35C**





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256K x 16-Bit 3.3-V Asynchronous Magnetoresistive RAM

MR2A16A



44-TSOP
 Case 924A-02

Introduction

The MR2A16A is a 4,194,304-bit magnetoresistive random access memory (MRAM) device organized as 262,144 words of 16 bits. The MR2A16A is equipped with chip enable (\bar{E}), write enable (\bar{W}), and output enable (\bar{G}) pins, allowing for significant system design flexibility without bus contention. Because the MR2A16A has separate byte-enable controls ($\bar{L}B$ and $\bar{U}B$), individual bytes can be written and read.

MRAM is a nonvolatile memory technology that protects data in the event of power loss and does not require periodic refreshing. The MR2A16A is the ideal memory solution for applications that must permanently store and retrieve critical data quickly.

The MR2A16A is available in a 400-mil, 44-lead plastic small-outline TSOP type-II package with an industry-standard center power and ground SRAM pinout.

The MR2A16A is available in Commercial (0°C to 70°C), Industrial (-40°C to 85°C) and Extended (-40°C to 105°C) ambient temperature ranges.

Features

- Single 3.3-V power supply
- Commercial temperature range (0°C to 70°C), Industrial temperature range (-40°C to 85°C) and Extended temperature range (-40°C to 105°C)
- Symmetrical high-speed read and write with fast access time (35 ns)
- Flexible data bus control — 8 bit or 16 bit access
- Equal address and chip-enable access times
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- All inputs and outputs are transistor-transistor logic (TTL) compatible
- Fully static operation
- Full nonvolatile operation with 20 years minimum data retention

Device Pin Assignment

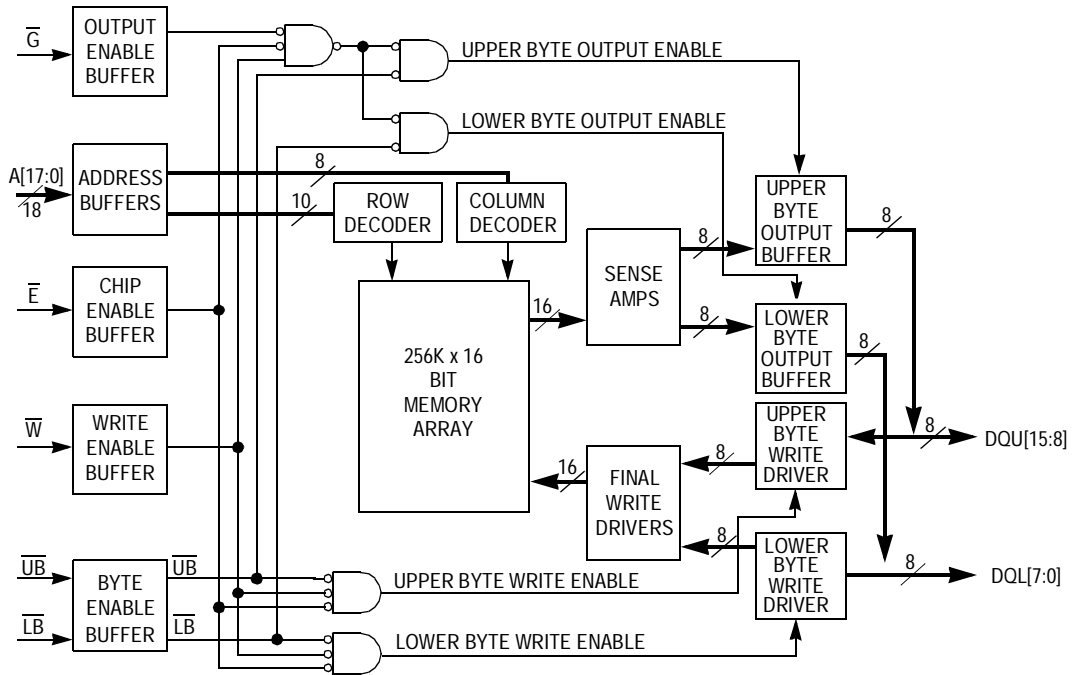


Figure 1. Block Diagram

Device Pin Assignment

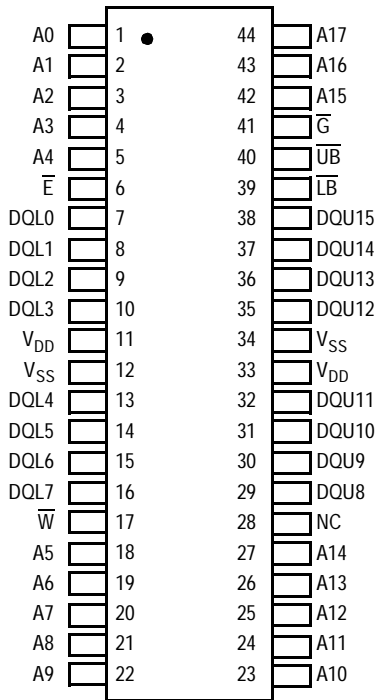


Table 1. Pin Functions

Signal Name	Function
A	Address input
\bar{E}	Chip enable
\bar{W}	Write enable
\bar{G}	Output enable
\bar{UB}	Upper byte select
\bar{LB}	Lower byte select
DQL	Data I/O, lower byte
DQU	Data I/O, upper byte
V_{DD}	Power supply
V_{SS}	Ground
NC	Do not connect this pin

Figure 2. MR2A16A in 44-Pin TSOP Type II Package

Table 2. Operating Modes

\bar{E}^1	\bar{G}^1	\bar{W}^1	\bar{LB}^1	\bar{UB}^1	Mode	V_{DD} Current	DQL[7:0] ²	DQU[15:8] ²
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower byte read	I_{DDR}	D_{Out}	Hi-Z
L	L	H	H	L	Upper byte read	I_{DDR}	Hi-Z	D_{Out}
L	L	H	L	L	Word read	I_{DDR}	D_{Out}	D_{Out}
L	X	L	L	H	Lower byte write	I_{DDW}	D_{In}	Hi-Z
L	X	L	H	L	Upper byte write	I_{DDW}	Hi-Z	D_{In}
L	X	L	L	L	Word write	I_{DDW}	D_{In}	D_{In}

NOTES:

- ¹ H = high, L = low, X = don't care
- ² Hi-Z = high impedance

Electrical Specifications

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

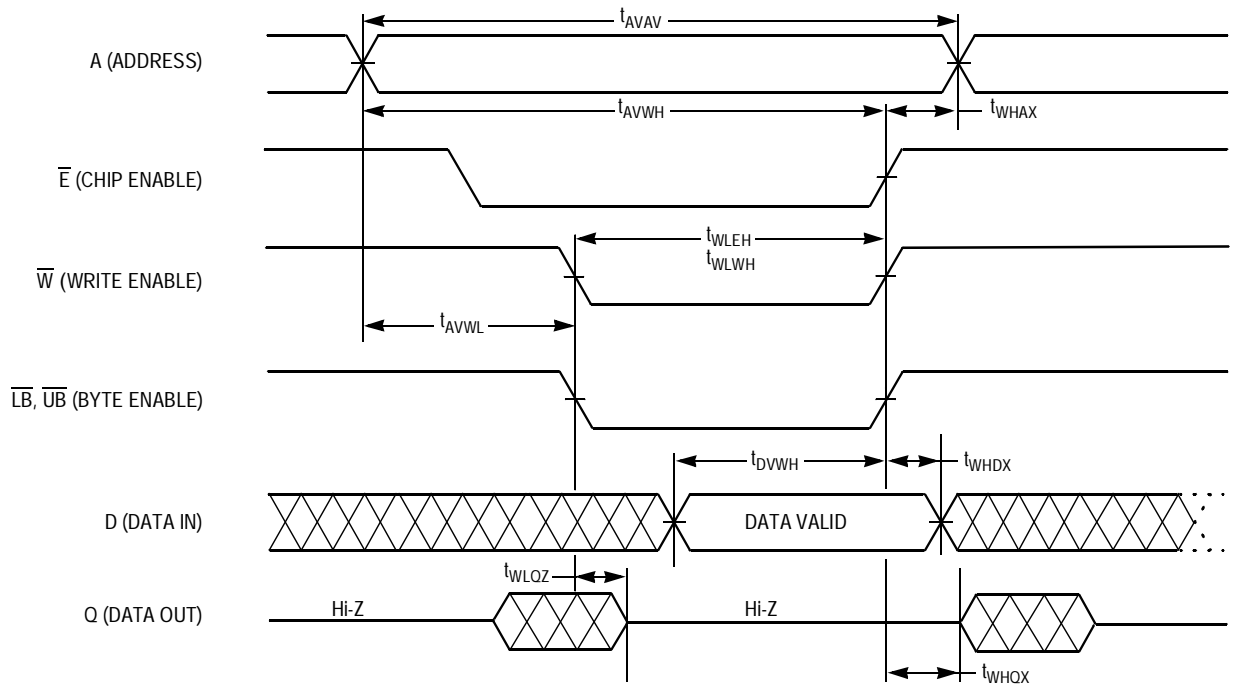


Figure 6. Write Cycle 1 (\overline{W} Controlled)

Table 12. Write Cycle Timing 3 ($\overline{\text{LB}}/\overline{\text{UB}}$ Controlled)^{1, 2, 3, 4, 5, 6}

Parameter	Symbol	Min	Max	Unit
Write cycle time ⁷	t_{AVAV}	35	—	ns
Address set-up time	t_{AVBL}	0	—	ns
Address valid to end of write ($\overline{\text{G}}$ high)	t_{AVBH}	18	—	ns
Address valid to end of write ($\overline{\text{G}}$ low)	t_{AVBH}	20	—	ns
Byte pulse width ($\overline{\text{G}}$ high)	t_{BLEH} t_{BLWH}	15	—	ns
Byte pulse width ($\overline{\text{G}}$ low)	t_{BLEH} t_{BLWH}	15	—	ns
Data valid to end of write	t_{DVBH}	10	—	ns
Data hold time	t_{BHDX}	0	—	ns
Write recovery time	t_{BHAX}	12	—	ns

NOTES:

- ¹ A write occurs during the overlap of $\overline{\text{E}}$ low and $\overline{\text{W}}$ low.
- ² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- ³ If $\overline{\text{G}}$ goes low at the same time or after $\overline{\text{W}}$ goes low, the output will remain in a high-impedance state.
- ⁴ After $\overline{\text{W}}$, $\overline{\text{E}}$, or $\overline{\text{UB}}/\overline{\text{LB}}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- ⁵ If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them.
- ⁶ The minimum time between $\overline{\text{E}}$ being asserted low in one cycle to $\overline{\text{E}}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- ⁷ All write cycle timings are referenced from the last valid address to the first transition address.

Package Information

Table 13. Package Information

Device	Pin Count	Package Type	Designator	Case No.	Document No.	RoHS Compliant
MR2A16A	44	TSOP Type II	TS/YS ¹	924A-02	98ASS23673W	True

NOTES:

- ¹ TS and YS are both valid package codes for TSOP packages. The package is identical for both TS and YS codes.

Revision History

Revision History

Revision	Date	Description of Change
4	18 Jun 2007	Added new Industrial and Extended temperature product information; updated part ordering information; changed to 2 ms delay after power up; power supply characteristics values updated to TBD for industrial and extended temperature devices.
5	21 Sep 2007	Changed MR2A16ATS35C product description to Legacy Commercial. Added the New Commercial temperature product (MR2A16AYS35) information. Table 3: MR2A16AYS35 H _{max_write} = 25 Oe. Table 4: MR2A16AYS35 has a 2 ms power up waiting period. Table 6: Applied values to TBD's in IDD specifications.
6	12 Nov 2007	Table 2: Changed IDDA to IDDR or IDDW. Table 13: Added note indicating that TS and YS are both valid package codes. Current Part Numbering System: Added commercial (missing letter) temperature range.

Mechanical Drawing

The following pages detail the package available to MR2A16A.

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