THE DATASHEET OF

MP6515GL-Z

www.win-source.net 0086-755-83957316

The Future of Analog IC Technology®

MP6515

35V, 2.8A, Phase/Enable Control H-Bridge Motor Driver in QFN 3x4 and TSSOP-EP Packages

DESCRIPTION

The MP6515 is an H-bridge motor driver. It operates from a supply voltage of up to 35V and delivers motor current up to 2.8A. Typically, the MP6515 is used to drive a DC brush motor. For the MP6515, control of the outputs is accomplished through the PHASE, ENBL, BRAKE, and BMODE pins.

An internal current sensing circuit provides an output with voltage proportional to the load current. In addition, cycle-by-cycle current regulation/limiting is provided. These features do not require the use of a low-ohm shunt resistor.

Internal safety features include over-current protection, input over-voltage protection, under-voltage lockout (UVLO), and thermal shutdown.

The MP6515 is available in 16-pin 5.0mmx6.4mm TSSOP-EP and 3mmx4mm QFN package with exposed thermal pad.

FEATURES

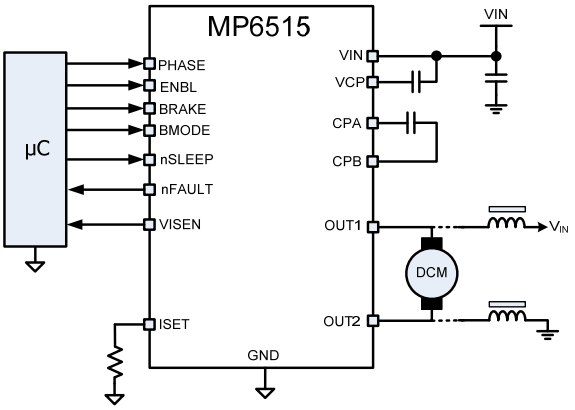
- Wide 5.4V to 35V Input Voltage Range
- 2.8A Peak Output Current
- Internal Full H-Bridge Driver
- PHASE/ENABLE control, input logic (PHASE, EN, BRAKE, BMODE)
- Cycle-by-Cycle Current Regulation/Limit
- Low On Resistance (HS:250mΩ;LS:250mΩ)
- Simple, Versatile Logic Interfaces
- 3.3V and 5V Compatible Logic Supply
- Over-Current Protection
- Over-Voltage Protection
- Thermal Shutdown
- Under-Voltage Lockout
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package

APPLICATIONS

- Solenoid Drivers
- DC Brush Motor Drive

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6515GF*	TSSOP-16 EP (5.0mm × 6.4mm)	*See Below*
MP6515GL**	QFN-20 (3mm x 4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6515GF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP6515GL–Z)

TOP MARKING (TSSOP-16EP)

MPSYYWW
MP6515
LLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6515: Part number
LLLLLL: Lot number

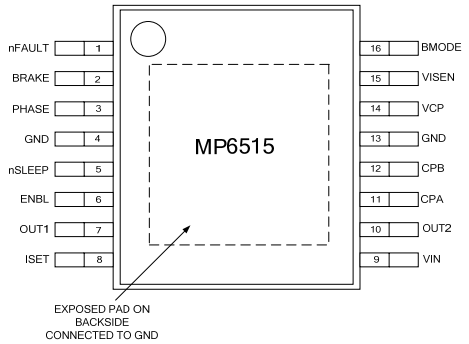
TOP MARKING (QFN-20)

MPYW
6515
LLL

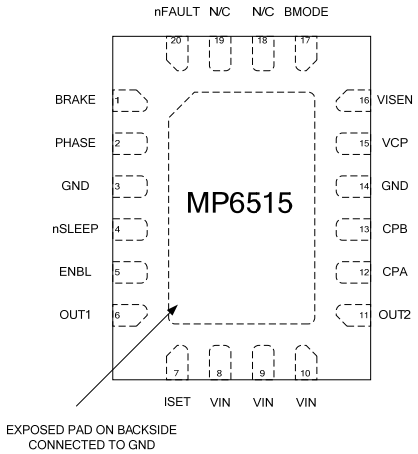
MP: MPS prefix
Y: Year code
W: Week code
6515: First four digits of the part number
LLL: Lot number

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE REFERENCE



TSSOP-16 EP (5.0mm × 6.4mm)



QFN-20 (3mm x 4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... –0.3V to 40V
OUTx voltage ($V_{OUT1/2}$) ..... -0.7V to 40V
VCP, CPB ..... V_{IN} to V_{IN}+6.5V
ESD Rating (HBD) 2kV
ISET ..... -0.3V to 4.5V
All other pins to GND ..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
TSSOP-16 EP……..2.77W
QFN-20 (3mmx4mm)……2.60W
Storage temperature .....-55°C to +150°C
Junction temperature ..... +150°C
Lead temperature (solder) ..... +260°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 5.4V to 35V
Continuous output current (I_{OUT}) ..... ±1.5A(4)
Load current (I_{VISEN}) ..... ±2mA
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}
TSSOP-16 EP	45	10 °C/W
QFN-20 (3mmx4mm)	48	10 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Continuous current depends on PCB layout and ambient temperature.
5) Measured on JESD51-7, 4-layer PCB

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		5.4	24	35	V
Quiescent current	I_Q	V_{IN} = 24V; nSLEEP = 1 No load current		1.5	2	mA
	I_{SLEEP}	V_{IN} = 24V; nSLEEP = 0			1	μA
Charge pump frequency	f_{CP}			680		kHz
Internal MOSFETs						
Output on resistance	R_{HS}	V_{IN} = 24V, I_{OUT} = 1A, T_J = 25°C		0.25	0.3	Ω
		V_{IN} = 24V, I_{OUT} = 1A, T_J = 85°C		0.3		Ω
	R_{LS}	V_{IN} = 24V, I_{OUT} = 1A, T_J = 25°C		0.25	0.3	Ω
		V_{IN} = 24V, I_{OUT} = 1A, T_J = 85°C		0.3		Ω
Body diode forward voltage	V_F	I_{OUT} = 1.5A			1.1	V
Control Logic						
Input logic 'low' threshold	V_{IL}				0.8	V
Input logic 'high' threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		20	μA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		20	μA
Internal pull-down resistance	R_{PD}			515		kΩ
nFault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_O = 5mA			0.5	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	μA
Protection Circuits						
UVLO rising threshold	V_{IN_RISE}			5	5.3	V
UVLO hysteresis	V_{HYS}			310		mV
Input OVP threshold	V_{OVP}		36	38	40	V
Input OVP hysteresis	ΔV_{OVP}			2000		mV
Over-current trip level	I_{OCP1}	Sinking	3.2	4	5	A
	I_{OCP2}	Sourcing	3.2	4	5	A
Over-current deglitch time(6)	t_{OCPD}			500		ns
Over-current retry time	t_{OCP}			0.9		ms
Thermal shutdown	T_{TSD}			165		°C
Thermal shutdown hysteresis	ΔT_{TSD}			30		°C

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_A = +25°C, unless otherwise noted.

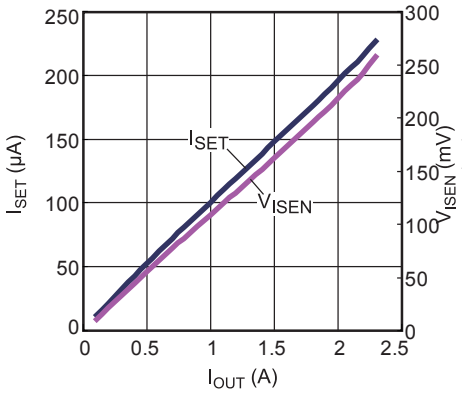
Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Control						
Off time	t_{ITRIP}	After ITRIP		16		μs
ISET current	I_{ISET}		90	100	110	μA/A
Current trip voltage (rising)	$V_{ITRIP-R}$	At VISEN pin	1.44	1.5	1.56	V
Current trip voltage (falling)	$V_{ITRIP-F}$	At VISEN pin	1.15	1.2	1.25	V
VISEN output						
Output voltage accuracy	ΔV_{VISEN}	V_{ISET} > 0.5V	-5		5	%

6) Guarantee by design

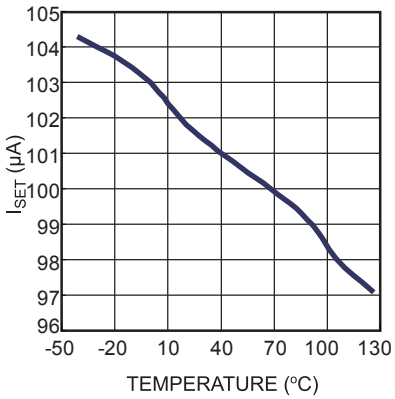
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

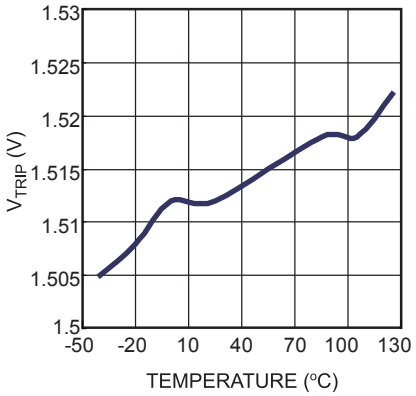
Current Sense
I_{SET} Resistor=1k



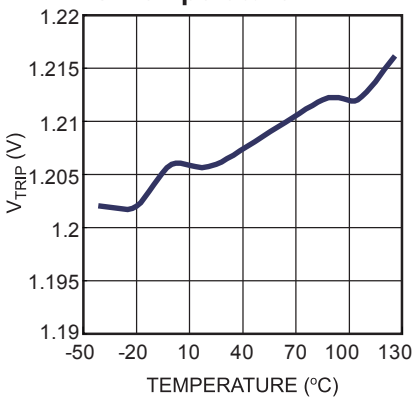
I_{SET} vs. Temperature
I_{OUT} =1A



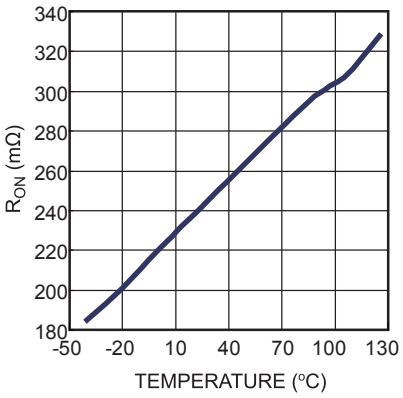
Current Trip Voltage (Rising) vs. Temperature



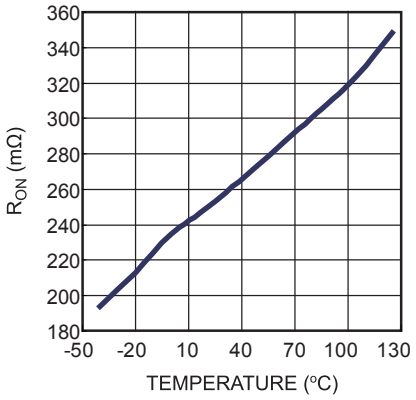
Current Trip Voltage (Falling) vs. Temperature



HS R_{ON} vs. Temperature
I_{OUT} =1A



LS R_{ON} vs. Temperature
I_{OUT} =1A

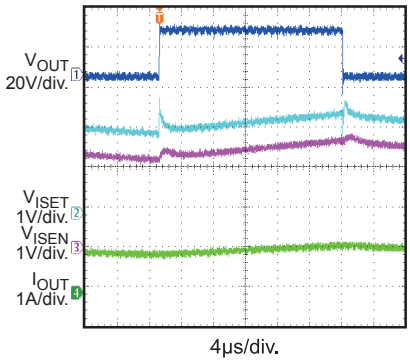


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

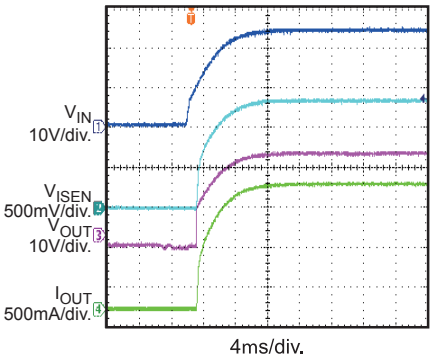
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

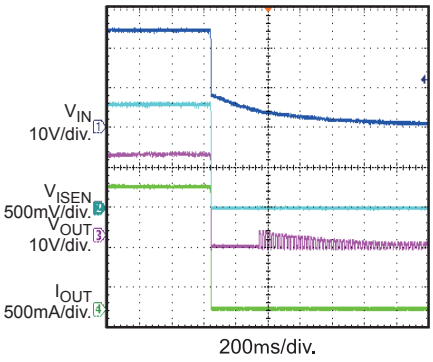
Steady State



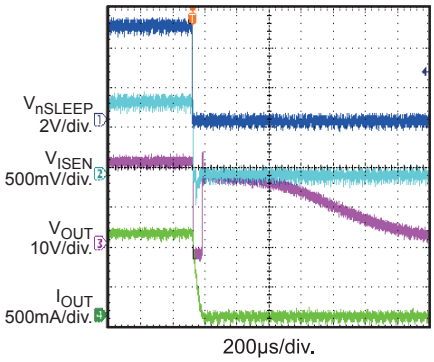
Input Power Start-Up



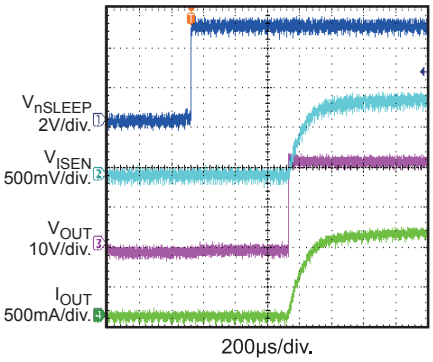
Input Power Shutdown



Sleep Shutdown

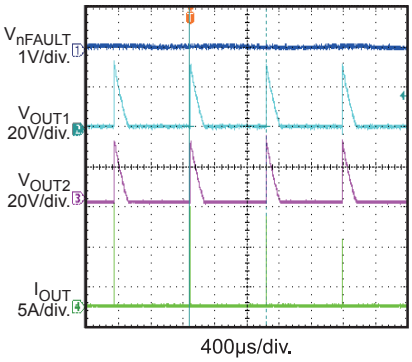


Sleep Start-Up



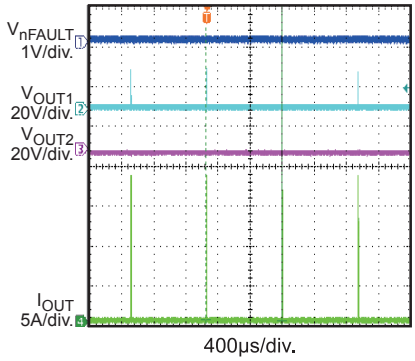
SCP

V_{IN} = 35V, OUT1 Short to OUT2



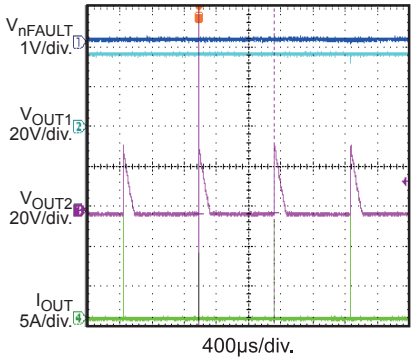
SCP

V_{IN} = 35V, OUT1 Short to GND



SCP

V_{IN} = 35V, OUT1 Short to VIN



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PIN FUNCTIONS

TSSOP16 Pin #	QFN20 Pin #	Name	Description
1	20	nFAULT	**Fault indication.** Open-drain output, logic low when in fault condition (OCP, OTP, OVP).
2	1	BRAKE	**Brake input.** Internal pulldown.
3	2	PHASE	**H-bridge phase input (motor direction).** Internal pulldown.
4, 13	3, 14	GND	**System ground connection.**
5	4	nSLEEP	**Sleep mode input.** Logic low to enter low-power sleep mode. Internal pulldown.
6	5	ENBL	**H-bridge enable input.** High to enable H-bridge. Internal pulldown.
7	6	OUT1	**Output terminal 1.**
8	7	ISET	**Current programming resistor.** Connect a resistor to ground to set the current limit and VISEN output voltage.
9	8, 9, 10	VIN	**Input supply voltage.** Decouple to GND with a minimum 100nF ceramic capacitor to GND.
10	11	OUT2	**Output terminal 2.**
11	12	CPA	**Charge pump flying capacitor.** Connect a 100nF ceramic capacitor between CPA and CPB.
12	13	CPB	
14	15	VCP	**Charge pump output.** Connect a 100nF capacitor to VIN.
15	16	VISEN	**Current sense output voltage.**
16	17	BMODE	**Brake mode.** Internal pulldown.
-	18, 19	NC	**No connection.**
EP	EP	GND	**The exposed pad MUST be connected to ground.**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

BLOCK DIAGRAM

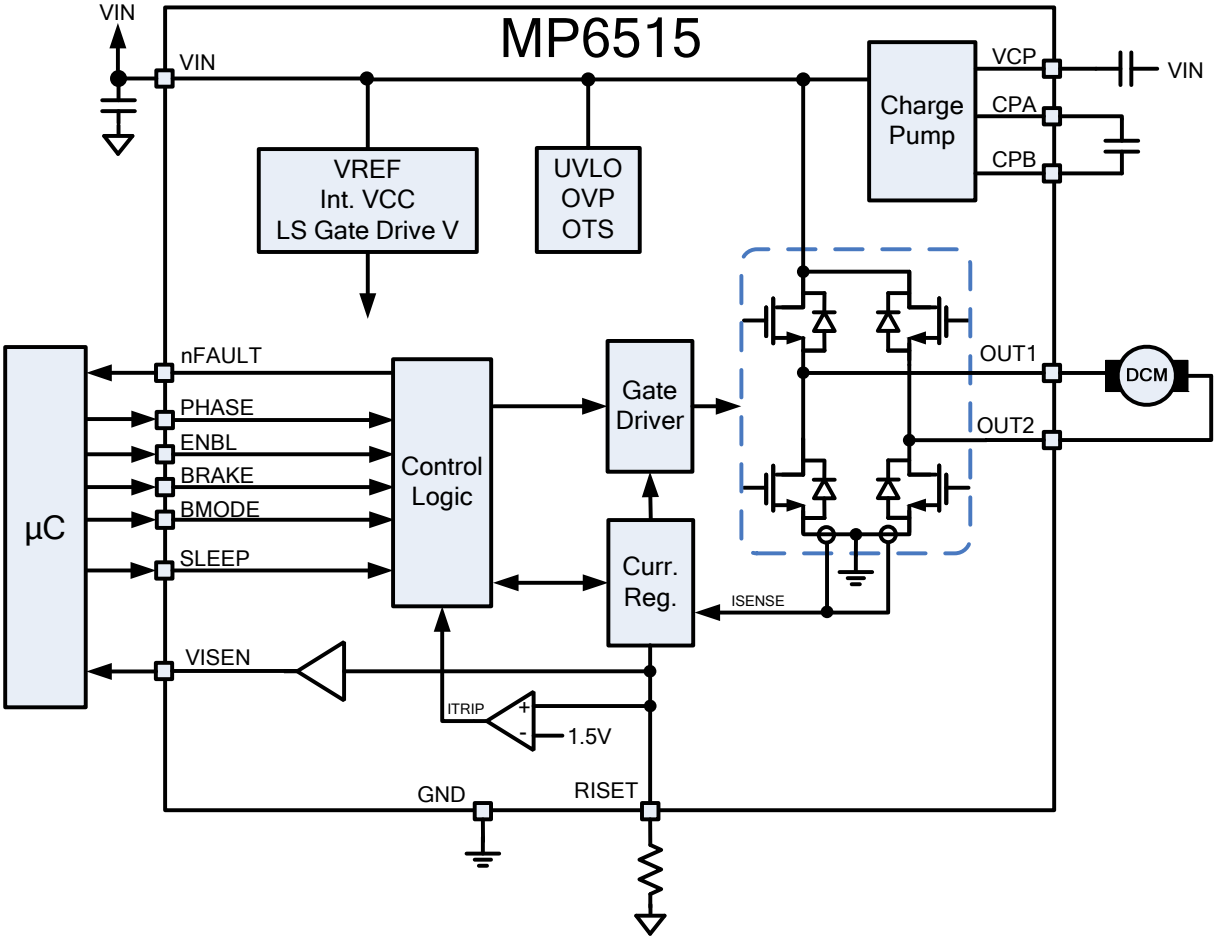


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

OPERATION

The MP6515 is an H-bridge motor driver, which integrates four N-channel power MOSFETs with 2.8A peak current capability. It operates over a wide input voltage range of 5.4V to 35V. It is designed to drive bipolar stepper motors, DC brush motors, solenoids, or other loads.

Current Sensing

The current flowing in the two low-side MOSFETs is sensed with an internal current sensing circuit. A voltage that is proportional to the output current is sourced on VISEN.

The VISEN output voltage scaling is set by a resistor connected between ISET and ground. For 1A of output current, 100μA of current is sourced into the resistor connected to ISET. For example, if a 10kΩ resistor is connected between ISET and ground, the output voltage on VISEN will be 1V/A of output current.

Current is sensed when one of the low-side MOSFETs is turned on, including during slow decay (brake) mode.

The load current applied to VISEN should be kept below 2mA, with no more than 500pF of capacitance.

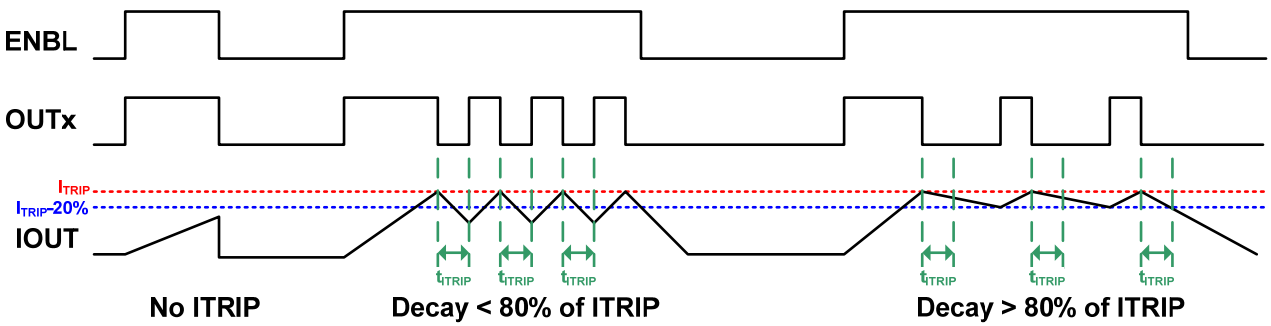
Current Limit/Regulation

The current in the outputs is limited using constant off-time pulse width modulation (PWM) control circuitry. Operation is as follows:

- Initially, a diagonal pair of MOSFETs turns on and drives current through the load.
- The current increases in the load, which is sensed by the internal current sense circuit.
- If the load current reaches the current trip threshold, the H-bridge switches to slow decay mode, with the two low-side MOSFETs turned on.
- After a fixed off-time (t_{ITRIP}), if the load current falls at least 20% below the current limit threshold, the FETs are re-enabled and the cycle repeats.
- If the current is still higher than this level, the off time is extended until the current falls to 20% below the current limit threshold.

The current limit threshold is reached when VISEN reaches 1.5V. For example, with a 10kΩ resistor from ISET to ground, the VISEN voltage is 1V/A of output current. Thererfore, when the current reaches 1.5A, VISET voltage reaches 1.5V, and a current trip occurs.

During current regulation, nFAULT is not activated. See below:



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

Blanking Time

There is often a current spike during the turn-on, due to the body diode's reverse-recovery current or the shunt capacitance of the load. This current spike requires filtering to prevent it from erroneously shutting down the high-side MOSFET. An internal fixed blanking time (t_{OCPD}) blanks the output of the current sense comparator when the outputs are switched. This blanking time also sets the minimum on time for the high-side MOSFET.

Input Logic

For the MP6515, control of the outputs is accomplished through the PHASE, ENBL, BRAKE, and BMODE pins. See Table 1:

Table 1: Output Control Pins

ENBL	PHASE	BRAKE	BMODE	OUT1	OUT2	*Function*
1	0	X	X	L	H	*Reverse*
1	1	X	X	H	L	*Forward*
0	X	1	0	L	L	*Brake (low)*
0	X	1	1	H	H	*Brake (high)*
0	0	0	X	H*	L*	*Sync fast decay*
0	1	0	X	L*	H*	*Sync fast decay*

* As the current through the H-bridge approaches zero, the outputs are tri-stated

nSLEEP Operation

Driving nSLEEP low puts the device into a low power sleep state. In this state, all internal circuits, including the gate drive charge pump, are disabled, and the H-bridge outputs are turned off. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, time (approximately 1ms) must pass before the outputs will operate.

Fault

The MP6515 provides an nFAULT pin, which is driven active low if any of the protection circuits are activated. These fault conditions include over-current, over-temperature, and over-voltage. nFAULT is not driven low when a current limit trip occurs. nFAULT is an open-drain output and requires an external pull-up resistor. When the fault condition is removed, nFAULT is pulled inactive high by the pull-up resistor.

Over-Current Protection

The over-current protection circuit limits the current through each FET by reducing the gate drive to the FET. If the FET remains in the current limit condition for longer than the over-current deglitch time, all MOSFETs in the H-bridge will be disabled, and nFAULT will be driven low. The driver will remain disabled for t_{OCP}, at which point it will be re-enabled automatically. Over-current conditions are sensed on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will result in an over-current shutdown. Note that over-current protection does not use the current sense circuitry used for PWM current control, and it is independent of the ISET resistor value.

Over-Voltage Protection

If the input voltage applied to VIN is higher than the OVP threshold, the H-bridge output will be disabled, and nFAULT will be driven low. This protection is released when VIN drops to a safe level.

Input UVLO Protection

If at any time the voltage on VIN falls below the under-voltage lockout threshold, all circuitry in the device will be disabled and the internal logic will be reset. Operation will resume when VIN rises above the UVLO threshold.

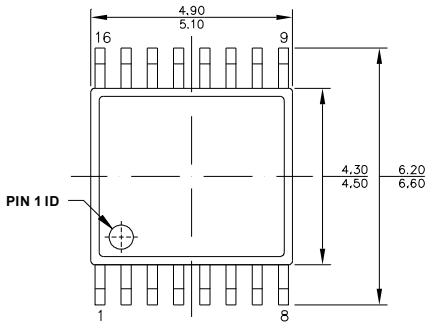
Thermal Shutdown

If the die temperature exceeds safe limits, all MOSFETs in the H-bridge will be disabled, and nFAULT will be driven low. Once the die temperature has fallen to a safe level, operation will resume automatically.

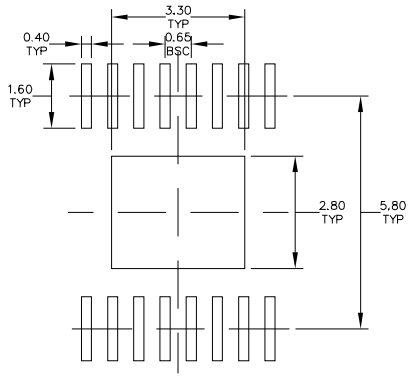
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE INFORMATION

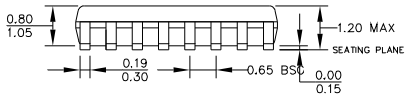
TSSOP16-EP (5.0×6.4mm)



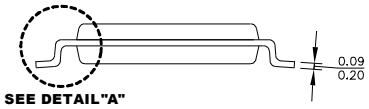
TOP VIEW



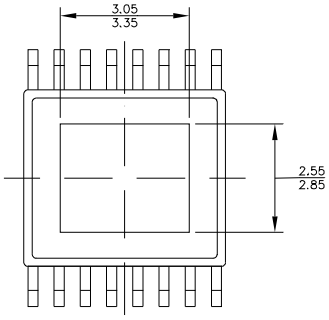
RECOMMENDED LAND PATTERN



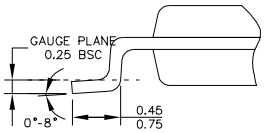
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

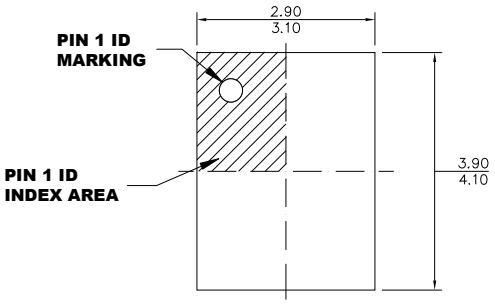
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6) DRAWING IS NOT TO SCALE

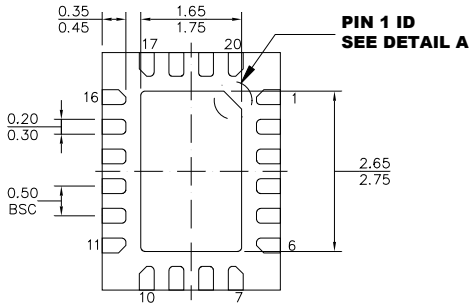
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2019 MPS. All Rights Reserved.

PACKAGE INFORMATION

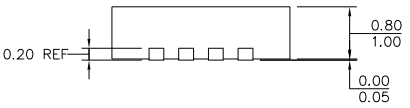
QFN-20 (3mmx4mm)



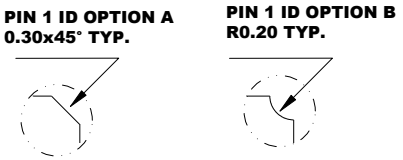
TOP VIEW



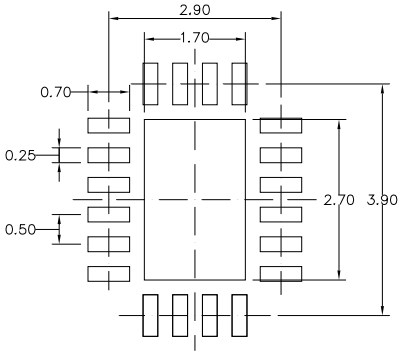
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

© 2019 MPS. All Rights Reserved.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MP6515GL-Z on WIN SOURCE
- Monolithic Power Systems Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management