



**THE DATASHEET OF  
MM74HC4051MTC**



## MM74HC4051 • MM74HC4052 • MM74HC4053

### 8-Channel Analog Multiplexer • Dual 4-Channel Analog Multiplexer • Triple 2-Channel Analog Multiplexer

#### General Description

The MM74HC4051, MM74HC4052 and MM74HC4053 multiplexers are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to  $\pm 6V$  (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for  $V_{CC}$ , ground, and  $V_{EE}$ . This enables the connection of 0–5V logic signals when  $V_{CC} = 5V$  and an analog input range of  $\pm 5V$  when  $V_{EE} = 5V$ . All three devices also have an inhibit control which when HIGH will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to  $V_{CC}$  and ground.

MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is "on", and connects one of the eight inputs to the common output.

MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4-channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4-channel differential multiplexer.

MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configurations. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

#### Features

- Wide analog input voltage range:  $\pm 6V$
- Low "on" resistance:
  - 50 typ. ( $V_{CC} - V_{EE} = 4.5V$ )
  - 30 typ. ( $V_{CC} - V_{EE} = 9V$ )
- Logic level translation to enable 5V logic with  $\pm 5V$  analog signals
- Low quiescent current: 80  $\mu A$  maximum (74HC)
- Matched Switch characteristic

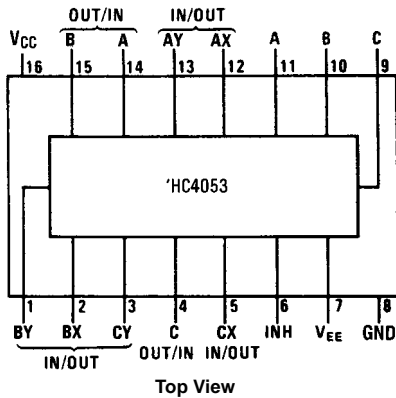
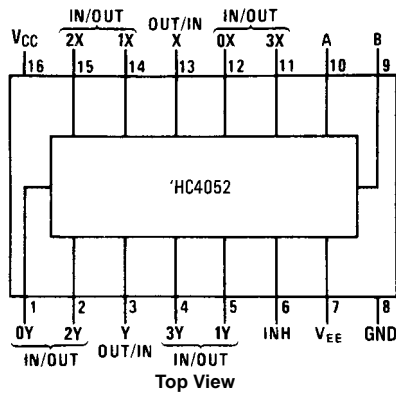
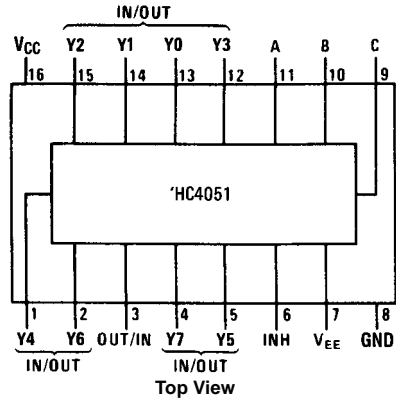
#### Ordering Code:

Order Number	Package Number	Package Description
MM74HC4051M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4051WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC4051SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4051MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4051N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-0010.300" Wide
MM74HC4052M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4052WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC4052SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4052MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4052N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-0010.300" Wide
MM74HC4053M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4053WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC4053SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4053MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4053N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-0010.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP



## Truth Tables

MM744051

Inh	Input			"ON" Channel
	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

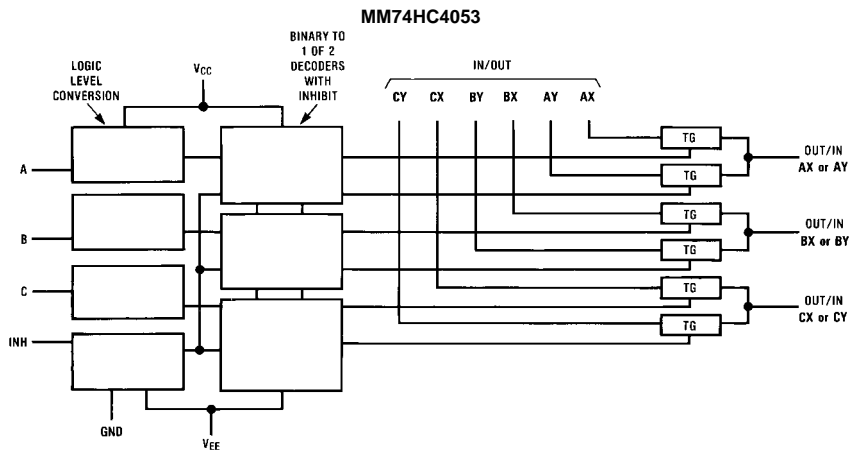
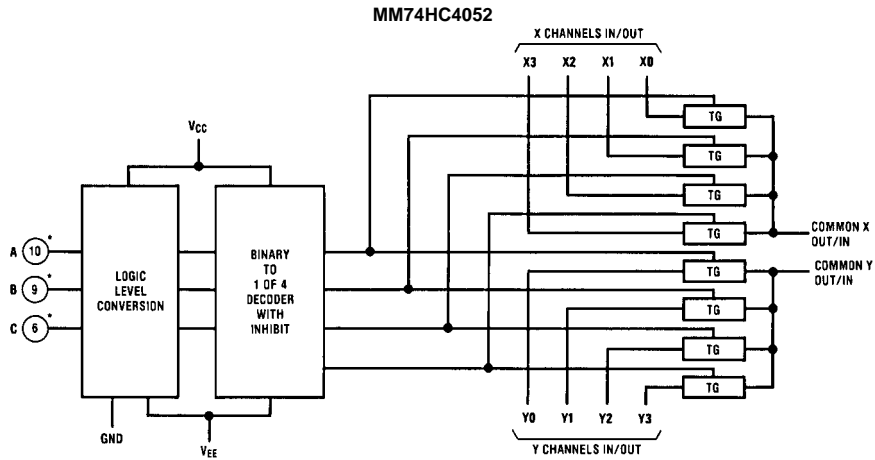
MM744052

Inh	Inputs		"ON" Channels	
	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

MM744053

Inh	Input			"ON" Channels		
	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AX
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AX
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AX
L	H	H	H	CY	BY	AY

# Logic Diagrams



MM74HC4051 • MM74HC4052 • MM74HC4053

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions			
(Note 2)			<b>Min</b>	<b>Max</b>	<b>Units</b>
Supply Voltage ( $V_{CC}$ )	-0.5 to +7.5V	Supply Voltage ( $V_{CC}$ )	2	6	V
Supply Voltage ( $V_{EE}$ )	+0.5 to -7.5V	Supply Voltage ( $V_{EE}$ )	0	-6	V
Control Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC}$ +1.5V	DC Input or Output Voltage			
Switch I/O Voltage ( $V_{IO}$ )	$V_{EE}$ -0.5 to $V_{CC}$ +0.5V	( $V_{IN}$ , $V_{OUT}$ )	0	$V_{CC}$	V
Clamp Diode Current ( $I_{IK}$ , $I_{OK}$ )	$\pm 20$ mA	Operating Temperature Range ( $T_A$ )	-40	+85	$^{\circ}$ C
Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA	Input Rise or Fall Times			
$V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA	( $t_r$ , $t_f$ ) $V_{CC} = 2.0V$		1000	ns
Storage Temperature Range ( $T_{STG}$ )	-65 $^{\circ}$ C to +150 $^{\circ}$ C	$V_{CC} = 4.5V$		500	ns
Power Dissipation ( $P_D$ )		$V_{CC} = 6.0V$		400	ns
(Note 3)	600 mW				
S.O. Package only	500 mW				
Lead Temperature ( $T_L$ )					
(Soldering 10 seconds)	260 $^{\circ}$ C				

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.  
**Note 2:** Unless otherwise specified all voltages are referenced to ground.  
**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/ $^{\circ}$ C from 65 $^{\circ}$ C to 85 $^{\circ}$ C.

**DC Electrical Characteristics (Note 4)**

Symbol	Parameter	Conditions	$V_{EE}$	$V_{CC}$	$T_A = 25^{\circ}\text{C}$		$T_A = -40$ to $85^{\circ}\text{C}$	$T_A = -55$ to $125^{\circ}\text{C}$	Units
					Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage			2.0V	1.5	1.5	1.5	V	
				4.5V	3.15	3.15	3.15	V	
				6.0V	4.2	4.2	4.2	V	
$V_{IL}$	Maximum LOW Level Input Voltage			2.0V	0.5	0.5	0.5	V	
				4.5V	1.35	1.35	1.35	V	
				6.0V	1.8	1.8	1.8	V	
$R_{ON}$	Maximum "ON" Resistance (Note 5)	$V_{INH} = V_{IL}$ , $I_S = 2.0$ mA $V_{IS} = V_{CC}$ to $V_{EE}$ (Figure 1)	GND	4.5V	40	160	200	240	$\Omega$
			-4.5V	4.5V	30	120	150	170	$\Omega$
			-6.0V	6.0V	20	100	125	140	$\Omega$
		$V_{INH} = V_{IL}$ , $I_S = 2.0$ mA $V_{IS} = V_{CC}$ or $V_{EE}$ (Figure 1)	GND	2.0V	100	230	280	320	$\Omega$
			GND	4.5V	40	110	140	170	$\Omega$
			-4.5V	4.5V	20	90	120	140	$\Omega$
$R_{ON}$	Maximum "ON" Resistance Matching	$V_{CTL} = V_{IL}$ $V_{IS} = V_{CC}$ to GND	GND	4.5V	10	20	25	25	$\Omega$
			-4.5V	4.5V	5	10	15	15	$\Omega$
			-6.0V	6.0V	5	10	12	15	$\Omega$
$I_{IN}$	Maximum Control Input Current	$V_{IN} = V_{CC}$ or GND $V_{CC} = 2-6V$				$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu\text{A}$	GND	6.0V		8	80	160	$\mu\text{A}$
			-6.0V	6.0V		16	160	320	$\mu\text{A}$
$I_{IZ}$	Maximum Switch "OFF" Leakage Current (Switch Input)	$V_{OS} = V_{CC}$ or $V_{EE}$ $V_{IS} = V_{EE}$ or $V_{CC}$ $V_{INH} = V_{IH}$ (Figure 2)	GND	6.0V		$\pm 60$	$\pm 600$	$\pm 600$	nA
			-6.0V	6.0V		$\pm 100$	$\pm 1000$	$\pm 1000$	nA
$I_{IZ}$	Maximum Switch "ON" Leakage Current	HC4051 $V_{IS} = V_{CC}$ to $V_{EE}$ $V_{INH} = V_{IL}$ (Figure 3)	GND	6.0V		$\pm 0.2$	$\pm 2.0$	$\pm 2.0$	$\mu\text{A}$
			-6.0V	6.0V		$\pm 0.4$	$\pm 4.0$	$\pm 4.0$	$\mu\text{A}$
		HC4052 $V_{IS} = V_{CC}$ to $V_{EE}$ $V_{INH} = V_{IL}$ (Figure 3)	GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
			-6.0V	6.0V		$\pm 0.2$	$\pm 2.0$	$\pm 2.0$	$\mu\text{A}$
HC4053 $V_{IS} = V_{CC}$ to $V_{EE}$ $V_{INH} = V_{IL}$ (Figure 3)	GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$		
	-6.0V	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$		

## DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>EE</sub>	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	Units
					Typ	Guaranteed Limits			
I <sub>IZ</sub>	Maximum Switch "OFF" Leakage Current (Common Pin)	HC4051 V <sub>OS</sub> = V <sub>CC</sub> or V <sub>EE</sub> V <sub>IS</sub> = V <sub>EE</sub> or V <sub>CC</sub> V <sub>INH</sub> = V <sub>IH</sub>	GND	6.0V		±0.2	±2.0	±2.0	μA
			-6.0V	6.0V		±0.4	±4.0	±4.0	μA
			GND	6.0V		±0.1	±1.0	±1.0	μA
HC4052	V <sub>OS</sub> = V <sub>CC</sub> or V <sub>EE</sub> V <sub>IS</sub> = V <sub>EE</sub> or V <sub>CC</sub> V <sub>INH</sub> = V <sub>IH</sub>	GND	6.0V		±0.1	±1.0	±1.0	μA	
		-6.0V	6.0V		±0.2	±2.0	±2.0	μA	
		GND	6.0V		±0.1	±1.0	±1.0	μA	
HC4053	V <sub>OS</sub> = V <sub>CC</sub> or V <sub>EE</sub> V <sub>IS</sub> = V <sub>EE</sub> or V <sub>CC</sub> V <sub>INH</sub> = V <sub>IH</sub>	GND	6.0V		±0.1	±1.0	±1.0	μA	
		-6.0V	6.0V		±0.1	±1.0	±1.0	μA	
		GND	6.0V		±0.1	±1.0	±1.0	μA	

**Note 4:** For a power supply of 5V ±10% the worst case on resistances (R<sub>ON</sub>) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub> = 5.5V and 4.5V respectively. (The V<sub>IH</sub> value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

**Note 5:** At supply voltages (V<sub>CC</sub>-V<sub>EE</sub>) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

## AC Electrical Characteristics

V<sub>CC</sub> = 2.0V–6.0V, V<sub>EE</sub> = 0V–6V, C<sub>L</sub> = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V <sub>EE</sub>	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	Units
					Typ	Guaranteed Limits			
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay Switch In to Out		GND	2.0V	25	60	75	90	ns
			GND	4.5V	5	12	15	18	ns
			-4.5V	4.5V	4	8	12	14	ns
			-6.0V	6.0V	3	7	11	13	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Switch Turn "ON" Delay	R <sub>L</sub> = 1 kΩ	GND	2.0V	92	355	435	515	ns
			GND	4.5V	69	46	58	69	ns
			-4.5V	4.5V	16	46	58	69	ns
			-6.0V	6.0V	15	41	51	62	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Switch Turn "OFF" Delay		GND	2.0V	65	290	365	435	ns
			GND	4.5V	28	58	73	87	ns
			-4.5V	4.5V	18	37	46	56	ns
			-6.0V	6.0V	16	32	41	48	ns
f <sub>MAX</sub>	Minimum Switch Frequency Response 20 log (V <sub>I</sub> /V <sub>O</sub> ) = 3 dB		GND	4.5V	30				MHz
			-4.5V	4.5V	35				MHz
	Control to Switch Feedthrough Noise	R <sub>L</sub> = 600Ω, f = 1 MHz, C <sub>L</sub> = 50 pF	V <sub>IS</sub> = 4 V <sub>PP</sub>	0V	4.5V	1080			mV
			V <sub>IS</sub> = 8 V <sub>PP</sub>	-4.5V	4.5V	250			mV
	Crosstalk between any Two Switches	R <sub>L</sub> = 600Ω, f = 1 MHz	V <sub>IS</sub> = 4 V <sub>PP</sub>	0V	4.5	-52			dB
			V <sub>IS</sub> = 8 V <sub>PP</sub>	-4.5V	4.5V	-50			dB
	Switch OFF Signal Feedthrough Isolation	R <sub>L</sub> = 600Ω, f = 1 MHz, V <sub>CTL</sub> = V <sub>IL</sub>	V <sub>IS</sub> = 4 V <sub>PP</sub>	0V	4.5V	-42			dB
			V <sub>IS</sub> = 8 V <sub>PP</sub>	-4.5V	4.5V	-44			dB
THD	Sinewave Harmonic Distortion	R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF, f = 1 kHz	V <sub>IS</sub> = 4 V <sub>PP</sub>	0V	4.5V	0.013			%
			V <sub>IS</sub> = 8 V <sub>PP</sub>	-4.5V	4.5V	0.008			%
C <sub>IN</sub>	Maximum Control Input Capacitance				5	10	10	10	pF
C <sub>IN</sub>	Maximum Switch Input Capacitance	Input			15				pF
		4051 Common			90				pF
		4052 Common			45				pF
	4053 Common				30			pF	
C <sub>IN</sub>	Maximum Feedthrough Capacitance				5				pF

### AC Test Circuits and Switching Time Waveforms

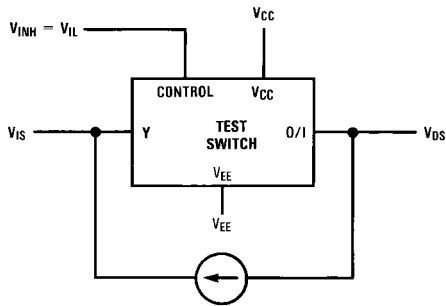


FIGURE 1. "ON" Resistance

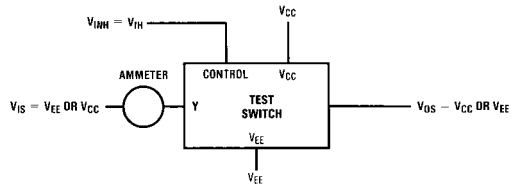


FIGURE 2. "OFF" Channel Leakage Current

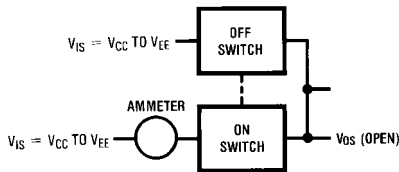


FIGURE 3. "ON" Channel Leakage Current

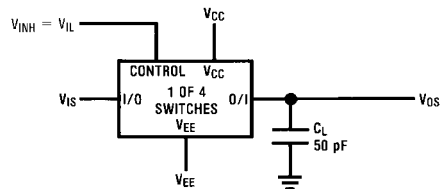


FIGURE 4.  $t_{PHL}$ ,  $t_{PLH}$  Propagation Delay Time Signal Input to Signal Output

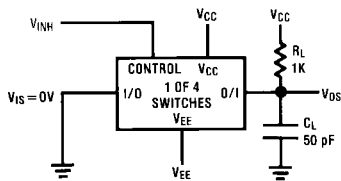
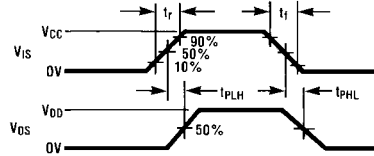


FIGURE 5.  $t_{PZL}$ ,  $t_{PLZ}$  Propagation Delay Time Control to Signal Output

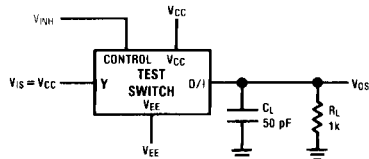
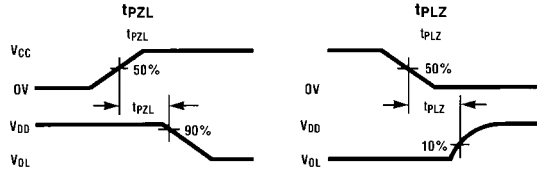
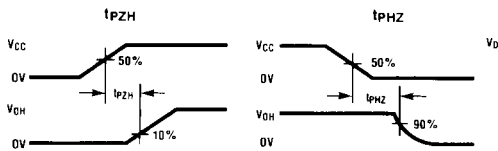


FIGURE 6.  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output



AC Test Circuits and Switching Time Waveforms (Continued)

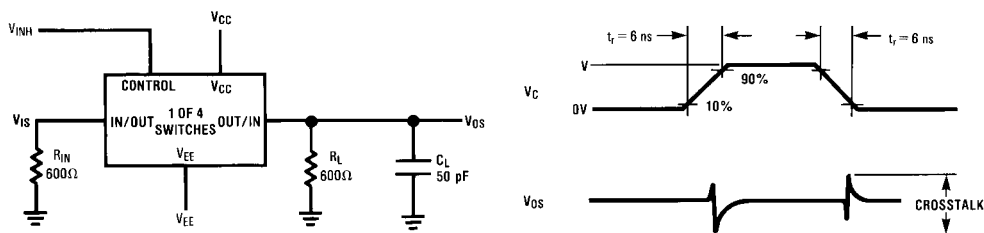


FIGURE 7. Crosstalk: Control Input to Signal Output

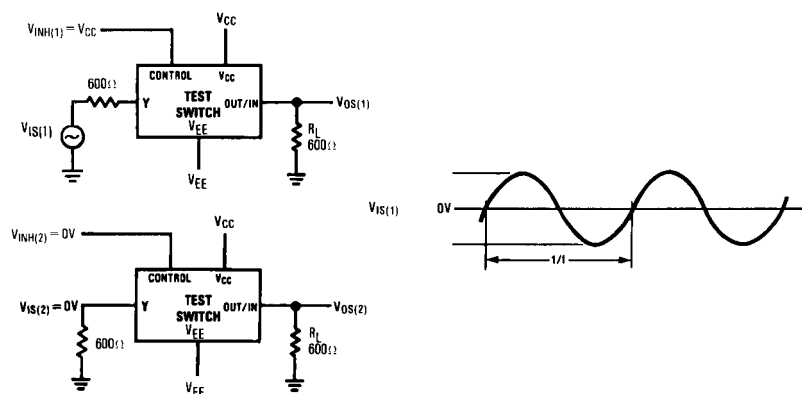
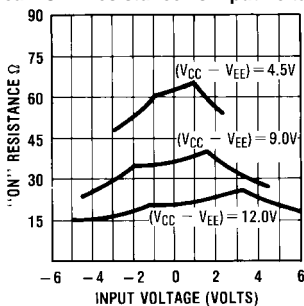


FIGURE 8. Crosstalk Between Any Two Switches

Typical Performance Characteristics

Typical "On" Resistance vs Input Voltage



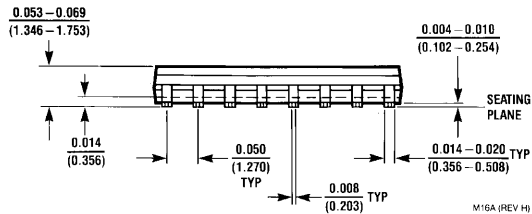
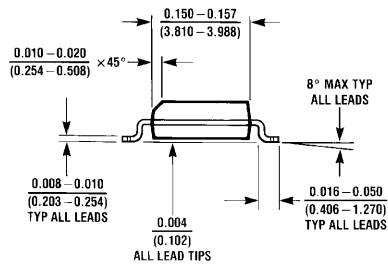
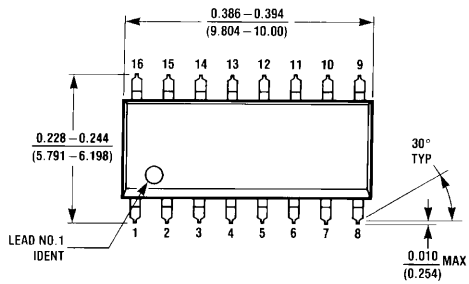
$V_{CC} = -V_{EE}$

Special Considerations

In certain applications the external load-resistor current may include both  $V_{CC}$  and signal line components. To

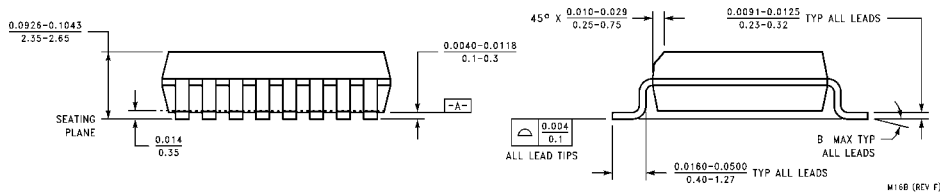
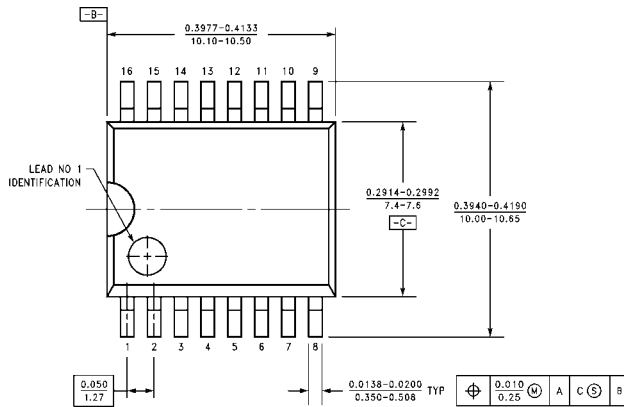
avoid drawing  $V_{CC}$  current when switch current flows into the analog switch pins, the voltage drop across the switch must not exceed 1.2V (calculated from the ON resistance).

**Physical Dimensions** inches (millimeters) unless otherwise noted



M16A (REV H)

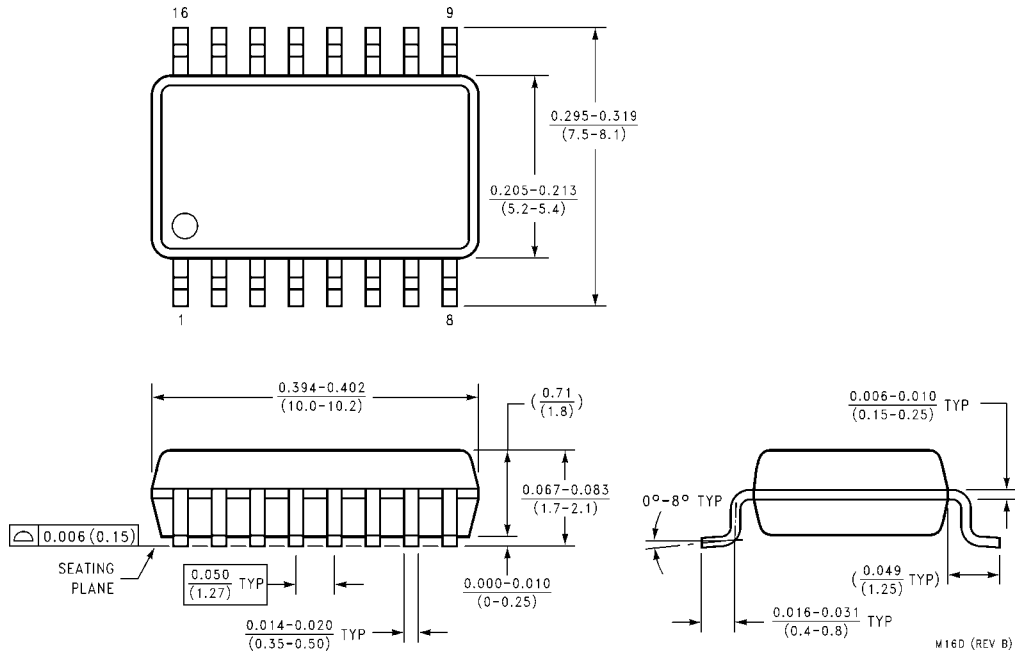
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**



M16B (REV F)

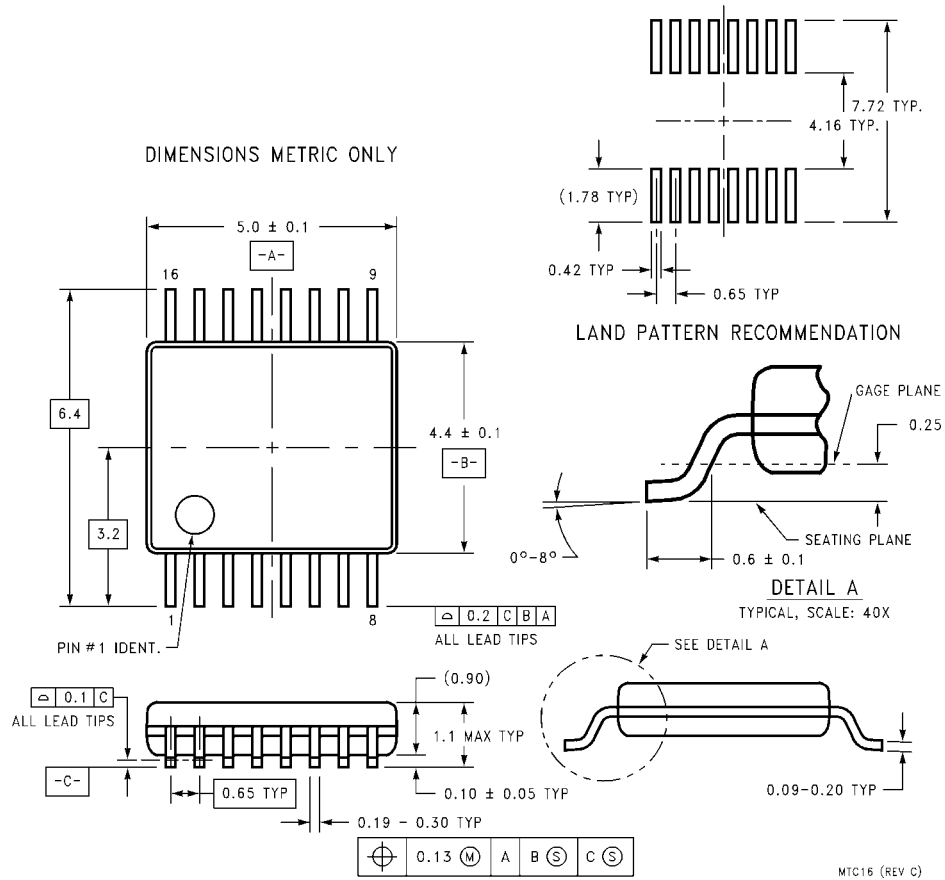
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M16B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

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