



**THE DATASHEET OF
MC56F81768VLH**



MC56F81XXX

MC56F81xxx

Supports MC56F81xxx

Features

- This family of digital signal controllers (DSCs) is based on the 32-bit 56800EX core. On a single chip, each device combines the processing power of a DSP and the functionality of an MCU, with a flexible set of peripherals to support many target applications:
 - Industrial control
 - Motion control
 - Home appliances
 - General-purpose inverters
 - Smart sensors, fire and security systems
 - Wireless charging
 - Switched-mode power supply and power management
 - Uninterruptible power supplies (UPS)
 - Solar inverter
 - Medical monitoring applications
- DSC based on 32-bit 56800EX core
 - Up to 100 MIPS at 100 MHz core frequency in fast mode
 - DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
 - Up to 128 KB flash memory
 - Up to 20 KB data/program RAM
 - Both on-chip flash memory and RAM can be mapped into both program and data memory spaces
 - Boot ROM (supports boot from SCI, I2C)
- Analog
 - Two high-speed, 12-bit ADCs with dynamic x1, x2, and x4 programmable amplifier
 - Two operational amplifiers, programmable gain up to x16
 - Up to four analog comparators with integrated 8-bit DAC references
 - One 12-bit digital-to-analog converters (DAC)
 - On-chip temperature sensors
- One high resolution eFlexPWM module with up to 12 PWM outputs, including 8 channels with 312ps resolution NanoEdge placement
- Communication interfaces
 - Up to two high-speed queued SCI (QSCI) modules with LIN slave functionality
 - One queued SPI (QSPI) modules
 - Up to two LPI2C modules (Support Full PMBus)
- Timers
 - One 16-bit quad timer (1 x 4 16-bit timer)
 - Two 32-bit Periodic Interval Timers (PITs)
 - One Quadrature Decoder (QDC)
- Security and integrity
 - Cyclic Redundancy Check (CRC) generator
 - Windowed Computer operating properly (COP) watchdog
 - External Watchdog Monitor (EWM)
- Clocks
 - On-chip oscillators: 200 kHz, and 8/2MHz IRC
 - Crystal / resonator oscillator
- System
 - 4-channel enhanced DMA controller, supporting up to 63 request sources
 - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
 - Inter-Module Crossbar and Event Generator
 - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging
- Operating characteristics
 - Single supply: 2.7 V to 3.6 V
 - Operation ambient temperature (V): -40 to 105°C
 - Operation ambient temperature (M): -40 to 125°C
- 64-pin LQFP, 48-pin LQFP, 32-pin LQFP and QFN packages

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1 Overview

1.1 Product Family

Table 1. MC56F81xxx Family

| Feature | MC56F81 | | | | | | | | | | | |
|---------------------------------|--|-----|-------------------|-----|--------------------------|-----|--------------------------------|-----|--------------------------|-----|--------------------------|-----|
| | 768 | 748 | 766 | 746 | 763 | 743 | 668 | 648 | 666 | 646 | 663 | 643 |
| Core frequency (MHz) | 100 / 50 | | | | | | | | | | | |
| Flash memory (KB) | 128 | 64 | 128 | 64 | 128 | 64 | 128 | 64 | 128 | 64 | 128 | 64 |
| RAM (KB) | 20 | 12 | 20 | 12 | 20 | 12 | 20 | 12 | 20 | 12 | 20 | 12 |
| Boot ROM | Yes (supports SCI, I2C) | | | | | | | | | | | |
| Inter Module Xbar | Yes | | | | | | | | | | | |
| Event Generator | 4 | | | | | | | | | | | |
| Windowed Watchdog | 1 | | | | | | | | | | | |
| External Watchdog Monitor | 1 | | | | | | | | | | | |
| eDMA | 4CH | | | | | | | | | | | |
| Internal OSC | 8 MHz / 200 KHz | | | | | | | | | | | |
| External Crystal Oscillator | Yes (4 MHz ~ 16 MHz) | | | | | | | | | | | |
| Comparator + 8bit DAC | 4 | | | 3 | | | 4 | | | 3 | | |
| Operational Amplifier | 2 | | | 1 | | | 2 | | | 1 | | |
| 12-bit Cyclic ADC channels | 2 x 8-ch | | 2 x 5-ch | | 2 x 3-ch | | 2 x 8-ch | | 2 x 5-ch | | 2 x 3-ch | |
| NanoEdge PWM: high-resolution | 8-ch | | 6-ch ¹ | | | | — | | | | | |
| Standard PWM with Input capture | 4-ch | | 2-ch | | — | | 8-ch + 4-ch | | 6-ch + 2-ch ¹ | | 6-ch ¹ | |
| QTimers | 4 x 16bit | | | | | | | | | | | |
| Quadrature Decoder | 1 | | | — | | | 1 | | | — | | |
| Periodic Interval Timers | 2 x 32bit | | | | | | | | | | | |
| 12bit DAC | 1 | | | | | | — | | | | | |
| LPI2C (supports Full PMBus) | 2 | | | | 1 | | | | | | | |
| QSCI | 2 | | | | 1 | | 2 | | | | 1 | |
| QSPI | 1 | | | | | | — | | | | | |
| GPIO | 54 | | 39 | | 26 | | 54 | | 39 | | 26 | |
| Operating Temperature | -40°C to 105°C (V temperature) -40°C to 125°C (M temperature) | | | | | | -40°C to 105°C (V temperature) | | | | | |
| Package | 64 LQFP | | 48 LQFP | | 32 LQFP/QFN ² | | 64 LQFP | | 48 LQFP | | 32 LQFP/QFN ² | |

1. Only include the PWM channels with output pins. All internal 8 channels PWM are available through the on-chip inter-module crossbar.
2. The 32 LQFP and 32 QFN packages for this product are not yet available. However, the pin-out and pricing information of these packages are readily available. These devices are then committed for sampling and production based on customer demand.

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
 - Three internal address buses
 - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
 - 32-bit data accesses
 - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
 - 20 addressing modes
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16×16 -bit \rightarrow 32-bit and 32×32 -bit \rightarrow 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- 50 MHz core frequency in normal mode, 100 MHz core frequency in fast mode.
- Operation ambient temperature:

- V Temperature option: -40 °C to 105 °C
- M Temperature option: -40 °C to 125 °C
- Single 3.3 V power supply
- Supply range: $V_{DD} - V_{SS} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{DDA} - V_{SSA} = 2.7 \text{ V to } 3.6 \text{ V}$

1.4 Interrupt Controller

- Five interrupt priority levels
 - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
 - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
 - Interrupt level 3 is highest priority and non-maskable. Its sources include:
 - Illegal instructions
 - Hardware stack overflow
 - SWI instruction
 - EOnce interrupts
 - Misaligned data accesses
 - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.5 Peripheral highlights

1.5.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs
- PWMA with NanoEdge high resolution
 - Fractional delay for enhanced resolution of the PWM period and edge placement
 - Arbitrary PWM edge placement
 - 312 ps PWM frequency and duty-cycle resolution when NanoEdge functionality is enabled.
- PWM outputs can be configured as complementary output pairs or independent outputs

- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:
 - Channels not used for PWM generation can be used for buffered output compare functions.
 - Channels not used for PWM generation can be used for input capture functions.
 - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware (or other PWM) is supported.
- Double-buffered PWM registers
 - Integral reload rates from 1 to 16
 - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware.
- Support for double-switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
 - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event.
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
 - Crossbar module outputs
 - External ADC input, taking into account values set in ADC high and low limit registers
- 312 ps resolution can be enabled for period, duty and deadtime related registers
- Direct phase shift controls among each submodule
- Trigger signal can share the same load frequency as reload signal in each submodule

1.5.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs):
 - 2 x 8-channel external inputs
 - Built-in x1, x2, x4 programmable gain pre-amplifier
 - Maximum ADC clock frequency up to 12.5 MHz, having period as low as 80 ns
 - Single conversion time of 10 ADC clock cycles
 - Additional conversion time of 8 ADC clock cycles
- Support of analog inputs for single-ended and differential (including unipolar differential) conversions
- Sequential and parallel scan modes. Parallel mode includes simultaneous and independent scan modes.

- Samples of each ADC have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by *any* module connected to the internal crossbar module, such as PWM, timer, GPIO, and comparator modules.
- Support for hardware-triggering and software-triggering conversions
- Support for a multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results.
- Current injection protection

1.5.3 Operational Amplifier (OPAMP)

- Up to four sets for rotation configuration
- Configurable gain through internal channels
- Obtain gain through external channels
- Optional clocks for counter
- Low power technology
- Optimize transient response

1.5.4 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, or optionally to an off-chip destination

1.5.5 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 8-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.5.6 Periodic Interrupt Timer (PIT) Modules

- 32-bit counter with programmable count modulo
- PIT0 is master and PIT1 is slave (if synchronizing both PITs)
- The output signals of both PIT0 and PIT1 are internally connected to a peripheral crossbar module
- Can run when the CPU is in Wait/Stop modes. Can also wake up the CPU from Wait/Stop modes.
- In addition to its existing bus clock (up to 50 MHz), 3 alternate clock sources for the counter clock are available:
 - Crystal oscillator output
 - 8 MHz / 2 MHz internal RC output
 - On-chip low-power 200 kHz oscillator

1.5.7 Quadrature Decoder (QDC)

- Includes logic to decode quadrature signals
- Inputs can be connected to a general purpose timer to make low speed velocity measurements
- Configurable digital filter for inputs
- Quadrature decoder filter can be bypassed
- 32-bit position counter capable of modulo counting
- Position counter can be initialized by software or external events
- 16-bit position difference register
- Compare function can indicate when shaft has reached a defined position
- A watchdog timer can detect a non-rotating shaft condition
- Preloadable 16-bit revolution counter
- Maximum count frequency equals the peripheral clock rate
- Optional interrupt when both PHASEA and PHASEB inputs change in the same cycle

1.5.8 Inter-Module Crossbar and Event Generator (EVTG) logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, comparators, quad-timers, eFlexPWMs, EWM, quadrature decoder, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar

- Write-once protection for all registers
- The EVTG module mainly includes two parts: Two AND/OR/INVERT (known simply as the AOI) modules and one configurable Flip-Flop. It supports the generation of a configurable number of EVENT signals. The inputs are from crossbar (XBAR) outputs, and the outputs feed to XBAR inputs.

1.5.9 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

1.5.10 Queued Serial Communications Interface (QSCI) modules with LIN Slave Functionality

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
 - Idle line
 - Address mark
- 1/16 bit-time noise detection
- Support for Local Interconnect Network (LIN) slave operation

1.5.11 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 25 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as the maximum Baud rate / 4096
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers

- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB or LSB as first bit transmitted)

1.5.12 Low Power Inter-Integrated Circuit (LPI2C)

The LPI2C supports:

- Standard, Fast, Fast+ and Ultra Fast modes are supported
- High speed mode (HS) in slave mode
- High speed mode (HS) in master mode, if SCL pin implements current source pull-up (device-specific)
- Multi-master support, including synchronization and arbitration. Multi-master means any number of master nodes can be present. Additionally, master and slave roles may be changed between messages (after a STOP is sent).
- Clock stretching: Sometimes multiple I2C nodes may be driving the lines at the same time. If any I2C node is driving a line low, then that line will be low. I2C nodes that are starting to transmit a logical one (by letting the line float high) can detect that the line is low, and thereby know that another I2C node is active at the same time.
 - When node detection is used on the SCL line, it is called *clock stretching*, and clock stretching is used as a I2C flow control mechanism for multiple slaves.
 - When node detection is used on the SDA line, it is called *arbitration*, and arbitration ensures that there is only one I2C node transmitter at a time.
- General call, 7-bit and 10-bit addressing
- Software reset, START byte and Device ID (also require software support)

The LPI2C master supports:

- Command/transmit FIFO of 4 words.
- Receive FIFO of 4 words.
- Command FIFO will wait for idle I2C bus before initiating transfer
- Command FIFO can initiate (repeated) START and STOP conditions and one or more master-receiver transfers
- STOP condition can be generated from command FIFO, or generated automatically when the transmit FIFO is empty
- Host request input to control the start time of an I2C bus transfer
- Flexible receive data match can generate interrupt on data match and/or discard unwanted data
- Flag and optional interrupt to signal Repeated START condition, STOP condition, loss of arbitration, unexpected NACK, and command word errors
- Supports configurable bus idle timeout and pin-stuck-low timeout

The LPI2C slave supports:

- Separate I2C slave registers to minimize software overhead because of master/slave switching
- Support for 7-bit or 10-bit addressing, address range, SMBus alert and general call address
- Transmit data register that supports interrupt or DMA requests
- Receive data register that supports interrupt or DMA requests
- Software-controllable ACK or NACK, with optional clock stretching on ACK/NACK bit
- Configurable clock stretching, to avoid transmit FIFO underrun and receive FIFO overrun errors
- Flag and optional interrupt at end of packet, STOP condition, or bit error detection

1.5.13 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
 - External crystal oscillator
 - On-chip low-power 200 kHz oscillator
 - System bus (IPBus up to 50 MHz)
 - 8 MHz / 2 MHz IRC
- Support for interrupt generation

1.5.14 External Watchdog Monitor (EWM)

- Monitors external circuit as well as the software flow
- Programmable timeout period
- Interrupt capability prior to timeout
- Independent output (EWM_OUT_b) that places external circuit (but not CPU and peripheral) in a safe mode when EWM timeout occurs
- Selectable reference clock source in support of EN60730 and IEC61508
- Wait mode and Stop mode operation is not supported.
- Selectable clock sources:
 - External crystal oscillator
 - On-chip low-power 200 kHz oscillator
 - System bus (IPBus up to 50 MHz)
 - 8 MHz / 2 MHz IRC

1.5.15 Power supervisor

- Power-on reset (POR) is released after $V_{DD} > 2.7$ V during supply is ramped up; CPU, peripherals, and JTAG/EOnCE controllers exit RESET state
- Brownout reset ($V_{DD} < 2.0$ V)
- Critical warn low-voltage interrupt (LVI 2.2 V)
- Peripheral low-voltage warning interrupt (LVI 2.7 V)

1.5.16 Phase-locked loop

- Output frequency range is optimized from 200 MHz to 550 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

1.5.17 Clock sources

1.5.17.1 On-chip oscillators

- Tunable 8 MHz RC oscillator with 2 MHz at standby mode
- 200 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.5.17.2 Crystal oscillator

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

1.5.18 Cyclic Redundancy Check (CRC) generator

- Hardware 16/32-bit CRC generator
- High-speed hardware CRC calculation
- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Option to transpose input data or output data (CRC result) bitwise or byte-wise,¹ which is required for certain CRC standards
- Option for inversion of final CRC result

1. A bitwise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bitwise transposition.

1.5.19 General Purpose I/O (GPIO)

- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG, RESET_B) default to be GPIO inputs
- Controllable output slew rate

1.6 System Block Diagram

NOTE

The following figure shows the maximum memory configurations supported.

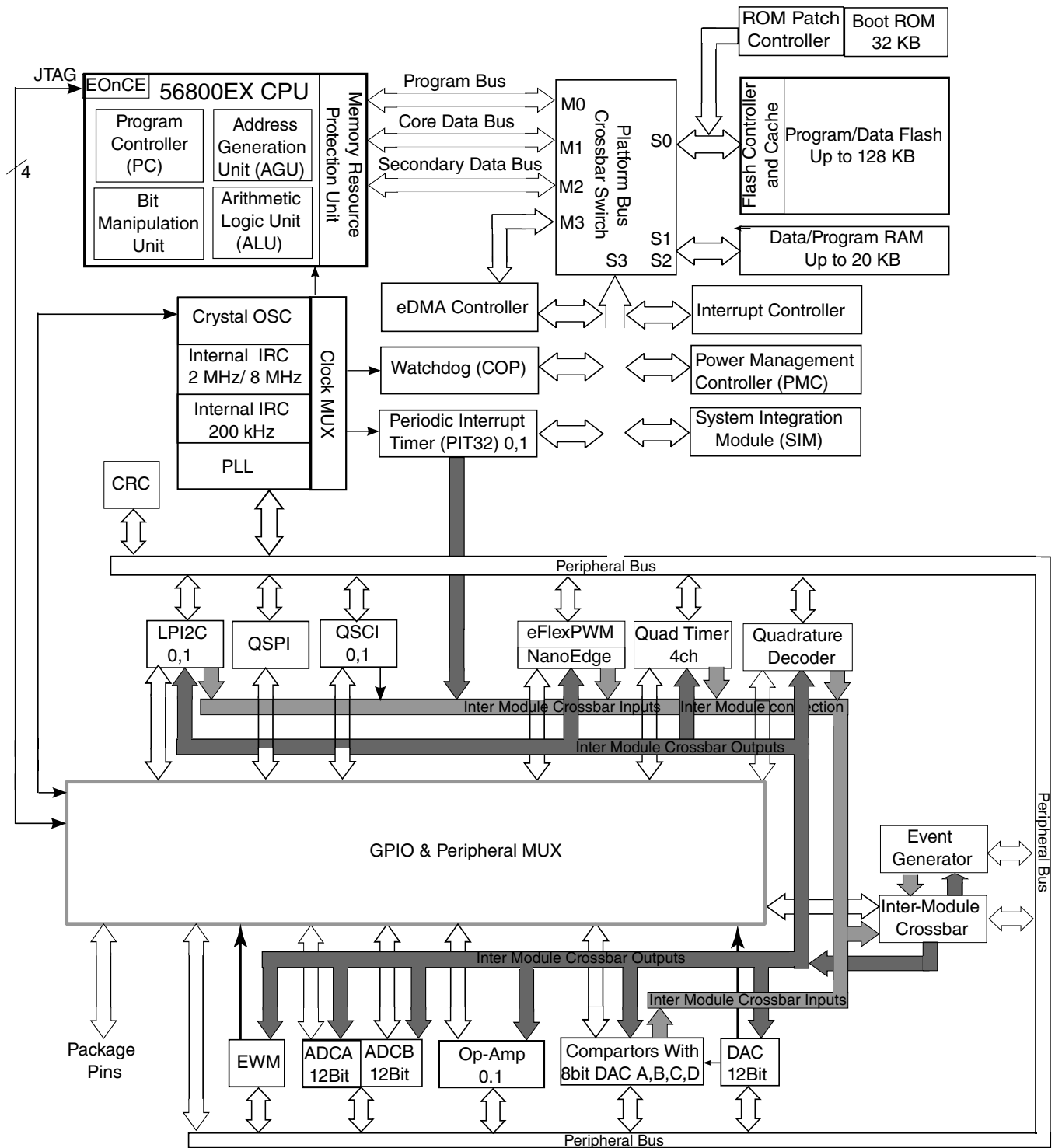


Figure 1. System block diagram

2 MC56F81xxx signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIOx_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

For the MC56F81xxx products, which use 64-pin LQFP, 48-pin LQFP and 32-pin LQFP packages:

Table 2. Signal descriptions

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|------------------|---------|---------|-------------|--------------------------------|--------------------------|--|
| V _{DD} | 29 | — | — | Supply | Supply | I/O Power — Supplies 3.3 V power to the chip I/O interface. |
| | 44 | 32 | — | | | |
| | 60 | 44 | 28 | | | |
| V _{SS} | 30 | 22 | 14 | Supply | Supply | I/O Ground — Provide ground for the device I/O interface. |
| | 43 | 31 | — | | | |
| | 61 | 45 | 29 | | | |
| V _{DDA} | 22 | 15 | 9 | Supply | Supply | Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply. |
| V _{SSA} | 23 | 16 | 10 | Supply | Supply | Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply. |
| V _{CAP} | 26 | 19 | — | On-chip regulator output | On-chip regulator output | Connect a 2.2 μ F or greater bypass capacitor between this pin and V _{SS} to stabilize the core voltage regulator output required for proper device operation. NOTE: The total bypass capacitor value between all V _{CAP} pins and V _{SS} recommends between 4.0 μ F ~ 5.0 μ F. |
| | 57 | 43 | 27 | | | |
| TDI | 64 | 48 | 32 | Input, internal pullup enabled | Input | Test Data Input — Provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI. |
| (GPIOD0) | | | | | Input/Output | GPIO Port D0. |
| TDO | 62 | 46 | 30 | Output | Output | Test Data Output — This tri-state-able pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO. |
| (GPIOD1) | | | | | Input/Output | GPIO Port D1. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|--------------------------------|---------|---------|-------------|----------------------------------|-------------------------|---|
| TCK | 1 | 1 | 1 | Input, internal pulldown enabled | Input | Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pulldown resistor. A Schmitt-trigger input is used for noise immunity. After reset, the default state is TCK. |
| (GPIOD2) | | | | | Input/Output | GPIO Port D2. |
| TMS | 63 | 47 | 31 | Input, internal pullup enabled | Input | Test Mode Select Input — Used to sequence the JTAG TAP controller state machine. It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TMS. NOTE: Always tie the TMS pin to V _{DD} through a 2.2 kΩ resistor if need to keep on-board debug capability. Otherwise, directly tie to V _{DD} . Except being configured as GPIO. |
| (GPIOD3) | | | | | Input/Output | GPIO Port D3. |
| RESET | 2 | 2 | 2 | Input, internal pullup enabled | Input | Reset — A direct hardware reset on the processor. When RESET is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronously with the internal clocks after a fixed number of internal clocks. After reset, the default state is RESET. Recommended a capacitor of 0.1 μF for filtering noise and up to 22 μF for time delay if required. |
| (GPIOD4) | | | | | Input/Open-drain Output | GPIO Port D4 — Can be individually programmed as an input or open-drain output pin. RESET functionality is disabled in this mode and the device can be reset only through Power-On Reset (POR), COP reset, or software reset. |
| GPIOA0 | 13 | 9 | 6 | Input | Input/Output | GPIO Port A0 — After reset, the default state is GPIOA0. |
| (ANA0 & CMPA_IN3 & OPAMPA_IN3) | | | | | Input | ANA0 — ADCA input channel 0. CMPA_IN3 — Analog comparator A input 3 OPAMPA_IN3 — Operational amplifier A input 3 When used as an analog input, the signal goes to ANA0 and CMPA_IN3 and OPAMPA_IN3. ¹ |
| (CMPC_O) | | | | | Output | Analog comparator C output. |
| GPIOA1 | 14 | 10 | 7 | Input | Input/Output | GPIO Port A1 — After reset, the default state is GPIOA1. |
| (ANA1 & CMPA_IN0) | | | | | Input | ANA1 — ADCA input channel 1. CMPA_IN0 — Analog comparator A input 0. OPAMPA_IN0 — Operational amplifier A input 0. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/ QFN | State During Reset | Type | Signal Description |
|---|---------|---------|-----------------|--------------------|------------------|---|
| & OPAMPA_IN0) | | | | | | When used as an analog input, the signal goes to ANA1 and CMPA_IN0 and OPAMPA_IN0. ¹ |
| GPIOA2 | 15 | 11 | 8 | Input | Input/ Output | GPIO Port A2 — After reset, the default state is GPIOA2. |
| (ANA2 & VREFHA & CMPA_IN1 & OPAMPA_IN1) | | | | | Input | ANA2 — ADCA input channel 2. VREFHA — ADCA analog reference high. CMPA_IN1 — Analog comparator A input 1. OPAMPA_IN1 — Operational amplifier A input 1. When used as an analog input, the signal goes to ANA2 (or VREFHA) and CMPA_IN1 and OPAMPA_IN1. ¹ NOTE: ADC input can be configured as either ANA2 or VREFHA in the ADC Calibration Register. |
| GPIOA3 | 16 | 12 | — | Input | Input/ Output | GPIO Port A3 — After reset, the default state is GPIOA3. |
| (ANA3 & VREFLA & CMPA_IN2 & OPAMPA_IN2) | | | | | Input | ANA3 — ADCA input channel 3. VREFLA — ADCA analog reference low. CMPA_IN2 — Analog comparator A input 2. OPAMPA_IN2 — Operational amplifier A input 2. When used as an analog input, the signal goes to ANA3 (or VREFLA) and CMPA_IN2 and OPAMPA_IN2. ¹ NOTE: ADC input can be configured as either ANA3 or VREFLA in the ADC Calibration Register. |
| GPIOA4 | 12 | 8 | — | Input | Input/ Output | GPIO Port A4 — After reset, the default state is GPIOA4. |
| (ANA4 & CMPD_IN0) | | | | | Input | ANA4 — ADCA input channel 4. CMPD_IN0 — Analog comparator D input 0. When used as an analog input, the signal goes to ANA4 and CMPD_IN0. ¹ |
| GPIOA5 | 11 | — | — | Input | Input/ Output | GPIO Port A5 — After reset, the default state is GPIOA5. |
| (ANA5 & CMPD_IN1) | | | | | Input | ANA5 — ADCA input channel 5. CMPD_IN1 — Analog comparator D input 1. When used as an analog input, the signal goes to ANA5 and CMPD_IN1. ¹ |
| GPIOA6 | 10 | — | — | Input | Input/ Output | GPIO Port A6 — After reset, the default state is GPIOA6. |
| (ANA6 & CMPD_IN2) | | | | | Input | ANA6 — ADCA input channel 6. CMPD_IN2 — Analog comparator D input 2. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|--------------------------------|---------|---------|-------------|--------------------|--------------|---|
| | | | | | | When used as an analog input, the signal goes to ANA6 and CMPD_IN2. [†] |
| GPIOA7 | 9 | — | — | Input | Input/Output | GPIO Port A7 — After reset, the default state is GPIOA7. |
| (ANA7 & CMPD_IN3) | | | | | Input | ANA7 — ADCA input channel 7. CMPD_IN3 — Analog comparator D input 3. When used as an analog input, the signal goes to ANA7 and CMPD_IN3. [†] |
| GPIOB0 | 24 | 17 | 11 | Input | Input/Output | GPIO Port B0 — After reset, the default state is GPIOB0. |
| (ANB0 & CMPB_IN3 & OPAMPB_IN3) | | | | | Input | ANB0 — ADCB input channel 0. CMPB_IN3 — Analog comparator B input 3. OPAMPB_IN3 — Operational amplifier B input 3. When used as an analog input, the signal goes to ANB0 and CMPB_IN3 and OPAMPB_IN3. [†] |
| GPIOB1 | 25 | 18 | 12 | Input | Input/Output | GPIO Port B1 — After reset, the default state is GPIOB1. |
| (ANB1 & CMPB_IN0 & OPAMPB_IN0) | | | | | Input | ANB1 — ADCB input channel 1. CMPB_IN0 — Analog comparator B input 0. OPAMPB_IN0 — Operational amplifier B input 0. When used as an analog input, the signal goes to ANB1 and CMPB_IN0 and OPAMPB_IN0. [†] |
| GPIOB2 | 27 | 20 | 13 | Input | Input/Output | GPIO Port B2 — After reset, the default state is GPIOB2. |
| (ANB2 & VREFHB & CMPC_IN3) | | | | | Input | ANB2 — ADCB input channel 2. VREFHB — ADCB analog reference high. CMPC_IN3 — Analog comparator C input 3. When used as an analog input, the signal goes to ANB2 (or VREFHB) and CMPC_IN3. [†] NOTE: ADC input can be configured as either ANB2 or VREFHB in the ADC Calibration Register. |
| GPIOB3 | 28 | 21 | — | Input | Input/Output | GPIO Port B3 — After reset, the default state is GPIOB3. |
| (ANB3 & VREFLB & CMPC_IN0) | | | | | Input | ANB3 — ADCB input channel 3. VREFLB — ADCB analog reference low. CMPC_IN0 — Analog comparator C input 0. When used as an analog input, the signal goes to ANB3 (or VREFHB) and CMPC_IN0. [†] NOTE: ADC input can be configured as either ANB3 or VREFLB in the ADC Calibration Register. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|--------------------------------|---------|---------|-------------|--------------------|--------------|--|
| GPIOB4 | 21 | 14 | — | Input | Input/Output | GPIO Port B4 — After reset, the default state is GPIOB4. |
| (ANB4 & CMPC_IN1) | | | | | Input | ANB4 — ADCB input channel 4. CMPC_IN1 — Analog comparator C input 1. When used as an analog input, the signal goes to ANB4 and CMPC_IN1. ¹ |
| GPIOB5 | 20 | — | — | Input | Input/Output | GPIO Port B5 — After reset, the default state is GPIOB5. |
| (ANB5 & CMPC_IN2) | | | | | Input | ANB5 — ADCB input channel 5. CMPC_IN2 — Analog comparator C input 2. When used as an analog input, the signal goes to ANB5 and CMPC_IN2. ¹ |
| GPIOB6 | 19 | — | — | Input | Input/Output | GPIO Port B6 — After reset, the default state is GPIOB6. |
| (ANB6 & CMPB_IN1 & OPAMPB_IN1) | | | | | Input | ANB6 — ADCB input channel 6. CMPB_IN1 — Analog comparator B input 1. OPAMPB_IN1 — Operational amplifier B input 1. When used as an analog input, the signal goes to ANB6 and CMPB_IN1 and OPAMPB_IN1. ¹ |
| GPIOB7 | 17 | — | — | Input | Input/Output | GPIO Port B7 — After reset, the default state is GPIOB7. |
| (ANB7 & CMPB_IN2 & OPAMPB_IN2) | | | | | Input | ANB7 — ADCB input channel 7. CMPB_IN2 — Analog comparator B input 2. OPAMPB_IN2 — Operational amplifier B input 2. When used as an analog input, the signal goes to ANB7 and CMPB_IN2 and OPAMPB_IN2. ¹ |
| GPIOC0 | 3 | 3 | — | Input | Input/Output | GPIO Port C0 — After reset, the default state is GPIOC0. |
| (EXTAL) | | | | | Input | External crystal oscillator input (EXTAL) connects the internal crystal oscillator input to an external crystal or ceramic resonator. |
| (CLKIN0) | | | | | Input | External clock input 0 to OCCS. NOTE: If this pin is selected as the device's external clock input, then both SIM_GPSCl[C0] bit in SIM and OSCTL1[EXT_SEL] bit in OCCS must be set. The crystal oscillator should be powered down. |
| GPIOC1 | 4 | 4 | — | Input | Input/Output | GPIO Port C1 — After reset, the default state is GPIOC1. |
| (XTAL) | | | | | Output | External crystal oscillator output (XTAL) connects the internal crystal oscillator output to an external crystal or ceramic resonator. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|---------------|---------|---------|-------------|--------------------|--------------|---|
| GPIOC2 | 5 | 5 | 3 | Input | Input/Output | GPIO Port C2 — After reset, the default state is GPIOC2. |
| (TXD0) | | | | | Output | SCI0 transmit data output or transmit/receive in single wire operation. |
| (XB_OUT11) | | | | | Output | Crossbar module output 11. |
| (XB_IN2) | | | | | Input | Crossbar module input 2. |
| (CLKO0) | | | | | Output | Buffered clock output 0. NOTE: The clock source is selected by SIM_CLKOUT[CLKOSEL0] bits in SIM. |
| GPIOC3 | 7 | 6 | 4 | Input | Input/Output | GPIO Port C3 — After reset, the default state is GPIOC3. |
| (TA0) | | | | | Input/Output | Quad timer channel 0 input/output. |
| (CMPA_O) | | | | | Output | Analog comparator A output. |
| (RXD0) | | | | | Input | SCI0 receive data input. |
| (CLKIN1) | | | | | Input | External clock input 1 to OCCS. NOTE: If this pin is selected as device's external clock input, then both SIM_GPSCCL[C3] bits in SIM and OSCTL1[EXT_SEL] bit in OCCS must be set. |
| GPIOC4 | 8 | 7 | 5 | Input | Input/Output | GPIO Port C4 — After reset, the default state is GPIOC4. |
| (TA1) | | | | | Input/Output | Quad timer channel 1 input/output. |
| (CMPB_O) | | | | | Output | Analog comparator B output. |
| (XB_IN8) | | | | | Input | Crossbar module input 8. |
| (OPAMPA_OUT) | | | | | Output | Operational amplifier A output. |
| GPIOC5 | 18 | 13 | — | Input | Input/Output | GPIO Port C5 — After reset, the default state is GPIOC5. |
| (DACA_O) | | | | | Output | 12-bit digital-to-analog output. |
| (XB_IN7) | | | | | Input | Crossbar module input 7. |
| GPIOC6 | 31 | 23 | 15 | Input | Input/Output | GPIO Port C6 — After reset, the default state is GPIOC6. |
| (TA2) | | | | | Input/Output | Quad timer channel 2 input/output. |
| (XB_IN3) | | | | | Input | Crossbar module input 3. |
| (CMP_REF) | | | | | Input | Input 5 of analog comparator A and B and C and D. |
| (SS0_B) | | | | | Input/Output | SPI0 slave select. |
| GPIOC7 | 32 | 24 | — | Input | Input/Output | GPIO Port C7 — After reset, the default state is GPIOC7. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|----------------|---------|---------|-------------|--------------------|-------------------------|---|
| (SS0_B) | | | | | Input/Output | SPI0 slave select. |
| (TXD0) | | | | | Output | SCI0 transmit data output or transmit/receive in single wire operation. |
| (XB_IN8) | | | | | Input | Crossbar module input 8. |
| (XB_OUT6) | | | | | Output | Crossbar module output 6. |
| GPIOC8 | 33 | 25 | 16 | Input | Input/Output | GPIO Port C8 — After reset, the default state is GPIOC8. |
| (MISO0) | | | | | Input/Output | SPI0 master in/slave out. |
| (RXD0) | | | | | Input | SCI0 receive data input. |
| (XB_IN9) | | | | | Input | Crossbar module input 9. |
| GPIOC9 | 34 | 26 | 17 | Input | Input/Output | GPIO Port C9 — After reset, the default state is GPIOC9. |
| (SCLK0) | | | | | Input/Output | SPI0 serial clock. |
| (XB_IN4) | | | | | Input | Crossbar module input 4. |
| (TXD0) | | | | | Output | SCI0 transmit data output or transmit/receive in single wire operation. |
| (XB_OUT8) | | | | | Output | Crossbar module output 8. |
| GPIOC10 | 35 | 27 | 18 | Input | Input/Output | GPIO Port C10 — After reset, the default state is GPIOC10. |
| (MOSI0) | | | | | Input/Output | SPI0 master out/slave. |
| (XB_IN5) | | | | | Input | Crossbar module input 5. |
| (MISO0) | | | | | Input/Output | SPI0 master in/slave out. |
| (XB_OUT9) | | | | | Output | Crossbar module output 9. |
| GPIOC11 | 37 | 29 | — | Input | Input/Output | GPIO Port C11 — After reset, the default state is GPIOC11. |
| (LP_SCLS0) | | | | | Output | I ² C0 secondary serial clock line. NOTE: In 4-wire mode, this is the I ² C slave SCL output for voltage level shift. |
| (LP_SCL1) | | | | | Input/Open-drain Output | I ² C1 serial clock line. NOTE: In 4-wire mode, this is the I ² C slave SCL input. |
| (TXD1) | | | | | Output | SCI1 transmit data output or transmit/receive in single wire operation. |
| (PWMA_0X) | | | | | Output | PWM submodule 0, output X or input capture X. |
| GPIOC12 | 38 | 30 | — | Input | Input/Output | GPIO Port C12 — After reset, the default state is GPIOC12. |
| (LP_SDAS0) | | | | | Output | I ² C0 secondary serial data line. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|----------------|---------|---------|-------------|--------------------|--------------------------------|---|
| | | | | | | NOTE: In 4-wire mode, this is the I ² C slave SDA output for voltage level shift. |
| (LP_SDA1) | | | | | Input/ Open-drain Output | I ² C1 serial data line NOTE: In 4-wire mode, this is the I ² C slave SDA input. |
| (RXD1) | | | | | Input | SCI1 receive data input |
| (PWMA_1X) | | | | | Output | PWM submodule 1, output X or input capture X. |
| GPIOC13 | 49 | 37 | — | Input | Input/ Output | GPIO Port C13 — After reset, the default state is GPIOC13. |
| (TA3) | | | | | Input/ Output | Quad timer channel 3 input/output. |
| (XB_IN6) | | | | | Input | Crossbar module input 6. |
| (EWM_OUT_B) | | | | | Output | External Watchdog Module output. |
| GPIOC14 | 55 | 41 | — | Input | Input/ Output | GPIO Port C14 — After reset, the default state is GPIOC14. |
| (LP_SDA0) | | | | | Input/ Open-drain Output | I ² C0 serial data line NOTE: In 4-wire mode, this is the I ² C slave SDA input. |
| (XB_OUT4) | | | | | Output | Crossbar module output 4. |
| (PWMA_FAULT4) | | | | | Input | PWM Fault input 4 for disabling selected PWM outputs. |
| GPIOC15 | 56 | 42 | — | Input | Input/ Output | GPIO Port C15: After reset, the default state is GPIOC15. |
| (LP_SCL0) | | | | | Input/ Open-drain Output | I ² C0 serial clock line NOTE: In 4-wire mode, this is the I ² C slave SCL input. |
| (XB_OUT5) | | | | | Output | Crossbar module output 5. |
| (PWMA_FAULT5) | | | | | Input | PWM Fault input 5 for disabling selected PWM outputs. |
| GPIOE0 | 45 | 33 | 21 | Input | Input/ Output | GPIO Port E0 — After reset, the default state is GPIOE0. |
| (PWMA_0B) | | | | | Input/ Output | PWM submodule 0, high resolution output B or input capture B. |
| XB_OUT4 | | | | | Output | Crossbar module output 4. |
| GPIOE1 | 46 | 34 | 22 | Input | Input/ Output | GPIO Port E1 — After reset, the default state is GPIOE1. |
| (PWMA_0A) | | | | | Input/ Output | PWM submodule 0, high resolution output A or input capture A. |
| (XB_OUT5) | | | | | Output | Crossbar module output 5. |
| GPIOE2 | 47 | 35 | 23 | Input | Input/ Output | GPIO Port E2 — After reset, the default state is GPIOE2. |
| (PWMA_1B) | | | | | Input/ Output | PWM submodule 1, high resolution output B or input capture B. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|---------------|---------|---------|-------------|--------------------|-------------------------|---|
| XB_OUT6 | | | | | Output | Crossbar module output 6. |
| GPIOE3 | 48 | 36 | 24 | Input | Input/Output | GPIO Port E3 — After reset, the default state is GPIOE3. |
| (PWMA_1A) | | | | | Input/Output | PWM submodule 1, high resolution output A or input capture A. |
| (XB_OUT7) | | | | | Output | Crossbar module output 7. |
| GPIOE4 | 51 | 39 | 25 | Input | Input/Output | GPIO Port E4 — After reset, the default state is GPIOE4. |
| (PWMA_2B) | | | | | Input/Output | PWM submodule 2, high resolution output B or input capture B. |
| (XB_IN2) | | | | | Input | Crossbar module input 2 |
| (LP_SCL1) | | | | | Input/Open-drain Output | I ² C1 serial clock line NOTE: In 4-wire mode, this is the I ² C slave SCL input. |
| (XB_OUT8) | | | | | Output | Crossbar module output 8. |
| GPIOE5 | 52 | 40 | 26 | Input | Input/Output | GPIO Port E5 — After reset, the default state is GPIOE5. |
| (PWMA_2A) | | | | | Input/Output | PWM submodule 2, high resolution output A or input capture A |
| (XB_IN3) | | | | | Input | Crossbar module input 3. |
| (LP_SDA1) | | | | | Input/Open-drain Output | I ² C1 serial data line NOTE: In 4-wire mode, this is the I ² C slave SDA input. |
| (XB_OUT9) | | | | | Output | Crossbar module output 9. |
| GPIOE6 | 53 | — | — | Input | Input/Output | GPIO Port E6 — After reset, the default state is GPIOE6. |
| (PWMA_3B) | | | | | Input/Output | PWM submodule 3, high resolution output B or input capture B. |
| (XB_IN4) | | | | | Input | Crossbar module input 4 |
| (XB_OUT10) | | | | | Output | Crossbar module output 10. |
| GPIOE7 | 54 | — | — | Input | Input/Output | GPIO Port E7 — After reset, the default state is GPIOE7. |
| (PWMA_3A) | | | | | Input/Output | PWM ,submodule 3, high resolution output A or input capture A. |
| (XB_IN5) | | | | | Input | Crossbar module input 5. |
| (XB_OUT11) | | | | | Output | Crossbar module output 11. |
| GPIOF0 | 36 | 28 | — | Input | Input/Output | GPIO Port F0 — After reset, the default state is GPIOF0. |
| (XB_IN6) | | | | | Input | Crossbar module input 6 |
| (OPAMPB_OUT) | | | | | Output | Operational amplifier B output. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|---------------|---------|---------|-------------|--------------------|-------------------------|---|
| GPIOF1 | 50 | 38 | — | Input | Input/Output | GPIO Port F1 — After reset, the default state is GPIOF1. |
| (CLKO1) | | | | | Output | Buffered clock output 1. NOTE: The clock source is selected by SIM_CLKOUT[CLKOSEL1] bits in SIM. |
| (XB_IN7) | | | | | Input | Crossbar module input 7. |
| (CMPD_O) | | | | | Output | Analog comparator D output. |
| GPIOF2 | 39 | — | 19 | Input | Input/Output | GPIO Port F2 — After reset, the default state is GPIOF2. |
| (LP_SCL1) | | | | | Input/Open-drain Output | I ² C1 serial clock line NOTE: In 4-wire mode, this is the I ² C slave SCL input. |
| (XB_OUT6) | | | | | Output | Crossbar module output 6 |
| (LP_SDA0) | | | | | Input/Open-drain Output | I ² C0 serial data line. NOTE: In 4-wire mode, this is the I ² C slave SDA input. |
| GPIOF3 | 40 | — | 20 | Input | Input/Output | GPIO Port F3 — After reset, the default state is GPIOF3. |
| (LP_SDA1) | | | | | Input/Open-drain Output | I ² C1 serial data line. NOTE: In 4-wire mode, this is the I ² C slave SDA input. |
| (XB_OUT7) | | | | | Output | Crossbar module output 7 |
| (LP_SCL0) | | | | | Input/Output | I ² C0 serial clock line NOTE: In 4-wire mode, this is the I ² C slave SCL input. |
| GPIOF4 | 41 | — | — | Input | Input/Output | GPIO Port F4 — After reset, the default state is GPIOF4. |
| (TXD1) | | | | | Output | SCI1 transmit data output or transmit/receive in single wire operation |
| (XB_OUT8) | | | | | Output | Crossbar module output 8 |
| (PWMA_0X) | | | | | Input/Output | PWM submodule 0, output X or input capture X. |
| (PWMA_FAULT6) | | | | | Input | PWM Fault input 6 for disabling selected PWM outputs. |
| GPIOF5 | 42 | — | — | Input | Input/Output | GPIO Port F5 — After reset, the default state is GPIOF5. |
| (RXD1) | | | | | Input | SCI1 receive data input. |
| (XB_OUT9) | | | | | Output | Crossbar module output 9. |
| (PWMA_1X) | | | | | Input/Output | PWM submodule 1, output X or input capture X. |
| (PWMA_FAULT7) | | | | | Input | PWM Fault input 7 for disabling selected PWM outputs. |

Table continues on the next page...

Table 2. Signal descriptions (continued)

| Signal Name | 64 LQFP | 48 LQFP | 32 LQFP/QFN | State During Reset | Type | Signal Description |
|---------------|---------|---------|-------------|--------------------|--------------|---|
| GPIOF6 | 58 | — | — | Input | Input/Output | GPIO Port F6 — After reset, the default state is GPIOF6. |
| (PWMA_3X) | | | | | Input/Output | PWM submodule 3, output X or input capture X. |
| LP_SCLS1 | | | | | Output | I ² C1 secondary serial clock line. NOTE: In 4-wire mode, this is the I ² C slave SCL output for voltage level shift. |
| (XB_IN2) | | | | | Input | Crossbar module input 2. |
| GPIOF7 | 59 | — | — | Input | Input/Output | GPIO Port F7 — After reset, the default state is GPIOF7. |
| (CMPC_O) | | | | | Output | Analog comparator C output. |
| LP_SDAS1 | | | | | Output | I ² C1 secondary serial data line. NOTE: In 4-wire mode, this is the I ² C slave SDA output for voltage level shift. |
| (XB_IN3) | | | | | Input | Crossbar module input 3. |
| GPIOF8 | 6 | — | — | Input | Input/Output | GPIO Port F8 — After reset, the default state is GPIOF8. |
| (RXD0) | | | | | Input | SCI0 receive data input. |
| (XB_OUT10) | | | | | Output | Crossbar module output 10. |
| (CMPD_O) | | | | | Output | Analog comparator D output. |
| (PWMA_2X) | | | | | Output | PWM submodule 2, output X or input capture X. |

1. The glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.

3 Signal groups

The input and output signals of the MC56F81xxx are organized into functional groups, as detailed in the following table.

Table 3. Functional Group Pin Allocations

| Functional Group | Number of Pins | | |
|--|----------------|--------|--------|
| | 32LQFP | 48LQFP | 64LQFP |
| Power Inputs (V_{DD} , V_{DDA}), Power output (V_{CAP}) | 3 | 5 | 6 |
| Ground (V_{SS} , V_{SSA}) | 3 | 4 | 4 |
| Reset | 1 | 1 | 1 |
| eFlexPWM outputs high resolution PWM | 6 | 6 | 8 |
| eFlexPWM outputs without high resolution PWM | 0 | 2 | 6 |
| Queued Serial Peripheral Interface (QSPI0) ports | 4 | 5 | 5 |
| Queued Serial Communications Interface (QSCI0 and QSCI1 ¹) ports | 4 | 7 | 10 |

Table continues on the next page...

**Table 3. Functional Group Pin Allocations
(continued)**

| Functional Group | Number of Pins | | |
|---|----------------|----------------|--------|
| | 32LQFP | 48LQFP | 64LQFP |
| Inter-Integrated Circuit Interface (LPI ² C0 and LPI ² C1) ports | 4 ² | 6 ³ | 10 |
| 12-bit Analog-to-Digital Converter (ADC) inputs | 6 | 10 | 16 |
| Analog Comparator inputs/outputs | 7/3 | 11/4 | 17/6 |
| Analog Operational Amplifier inputs/outputs | 5/1 | 6/2 | 8/2 |
| 12-bit Digital-to-Analog output | 0 | 1 | 1 |
| Quad Timer Module (TMR) ports | 3 | 4 | 4 |
| Inter-Module Crossbar inputs/outputs | 8/11 | 13/12 | 17/19 |
| Clock inputs/outputs | 1/1 | 2/2 | 2/2 |
| JTAG / Enhanced On-Chip Emulation (EOnCE) | 4 | 4 | 4 |

1. Not available in 32-pin package.
2. 4-wire mode does not support.
3. Only LPI²C0 supports 4-wire mode.

4 Pinout

4.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 64 LQFP | 48 LQFP | 32 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---------|---------|---------|----------|---------|--------------------------|----------|--------|------------|
| 1 | 1 | 1 | TCK | TCK | GPIOD2 | | | |
| 2 | 2 | 2 | RESET_B | RESET_B | GPIOD4 | | | |
| 3 | 3 | — | GPIOC0 | GPIOC0 | EXTAL | CLKIN0 | | |
| 4 | 4 | — | GPIOC1 | GPIOC1 | XTAL | | | |
| 5 | 5 | 3 | GPIOC2 | GPIOC2 | TXD0 | XB_OUT11 | XB_IN2 | CLKO0 |
| 6 | — | — | GPIOF8 | GPIOF8 | RXD0 | XB_OUT10 | CMPD_O | PWMA_2X |
| 7 | 6 | 4 | GPIOC3 | GPIOC3 | TA0 | CMPA_O | RXD0 | CLKIN1 |
| 8 | 7 | 5 | GPIOC4 | GPIOC4 | TA1 | CMPB_O | XB_IN8 | OPAMPA_OUT |
| 9 | — | — | GPIOA7 | GPIOA7 | ANA7+CMPD_IN3 | | | |
| 10 | — | — | GPIOA6 | GPIOA6 | ANA6+CMPD_IN2 | | | |
| 11 | — | — | GPIOA5 | GPIOA5 | ANA5+CMPD_IN1 | | | |
| 12 | 8 | — | GPIOA4 | GPIOA4 | ANA4+CMPD_IN0 | | | |
| 13 | 9 | 6 | GPIOA0 | GPIOA0 | ANA0+CMPA_IN3+OPAMPA_IN3 | CMPC_O | | |

| 64 LQFP | 48 LQFP | 32 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|------------|------------|------------|----------|---------|---------------------------------|---------|---------|-------------|
| 14 | 10 | 7 | GPIOA1 | GPIOA1 | ANA1+CMPA_IN0+OPAMPA_IN0 | | | |
| 15 | 11 | 8 | GPIOA2 | GPIOA2 | ANA2+VREFHA+CMPA_IN1+OPAMPA_IN1 | | | |
| 16 | 12 | — | GPIOA3 | GPIOA3 | ANA3+VREFLA+CMPA_IN2+OPAMPA_IN2 | | | |
| 17 | — | — | GPIOB7 | GPIOB7 | ANB7+CMPB_IN2+OPAMPB_IN2 | | | |
| 18 | 13 | — | GPIOC5 | GPIOC5 | DACA_0 | XB_IN7 | | |
| 19 | — | — | GPIOB6 | GPIOB6 | ANB6+CMPB_IN1+OPAMPB_IN1 | | | |
| 20 | — | — | GPIOB5 | GPIOB5 | ANB5+CMPC_IN2 | | | |
| 21 | 14 | — | GPIOB4 | GPIOB4 | ANB4+CMPC_IN1 | | | |
| 22 | 15 | 9 | VDDA | VDDA | | | | |
| 23 | 16 | 10 | VSSA | VSSA | | | | |
| 24 | 17 | 11 | GPIOB0 | GPIOB0 | ANB0+CMPB_IN3+OPAMPB_IN3 | | | |
| 25 | 18 | 12 | GPIOB1 | GPIOB1 | ANB1+CMPB_IN0+OPAMPB_IN0 | | | |
| 26 | 19 | — | VCAP | VCAP | | | | |
| 27 | 20 | 13 | GPIOB2 | GPIOB2 | ANB2+VREFHB+CMPC_IN3 | | | |
| 28 | 21 | — | GPIOB3 | GPIOB3 | ANB3+VREFLB+CMPC_IN0 | | | |
| 29 | — | — | VDD | VDD | | | | |
| 30 | 22 | 14 | VSS | VSS | | | | |
| 31 | 23 | 15 | GPIOC6 | GPIOC6 | TA2 | XB_IN3 | CMP_REF | SS0_B |
| 32 | 24 | — | GPIOC7 | GPIOC7 | SS0_B | TXD0 | XB_IN8 | XB_OUT6 |
| 33 | 25 | 16 | GPIOC8 | GPIOC8 | MISO0 | RXD0 | XB_IN9 | |
| 34 | 26 | 17 | GPIOC9 | GPIOC9 | SCLK0 | XB_IN4 | TXD0 | XB_OUT8 |
| 35 | 27 | 18 | GPIOC10 | GPIOC10 | MOSI0 | XB_IN5 | MISO0 | XB_OUT9 |
| 36 | 28 | — | GPIOF0 | GPIOF0 | XB_IN6 | | | OPAMPB_OUT |
| 37 | 29 | — | GPIOC11 | GPIOC11 | LP_SCLS0 | LP_SCL1 | TXD1 | PWMA_0X |
| 38 | 30 | — | GPIOC12 | GPIOC12 | LP_SDA0 | LP_SDA1 | RXD1 | PWMA_1X |
| 39 | — | 19 | GPIOF2 | GPIOF2 | LP_SCL1 | XB_OUT6 | LP_SDA0 | |
| 40 | — | 20 | GPIOF3 | GPIOF3 | LP_SDA1 | XB_OUT7 | LP_SCL0 | |
| 41 | — | — | GPIOF4 | GPIOF4 | TXD1 | XB_OUT8 | PWMA_0X | PWMA_FAULT6 |
| 42 | — | — | GPIOF5 | GPIOF5 | RXD1 | XB_OUT9 | PWMA_1X | PWMA_FAULT7 |
| 43 | 31 | — | VSS | VSS | | | | |
| 44 | 32 | — | VDD | VDD | | | | |
| 45 | 33 | 21 | GPIOE0 | GPIOE0 | PWMA_0B | | | XB_OUT4 |
| 46 | 34 | 22 | GPIOE1 | GPIOE1 | PWMA_0A | | | XB_OUT5 |
| 47 | 35 | 23 | GPIOE2 | GPIOE2 | PWMA_1B | | | XB_OUT6 |
| 48 | 36 | 24 | GPIOE3 | GPIOE3 | PWMA_1A | | | XB_OUT7 |

Pinout

| 64 LQFP | 48 LQFP | 32 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|------------|------------|------------|----------|---------|---------|---------|-------------|----------|
| 49 | 37 | — | GPIOC13 | GPIOC13 | TA3 | XB_IN6 | EWM_OUT_B | |
| 50 | 38 | — | GPIOF1 | GPIOF1 | CLKO1 | XB_IN7 | CMPD_O | |
| 51 | 39 | 25 | GPIOE4 | GPIOE4 | PWMA_2B | XB_IN2 | LP_SCL1 | XB_OUT8 |
| 52 | 40 | 26 | GPIOE5 | GPIOE5 | PWMA_2A | XB_IN3 | LP_SDA1 | XB_OUT9 |
| 53 | — | — | GPIOE6 | GPIOE6 | PWMA_3B | XB_IN4 | | XB_OUT10 |
| 54 | — | — | GPIOE7 | GPIOE7 | PWMA_3A | XB_IN5 | | XB_OUT11 |
| 55 | 41 | — | GPIOC14 | GPIOC14 | LP_SDA0 | XB_OUT4 | PWMA_FAULT4 | |
| 56 | 42 | — | GPIOC15 | GPIOC15 | LP_SCL0 | XB_OUT5 | PWMA_FAULT5 | |
| 57 | 43 | 27 | VCAP | VCAP | | | | |
| 58 | — | — | GPIOF6 | GPIOF6 | | PWMA_3X | LP_SCLS1 | XB_IN2 |
| 59 | — | — | GPIOF7 | GPIOF7 | | CMPC_O | LP_SDAS1 | XB_IN3 |
| 60 | 44 | 28 | VDD | VDD | | | | |
| 61 | 45 | 29 | VSS | VSS | | | | |
| 62 | 46 | 30 | TDO | TDO | GPIOD1 | | | |
| 63 | 47 | 31 | TMS | TMS | GPIOD3 | | | |
| 64 | 48 | 32 | TDI | TDI | GPIOD0 | | | |

4.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

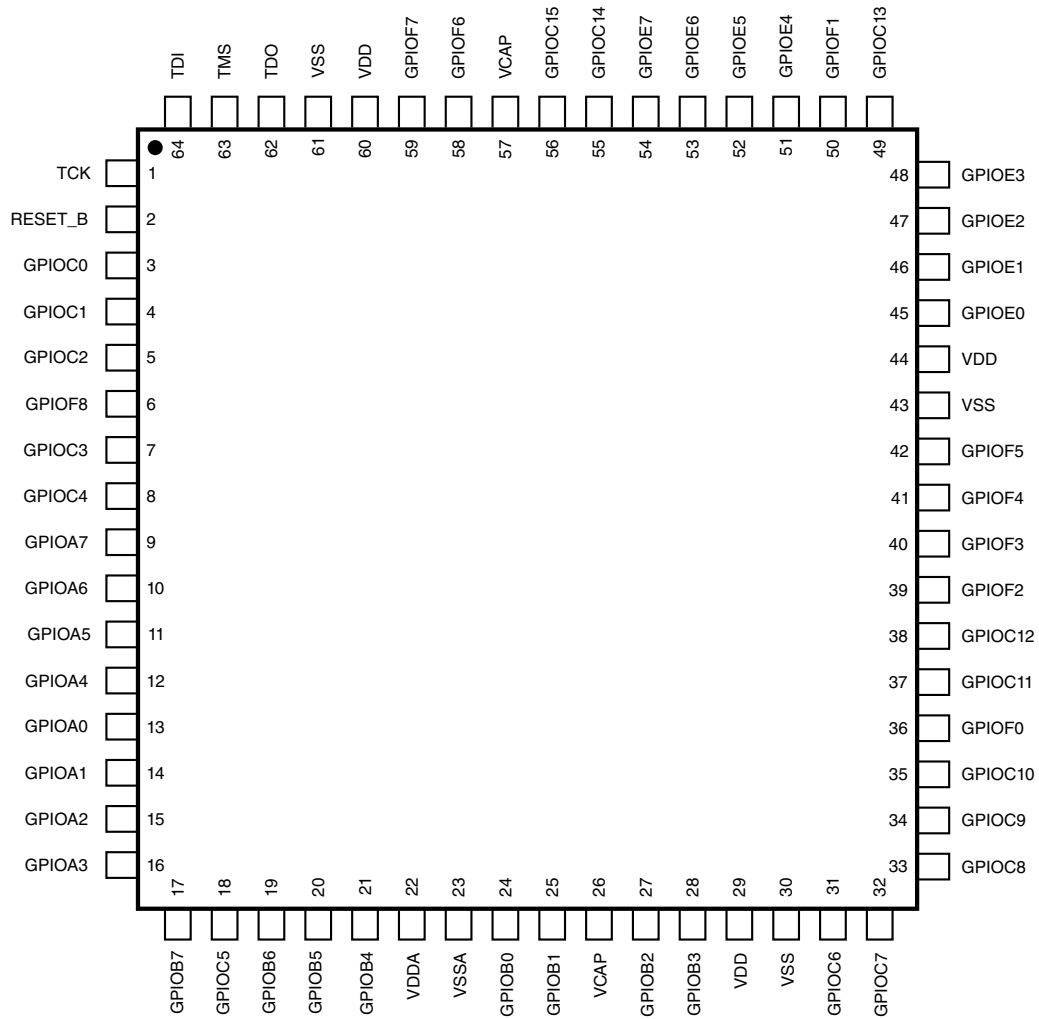


Figure 2. 64-pin LQFP

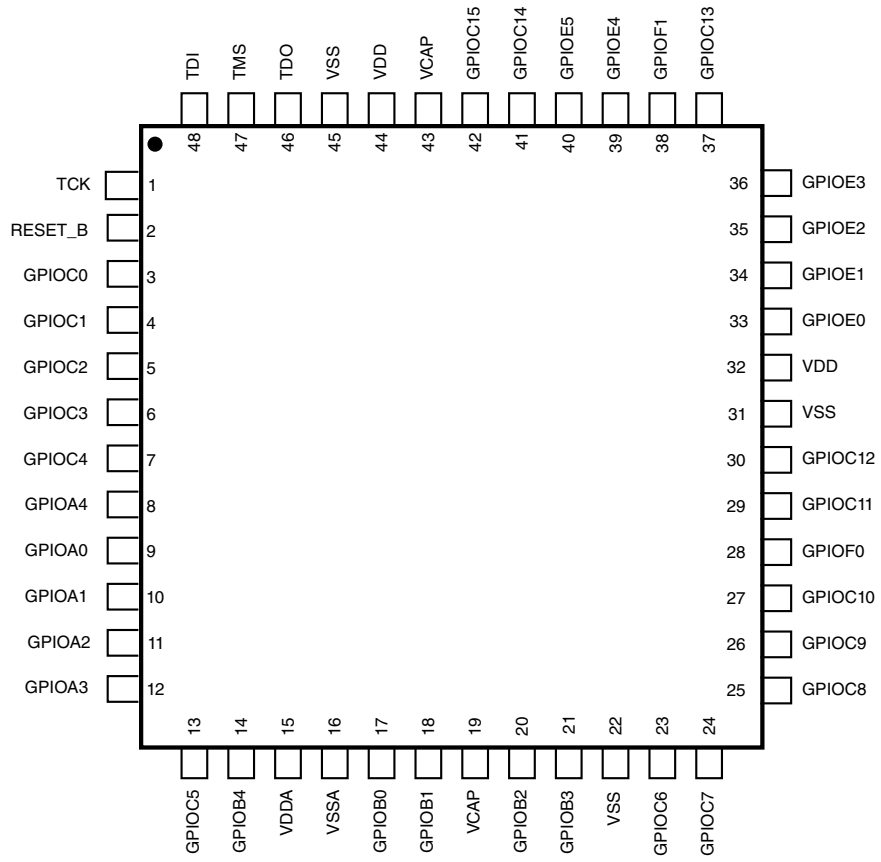


Figure 3. 48-pin LQFP

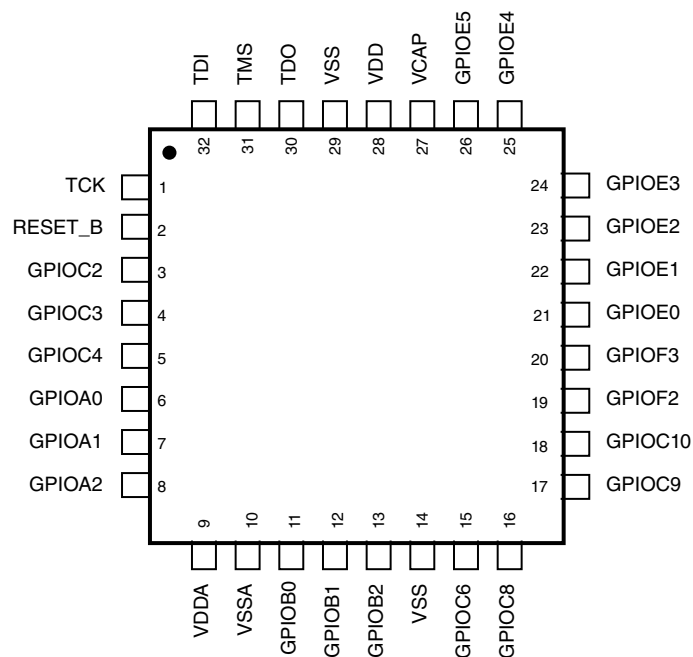


Figure 4. 32-pin LQFP

5 Ordering parts

5.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MC56F81

5.2 Part number list

The following table shows a part number list for this device.

Table 4. Part numbers

| Part Number | Flash Size | Operating Temperature | Package |
|---------------|------------|-----------------------|---------|
| MC56F81768VLH | 128 KB | -40 to 105°C | 64 LQFP |
| MC56F81748VLH | 64 KB | -40 to 105°C | 64 LQFP |
| MC56F81766VLF | 128 KB | -40 to 105°C | 48 LQFP |
| MC56F81746VLF | 64 KB | -40 to 105°C | 48 LQFP |
| MC56F81763VLC | 128 KB | -40 to 105°C | 32 LQFP |
| MC56F81743VLC | 64 KB | -40 to 105°C | 32 LQFP |
| MC56F81763VFM | 128 KB | -40 to 105°C | 32 QFN |
| MC56F81743VFM | 64 KB | -40 to 105°C | 32 QFN |
| MC56F81668VLH | 128 KB | -40 to 105°C | 64 LQFP |
| MC56F81648VLH | 64 KB | -40 to 105°C | 64 LQFP |
| MC56F81666VLF | 128 KB | -40 to 105°C | 48 LQFP |
| MC56F81646VLF | 64 KB | -40 to 105°C | 48 LQFP |
| MC56F81663VLC | 128 KB | -40 to 105°C | 32 LQFP |
| MC56F81643VLC | 64 KB | -40 to 105°C | 32 LQFP |
| MC56F81768MLH | 128 KB | -40 to 125°C | 64 LQFP |
| MC56F81748MLH | 64 KB | -40 to 125°C | 64 LQFP |
| MC56F81766MLF | 128 KB | -40 to 125°C | 48 LQFP |
| MC56F81746MLF | 64 KB | -40 to 125°C | 48 LQFP |

6 Part identification

6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

6.2 Format

Part numbers for this device have the following format: Q 56F8 1 C F P T PP N

6.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|-------|---|---|
| Q | Qualification status | <ul style="list-style-type: none"> MC = Fully qualified, general market flow PC = Prequalification |
| 56F8 | DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core | <ul style="list-style-type: none"> 56F8 |
| 1 | DSC subfamily | <ul style="list-style-type: none"> 1 |
| C | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> 6 = 100 MHz 7 = 100 MHz |
| F | Primary program flash memory size | <ul style="list-style-type: none"> 4 = 64 KB 6 = 128 KB |
| P | Pin count | <ul style="list-style-type: none"> 3 = 32 6 = 48 8 = 64 |
| T | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 M = -40 to 125 |
| PP | Package identifier | <ul style="list-style-type: none"> LC = 32LQFP FM = 32QFN LF = 48LQFP LH = 64LQFP |
| N | Packaging type | <ul style="list-style-type: none"> R = Tape and reel (Blank) = Trays |

6.4 Example

This is an example part number: MC56F81768VLH

7 Package marking information

The MC56F81xxx 64LQFP package has the following top-side marking:

- First line: aaaaaaaaaa
- Second line: mmmmm
- Third line: xxxyywx

The MC56F81xxx 48LQFP package has the following top-side marking:

- First line: aaaaaaaaaa
- Second line: mmmmm
- Third line: xxywx

The detailed code format for these identifiers is show in the table below.

| Identifier | Description |
|------------|-------------|
|------------|-------------|

Table continues on the next page...

Terminology and guidelines

| | |
|---|---|
| a | Part number code, refer to the "Part identification" section. For example, in 48LQFP package, the last digit 'V' stands for VLF. |
| m | Mask set |
| y | Work year |
| w | Work week |
| x | NXP internal use |

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

| Symbol | Description | Min. | Max. | Unit |
|----------|--|------|------|---------------|
| I_{WP} | Digital I/O weak pullup/pulldown current | 10 | 130 | μA |

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|-------------|---------------------------------|------|------|-------------|
| C_{IN_D} | Input capacitance: digital pins | — | 7 | pF |

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

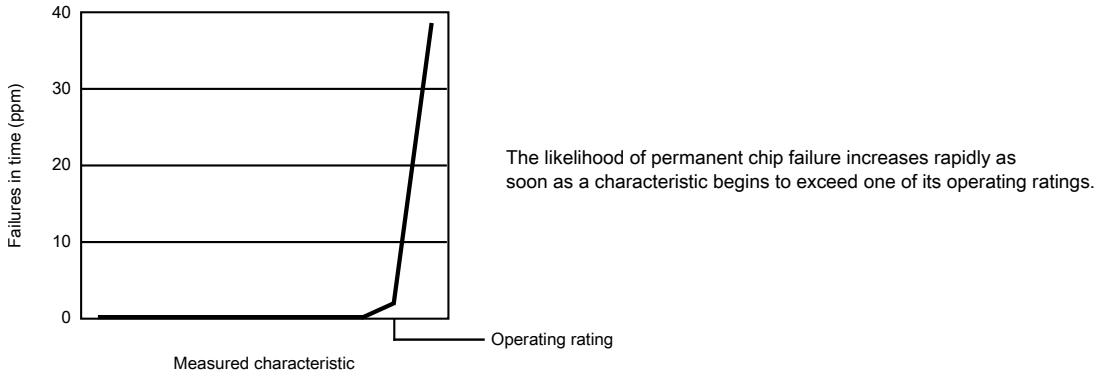
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

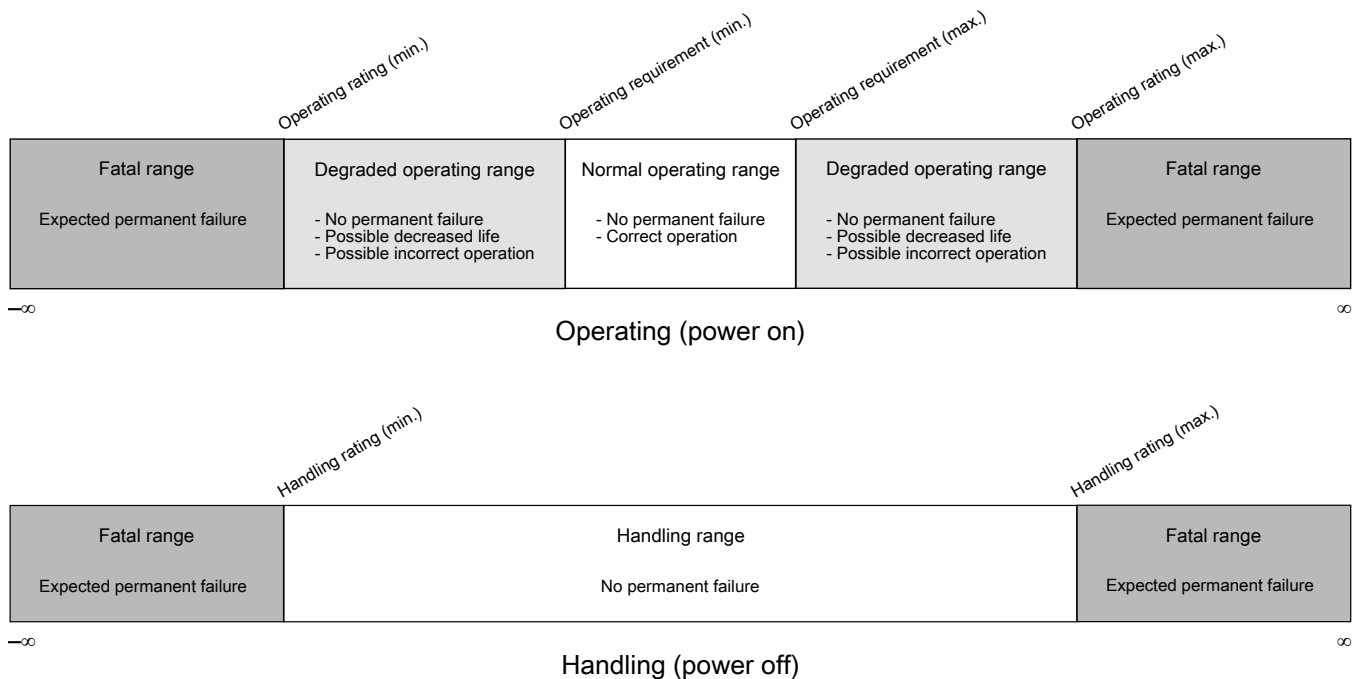
This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|----------|---------------------------|------|------|------|
| V_{DD} | 1.0 V core supply voltage | -0.3 | 1.2 | V |

8.5 Result of exceeding a rating



8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

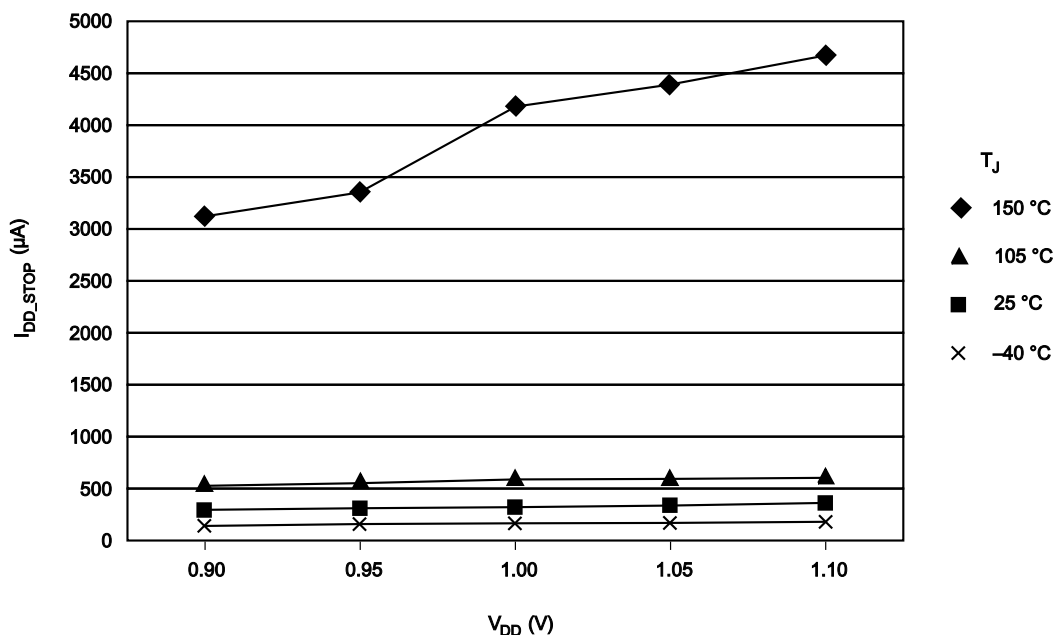
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------|--|------|------|------|---------------|
| I_{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|----------|----------------------|-------|------|
| T_A | Ambient temperature | 25 | °C |
| V_{DD} | 3.3 V supply voltage | 3.3 | V |

9 Ratings

9.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|-------------------------------|------|------|------|-------|
| T_{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T_{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

9.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

9.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

A device is defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed as per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD/Latch-up Protection

| Characteristic ¹ | Min | Max | Unit | Notes |
|---|-------|-------|------|-------|
| ESD for Human Body Model (V_{HBM}) | -2000 | +2000 | V | 2 |
| ESD for Charge Device Model (V_{CDM}) | -500 | +500 | V | 3 |
| Latch-up current at $T_A = 85^\circ\text{C}$ (I_{LAT}) (V part) | -100 | +100 | mA | 4 |

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.
2. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
3. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
4. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

9.4 Voltage and current operating ratings

Table 6. Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|-----------|---|----------------|----------------|------|
| V_{DD} | Digital supply voltage | -0.3 | 3.8 | V |
| I_{DD} | Digital supply current | — | 120 | mA |
| V_{IO} | IO pin input voltage | -0.3 | $V_{DD} + 0.3$ | V |
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |

10 General

10.1 General characteristics

Absolute maximum ratings in the table of "Voltage and current operating ratings" section are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

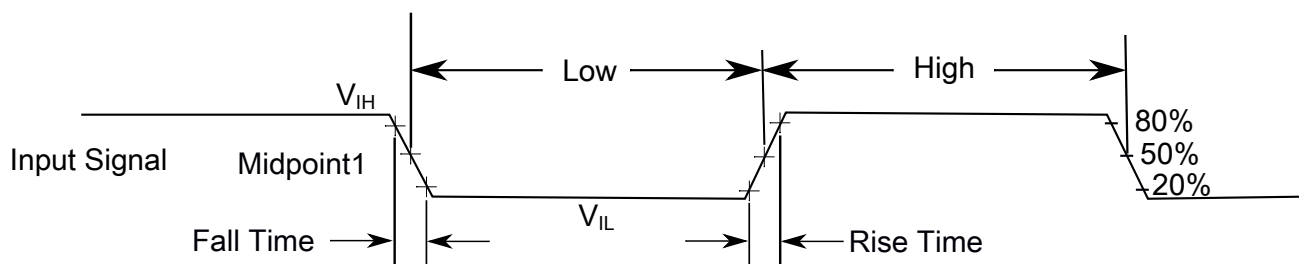
Unless otherwise stated, all specifications within this chapter apply to the temperature range specified in the table of "Voltage and current operating ratings" section over the following supply ranges: $V_{SS} = V_{SSA} = 0\text{ V}$, $V_{DD} = V_{DDA} = 3.0\text{ V}$ to 3.6 V , $CL \leq 50\text{ pF}$, $f_{OP} = 50\text{ MHz}$.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

10.2 AC electrical characteristics

Tests are conducted using the input levels specified in the section "Voltage and current operating behaviors". Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 20% and 80% points, as shown in Figure 5.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 5. Input signal measurement references

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L = 30\text{ pF}$ loads
- Slew rate disabled
- Normal drive strength

Figure 6 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

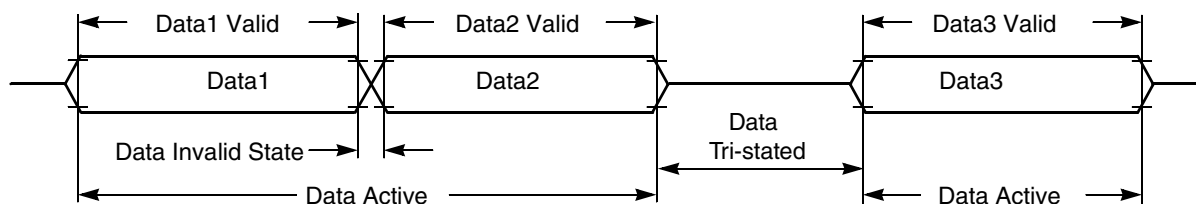


Figure 6. Signal states

10.3 Nonswitching electrical specifications

10.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

Table 7. Voltage and current operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|----------------------|------|----------------------|------|-------|
| V_{DD} | Supply voltage | 2.7 | 3.3 | 3.6 | V | — |
| V_{DDA} | Analog supply voltage | 2.7 | 3.3 | 3.6 | V | — |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | | 0.1 | V | — |
| $V_{SS} - V_{SSA}$ | V_{SS} -to- V_{SSA} differential voltage | -0.1 | | 0.1 | V | — |
| V_{IH} | Input high voltage • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | $0.7 \times V_{DD}$ | | — | V | — |
| V_{IL} | Input low voltage • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | — | | $0.35 \times V_{DD}$ | V | — |
| V_{HYS} | Input hysteresis | $0.06 \times V_{DD}$ | | — | V | — |
| V_{IHOSC} | Oscillator Input Voltage High XTAL driven by an external clock source | 2.0 | | $V_{DD} + 0.3$ | V | — |
| V_{ILOSC} | Oscillator Input Voltage Low | -0.3 | | 0.8 | V | — |
| I_{ICIO} | IO pin negative DC injection current—single pin • $V_{IN} < V_{SS} - 0.3\text{V}$ | -3 | | — | mA | 1 |
| I_{ICcont} | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins | | | | | — |

Table 7. Voltage and current operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|--|------|------|------|------|-------|
| | <ul style="list-style-type: none"> Negative current injection | -25 | | — | mA | |

- All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3$ V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.

10.3.2 LVD and POR operating requirements

Table 8. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------------------------|---------|-----|------|-----|------|
| POR Assert Voltage ¹ | POR | | 2.0 | | V |
| POR Release Voltage ² | POR | | 2.7 | | V |
| Low-Voltage Warning Interrupt | LVI_2p7 | | 2.73 | | V |
| Low-Voltage Alarm Interrupt | LVI_2p2 | | 2.23 | | V |

- During 3.3-volt V_{DD} power supply ramp down
- During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

10.3.3 Voltage and current operating behaviors

Table 9. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|--|----------------|-------|---------------|-------|
| V_{OH} | Output high voltage — Normal drive pad (except RESET) <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -5\text{ mA}$ | $V_{DD} - 0.5$ | — | V | 1 |
| V_{OH} | Output high voltage — High drive pad (except RESET) <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -20\text{ mA}$ | $V_{DD} - 0.5$ | — | V | 2, 1 |
| I_{OHT} | Output high current total for all ports | — | 100 | mA | — |
| V_{OL} | Output low voltage — Normal drive pad (except RESET) <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 5\text{ mA}$ | — | 0.5 | V | 1 |
| V_{OL} | Output low voltage — High drive pad (except RESET) <ul style="list-style-type: none"> $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 20\text{ mA}$ | — | 0.5 | V | 2, 1 |
| I_{OLT} | Output low current total for all ports | — | 100 | mA | — |
| I_{IN} | Input leakage current (per pin) for full temperature range | — | 1 | μA | 3 |
| I_{IN} | Input leakage current (per pin) at 25 °C | — | 0.025 | μA | 3 |

Table continues on the next page...

Table 9. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|----------|---|------|------|------------------|-------|
| I_{IN} | Input leakage current (total all pins) for full temperature range | — | 41 | μA | 3 |
| I_{OZ} | Hi-Z (off-state) leakage current (per pin) | — | 1 | μA | — |
| R_{PU} | Internal pullup resistors | 20 | 50 | $\text{k}\Omega$ | 4 |
| R_{PD} | Internal pulldown resistors | 20 | 50 | $\text{k}\Omega$ | 5 |

1. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
2. GPIOC2, GPIOC7~12, GPIOF2~3 and GPIOC14~15 support high drive strength mode.
3. Measured at $V_{DD} = 3.6\text{ V}$
4. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$
5. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$

10.3.4 Power mode transition operating behaviors

Parameters listed are guaranteed by design.

NOTE

All address and data buses described here are internal.

Table 10. Reset, stop, wait, and interrupt timing

| Characteristic | Symbol | Typical Min | Typical Max | Unit | See Figure |
|---|-----------|-----------------------------------|-------------|------|------------|
| Minimum $\overline{\text{RESET}}$ Assertion Duration | t_{RA} | 16 ¹ | — | ns | — |
| $\overline{\text{RESET}}$ deassertion to First Address Fetch | t_{RDA} | $865 \times T_{OSC} + 8 \times T$ | — | ns | — |
| Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop) | t_{IF} | 361.3 | 570.9 | ns | — |

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns. Recommended a capacitor of up to 0.1 μF on $\overline{\text{RESET}}$.

NOTE

In Table 10, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 50MHz, $T=20$ ns. At 4 MHz (used coming out of reset and stop modes), $T=250$ ns.

Table 11. Power mode transition behavior

| Symbol | Description | Typical | Max | Unit | Notes ¹ |
|-----------|--|---------|------|---------------|--------------------|
| T_{POR} | After a POR event, the amount of delay from when V_{DD} reaches 2.7 V to when the first instruction executes (over the operating temperature range). | 250 | 288 | μs | |
| | STOP mode to RUN mode | 7.10 | 8.17 | μs | 2 |

Table continues on the next page...

Table 11. Power mode transition behavior (continued)

| Symbol | Description | Typical | Max | Unit | Notes ¹ |
|--------|-----------------------------|---------|-------|------|--------------------|
| | LPS mode to LPRUN mode | 285 | 328 | μs | 3 |
| | VLPS mode to VLPRUN mode | 878 | 1010 | μs | 4 |
| | WAIT mode to RUN mode | 0.395 | 0.454 | μs | 5 |
| | LPWAIT mode to LPRUN mode | 285 | 328 | μs | 3 |
| | VLPWAIT mode to VLPRUN mode | 868 | 998 | μs | 4 |

1. Wakeup times are measured from GPIO toggle for wakeup till GPIO toggle at the wakeup interrupt subroutine from respective stop/wait mode.
2. Clock configuration: CPU clock=4 MHz. System clock source is 8 MHz IRC in normal mode.
3. CPU clock = 200 kHz and 8 MHz IRC on standby. Exit by an interrupt on PORTA GPIO.
4. Using 64 kHz external clock; CPU Clock = 32 kHz. Exit by an interrupt on PORTA GPIO.
5. Clock configuration: CPU and system clocks= 100 MHz. Bus Clock = 50MHz. Exit by interrupt on PORTA GPIO

10.3.5 Power consumption operating behaviors

Table 12. Current Consumption (Unit: mA)

| Mode | Maximum Frequency | Conditions | Typical at 3.3 V, 25°C | | Maximum at 3.6 V, 105°C | | Maximum at 3.6V, 125°C | |
|------|-------------------|--|------------------------------|------------------|------------------------------|------------------|------------------------------|------------------|
| | | | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} |
| RUN1 | 100 MHz | <ul style="list-style-type: none"> • 100 MHz Core • 50 MHz Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. TMRs and SCIs using 1X peripheral clock • NanoEdge within eFlexPWM using 2X peripheral clock • ADC/DAC (only one 12-bit DAC and all 8-bit DACs) powered on and clocked • Comparator powered on | 24.9 | 8.6 | 46.0 | 13.2 | 46.9 | 13.2 |
| RUN2 | 50 MHz | <ul style="list-style-type: none"> • 50 MHz Core and Peripheral clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. TMRs and SCIs using 1X peripheral clock • NanoEdge within eFlexPWM using 2X peripheral clock • ADC/DAC (only one 12-bit DAC and all 8-bit DACs) powered on and clocked • Comparator powered on | 20.3 | 8.7 | 43.0 | 12.2 | 43.4 | 12.3 |
| WAIT | 50 MHz | <ul style="list-style-type: none"> • 50 MHz Core and Peripheral clock | 17.3 | — | 35.0 | — | 35.7 | — |

Table continues on the next page...

Table 12. Current Consumption (Unit: mA) (continued)

| Mode | Maximum Frequency | Conditions | Typical at 3.3 V, 25°C | | Maximum at 3.6 V, 105°C | | Maximum at 3.6V, 125°C | |
|-----------------|-------------------|--|------------------------------|------------------|------------------------------|------------------|------------------------------|------------------|
| | | | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} |
| | | <ul style="list-style-type: none"> Regulators are in full regulation Relaxation Oscillator on PLL powered on Processor Core in WAIT state All Peripheral modules enabled. TMRs and SCIs using 1X Clock NanoEdge within PWMA using 2X clock ADC/DAC (single 12-bit DAC, all 8-bit DACs), Comparator powered off | | | | | | |
| STOP | 4 MHz | <ul style="list-style-type: none"> 4 MHz Device Clock Regulators are in full regulation Relaxation Oscillator on PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC/DAC/Comparator powered off | 4.4 | — | 12.5 | — | 13.1 | — |
| LPRUN (LsRUN) | 2 MHz | <ul style="list-style-type: none"> 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock ROSC in standby mode Regulators are in standby PLL disabled Repeat NOP instructions All peripheral modules enabled, except NanoEdge and cyclic ADCs. One 12-bit DAC and all 8-bit DACs enabled. Simple loop with running from platform instruction buffer | 1.1 | 2.4 | 11.1 | 4.0 | 12.8 | 4.0 |
| LPWAIT (LsWAIT) | 2 MHz | <ul style="list-style-type: none"> 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock ROSC in standby mode Regulators are in standby PLL disabled All peripheral modules enabled, except NanoEdge and cyclic ADCs. One 12-bit DAC and all 8-bit DACs enabled.² Processor core in wait mode | 1.0 | 2.4 | 11.1 | 4.0 | 12.8 | 4.0 |
| LPSTOP (LsSTOP) | 2 MHz | <ul style="list-style-type: none"> 200 kHz Device Clock from Relaxation Oscillator's (ROSC) low speed clock ROSC in standby mode Regulators are in standby PLL disabled Only PITs and COP enabled; other peripheral modules disabled and clocks gated off² Processor core in stop mode | 1.0 | — | 9.1 | — | 10.5 | — |
| VLPRUN | 200 kHz | <ul style="list-style-type: none"> 32 kHz Device Clock Clocked by a 64 kHz external clock source Oscillator in power down All ROSCs disabled Large regulator is in standby Small regulator is disabled | 0.4 | — | 7.5 | — | 9.0 | — |

Table continues on the next page...

Table 12. Current Consumption (Unit: mA) (continued)

| Mode | Maximum Frequency | Conditions | Typical at 3.3 V, 25°C | | Maximum at 3.6 V, 105°C | | Maximum at 3.6V, 125°C | |
|---------|-------------------|--|------------------------------|------------------|------------------------------|------------------|------------------------------|------------------|
| | | | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} | I _{DD} ¹ | I _{DDA} |
| | | <ul style="list-style-type: none"> • PLL disabled • Repeat NOP instructions • All peripheral modules, except COP and EWM, disabled and clocks gated off • Simple loop running from platform instruction buffer | | | | | | |
| VLPWAIT | 200 kHz | <ul style="list-style-type: none"> • 32 kHz Device Clock • Clocked by a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in wait mode | 0.4 | — | 7.5 | — | 9.0 | — |
| VLPSTOP | 200 kHz | <ul style="list-style-type: none"> • 32 kHz Device Clock • Clocked by a 64 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby. • Small regulator is disabled. • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode | 0.4 | — | 7.5 | — | 9.0 | — |

1. No output switching, all ports configured as inputs, all inputs low, no DC loads.
2. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 500 kHz due to the fixed frequency ratio of 1:2 between the CPU clock and the flash clock when running with 2 MHz external clock input and CPU running at 1 MHz.

10.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

10.3.7 Capacitance attributes

Table 13. Capacitance attributes

| Description | Symbol | Min. | Typ. | Max. | Unit |
|--------------------|-----------|------|------|------|------|
| Input capacitance | C_{IN} | — | 10 | — | pF |
| Output capacitance | C_{OUT} | — | 10 | — | pF |

10.4 Switching specifications

10.4.1 Device clock specifications

Table 14. Device clock specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------------|---|------------|------------|------|-------|
| Normal run mode | | | | | |
| f_{SYSCLK} | Device (system and core) clock frequency <ul style="list-style-type: none"> • using relaxation oscillator • using external clock source | 0.001 0 | 100 100 | MHz | |
| f_{BUS} | Bus clock | — | 50 | MHz | |

10.4.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO signals.

Table 15. General switching specifications

| Description | Min. | Max. | Unit | Notes |
|--|------|------|------------------|-------|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| Port rise and fall time | — | 36 | ns | 3 |

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

10.5 Thermal specifications

10.5.1 Thermal operating requirements

Table 16. Thermal operating requirements

| Symbol | Description | Grade | Min | Max | Unit |
|----------------|--------------------------|-------|-----|-----|------|
| T _J | Die junction temperature | V | -40 | 125 | °C |
| | | M | -40 | 135 | °C |
| T _A | Ambient temperature | V | -40 | 105 | °C |
| | | M | -40 | 125 | °C |

10.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for P_{I/O} in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

See [Thermal design considerations](#) for more detail on thermal design considerations.

| Board type ¹ | Symbol | Description | 48 LQFP | 64 LQFP | Unit | Notes |
|-------------------------|------------------|---|---------|---------|------|-------------------|
| Four-layer (2s2p) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 55 | 52 | °C/W | 2 |
| Single-layer (1s) | R _{θJC} | Thermal resistance, junction to case | 23 | 20 | °C/W | 3 |
| — | Ψ _{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 3 | 3 | °C/W | 2 |

1. Thermal test board meets JEDEC specification for this package (JESD51-7, 2s2p and JESD51-3, 1s).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction-to-Case (Top) thermal resistance is determined using an isothermal cold plate attached to the package top. Case (Top) temperature refers to the mold surface temperature at the center.

11 Peripheral operating requirements and behaviors

11.1 Core modules

11.1.1 JTAG timing

Table 17. JTAG timing

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|----------------------------|----------|-----|------------|------|------------|
| TCK frequency of operation | f_{OP} | DC | SYS_CLK/ 8 | MHz | Figure 7 |
| TCK clock pulse width | t_{PW} | 50 | — | ns | Figure 7 |
| TMS, TDI data set-up time | t_{DS} | 5 | — | ns | Figure 8 |
| TMS, TDI data hold time | t_{DH} | 5 | — | ns | Figure 8 |
| TCK low to TDO data valid | t_{DV} | — | 30 | ns | Figure 8 |
| TCK low to TDO tri-state | t_{TS} | — | 30 | ns | Figure 8 |

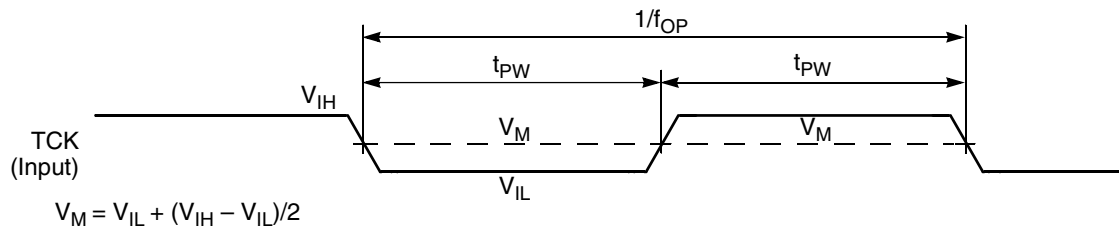


Figure 7. Test clock input timing diagram

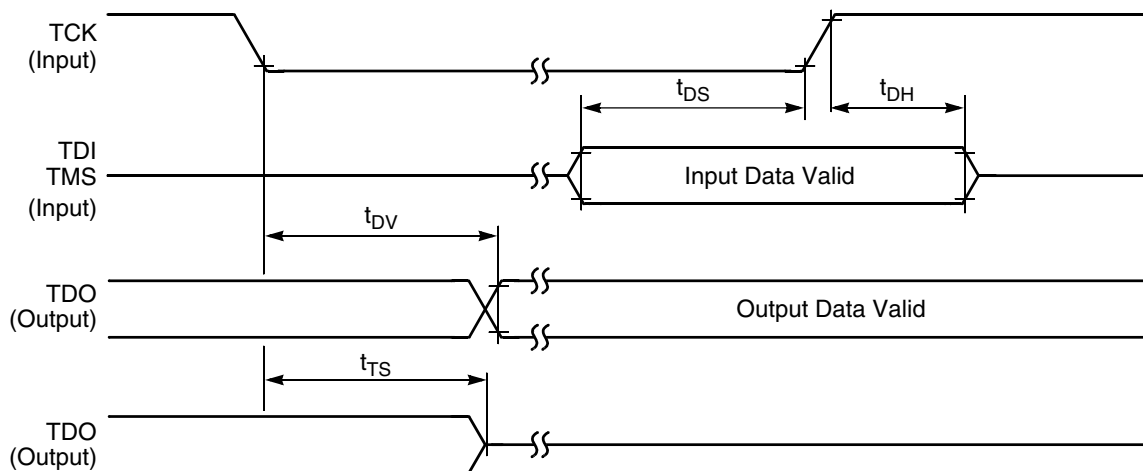


Figure 8. Test access port timing diagram

11.2 System modules

11.2.1 Voltage regulator specifications

The voltage regulator supplies approximately 1.2 V to the device's core logic. For proper operations, the voltage regulator requires a minimum external 2.2 μF capacitor on each V_{CAP} pin with total capacitors on all V_{CAP} pins at a minimum of 4.4 μF . Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in [Table 18](#).

Table 18. Regulator 1.2 V parameters

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|------------------|-----|------|-----|--------|
| Output Voltage ¹ | V_{CAP} | — | 1.23 | — | V |
| Short Circuit Current ² | I_{SS} | — | 600 | — | mA |
| Short Circuit Tolerance (V_{CAP} shorted to ground) | T_{RSC} | — | — | 1 | minute |

1. Value is after trim
2. Guaranteed by design

Table 19. Bandgap electrical specifications

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--------------------------------|------------------|-----|-------------------|-----|------|
| Reference Voltage (after trim) | V_{REF} | — | 1.24 ¹ | — | V |

1. Typical value is trimmed at 25°C. There could be ± 50 mV variation due to temperature change.

11.3 Clock modules

11.3.1 External clock operation timing

Parameters listed are guaranteed by design.

Table 20. External clock operation timing requirements

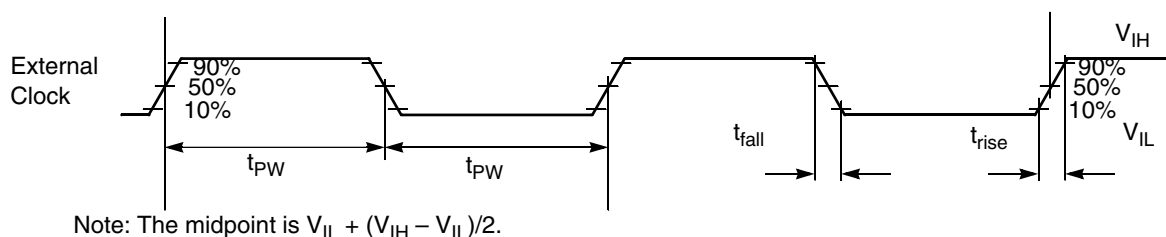
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-------------------|-----|-----|-----|------|
| Frequency of operation (external clock driver) ¹ | f_{osc} | — | — | 50 | MHz |
| Clock pulse width ² | t_{PW} | 8 | | | ns |
| External clock input rise time ³ | t_{rise} | — | — | 1 | ns |
| External clock input fall time ⁴ | t_{fall} | — | — | 1 | ns |

Table continues on the next page...

Table 20. External clock operation timing requirements (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------|----------------------|-----|---------------------|------|
| Input high voltage overdrive by an external clock | V_{ih} | $0.85 \times V_{DD}$ | — | — | V |
| Input low voltage overdrive by an external clock | V_{il} | — | — | $0.3 \times V_{DD}$ | V |

1. See the "External clock timing" figure for details on using the recommended connection of an external clock driver.
2. The chip may not function if the high or low pulse width is smaller than 6.25 ns.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.

**Figure 9. External clock timing**

11.3.2 Phase-Locked Loop timing

Table 21. Phase-Locked Loop timing

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------|-----|-----|-----|---------|
| PLL input reference frequency ¹ | f_{ref} | 8 | 8 | 16 | MHz |
| PLL output frequency ² | f_{op} | 200 | — | 550 | MHz |
| PLL lock time ³ | t_{plls} | — | — | 100 | μ s |
| Allowed Duty Cycle of input reference | t_{dc} | 40 | 50 | 60 | % |

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
2. The frequency of the core system clock cannot exceed 100 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.
3. This is the time required *after the PLL is enabled* to ensure reliable operation.

11.3.3 External crystal or resonator requirement

Table 22. Crystal or resonator requirement

| Characteristic | Symbol | Min | Typ | Max | Unit |
|------------------------|------------|-----|-----|-----|------|
| Frequency of operation | f_{XOSC} | 4 | 8 | 16 | MHz |

11.3.4 RC Oscillator Timing

Table 23. RC Oscillator Electrical Specifications

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|--|-----------------------------|--------|------|------|----------|------|
| 8 MHz Output Frequency ¹ | | | | | | |
| Run Mode | 0°C to 105°C | | 7.84 | 8 | 8.16 | MHz |
| | -40°C to 105°C | | 7.76 | 8 | 8.24 | MHz |
| | -40°C to 125°C | | 7.76 | 8 | 8.24 | MHz |
| 2M Mode (IRC trimmed @ 8 MHz) | -40°C to 105°C | | 1.9 | 2.0 | 2.1 | MHz |
| | -40°C to 125°C | | 1.9 | 2.0 | 2.1 | MHz |
| 8 MHz Frequency Variation over 25°C | | | | | | |
| RUN Mode | 0°C to 105°C | | | ±1.5 | ±2 | % |
| | -40°C to 105°C | | | ±1.5 | ±3 | % |
| | -40°C to 125°C | | | ±1.5 | -3 to +3 | % |
| 200 kHz Output Frequency ² | | | | | | |
| RUN Mode | -40°C to 105°C | | 194 | 200 | 206 | kHz |
| | -40°C to 125°C | | 192 | 200 | 208 | kHz |
| 200 kHz Output Frequency Variation over 25°C | | | | | | |
| RUN Mode | 0°C to 85°C | | | ±1.5 | ±2 | % |
| | -40°C to 105°C | | | ±1.5 | ±3 | % |
| | -40°C to 125°C | | | ±1.5 | ±4 | % |
| Stabilization Time | 8 MHz output ³ | tstab | 1 | - | 15 | µs |
| | 200 kHz output ³ | | - | 125 | 375 | µs |
| Output Duty Cycle | | | 45 | 50 | 55 | % |

1. Frequency after factory trim
2. Frequency after factory trim
3. Power down to run mode transition

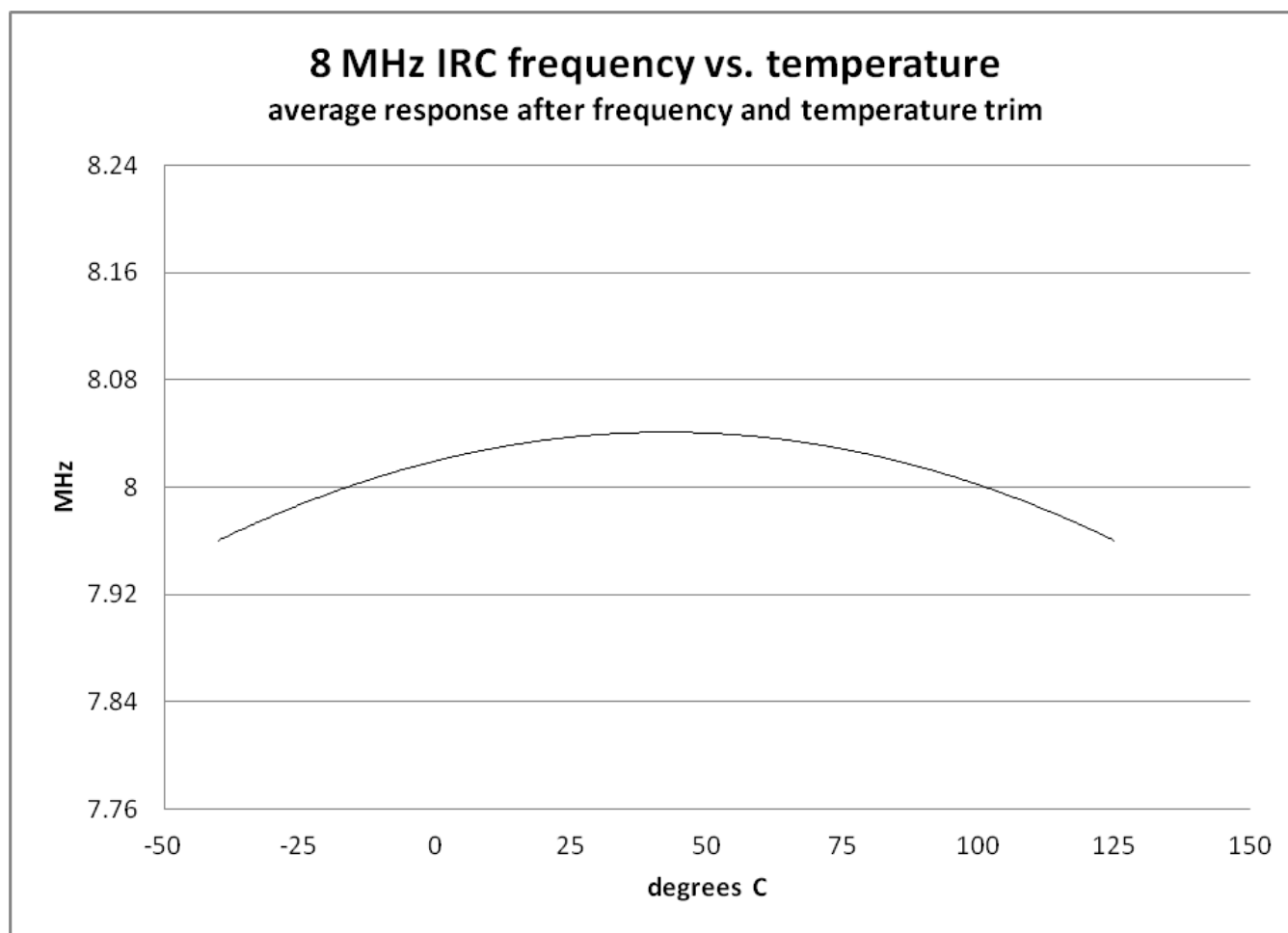


Figure 10. RC Oscillator Temperature Variation (Typical) After Trim (Preliminary)

11.4 Memories and memory interfaces

11.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

11.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 24. NVM program/erase timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------|------------------------------------|------|------|------|---------|-------|
| t_{hvpgm4} | Longword Program high-voltage time | — | 7.5 | 18 | μ s | — |

Table continues on the next page...

Table 24. NVM program/erase timing specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------|--------------------------------|------|------|------|------|-------|
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 52 | 452 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

11.4.1.2 Flash timing specifications — commands

Table 25. Flash command timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------|---|------|------|------|---------|-------|
| $t_{rd1sec1k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | μ s | 1 |
| t_{pgmchk} | Program Check execution time | — | — | 45 | μ s | 1 |
| t_{rdsrc} | Read Resource execution time | — | — | 30 | μ s | 1 |
| t_{pgm4} | Program Longword execution time | — | 65 | 145 | μ s | — |
| t_{ersscr} | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| t_{rd1all} | Read 1s All Blocks execution time | — | — | 1.8 | ms | 1 |
| t_{rdonce} | Read Once execution time | — | — | 25 | μ s | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | μ s | — |
| t_{ersall} | Erase All Blocks execution time | — | 88 | 650 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 30 | μ s | 1 |
| $t_{ersallu}$ | Erase All Blocks Unsecure execution time | — | 88 | 650 | ms | 2 |

- Assumes 25 MHz flash clock frequency.
- Maximum times for erase parameters based on expectations at cycling end-of-life.

11.4.1.3 Flash high voltage current behaviors

Table 26. Flash high voltage current behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|------|
| I_{DD_PGM} | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| I_{DD_ERS} | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

11.4.1.4 Reliability specifications

Table 27. NVM reliability specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|---------------|--|------|-------------------|------|-------|-------|
| Program Flash | | | | | | |
| $t_{nvmp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | — |
| t_{nvmp1k} | Data retention after up to 1 K cycles | 20 | 100 | — | years | — |

Table continues on the next page...

Table 27. NVM reliability specifications (continued)

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|---------------|-------------------|------|-------------------|------|--------|-------|
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |
| $n_{nvmcycp}$ | Cycling endurance | 1 K | — | — | cycles | 3 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.
3. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 135\text{ °C}$. If the product application is exposed to $T_j > 125\text{ °C}$, the reduced W/E spec applies independent of the number of W/E cycles in the high T_j band.

11.5 Analog

11.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 28. 12-bit ADC Electrical Specifications

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------------|--------------------------|------------|-----------------------|------------------|
| Recommended Operating Conditions | | | | | |
| Supply Voltage ¹ | VDDA | 3 | 3.3 | 3.6 | V |
| VREFH (in external reference mode) | Vrefhx | VDDA-0.6 | | VDDA | V |
| ADC Conversion Clock ² | f_{ADCCLK} | 0.1 | | 12.5 | MHz |
| Conversion Range ³ | R_{AD} | | | $V_{REFH} - V_{REFL}$ | V |
| Fully Differential | | $-(V_{REFH} - V_{REFL})$ | | V_{REFH} | |
| Single Ended/Unipolar | | V_{REFL} | | | |
| Input Voltage Range (per input) ⁴ | V_{ADIN} | V_{REFL} | | V_{REFH} | V |
| External Reference | | 0 | | V_{DDA} | |
| Internal Reference | | | | | |
| Timing and Power | | | | | |
| Conversion Time ⁵ | t_{ADC} | | 8 | | ADC Clock Cycles |
| ADC Power-Up Time (from adc_pdn) | t_{ADPU} | | 13 | | ADC Clock Cycles |
| ADC RUN Current (per ADC block) | I_{ADRUN} | | 2.5 | | mA |
| ADC Powerdown Current (adc_pdn enabled) | $I_{ADPWRDWN}$ | | 0.1 | | μ A |
| V_{REFH} Current (in external mode) | I_{VREFH} | | 190 | 225 | μ A |
| Accuracy (DC or Absolute) | | | | | |
| Integral non-Linearity ⁶ | INL | | +/- 1.5 | +/- 2.2 | LSB ⁷ |
| Differential non-Linearity ⁶ | DNL | | +/- 0.5 | +/- 0.8 | LSB ⁷ |
| Monotonicity | | | GUARANTEED | | |
| Offset ⁸ | V_{OFFSET} | | | | mV |

Table continues on the next page...

Table 28. 12-bit ADC Electrical Specifications (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|--------------|-----|----------------|----------------|-------|
| Fully Differential | | | +/- 8 | | |
| Single Ended/Unipolar | | | +/- 12 | | |
| Gain Error | E_{GAIN} | | 0.996 to 1.004 | 0.990 to 1.010 | |
| AC Specifications⁹ | | | | | |
| Signal to Noise Ratio | SNR | | 66 | | dB |
| Total Harmonic Distortion | THD | | 75 | | dB |
| Spurious Free Dynamic Range | SFDR | | 77 | | dB |
| Signal to Noise plus Distortion | SINAD | | 66 | | dB |
| Effective Number of Bits | ENOB | | — | | bits |
| Gain = 1x (Fully Differential/Unipolar) | | | 10.6 | | |
| Gain = 2x (Fully Differential/Unipolar) | | | — | | |
| Gain = 4x (Fully Differential/Unipolar) | | | 10.3 | | |
| Gain = 1x (Single Ended) | | | 10.6 | | |
| Gain = 2x (Single Ended) | | | 10.4 | | |
| Gain = 4x (Single Ended) | | | 10.2 | | |
| Variation across channels ¹⁰ | | | 0.1 | | |
| ADC Inputs | | | | | |
| Input Leakage Current | I_{IN} | | 1 | | nA |
| Temperature sensor slope | T_{SLOPE} | | 1.3 | | mV/°C |
| Temperature sensor voltage at 25 °C | V_{TEMP25} | | 0.82 | | V |
| Disturbance | | | | | |
| Input Injection Current ¹¹ | I_{INJ} | | | +/-3 | mA |
| Channel to Channel Crosstalk ¹² | ISOXTLK | | -82 | | dB |
| Memory Crosstalk ¹³ | MEMXTLK | | -71 | | dB |
| Input Capacitance | C_{ADI} | | 4.8 | | pF |
| Sampling Capacitor | | | | | |

1. The ADC functions up to $V_{DDA} = 2.7$ V. When V_{DDA} is below 3.0 V, ADC specifications are not guaranteed
2. ADC clock duty cycle is 45% ~ 55%
3. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.
4. In unipolar mode, positive input must be ensured to be always greater than negative input.
5. First conversion takes 10 clock cycles.
6. INL/DNL is measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$ using Histogram method at x1 gain setting
7. Least Significant Bit = 0.806 mV at 3.3 V V_{DDA} , x1 gain Setting
8. Offset measured at 2048 code
9. Measured converting a 1 kHz input full scale sine wave
10. When code runs from internal RAM
11. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC
12. Any off-channel with 50 kHz full-scale input to the channel being sampled with DC input (isolation crosstalk)
13. From a previously sampled channel with 50 kHz full-scale input to the channel being sampled with DC input (memory crosstalk).

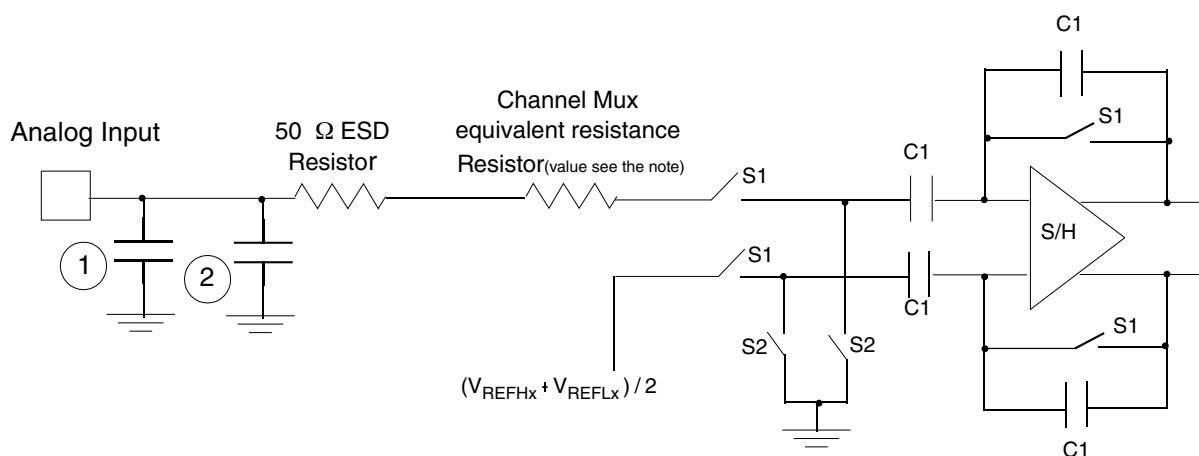
11.5.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 are dependent on the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times C_{\text{AdI}}} + 50 \text{ ohm} + \text{Resistor}$$

NOTE

Resistor=1200 ohm@gain1x, or 730 ohm@gain2x, or 500 ohm@gain4x



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. S1 and S2 switch phases are non-overlapping and depend on the ADC clock frequency

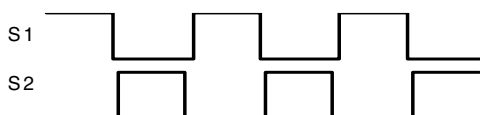


Figure 11. Equivalent circuit for A/D loading

11.5.2 12-bit Digital-to-Analog Converter (DAC) parameters

NOTE

RLD = 3 k Ω and CLD = 400 pF, unless otherwise specified.

Table 29. DAC parameters

| Parameter | Conditions/Comments | Symbol | Min | Typ | Max | Unit |
|-----------------------------|---|--------------|--------------------|---|--------------------|---------|
| DC Specifications | | | | | | |
| Resolution | | | 12 | 12 | 12 | bits |
| Settling time ¹ | At output load RLD = 3 k Ω CLD = 400 pF Range of input digital words: 410 to 3891 | | — | 1 (high-speed mode) 2 (low-speed mode) | | μ s |
| Power-up time | Time from release of PWRDWN signal until DACOUT signal is valid | t_{DAPU} | — | — | 11 | μ s |
| Accuracy | | | | | | |
| Integral non-linearity | Range of input digital words: 410 to 3891 (\$19A - \$F33) | INL | — | +/- 3 | +/- 4 | LSB |
| Differential non-linearity | Range of input digital words: 410 to 3891 (\$19A - \$F33) | DNL | — | +/- 0.5 | +/- 1 | LSB |
| Monotonicity | > 6 sigma monotonicity, < 3.4 ppm non-monotonicity | | guaranteed | | | — |
| Offset error | Range of input digital words: 410 to 3891 (\$19A - \$F33) | V_{OFFSET} | — | +/- 25 | +/- 43 | mV |
| Gain error | Range of input digital words: 410 to 3891 (\$19A - \$F33) | E_{GAIN} | — | +/- 0.5 | +/- 1.5 | % |
| DAC Output | | | | | | |
| Output voltage range | Within 40 mV of either V_{SSA} or V_{DDA} | V_{OUT} | $V_{SSA} + 0.04$ V | — | $V_{DDA} - 0.04$ V | V |
| AC Specifications | | | | | | |
| Signal-to-noise ratio | | SNR | — | 80 | — | dB |
| Spurious free dynamic range | | SFDR | — | -72 | — | dB |
| Effective number of bits | | ENOB | — | 10 | — | bits |
| I_{DD} from V_{DDA} | average I_{DD} of V_{DDA} (I_{DD} varies with DAC input word) | I_{DDA} | — | 3.2 | — | mA |

1. When DAC output is fed to other internal peripherals, the settling time is much shorter.

11.5.3 OPAMP electrical specifications

Table 30. OPAMP electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|------------------|---|------------------|------|-------------------------|------|
| V _{CC} | Power supply | 3.0 | — | 3.6 | V |
| I _{CC} | Supply current <ul style="list-style-type: none"> high-speed mode low-power mode | — | 500 | — | μA |
| V _{OS} | Input offset voltage <ul style="list-style-type: none"> high-speed mode low-power mode | — | ±1.5 | ±5 | mV |
| V _{IN} | Common input voltage | V _{SSA} | — | V _{DDA} - 1.2 | V |
| V _{OUT} | Output voltage range | 0.15 | — | V _{DDA} - 0.15 | V |
| CMRR | Input common mode rejection ratio | 60 | 80 | — | dB |
| PSRR | Power supply rejection ratio | 60 | 80 | — | dB |
| SR | Slew rate ¹ <ul style="list-style-type: none"> high-speed mode low-power mode | 4 | 8 | — | V/μs |
| GBW | Unity gain bandwidth ¹ <ul style="list-style-type: none"> high-speed mode low-power mode | — | 8 | — | MHz |
| | | | 1.5 | | |

1. R_L = 5 ~ 10 kΩ, C_L = 30 ~ 50 pf

11.5.4 CMP and 8-bit DAC electrical specifications

Table 31. Comparator and 8-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|---|-----------------------|------|-----------------|------|
| V _{DD} | Supply voltage | 3.0 | — | 3.6 | V |
| I _{DDHS} | Supply current, high-speed mode (EN=1, PMODE=1) | — | 300 | — | μA |
| I _{DDL} | Supply current, low-speed mode (EN=1, PMODE=0) | — | 36 | — | μA |
| V _{AIN} | Analog input voltage | V _{SS} | — | V _{DD} | V |
| V _{AIO} | Analog input offset voltage ¹ | — | — | 20 | mV |
| V _H | Analog comparator hysteresis <ul style="list-style-type: none"> CR0[HYSTCTR] = 00² CR0[HYSTCTR] = 01¹ CR0[HYSTCTR] = 10¹ CR0[HYSTCTR] = 11¹ | — | 5 | 13 | mV |
| | | — | 25 | 48 | mV |
| | | — | 55 | 105 | mV |
| | | — | 80 | 148 | mV |
| V _{CMPOH} | Output high | V _{DD} - 0.5 | — | — | V |
| V _{CMPOI} | Output low | — | — | 0.5 | V |
| t _{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) ³ | — | 25 | 70 | ns |
| t _{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0) ³ | — | 60 | 200 | ns |
| | Analog comparator initialization delay ⁴ | — | 40 | — | μs |

Table continues on the next page...

Table 31. Comparator and 8-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|---|------|----------|------|------------------|
| I_{DAC8b} | 8-bit DAC current adder (enabled) | — | 7 | — | μA |
| $V_{reference}$ | 8-bit DAC reference inputs, V_{in1} and V_{in2} There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range. | — | V_{DD} | — | V |
| INL | 8-bit DAC integral non-linearity | -1 | — | 1 | LSB ⁵ |
| DNL | 8-bit DAC differential non-linearity | -1 | — | 1 | LSB |

1. Measured with input voltage range limited to $0.7 \leq V_{in} \leq V_{DD} - 0.8$
2. Measured with input voltage range limited to 0 to V_{DD}
3. Input voltage range: $0.1V_{DD} \leq V_{in} \leq 0.9V_{DD}$, step = $\pm 100mV$, across all temperature. Does not include PCB and PAD delay.
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/256$

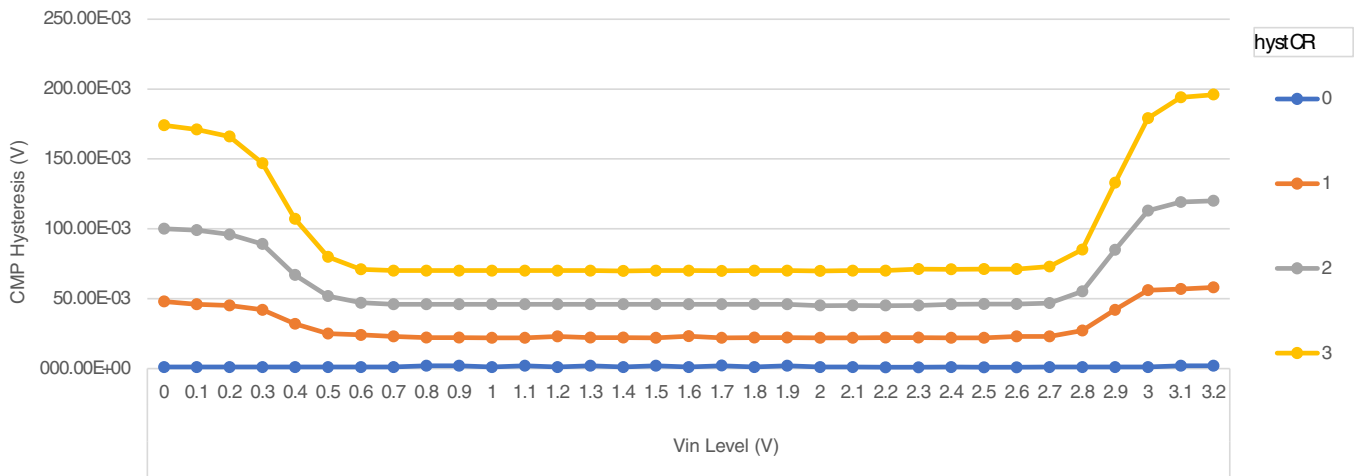


Figure 12. Typical hysteresis vs. Vin level ($V_{DD} = 3.3 V$, $PMODE = 0$)

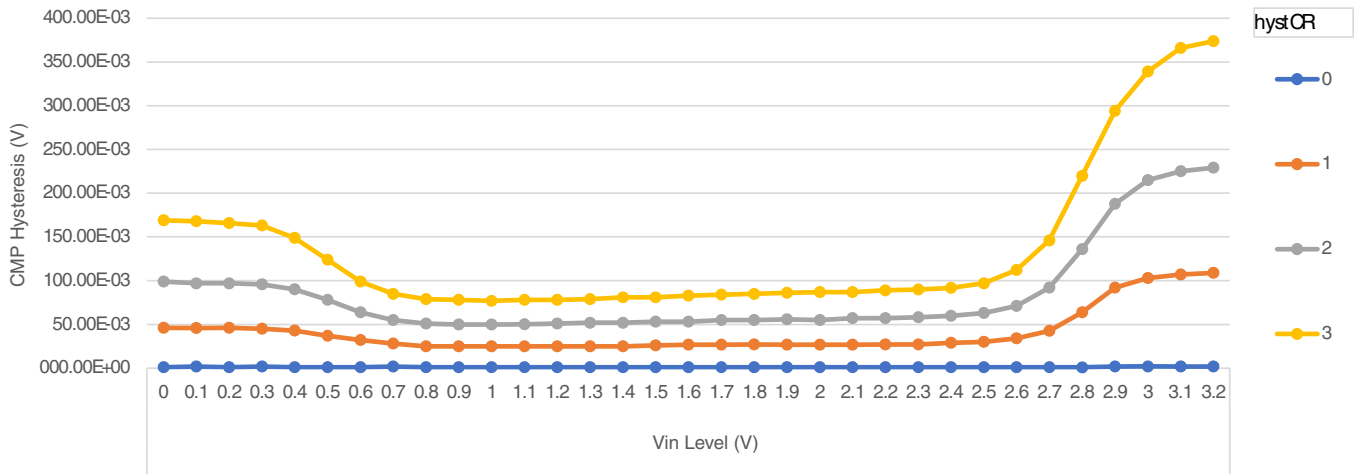


Figure 13. Typical hysteresis vs. Vin level ($V_{DD} = 3.3 V$, $PMODE = 1$)

11.6 PWMs and timers

11.6.1 Enhanced NanoEdge PWM characteristics

Table 32. NanoEdge PWM timing parameters

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|----------|-----|-----|-----|---------|
| PWM clock frequency | | | 100 | | MHz |
| NanoEdge Placement (NEP) Step Size ^{1, 2} | pwmp | | 312 | | ps |
| Delay for fault input activating to PWM output deactivated | | 1 | | 33 | ns |
| Power-up Time ³ | t_{pu} | | 25 | | μ s |
| Resolution of Deadtime | | | 312 | | ps |

1. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

11.6.2 Quad Timer timing

Parameters listed are guaranteed by design.

Table 33. Timer timing

| Characteristic | Symbol | Min ¹ | Max | Unit | See Figure |
|------------------------------|-------------|------------------|-----|------|------------|
| Timer input period | P_{IN} | $2T + 6$ | — | ns | Figure 14 |
| Timer input high/low period | P_{INHL} | $1T + 3$ | — | ns | Figure 14 |
| Timer output period | P_{OUT} | 20 | — | ns | Figure 14 |
| Timer output high/low period | P_{OUTHL} | 10 | — | ns | Figure 14 |

1. T = clock cycle. For 100 MHz operation, $T = 10$ ns.

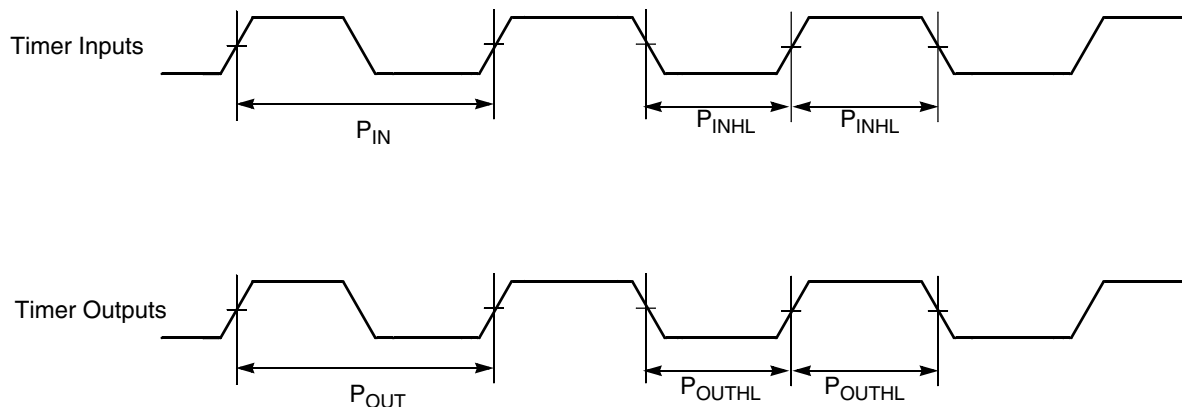


Figure 14. Timer timing

11.6.3 QDC Timing Specifications

Parameters listed are guaranteed by design.

Table 34. Quadrature Decoder Timing

| Characteristic | Symbol | Min ¹ | Max | Unit |
|----------------------------------|----------|------------------|-----|------|
| Quadrature input period | P_{IN} | $4T + 12$ | — | ns |
| Quadrature input high/low period | P_{HL} | $2T + 6$ | — | ns |
| Quadrature phase period | P_{PH} | $1T + 3$ | — | ns |

1. In the formulas listed, T equals the system clock cycle. For 50 MHz operation, T = 20 ns. For 100 MHz operation, T = 10 ns.

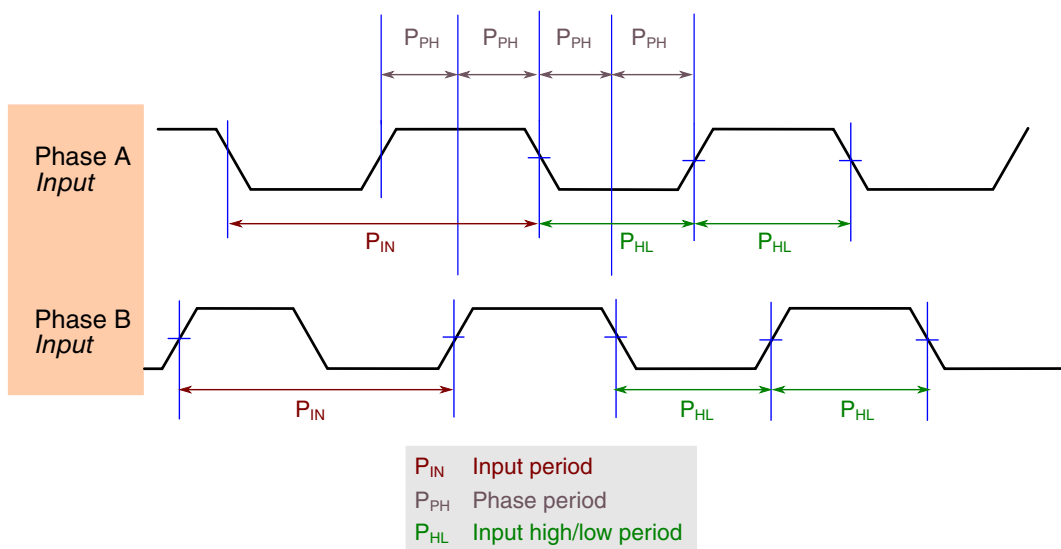


Figure 15. Quadrature Decoder Timing

11.7 Communication interfaces

11.7.1 Queued Serial Peripheral Interface (SPI) timing

Parameters listed are guaranteed by design.

Table 35. SPI timing

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|----------------|--------|-----|-----|------|---------------------------|
| Cycle time | t_c | 60 | — | ns | Figure 16 |

Table continues on the next page...

Table 35. SPI timing (continued)

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|-----------|-----|-----|------|------------|
| Master | | 60 | — | ns | Figure 17 |
| Slave | | | | | Figure 18 |
| | | | | | Figure 19 |
| Enable lead time | t_{ELD} | — | — | ns | Figure 19 |
| Master | | 20 | — | ns | |
| Slave | | | | | |
| Enable lag time | t_{ELG} | — | — | ns | Figure 19 |
| Master | | 20 | — | ns | |
| Slave | | | | | |
| Clock (SCK) high time | t_{CH} | | — | ns | Figure 16 |
| Master | | | — | ns | Figure 17 |
| Slave | | | | | Figure 18 |
| | | | | | Figure 19 |
| Clock (SCK) low time | t_{CL} | 28 | — | ns | Figure 19 |
| Master | | 28 | — | ns | |
| Slave | | | | | |
| Data set-up time required for inputs | t_{DS} | 20 | — | ns | Figure 16 |
| Master | | 1 | — | ns | Figure 17 |
| Slave | | | | | Figure 18 |
| | | | | | Figure 19 |
| Data hold time required for inputs | t_{DH} | 1 | — | ns | Figure 16 |
| Master | | 3 | — | ns | Figure 17 |
| Slave | | | | | Figure 18 |
| | | | | | Figure 19 |
| Access time (time to data active from high-impedance state) | t_A | 5 | — | ns | Figure 19 |
| Slave | | | | | |
| Disable time (hold time to high-impedance state) | t_D | 5 | — | ns | Figure 19 |
| Slave | | | | | |
| Data valid for outputs | t_{DV} | — | | ns | Figure 16 |
| Master | | — | | ns | Figure 17 |
| Slave (after enable edge) | | | | | Figure 18 |
| | | | | | Figure 19 |
| Data invalid | t_{DI} | 0 | — | ns | Figure 16 |
| Master | | 0 | — | ns | Figure 17 |
| Slave | | | | | Figure 18 |
| | | | | | Figure 19 |
| Rise time | t_R | | | | Figure 16 |

Table continues on the next page...

Table 35. SPI timing (continued)

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|----------------|--------|-----|-----|------|------------|
| Master | | — | 1 | ns | Figure 17 |
| Slave | | — | 1 | ns | Figure 18 |
| Fall time | t_F | — | 1 | ns | Figure 16 |
| Master | | — | 1 | ns | Figure 17 |
| Slave | | — | 1 | ns | Figure 18 |
| | | | | | Figure 19 |

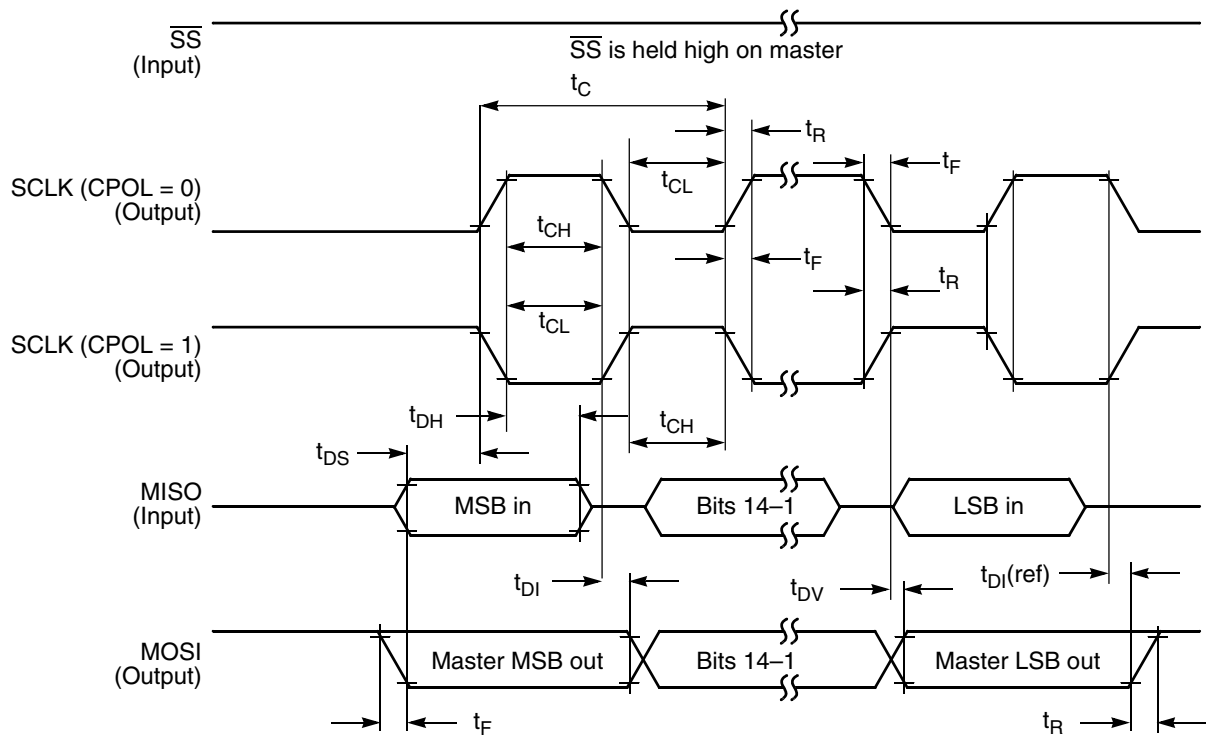


Figure 16. SPI master timing (CPHA = 0)

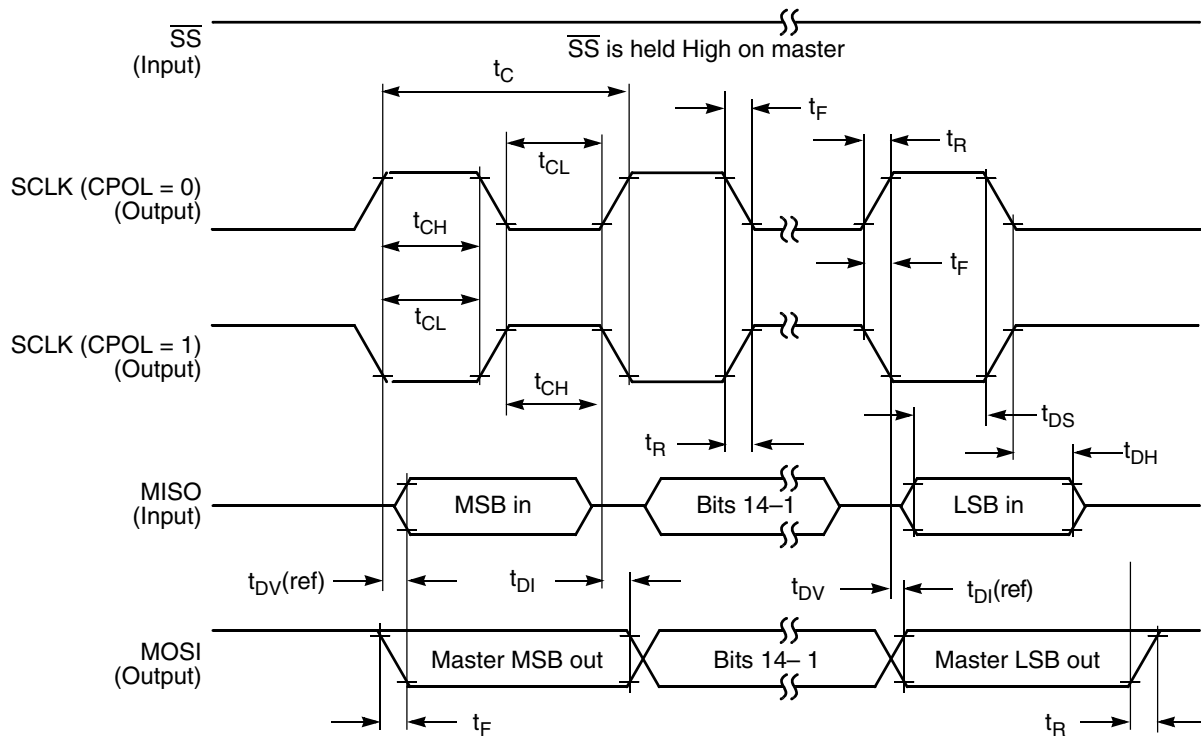


Figure 17. SPI master timing (CPHA = 1)

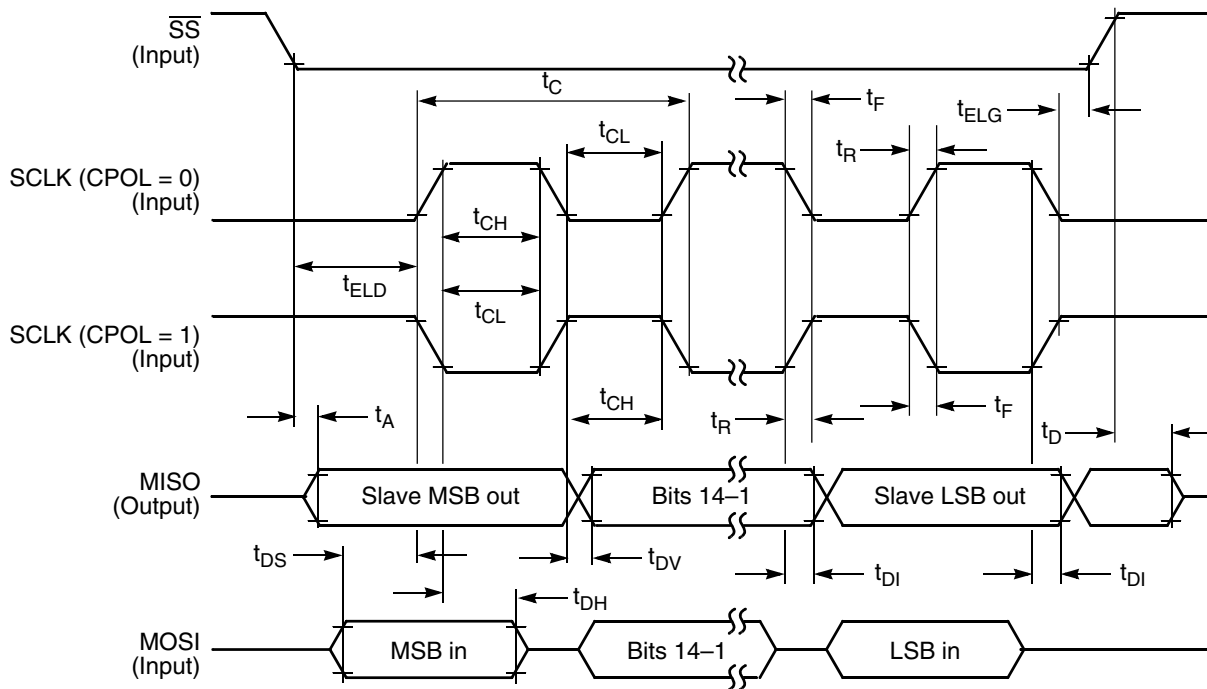


Figure 18. SPI slave timing (CPHA = 0)

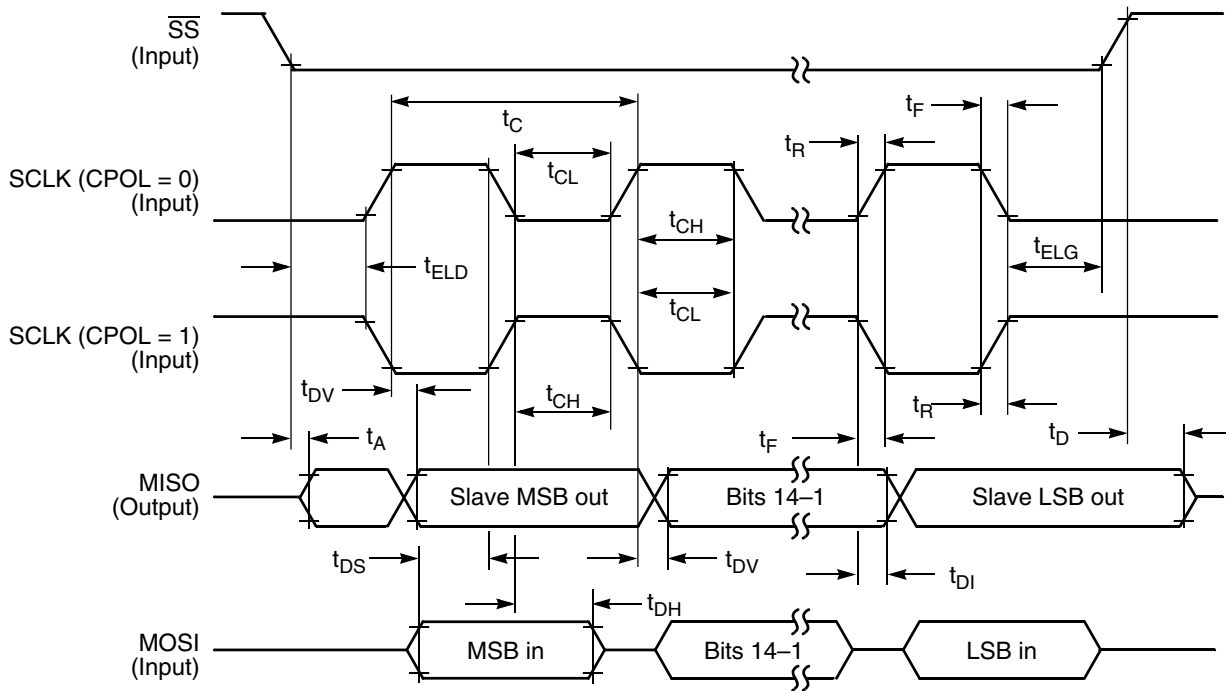


Figure 19. SPI slave timing (CPHA = 1)

11.7.2 Queued Serial Communication Interface (SCI) timing

Parameters listed are guaranteed by design.

Table 36. SCI timing

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|--------------------------|----------|------------------------|-------------------------|------------|
| Baud rate ¹ | BR | — | (f _{MAX} /16) | Mbit/s | — |
| RXD pulse width | RXD _{PW} | 0.965/BR | 1.04/BR | μs | Figure 20 |
| TXD pulse width | TXD _{PW} | 0.965/BR | 1.04/BR | μs | Figure 21 |
| LIN Slave Mode | | | | | |
| Deviation of slave node clock from nominal clock rate before synchronization | F _{TOL_UNSYNCH} | -14 | 14 | % | — |
| Deviation of slave node clock relative to the master node clock after synchronization | F _{TOL_SYNCH} | -2 | 2 | % | — |
| Minimum break character length | T _{BREAK} | 13 | — | Master node bit periods | — |
| | | 11 | — | Slave node bit periods | — |

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max.50 MHz depending on part number) or 2x bus clock (max. 100 MHz) for the devices.

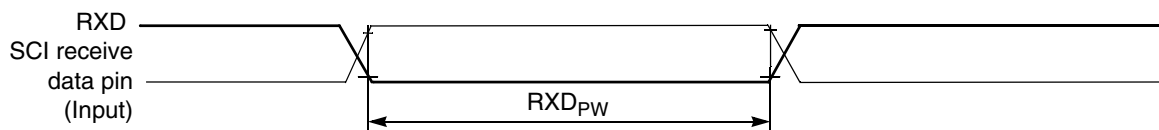


Figure 20. RXD pulse width

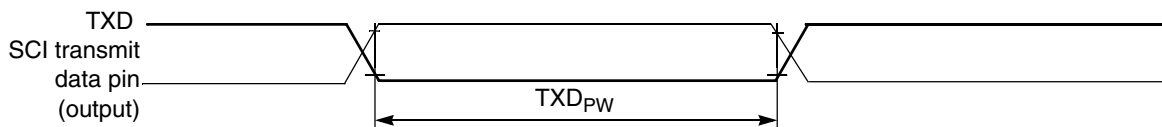


Figure 21. TXD pulse width

11.7.3 LPI²C

Table 37. LPI²C specifications

| Symbol | Description | | Min. | Max. | Unit | Notes |
|------------------|---------------------|---------------------------|------|------|------|---------|
| f _{SCL} | SCL clock frequency | Standard mode (Sm) | 0 | 100 | kHz | 1, 2, 3 |
| | | Fast mode (Fm) | 0 | 400 | | |
| | | Fast mode Plus (Fm+) | 0 | 1000 | | |
| | | Ultra Fast mode (UFm) | 0 | 5000 | | |
| | | High speed mode (Hs-mode) | 0 | 3400 | | |

1. Hs-mode is only supported in slave mode.
2. The maximum SCL clock frequency in Fast mode with maximum bus loading (400pF) can only be achieved with appropriate pull-up devices on the bus when using the high or normal drive pins across the full voltage range. The maximum SCL clock frequency in Fast mode Plus can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. The maximum SCL clock frequency in Ultra Fast mode can support maximum bus loading (400pF) when using the high drive pins. The maximum SCL clock frequency for slave in High speed mode can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. For more information on the required pull-up devices, see I²C Bus Specification.
3. See the section "General switching specifications".

12 Design Considerations

12.1 Thermal design considerations

An estimate of the chip junction temperature (T_J) can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

where

T_A = Ambient temperature for the package (°C)

R_{ΘJA} = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W).

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which T_J value is closer to the application depends on the power dissipated by other components on the board.

- The T_J value obtained on a single layer board is appropriate for a tightly packed printed circuit board.
- The T_J value obtained on a board with the internal planes is usually appropriate if the board has low-power dissipation and if the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

where

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$).

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where

T_T = Thermocouple temperature on top of package ($^{\circ}\text{C}/\text{W}$)

Ψ_{JT} = thermal characterization parameter ($^{\circ}\text{C}/\text{W}$)

P_D = Power dissipation in package (W).

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical design considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 μF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA} . Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 μF , plus the number of 0.1 μF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.

- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF} , V_{DDA} , and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, then connect a small inductor or ferrite bead in serial with V_{DDA} . Traces of V_{SS} and V_{SSA} should be shorted together.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I²C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the \overline{RESET} pin. The resistor value should be in the range of 4.7 k Ω –10 k Ω ; the capacitor value should be in the range of 0.1 μ F–4.7 μ F.
- Configuring the \overline{RESET} pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 k Ω external pullup on the TMS pin of the JTAG port to keep EOnCE in a reset state during normal operation if JTAG converter is not present. Furthermore, configure TMS, TDI, TDO and TCK to GPIO if operation environment is very noisy.
- During reset and after reset but before I/O initialization, all the GPIO pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10 Ω RC filter.

12.3 Power-on Reset design considerations

12.3.1 Improper power-up sequence between VDD/VSS and VDDA/VSSA:

It is recommended that VDD be kept within 100 mV of VDDA at all times, including power ramp-up and ramp-down. Failure to keep VDD within 100 mV of VDDA may cause a leakage current through the substrate, between the VDD and VDDA pad cells. This leakage current could prevent operation of the device after it powers up. The voltage

difference between VDD and VDDA must be limited to below 0.3 V at all times, to avoid permanent damage to the part (See the table in "Voltage and current operating ratings" section). Also see the table in "Voltage and current operating requirements" section.

12.3.2 Heavy capacitive load on power supply output:

In some applications, the low cost DC/DC converter may not regulate the output voltage well before it reaches the regulation point, which is roughly around 2.5V to 2.7V. However, the device might exit power-on reset at around 2.3V. If the initialization code enables the PLL to run the DSC at full speed right after reset, then the high current will be pulled by DSC from the supply, which can cause the supply voltage to drop below the operation voltage; see the captured graph (Figure 22). This can cause the DSC fail to start up.

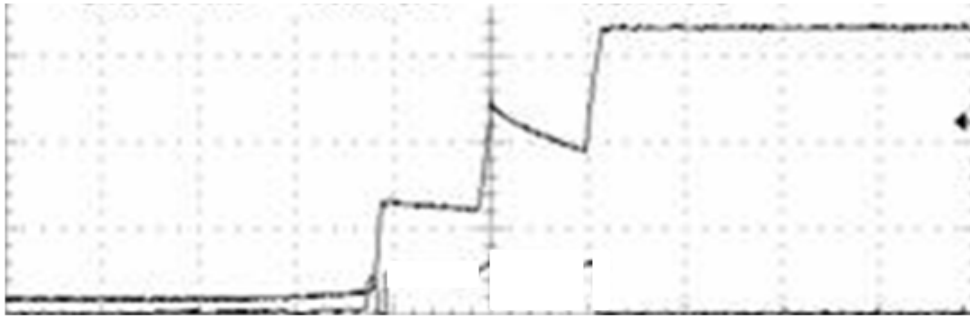


Figure 22. Supply Voltage Drop

A recommended initialization sequence during power-up is:

1. After POR is released, run a few hundred NOP instructions from the internal relaxation oscillator; this gives time for the supply voltage to stabilize.
2. Configure the peripherals (except the ADC) to the desired settings; the ADC should stay in low power mode.
3. Power up the PLL.
4. After the PLL locks, switch the clock from PLL prescale to postscale.
5. Configure the ADC.

13 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

| Drawing for package | Document number to be used |
|---------------------|----------------------------|
| 32LQFP | 98ASH70029A |
| 32QFN | 98ASA00473D |
| 48-pin LQFP | 98ASH00962A |
| 64-pin LQFP | 98ASS23234W |

14 Product documentation

The documents listed in [Table 38](#) are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at www.nxp.com.

Table 38. Device documentation

| Topic | Description | Document Number |
|---------------------------------------|---|------------------|
| DSP56800E/DSP56800EX Reference Manual | Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set | DSP56800ERM |
| MC56F81xxx Reference Manual | Detailed functional description and programming model | MC56F81XXXRM |
| MC56F81xxx Data Sheet | Electrical and timing specifications, pin descriptions, and package information (this document) | MC56F81XXX |
| MC56F81xxx Errata | Details any chip issues that might be present | MC56F81XXX_0N91Z |

15 Revision history

The following table provides a revision history for this document.

Table 39. Revision history

| Rev. | Date | Substantial Changes |
|------|---------|---|
| 1 | 08/2020 | Initial public release |
| 1.1 | 12/2020 | Added M-part devices (temperature range as -40 to 125°C), and updated related specifications: e.g. the "Current Consumption" table, the "NVM reliability specifications" table. |

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