



**THE DATASHEET OF
LTC4447IDD#PBF**



FEATURES

- Integrated Schottky Diode
- 4V to 6.5V V_{CC} Operating Voltage
- 38V Maximum Input Supply Voltage
- Adaptive Shoot-Through Protection
- Rail-to-Rail Output Drivers
- 3.2A Peak Pull-Up Current
- 4.5A Peak Pull-Down Current
- 8ns TG Risettime Driving 3000pF Load
- 7ns TG Falltime Driving 3000pF Load
- Separate Supply to Match PWM Controller
- Drives Dual N-Channel MOSFETs
- Undervoltage Lockout
- Low Profile (0.75mm) 3mm × 3mm DFN Package

APPLICATIONS

- Distributed Power Architectures
- High Density Power Modules

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DESCRIPTION

The LTC[®]4447 is a high frequency gate driver with integrated bootstrap Schottky diode that is designed to drive two N-Channel MOSFETs in a synchronous DC/DC converter. The powerful rail-to-rail driver capability reduces switching losses in MOSFETs with high gate capacitance.

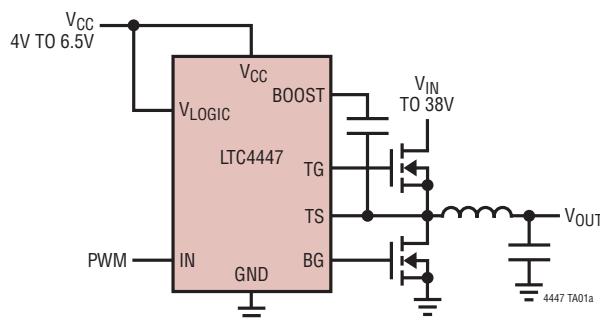
The LTC4447 features a separate supply for the input logic to match the signal swing of the controller IC. If the input signal is not being driven, the LTC4447 activates a shut-down mode that turns off both external MOSFETs. The input logic signal is internally level-shifted to the bootstrapped supply, which functions at up to 42V above ground. The Schottky diode required for the bootstrapped supply is integrated to simplify layout and reduce parts count.

The LTC4447 contains undervoltage lockout circuits on both the driver and logic supplies that turn off the external MOSFETs when an undervoltage condition is present. An adaptive shoot-through protection feature is also built-in to prevent the power loss resulting from MOSFET cross-conduction current.

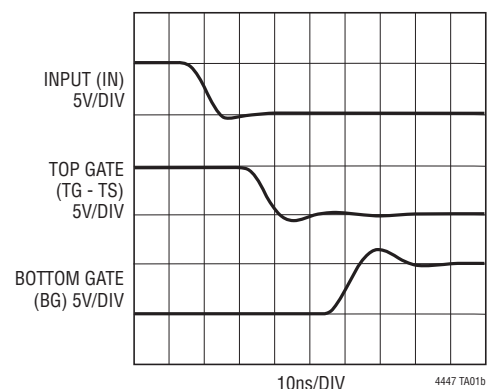
The LTC4447 is available in the 3mm × 3mm DFN package.

TYPICAL APPLICATION

Synchronous Buck Converter Driver



LTC4447 Driving 3000pF Capacitive Loads



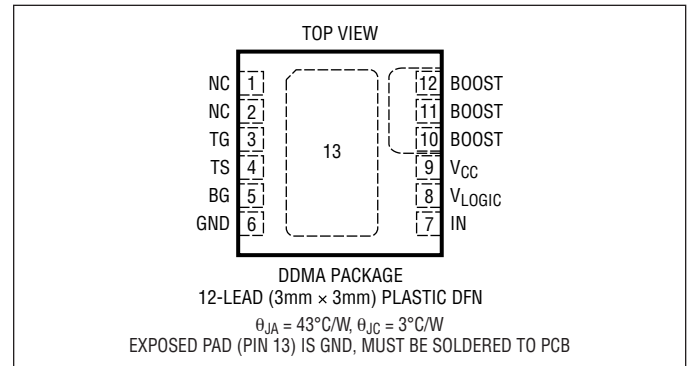
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage

V_{LOGIC}	-0.3V to 7V
V_{CC}	-0.3V to 7V
BOOST – TS	-0.3V to 7V
BOOST Voltage	-0.3V to 42V
BOOST – V_{CC}	38V
TS + V_{CC}	42V
IN Voltage	-0.3V to 7V
Driver Output TG (with Respect to TS).....	-0.3V to 7V
Driver Output BG.....	-0.3V to 7V
Operating Temperature Range (Note 2)....	-40°C to 85°C
Junction Temperature (Note 3)	125°C
Storage Temperature Range.....	-65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4447EDD#PBF	LTC4447EDD#TRPBF	LDHD	12-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC4447IDD#PBF	LTC4447IDD#TRPBF	LDHD	12-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *Temperature grades are identified by a label on the shipping container. Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{\text{CC}} = V_{\text{LOGIC}} = 5\text{V}$, $V_{\text{TS}} = \text{GND} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Supply (V_{LOGIC})						
V_{LOGIC}	Operating Range		3		6.5	V
I_{VLOGIC}	DC Supply Current	IN = Floating		730	900	μA
UVLO	Undervoltage Lockout Threshold	V_{LOGIC} Rising	● 2.5	2.75	3	V
		V_{LOGIC} Falling	● 2.4	2.65	2.9	V
		Hysteresis		100		mV
Gate Driver Supply (V_{CC})						
V_{CC}	Operating Range		4		6.5	V
I_{VCC}	DC Supply Current	IN = Floating		600	800	μA
UVLO	Undervoltage Lockout Threshold	V_{CC} Rising	● 2.75	3.20	3.65	V
		V_{CC} Falling	● 2.60	3.04	3.50	V
		Hysteresis		160		mV
V_{D}	Schottky Diode Forward Voltage	$I_{\text{D}} = 10\text{mA}$		0.38		V
		$I_{\text{D}} = 100\text{mA}$		0.48		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = V_{\text{LOGIC}} = 5\text{V}$, $V_{TS} = \text{GND} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Signal (IN)							
$V_{IH(TG)}$	TG Turn-On Input Threshold	$V_{\text{LOGIC}} \geq 5\text{V}$, IN Rising	●	3	3.5	4	V
		$V_{\text{LOGIC}} = 3.3\text{V}$, IN Rising	●	1.9	2.2	2.6	V
$V_{IL(TG)}$	TG Turn-Off Input Threshold	$V_{\text{LOGIC}} \geq 5\text{V}$, IN Falling	●	2.75	3.25	3.75	V
		$V_{\text{LOGIC}} = 3.3\text{V}$, IN Falling	●	1.8	2.09	2.5	V
$V_{IH(BG)}$	BG Turn-On Input Threshold	$V_{\text{LOGIC}} \geq 5\text{V}$, IN Falling	●	0.8	1.25	1.6	V
		$V_{\text{LOGIC}} = 3.3\text{V}$, IN Falling	●	0.8	1.1	1.4	V
$V_{IL(BG)}$	BG Turn-Off Input Threshold	$V_{\text{LOGIC}} \geq 5\text{V}$, IN Rising	●	1.05	1.5	1.85	V
		$V_{\text{LOGIC}} = 3.3\text{V}$, IN Rising	●	0.9	1.21	1.5	V
$I_{IN(SD)}$	Maximum Current Into or Out of IN in Shutdown Mode	$V_{\text{LOGIC}} \geq 5\text{V}$, IN Floating		150	300		μA
		$V_{\text{LOGIC}} = 3.3\text{V}$, IN Floating		75	150		μA
High Side Gate Driver Output (TG)							
$V_{OH(TG)}$	TG High Output Voltage	$I_{TG} = -100\text{mA}$, $V_{OH(TG)} = V_{\text{BOOST}} - V_{TG}$			140		mV
$V_{OL(TG)}$	TG Low Output Voltage	$I_{TG} = 100\text{mA}$, $V_{OL(TG)} = V_{TG} - V_{TS}$			80		mV
$I_{PU(TG)}$	TG Peak Pull-Up Current		●	2	3.2		A
$I_{PD(TG)}$	TG Peak Pull-Down Current		●	1.5	2.4		A
Low Side Gate Driver Output (BG)							
$V_{OH(BG)}$	BG High Output Voltage	$I_{BG} = -100\text{mA}$, $V_{OH(BG)} = V_{CC} - V_{BG}$			100		mV
$V_{OL(BG)}$	BG Low Output Voltage	$I_{BG} = 100\text{mA}$			100		mV
$I_{PU(BG)}$	BG Peak Pull-Up Current		●	2	3.2		A
$I_{PD(BG)}$	BG Peak Pull-Down Current		●	3	4.5		A
Switching Time							
$t_{PLH(TG)}$	BG Low to TG High Propagation Delay				14		ns
$t_{PHL(TG)}$	IN Low to TG Low Propagation Delay				13		ns
$t_{PLH(BG)}$	TG Low to BG High Propagation Delay				13		ns
$t_{PHL(BG)}$	IN High to BG Low Propagation Delay				11		ns
$t_r(TG)$	TG Output Risettime	10% to 90%, $C_L = 3\text{nF}$			8		ns
$t_f(TG)$	TG Output Falltime	10% to 90%, $C_L = 3\text{nF}$			7		ns
$t_r(BG)$	BG Output Risettime	10% to 90%, $C_L = 3\text{nF}$			7		ns
$t_f(BG)$	BG Output Falltime	10% to 90%, $C_L = 3\text{nF}$			4		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4447I is guaranteed to meet specifications from -40°C to 85°C . The LTC4447E is guaranteed to meet specifications from 0°C to 85°C with specifications over the -40°C to 85°C temperature range assured by design, characterization and correlation with statistical process controls.

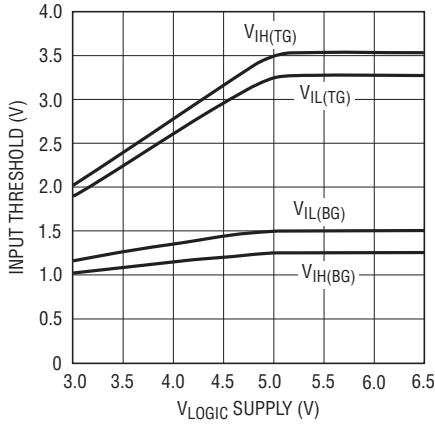
T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \cdot 43^\circ\text{C/W})$$

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

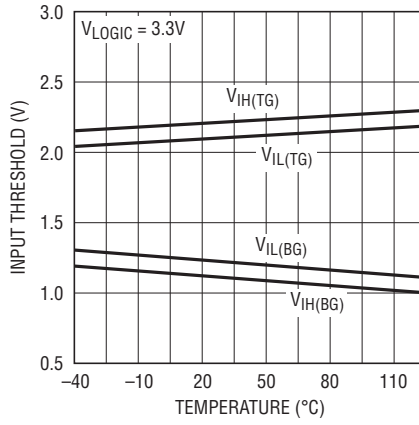
TYPICAL PERFORMANCE CHARACTERISTICS

Input Thresholds vs V_{LOGIC} Supply Voltage



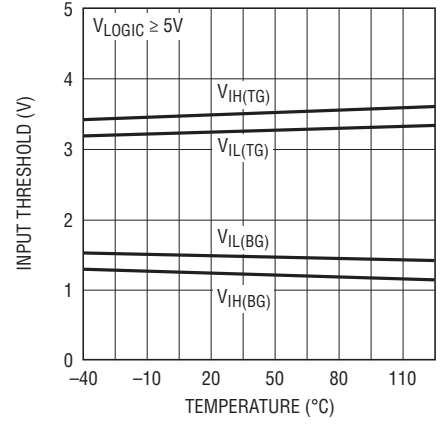
4447 G01

Input Thresholds for $V_{\text{LOGIC}} = 3.3\text{V}$ vs Temperature



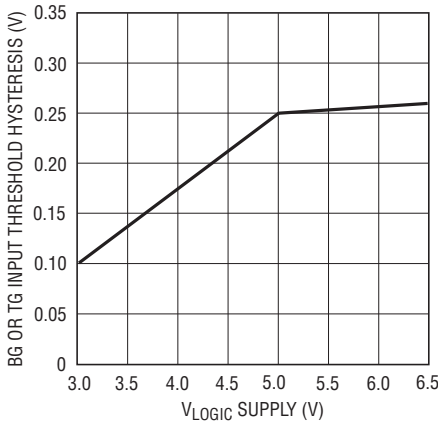
4447 G02

Input Thresholds for $V_{\text{LOGIC}} \geq 5\text{V}$ vs Temperature



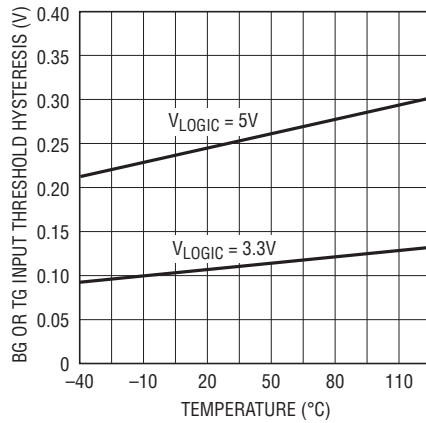
4447 G03

BG or TG Input Threshold Hysteresis vs V_{LOGIC} Supply Voltage



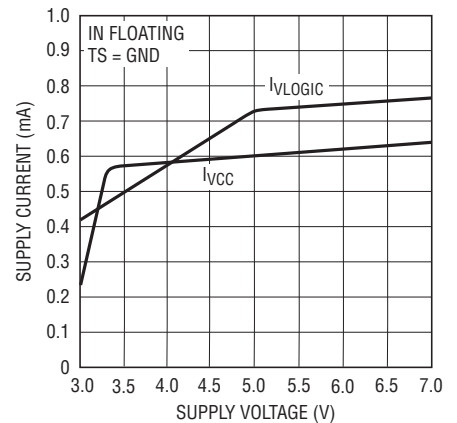
4447 G04

BG or TG Input Threshold Hysteresis vs Temperature



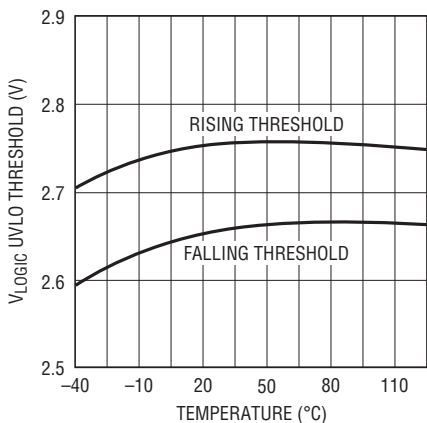
4447 G05

Quiescent Supply Current vs Supply Voltage



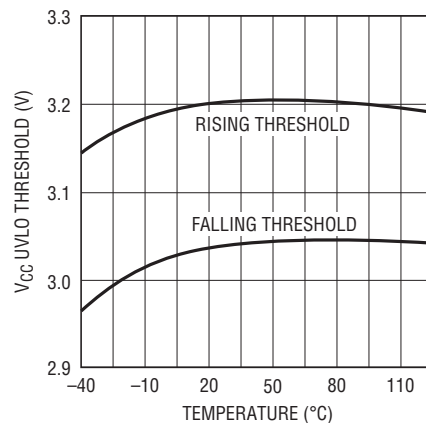
4447 G06

V_{LOGIC} Undervoltage Lockout Thresholds vs Temperature



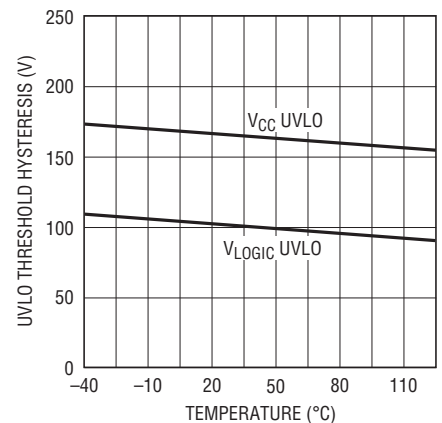
4447 G08

V_{CC} Undervoltage Lockout Thresholds vs Temperature



4447 G09a

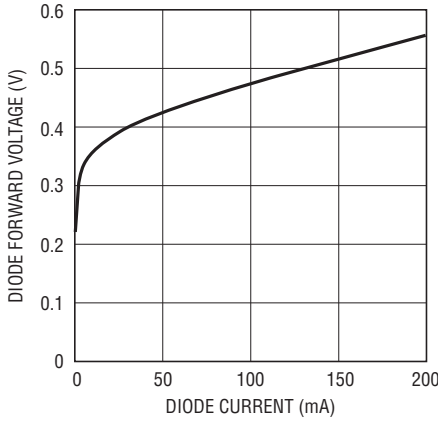
Undervoltage Lockout Threshold Hysteresis vs Temperature



4447 G09b

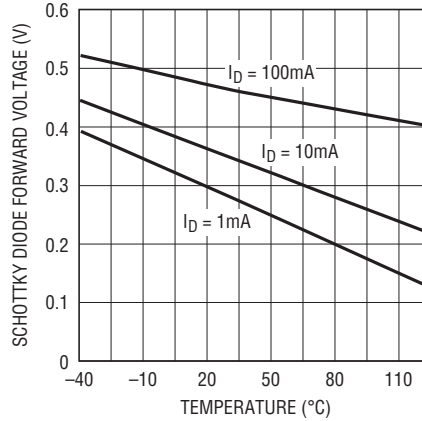
TYPICAL PERFORMANCE CHARACTERISTICS

Schottky Diode Forward Voltage vs Diode Current



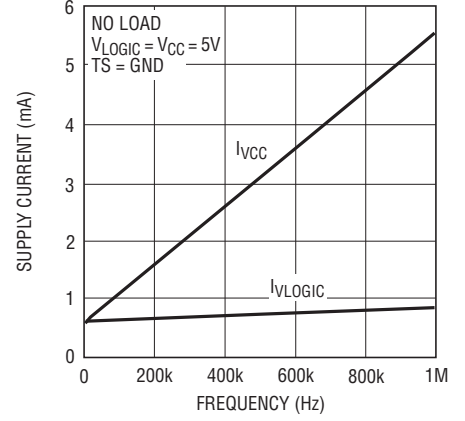
4447 G10

Schottky Diode Forward Voltage vs Temperature



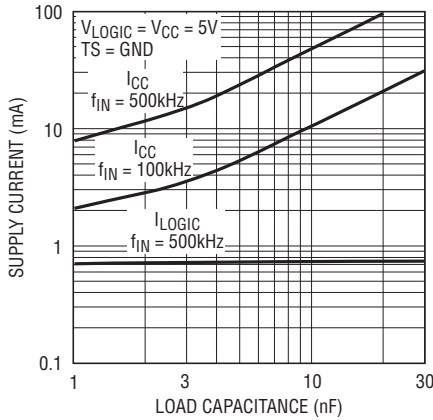
4447 G11

Supply Current vs Input Frequency



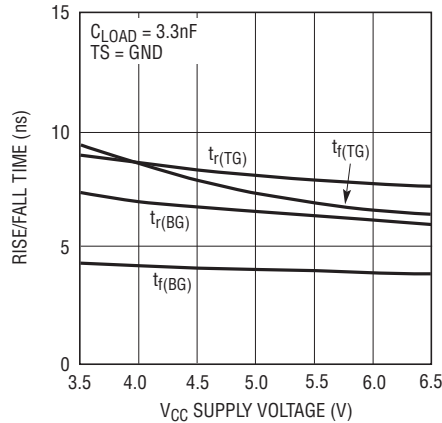
4447 G12

Switching Supply Current vs Load Capacitance



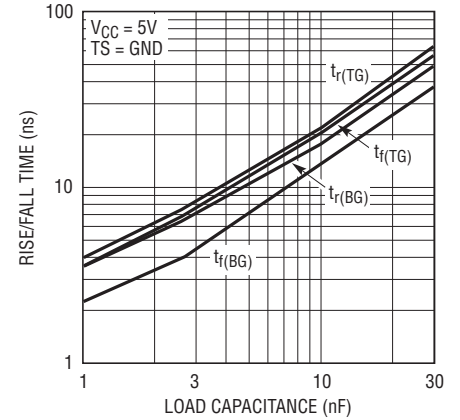
4447 G13

Rise and Fall Time vs V_{CC} Supply Voltage



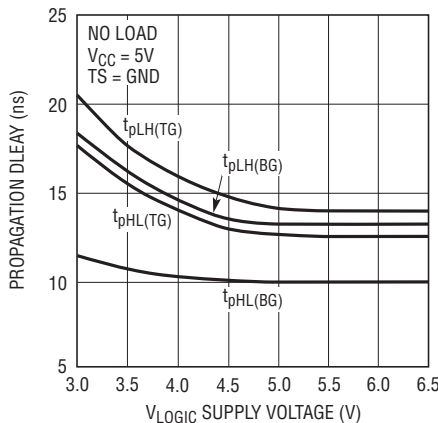
4447 G14

Rise and Fall Time vs Load Capacitance



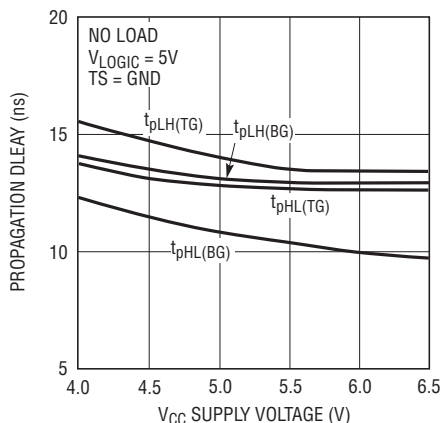
4447 G15

Propagation Delay vs V_{LOGIC} Supply Voltage



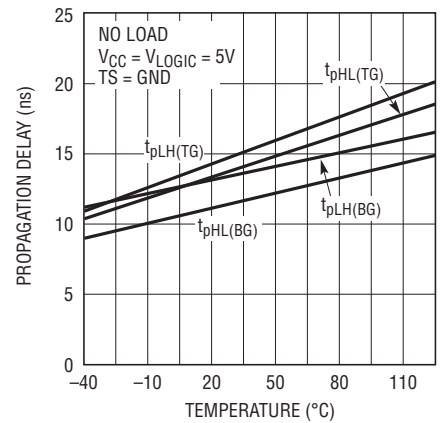
4447 G16

Propagation Delay vs V_{CC} Supply Voltage



4447 G17

Propagation Delay vs Temperature



4447 G18

PIN FUNCTIONS

NC (Pins 1, 2): No Connection Required.

TG (Pin 3): High Side Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

TS (Pin 4): High Side MOSFET Source Connection (Top Source).

BG (Pin 5): Low Side Gate Driver Output (Bottom Gate). This pin swings between V_{CC} and GND.

GND (Pin 6): Chip Ground.

IN (Pin 7): Input Signal. Input referenced to an internal supply baised off of V_{LOGIC} (Pin 8) and GND (Pin 6). If this pin is floating, an internal resistive divider triggers a shutdown mode in which both BG (Pin 5) and TG (Pin 3) are pulled low. Trace capacitance on this pin should be minimized to keep the shutdown time low.

V_{LOGIC} (Pin 8): Logic Supply. This pin powers the input buffer and logic. Connect this pin to the power supply

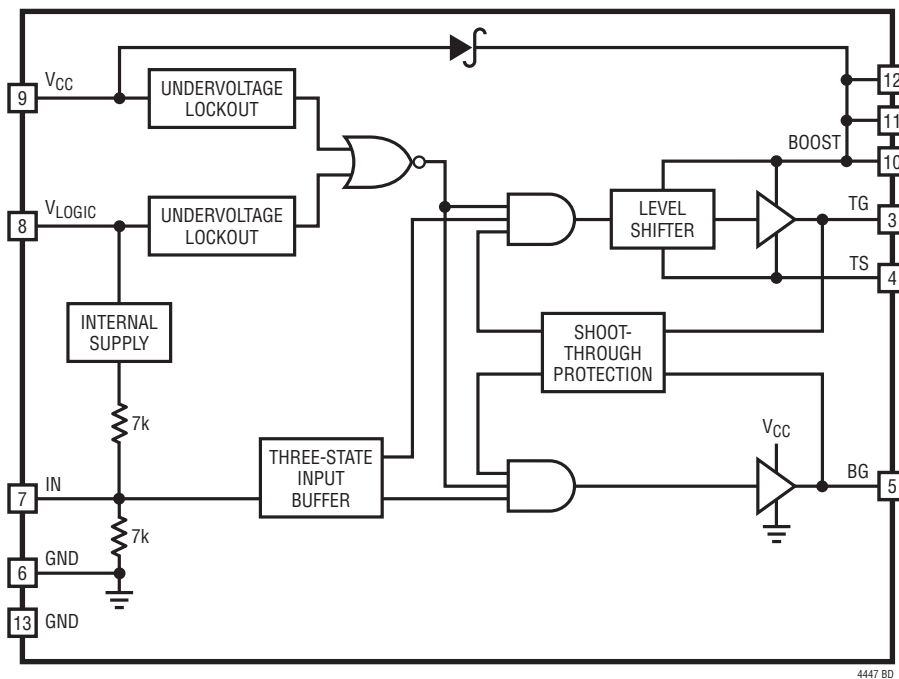
of the controller that is driving IN (Pin 7) to match input thresholds or to V_{CC} (Pin 9) to simplify PCB routing.

V_{CC} (Pin 9): Output Driver Supply. This pin powers the low side gate driver output directly and the high side gate driver output through an internal Schottky diode connected between this pin and BOOST. A low ESR ceramic bypass capacitor should be tied between this pin and GND (Pin 6).

BOOST (Pins 10, 11, 12): High Side Bootstrapped Supply. An external capacitor should be tied between these pins and TS (Pin 4). An internal Schottky diode is connected between V_{CC} (Pin 9) and these pins. Voltage swing at these pins is from $V_{CC} - V_D$ to $V_{IN} + V_{CC} - V_D$, where V_D is the forward voltage drop of the Schottky diode.

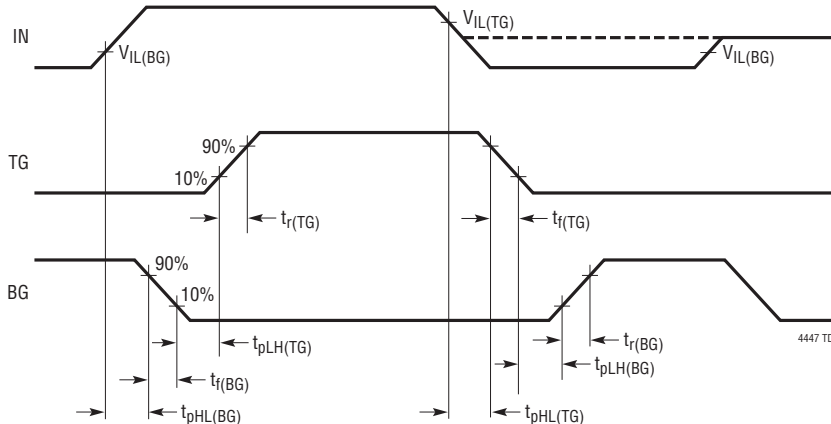
Exposed Pad (Pin 13): Ground. The exposed pad must be soldered to PCB ground for optimal electrical and thermal performance.

BLOCK DIAGRAM



4447 BD

TIMING DIAGRAM



OPERATION

Overview

The LTC4447 receives a ground-referenced, low voltage digital input signal to drive two N-channel power MOSFETs in a synchronous power supply configuration. The gate of the low side MOSFET is driven either to V_{CC} or GND, depending on the state of the input. Similarly, the gate of the high side MOSFET is driven to either BOOST or TS by a supply bootstrapped off of the switch node (TS).

Input Stage

The LTC4447 employs a unique three-state input stage with transition thresholds that are proportional to the V_{LOGIC} supply. The V_{LOGIC} supply can be tied to the controller IC's power supply so that the input thresholds will match those of the controller's output signal. Alternatively, V_{LOGIC} can be tied to V_{CC} to simplify routing. An internal voltage regulator in the LTC4447 limits the input threshold values for V_{LOGIC} supply voltages greater than 5V.

The relationship between the transition thresholds and the three input states of the LTC4447 is illustrated in Figure 1. When the voltage on IN is greater than the threshold $V_{IH(TG)}$, TG is pulled up to BOOST, turning the high side MOSFET on. This MOSFET will stay on until IN falls below $V_{IL(TG)}$. Similarly, when IN is less than $V_{IH(BG)}$, BG is pulled up to V_{CC} , turning the low side (synchronous) MOSFET on. BG will stay high until IN increases above the threshold $V_{IL(BG)}$.

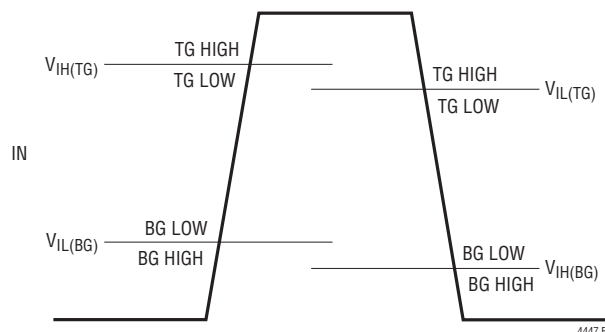


Figure 1. Three-State Input Operation

The thresholds are positioned to allow for a region in which both BG and TG are low. An internal resistive divider will pull IN into this region if the signal driving the IN pin goes into a high impedance state.

One application of this three-state input is to keep both of the power MOSFETs off while an undervoltage condition exists on the controller IC power supply. This can be accomplished by driving the IN pin with a logic buffer that has an enable pin. With the enable pin of the buffer tied to the power good pin of the controller IC, the logic buffer output will remain in a high impedance state until the controller confirms that its supply is not in an undervoltage state. The three-state input of the LTC4447 will therefore pull IN into the region where TG and BG are low until the controller has enough voltage to operate predictably.

OPERATION

The hysteresis between the corresponding V_{IH} and V_{IL} voltage levels eliminates false triggering due to noise during switch transitions; however, care should be taken to keep noise from coupling into the IN pin, particularly in high frequency, high voltage applications.

Undervoltage Lockout

The LTC4447 contains undervoltage lockout detectors that monitor both the V_{CC} and V_{LOGIC} supplies. When V_{CC} falls below 3.04V or V_{LOGIC} falls below 2.65V, the output pins BG and TG are pulled to GND and TS, respectively. This turns off both of the external MOSFETs. When V_{CC} and V_{LOGIC} have adequate supply voltage for the LTC4447 to operate reliably, normal operation will resume.

Adaptive Shoot-Through Protection

Internal adaptive shoot-through protection circuitry monitors the voltages on the external MOSFETs to ensure that they do not conduct simultaneously. The LTC4447 does not allow the bottom MOSFET to turn on until the gate-source voltage on the top MOSFET is sufficiently low, and vice-versa. This feature improves efficiency by eliminating cross-conduction current from flowing from the V_{IN} supply through the MOSFETs to ground during a switch transition.

Output Stage

A simplified version of the LTC4447's output stage is shown in Figure 2. The pull-up device on both the BG and TG outputs is an NPN bipolar junction transistor (Q1 and Q2) in parallel with a low resistance P-channel MOSFET (P1 and P2). This powerful combination rapidly pulls the BG and TG outputs to their positive rails (V_{CC} and BOOST, respectively). Both BG and TG have N-channel MOSFET pull-down devices (N1 and N2) which pull BG and TG down to their negative rails, GND and TS. An additional NPN bipolar junction transistor (Q3) is present on BG to increase its pull-down drive current capacity. The rail-to-rail voltage swing of the BG and TG output pins is important in driving external power MOSFETs, whose $R_{DS(ON)}$ is inversely proportional to its gate overdrive voltage ($V_{GS} - V_{TH}$).

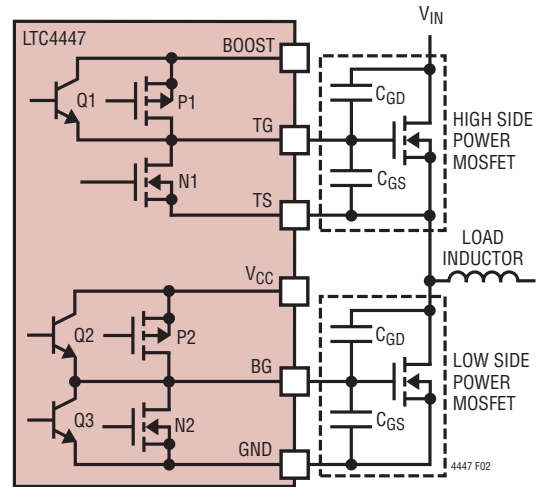


Figure 2. Capacitance Seen by BG and TG During Switching

Rise/Fall Time

Since the power MOSFETs generally account for the majority of power loss in a converter, it is important to quickly turn them on and off, thereby minimizing the transition time and power loss. The LTC4447's peak pull-up current of 3.2A for both BG and TG produces a rapid turn-on transition for the MOSFETs. This high current is capable of driving a 3nF load with an 8ns risetime.

It is also important to turn the power MOSFETs off quickly to minimize power loss due to transition time; however, an additional benefit of a strong pull-down on the driver outputs is the prevention of cross-conduction current. For example, when BG turns the low side power MOSFET off and TG turns the high side power MOSFET on, the voltage on the TS pin will rise to V_{IN} very rapidly. This high frequency positive voltage transient will couple through the C_{GD} capacitance of the low side power MOSFET to the BG pin. If the BG pin is not held down sufficiently, the voltage on the BG pin will rise above the threshold voltage of the low side power MOSFET, momentarily turning it back on. As a result, both the high side and low side MOSFETs will be conducting, which will cause significant cross-conduction current to flow through the MOSFETs from V_{IN} to ground, thereby introducing substantial power loss. A similar effect occurs on TG due to the C_{GS} and C_{GD} capacitances of the high side MOSFET.

OPERATION

The LTC4447's powerful parallel combination of the N-channel MOSFET (N2) and NPN (Q3) on the BG pull-down generates a phenomenal 4ns fall time on BG while driving a 3nF load. Similarly, the 0.8Ω pull-down

MOSFET (N1) on TG results in a rapid 7ns fall time with a 3nF load. These powerful pull-down devices minimize the power loss associated with MOSFET turn-off time and cross-conduction current.

APPLICATIONS INFORMATION

Power Dissipation

To ensure proper operation and long-term reliability, the LTC4447 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + (P_D)(\theta_{JA})$$

where:

T_J = junction temperature

T_A = ambient temperature

P_D = power dissipation

θ_{JA} = junction-to-ambient thermal resistance

Power dissipation consists of standby, switching and capacitive load power losses:

$$P_D = P_{DC} + P_{AC} + P_{QG}$$

where:

P_{DC} = quiescent power loss

P_{AC} = internal switching loss at input frequency f_{IN}

P_{QG} = loss due turning on and off the external MOSFET with gate charge Q_G at frequency f_{IN}

The LTC4447 consumes very little quiescent current. The DC power loss at $V_{LOGIC} = 5V$ and $V_{CC} = 5V$ is only $(730\mu A + 600\mu A)(5V) = 6.65mW$.

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal nodal capacitances and cross-conduction currents in the internal logic gates. The sum of the quiescent current and internal switching current with no

load are shown in the Typical Performance Characteristics plot of Switching Supply Current vs Input Frequency.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads C_{LOAD} on TG and BG at switching frequency f_{IN} , the load losses would be:

$$P_{CLOAD} = (C_{LOAD})(f_{IN})[(V_{BOOST} - V_{TS})^2 + (V_{CC})^2]$$

In a typical synchronous buck configuration, $V_{BOOST} - V_{TS}$ is equal to $V_{CC} - V_D$, where V_D is the forward voltage drop of the internal Schottky diode between V_{CC} and BOOST. If this drop is small relative to V_{CC} , the load losses can be approximated as:

$$P_{CLOAD} \approx 2(C_{LOAD})(f_{IN})(V_{CC})^2$$

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its V_{GS} voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge, Q_G . The Q_G value corresponding to the MOSFET's V_{GS} value (V_{CC} in this case) can be readily obtained from the manufacturer's Q_G vs V_{GS} curves. For identical MOSFETs on TG and BG:

$$P_{QG} \approx 2(V_{CC})(Q_G)(f_{IN})$$

To avoid damaging junction temperatures due to power dissipation, the LTC4447 includes a temperature monitor that will pull BG and TG low if the junction temperature exceeds 160°C. Normal operation will resume when the junction temperature cools to less than 135°C.

APPLICATIONS INFORMATION

Bypassing and Grounding

The LTC4447 requires proper bypassing on the V_{LOGIC} , V_{CC} and $V_{\text{BOOST-TS}}$ supplies due to its high speed switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimum performance from the LTC4447:

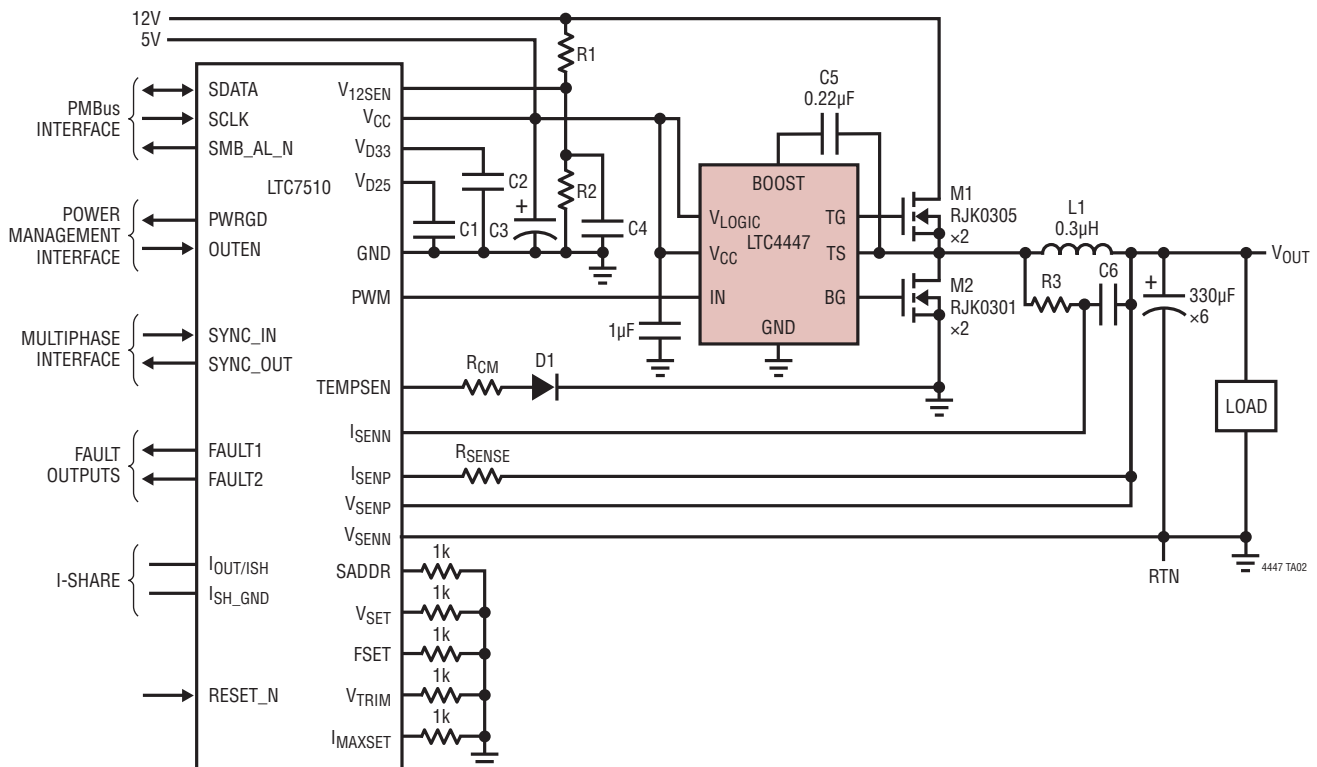
- Mount the bypass capacitors as close as possible between the V_{LOGIC} and GND pins, the V_{CC} and GND pins, and the BOOST and TS pins. The leads should be shortened as much as possible to reduce lead inductance.
- Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC4447 switches greater than

5A peak currents and any significant ground drop will degrade signal integrity.

- Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- Keep the copper trace between the driver output pin and the load short and wide.
- Be sure to solder the Exposed Pad on the back side of the LTC4447 packages to the board. Correctly soldered to a double-sided copper board, the LTC4447 has a thermal resistance of approximately 43°C/W. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater.

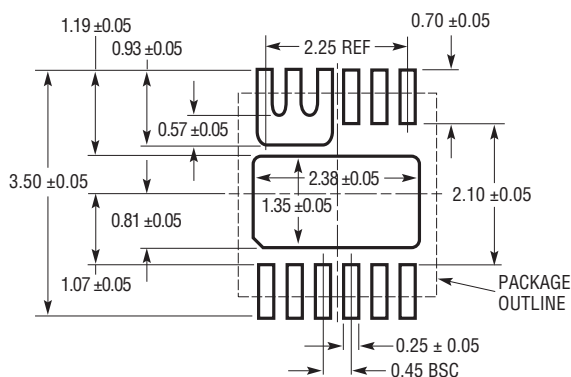
TYPICAL APPLICATION

LTC7510/LTC4447 12V to 1.5V/30A Digital Step-Down DC/DC Converter with PMBus Serial Interface

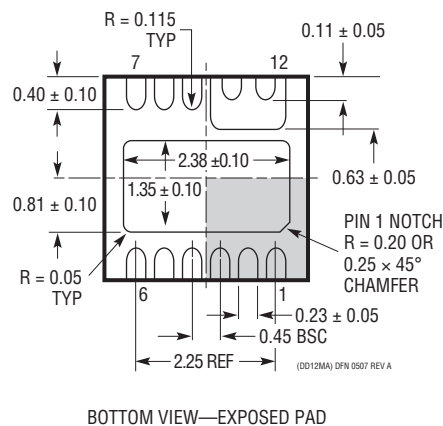
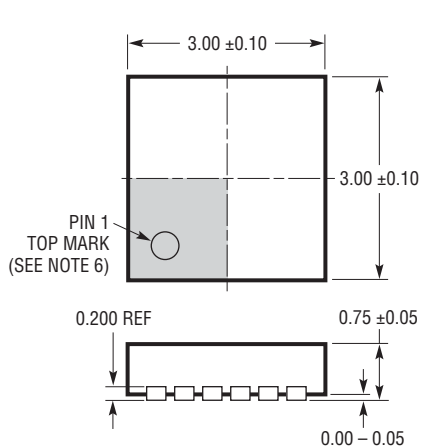


PACKAGE DESCRIPTION

DDMA Package 12-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1743 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:

1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1154	High Side Micropower MOSFET Driver	Internal Charge Pump 4.5V to 18V Supply Range
LTC1155	Dual Micropower High/Low Side Driver	Internal Charge Pump 4.5V to 18V Supply Range
LT®1161	Quad Protected High Side MOSFET Driver	8V to 48V Supply Range, $t_{ON} = 200\mu s$, $t_{OFF} = 28\mu s$
LTC1163	Triple 1.8V to 6V High Side MOSFET Driver	1.8V to 6V Supply Range, $t_{ON} = 95\mu s$, $t_{OFF} = 45\mu s$
LTC1693 Family	High Speed Single/Dual N-Channel MOSFET Drivers	1.5A Peak Output Current, $4.5V \leq V_{IN} \leq 13.2V$
LTC3900	Synchronous Rectifier Driver for Forward Converters	Pulse Drive Transformer Synchronous Input
LTC3901	Secondary Side Synchronous Driver for Push-Pull and Full-Bridge Converters	Gate Drive Transformer Synchronous Input
LTC4440	High Speed, High Voltage High Side Gate Driver	High Side Source Up to 100V, $8V \leq V_{CC} \leq 15V$
LTC4440-5	High Speed, High Voltage High Side Gate Driver	High Side Source Up to 80V, $4V \leq V_{CC} \leq 15V$
LTC4441	6A MOSFET Driver	6A Peak Output Current, Adjustable Gate Drive from 5V to 8V, $5V \leq V_{IN} \leq 25V$
LTC4442/LTC4442-1	High Speed Synchronous N-Channel MOSFET Driver	5A Peak Output Current, Three-State Input, 38V Maximum Input Supply Voltage, $6V \leq V_{CC} \leq 9.5V$, MS8E Package
LTC4443/LTC4443-1	High Speed Synchronous N-Channel MOSFET Driver	5A Peak Output Current, Internal Schottky Diode, 38V Maximum Input Supply Voltage, $6V \leq V_{CC} \leq 9.5V$, 3mm x 3mm DFN-12
LTC4444/LTC4444-5	High Voltage/High Speed Synchronous N-Channel MOSFET Driver	3A Peak Output Current, 100V Maximum Input Supply Voltage, $4.5V \leq V_{CC} \leq 13.5V$, with Adaptive Shoot Through Protection
LTC4446	High Voltage High Side/Low Side N-Channel MOSFET Driver	3A Output Current, 100V Input Supply Voltage, $7.2V \leq V_{CC} \leq 13.5V$, without Adaptive Shoot Through Protection
LTC7510	Digital DC/DC Controller with PMBus Interface	Digital Controller, PMBus Serial Interface, 150kHz to 2MHz Switching Frequency

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View LTC4447IDD#PBF on WIN SOURCE](#)
- ⊖ [Analog Devices Inc. Information](#)

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