THE DATASHEET OF

LTC4091EDJC#TRPBF

36V Battery Charger and Power Backup Manager

FEATURES

- **Seamless Transition Between Primary Power Source and Li-Ion Battery**
- **2A High Voltage Step-Down Regulator with Adaptive Output Control**
- **Internal 75mΩ Ideal Diode Plus Optional External Ideal Diode Controller Provides Low Loss PowerPath™ When Primary Supply Not Present**
- Wide Input Voltage Range: 6V to 36V (60V Abs Max)
- 4.45V Max Output Voltage
- Full Featured Li-Ion Battery Charger
- Pin Selectable 4.1V and 4.2V Charge Voltage Options
- Thermally Enhanced Low Profile (0.75mm) 6mm × 3mm 22-Lead DFN Package

APPLICATIONS

- Fleet and Asset Tracking
- Automotive GPS Data Loggers
- Automotive Telematics Systems
- Battery Backup Systems

DESCRIPTION

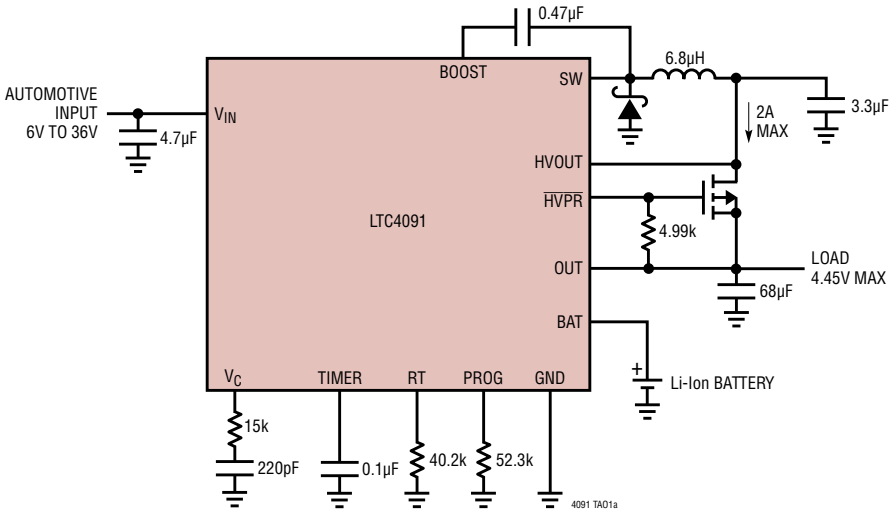
The LTC®4091 is a 36V Li-Ion battery charger and power backup manager. The integrated step-down switching regulator charges a battery from a primary power source while providing power to the load. If primary power is lost, the load is seamlessly transitioned to the backup Li-ion/polymer battery. To protect sensitive downstream loads, the maximum output voltage is 4.45V.

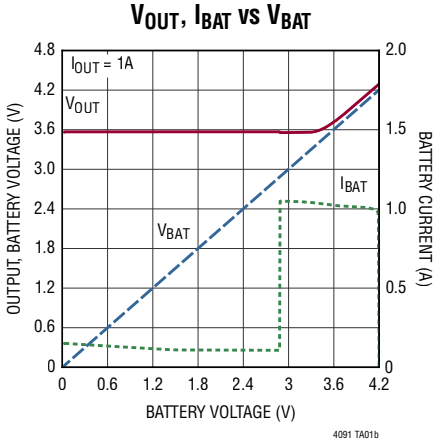
The LTC4091 provides an adaptive output that tracks the battery voltage for high efficiency charging. The charge current is programmable and an end-of-charge status output ($\overline{CHRG}$) indicates full charge. Also featured is a termination timer and an NTC thermistor input used to monitor battery temperature while charging.

During backup, an internal 75mΩ ideal diode connects the battery to the load. An optional external ideal diode FET driver is available to reduce the voltage drop even further. 4.1V or 4.2V battery charge voltages can be selected.

LT, LTC, LTM, Linear Technology, the Linear logo and Burst Mode are registered trademarks and PowerPath and Bat-Track are trademarks of Analog Devices, Inc. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION



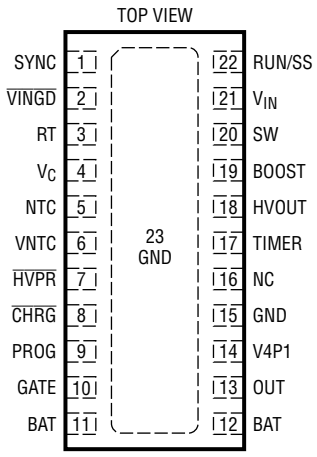


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3, 4)

V_{IN}, RUN/SS (Note 7) 60V
BOOST 56V
BOOST Above SW.....30V
$\overline{VINGD}$, SYNC.....30V
OUT, HVOUT
  t < 1ms and Duty Cycle < 1%.....–0.3V to 7V
  Steady State .....–0.3V to 6V
BAT, V4P1, V_C, $\overline{CHRG}$, $\overline{HVPR}$.....–0.3V to 6V
NTC, TIMER, PROG.....–0.3V to V_{CC} + 0.3V
I_{OUT}, I_{BAT}.....4A
Operating Junction Temperature Range.....–40°C to 125°C
Storage Temperature Range .....–65 to 150°C

PIN CONFIGURATION



DJC PACKAGE
22-LEAD (6mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 31.8°C/W
EXPOSED PAD (PIN 23) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC4091#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4091EDJC#PBF	LTC4091EDJC#TRPBF	4091	22-Lead (6mm × 3mm) Plastic DFN	–40°C to 125°C
LTC4091IDJC#PBF	LTC4091IDJC#TRPBF	4091	22-Lead (6mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = RUN/SS = 12V, BOOST = 17V, V_{BAT} = 3.7V and R_{PROG} = 105k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Step-Down Regulator							
V_{VIN}	Operating Supply Voltage		●	6		36	V
V_{OVLO}	V_{IN} Overvoltage Lockout Threshold		●	36	38	40	V
I_{VIN}	V_{IN} Bias Current	Shutdown; RUN/SS = 0.2V Charger Terminated, $R_{\overline{HVPR}}$ = 4.99k			0.01 1.1	1	µA mA
V_{OUT}	Output Voltage with V_{IN} Present	Assumes HVOUT to OUT Connection		3.45	V_{BAT}+0.1	4.45	V
f_{SW}	Switching Frequency	R_T = 8.66k R_T = 29.4k R_T = 187k		2.1 900 160	2.4 1000 200	2.7 1150 240	MHz kHz kHz
t_{OFF}	Minimum Switch Off-Time		●		60	150	ns
$I_{SW(MAX)}$	Switch Current Limit			2.5	3.8	5.0	A
V_{SAT}	Switch V_{CESAT}	I_{SW} = 2A			500		mV
I_R	Boost Schottky Reverse Leakage	SW = 10V, HVOUT = 0V			0.02	2	µA
$V_{B(MIN)}$	Minimum Boost Voltage (Note 6)		●		1.5	2.1	V
I_{BST}	BOOST Pin Current	I_{SW} = 1A			22	35	mA
Battery Management (Note 8)							
I_{BAT}	Battery Drain Current	V_{VIN} = 0V, BAT Powers OUT, No Load	●		60	100	µA
V_{CHG}	V_{BAT} Regulated Output Voltage	I_{BAT} = 2mA; V4P1 = Open I_{BAT} = 2mA; V4P1 = BAT		4.148 4.048	4.200 4.100	4.252 4.152	V V
I_{CHG}	Constant-Current Mode Charge Current	R_{PROG} = 105k, No Load R_{PROG} = 52.3k, No Load; 0 ≤ T_A ≤ 85°C	● ●	465 880	500 1000	550 1100	mA mA
$I_{CHG(MAX)}$	Maximum Charge Current	(Note 5)			1.5		A
V_{PROG}	PROG Pin Servo Voltage	R_{PROG} = 105k R_{PROG} = 52.3k	● ●	0.98 0.98	1.00 1.00	1.02 1.02	V V
k_{EOC}	Ratio of End-of-Charge Indication Current to Charge Current	V_{BAT} = V_{CHG} (4.2V)	●	0.08	0.1	0.13	mA/mA
I_{TRKL}	Trickle Charge Current	BAT = 2V		35	50	75	mA
V_{TRKL}	Trickle Charge Threshold Voltage	BAT Rising	●	2.75	2.9	3.0	V
V_{CEN}	Charger Enable Threshold Voltage	(V_{OUT} – V_{BAT}) Falling; V_{BAT} = 4V (V_{OUT} – V_{BAT}) Rising; V_{BAT} = 4V			55 80		mV mV
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{CHG}	●	–65	–100	–150	mV
t_{TIMER}	TIMER Accuracy	V_{BAT} = 4.3V		–10		10	%
	Recharge Time	Percent of Total Charge Time			50		%
	Low Battery Trickle Charge Time	Percent of Total Charge Time, V_{BAT} < V_{TRKL}			25		%
T_{LIM}	Junction Temperature in Constant Temperature Mode				105		°C
Internal Ideal Diode							
$R_{DIO,ON}$	On Resistance V_{BAT} to V_{OUT}	I_{OUT} = 2A			75		mΩ
V_{FWD}	Voltage Forward Drop (V_{BAT} – V_{OUT})	I_{OUT} = 5mA I_{OUT} = 100mA I_{OUT} = 1000mA	●	10	30 40 75	50	mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = RUN/SS = 12V, BOOST = 17V, V_{BAT} = 3.7V and R_{PROG} = 105k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
External Ideal Diode							
$V_{FWD,EXT}$	External Diode Forward Voltage				20		mV
Logic ($\overline{CHRG}$, $\overline{VINGD}$, $\overline{HVPR}$, TIMER, RUN/SS, SYNC)							
$V_{CHG,SD}$	Charger Shutdown Threshold Voltage on TIMER	V_{TIMER} Falling	●			0.1	V
$I_{CHG,SD}$	Charger Shutdown Pull-Up Current on TIMER	V_{TIMER} = 0V	●	5	14		µA
V_{OL}	Output Low Voltage	($\overline{CHRG}$, $\overline{HVPR}$); I_{SINK} = 5mA	●		0.1	0.4	V
$V_{RUN,H}$	RUN/SS High Threshold			3			V
$V_{RUN,L}$	RUN/SS Low Threshold					0.2	V
$I_{RUN/SS}$	RUN/SS Pin Bias Current	RUN/SS = 2.5V			5	10	µA
I_{VGLK}	$\overline{VINGD}$ Leakage	$\overline{VINGD}$ = 5V, RUN/SS = 0V			0.1	1	µA
I_{VG}	$\overline{VINGD}$ Sink Current	$\overline{VINGD}$ = 0.4V	●	100	400		µA
$V_{SYNC,L}$	SYNC Low Threshold					0.3	V
$V_{SYNC,H}$	SYNC High Threshold			1			V
I_{SYNC}	SYNC Pin Bias Current	V_{SYNC} = 0V			–0.1		µA
NTC							
I_{VNTC}	VNTC Pin Current	VNTC = 2.5V		1.4	2.5	3.5	mA
V_{VNTC}	VNTC Bias Voltage	I_{VNTC} = 500µA	●	4.4	4.85		V
I_{NTC}	NTC Input Leakage Current	NTC = 1V			0	±1	µA
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising NTC Voltage Hysteresis			0.738 • VNTC 0.02 • VNTC		V V
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling NTC Voltage Hysteresis			0.290 • VNTC 0.01 • VNTC		V V
V_{DIS}	NTC Disable Threshold Voltage	Falling NTC Voltage Hysteresis	●	75	100 35	125	mV mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4091 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4091E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4091I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (PD, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 31.8°C/W for the DJC package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 110°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4: V_{CC} is the greater of V_{OUT}, and V_{BAT}

Note 5: Accuracy of programmed current may degrade for currents greater than 1.5A.

Note 6: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the switch.

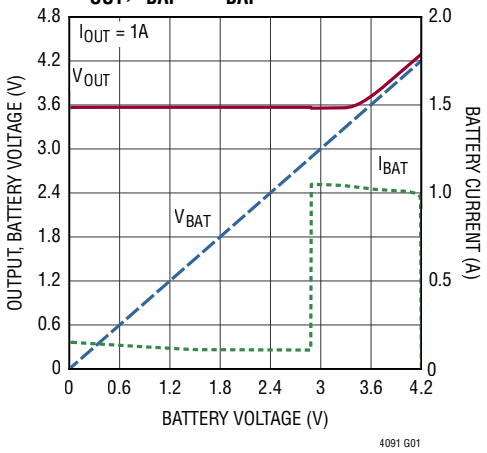
Note 7: Absolute Maximum Voltage at V_{IN} and RUN/SS pins is for nonrepetitive one second transients; 40V for continuous operation.

Note 8: Due to the thermal regulation feature of the battery charger, circuit parameters in the Battery Management section are not testable and do not apply above 85°C.

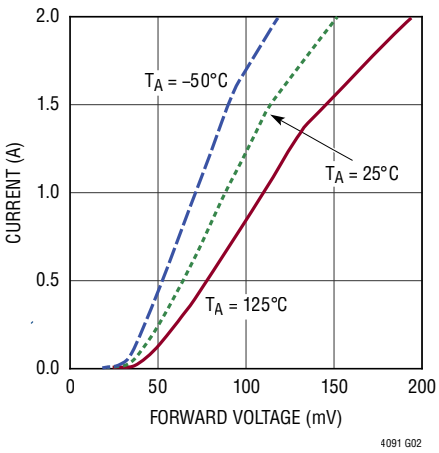
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

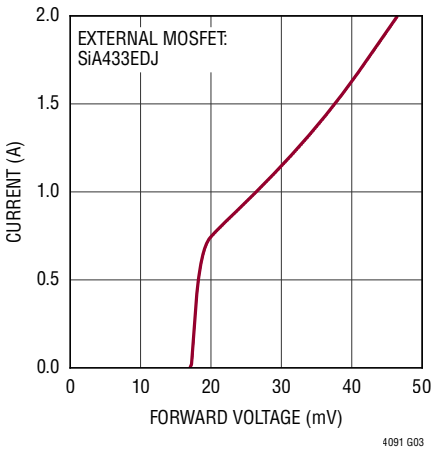
V_{OUT}, I_{BAT} vs V_{BAT}



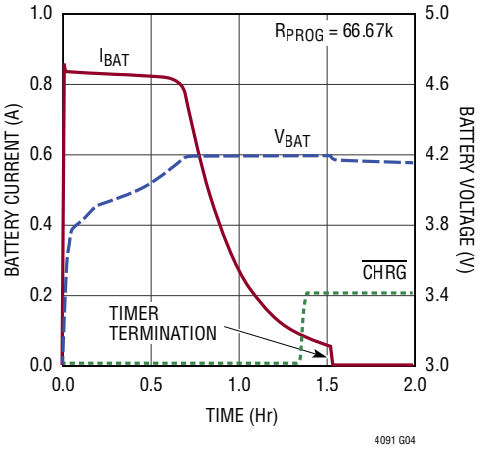
Internal Ideal Diode Current vs V_{FWD}



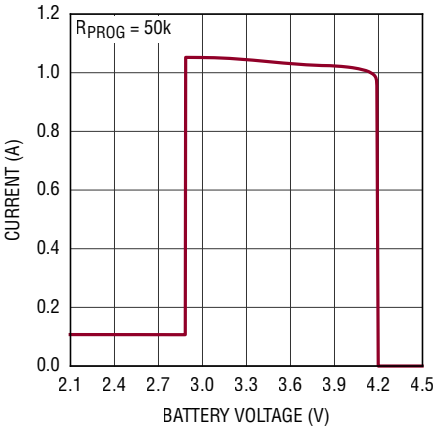
Internal and External Ideal Diode Current vs V_{FWD}



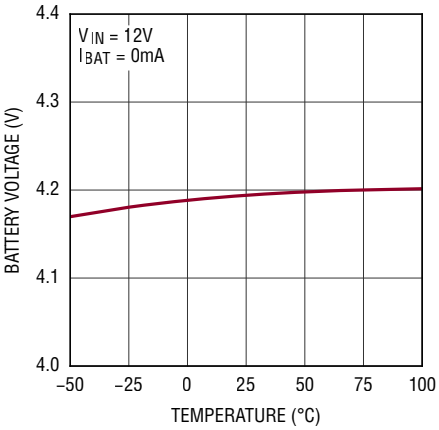
Battery Current and Voltage vs Time



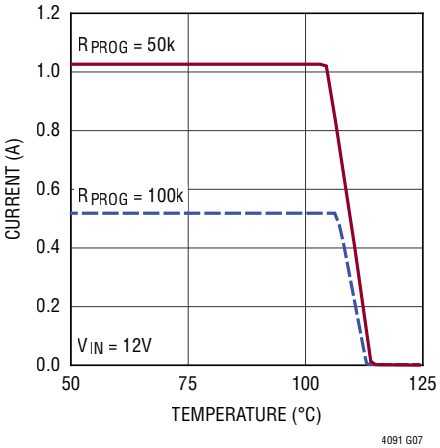
I_{BAT} vs V_{BAT}



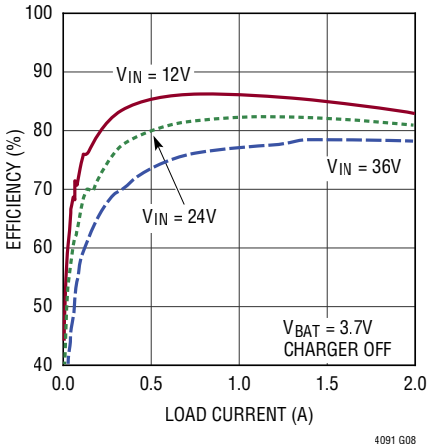
Battery Voltage vs Temperature



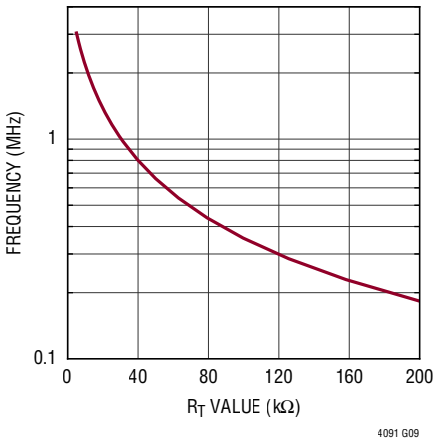
Charge Current vs Temperature (Thermal Regulation)



High Voltage Regulator Efficiency vs Output Load



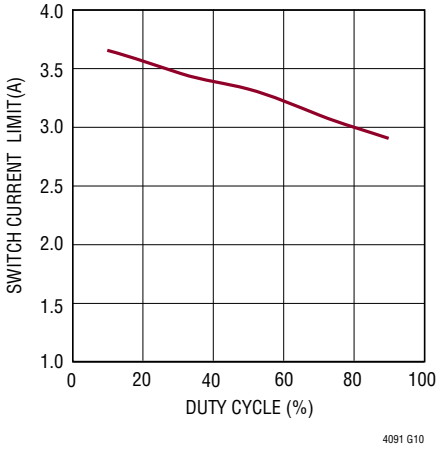
Oscillator Frequency vs R_T



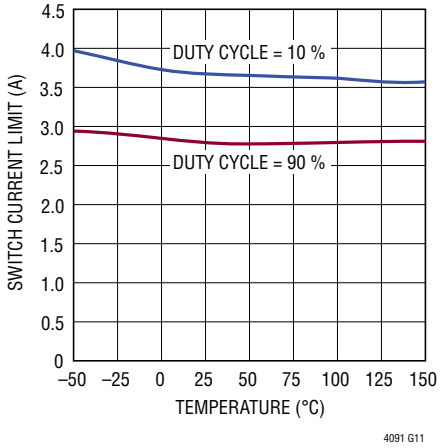
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

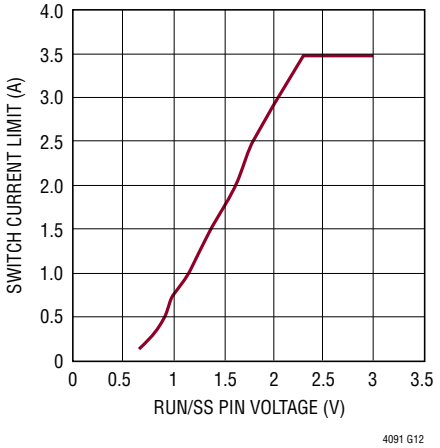
Switch Current Limit



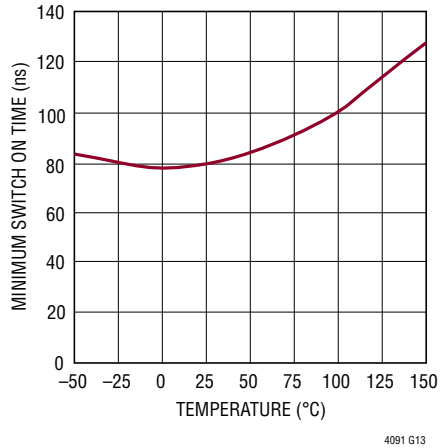
Switch Current Limit



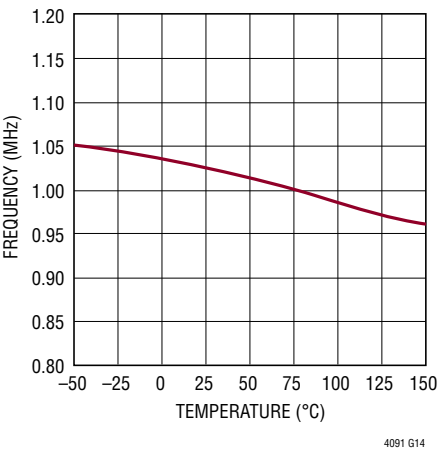
Soft-Start



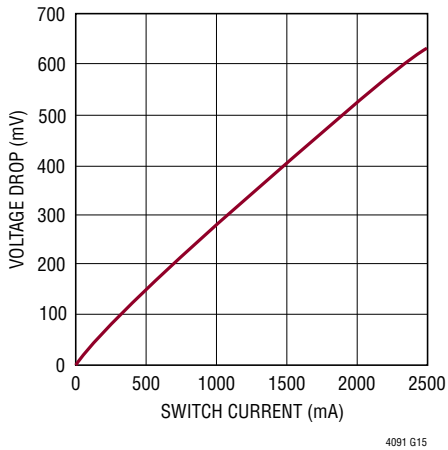
Minimum Switch On-Time



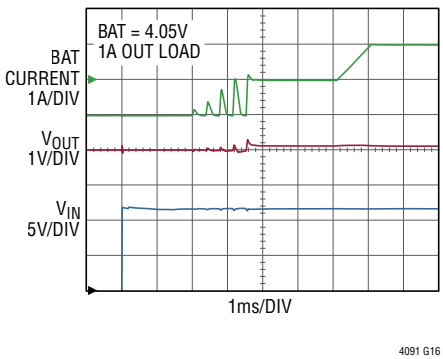
Switching Frequency



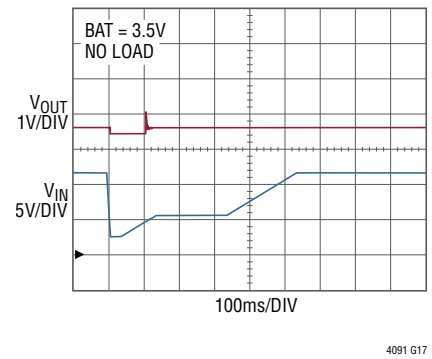
Switch Voltage Drop



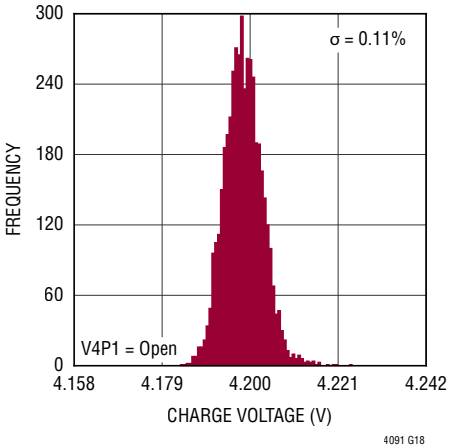
OUT During V_{IN} Hot-Plug



OUT During V_{IN} Cold Crank



Histogram of V_{CHG}



PIN FUNCTIONS

SYNC (Pin 1): External Clock Synchronization Input. See synchronizing section in Applications Information. Ground pin when not used.

$\overline{\text{VINGD}}$ (Pin 2): The $\overline{\text{VINGD}}$ pin is the open collector output of an internal comparator. $\overline{\text{VINGD}}$ remains high impedance until sufficient voltage is present on V_{IN} to enable the switching regulator and RUN/SS is high.

RT (Pin 3): Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency.

V_C (Pin 4): High Voltage Buck Regulator Control Pin. The voltage on this pin controls the peak switch current in the high voltage regulator. Tie an RC network from this pin to ground to compensate the control loop.

NTC (Pin 5): Input to the NTC Thermistor Monitoring Circuits. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery pack to determine if the battery is too hot or too cold to charge. If the battery temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from VNTC to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

VNTC (Pin 6): Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

$\overline{\text{HVPR}}$ (Pin 7): Open-Drain High Voltage Present Output (Active Low). A low on this pin indicates that the high voltage regulator has sufficient voltage to charge the battery.

$\overline{\text{CHRG}}$ (Pin 8): Open-Drain Charge Status Output. When the battery is being charged, the $\overline{\text{CHRG}}$ pin is pulled low by an internal N-channel MOSFET. When the timer runs out or the charge current drops below 10% of the programmed charge current or the input supply is removed, the $\overline{\text{CHRG}}$ pin is forced to a high impedance state.

PROG (Pin 9): Charge Current Program Pin. Connecting a resistor from PROG to ground programs the charge current:

$$I_{CHG}(A) = \frac{52,500V}{R_{PROG}}$$

GATE (Pin 10): External Ideal Diode Gate Connection. This pin controls the gate of an optional external P-channel MOSFET transistor used to supplement the internal ideal diode. The source of the P-channel MOSFET should be connected to OUT and the drain should be connected to BAT. When not in use, this pin should be left floating. It is important to maintain high impedance on this pin and minimize all leakage paths.

BAT (Pins 11, 12): Single-Cell Li-Ion Battery. This pin is used as an output when charging the battery and as an input when supplying power to OUT. When the OUT pin potential drops below the BAT pin potential, an ideal diode function connects BAT to OUT and prevents OUT from dropping more than 100mV below BAT. A precision internal resistor divider sets the final charge voltage on this pin.

OUT (Pin 13): Voltage Output. This pin is used to provide controlled power to a load from either the primary input (V_{IN}) or the battery (BAT). OUT should be bypassed with at least 68µF to GND.

V4P1 (Pin 14): 4.1V Charge Voltage Select Pin. Leave this pin disconnected to select a 4.2V charge voltage. Connect this pin to the BAT pin to select a 4.1V charge voltage. Care should be taken to avoid leakage on the V4P1 pin if it is left open.

GND (Pin 15): Ground Pin.

NC (Pin 16): No Connect. Nothing is connected to this pin.

TIMER (Pin 17): Timer Capacitor. Placing a capacitor, C_{TIMER}, to GND sets the timer period. The timer period is:

$$t_{TIMER}(hours) = C_{TIMER}\ (F) \bullet R_{PROG}\ (\Omega) \bullet 300$$

PIN FUNCTIONS

Charge time is increased if charge current is reduced due to thermal regulation.

Shorting the TIMER pin to GND disables the battery charging functions.

HVOUT (Pin 18): Voltage Output of the Switching Regulator. When sufficient voltage is present at HVOUT, the $\overline{\text{HVPR}}$ pin will be pulled low to indicate that the primary input has been detected. The LTC4091 switching regulator will maintain just enough differential voltage between HVOUT and BAT to keep the battery charger MOSFET out of dropout (typically 100mV from OUT to BAT). HVOUT should be bypassed with 3.3µF to GND.

BOOST (Pin 19): This pin is used to provide drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Place a 0.22µF to 1µF capacitor between BOOST and SW as close as possible to the IC. See Applications section for more information.

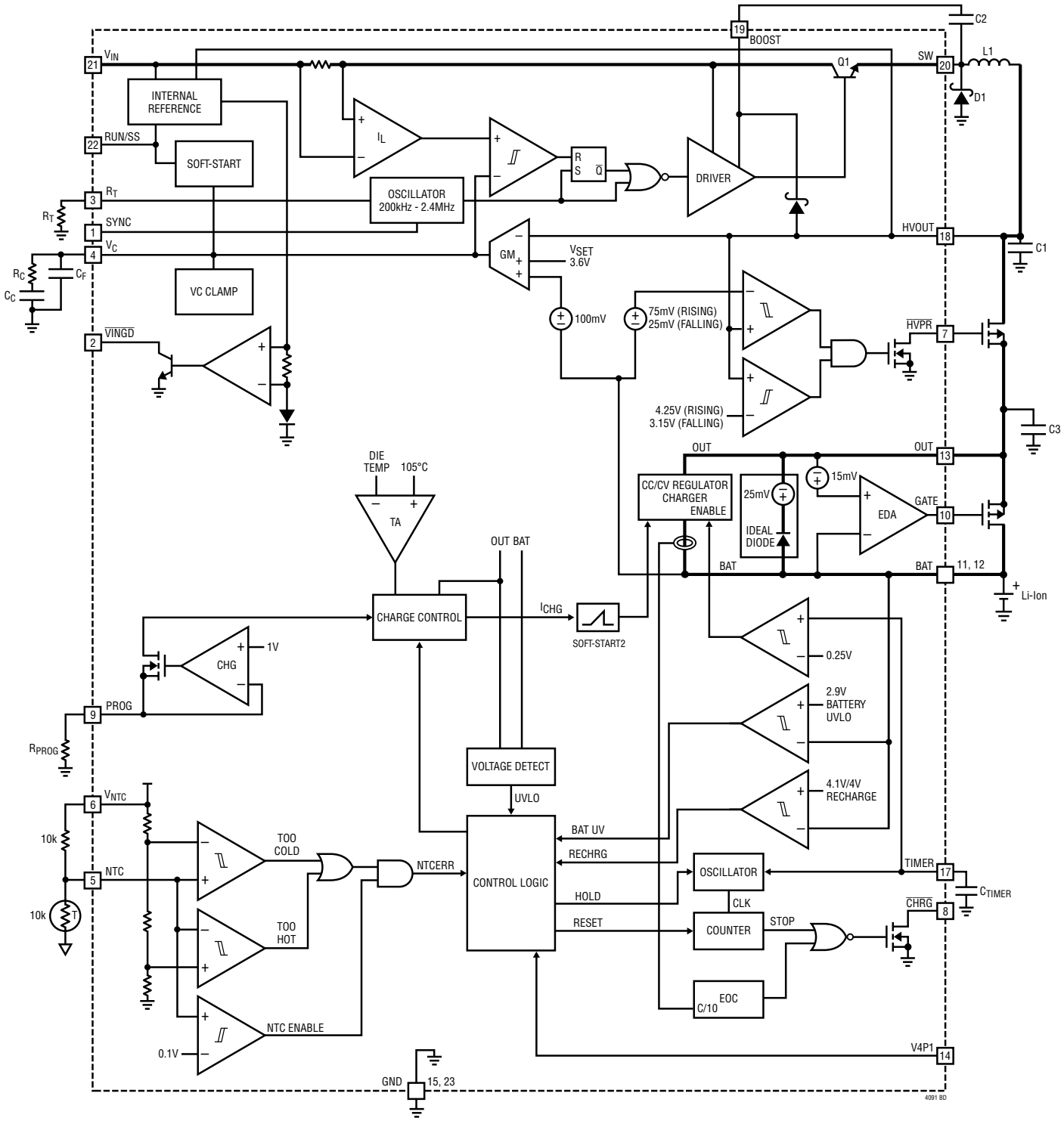
SW (Pin 20): The SW pin is the output of the internal high voltage power switch. Connect this pin to the inductor, catch diode and a boost capacitor.

V_{IN} (Pin 21): Switching Regulator Input. The V_{IN} pin supplies current to the internal high voltage regulator and to the internal high voltage power switch. This pin must be locally bypassed. See Applications Information section to determine value.

RUN/SS (Pin 22): High Voltage Regulator Enable Input. The RUN/SS pin is used to enable the high voltage regulator. Tie to ground to disable the high voltage input or tie to at least 3V to enable the high voltage path. If this feature is not used tie to the V_{IN} pin. This pin can also be used to soft-start the high voltage regulator; see the Applications Information section for more information.

GND (Exposed Pad Pin 23): Ground. The exposed package pad is ground and must be soldered to the PC board for proper functionality and for maximum heat transfer (use several vias directly under the LTC4091).

BLOCK DIAGRAM



OPERATION

Introduction

The LTC4091 is a high voltage switching battery charger and power supply as well as a battery backup manager. The LTC4091 is designed to receive power from a primary input source (e.g. automotive battery, 12V wall adapter, etc.) and a single-cell Li-Ion battery. The switching regulator produces a voltage between 3.6V and 4.45V to charge the battery and power the system load. If the primary source fails and can no longer power the load, the LTC4091 seamlessly transitions to the backup battery (see Figure 1 for a simplified block diagram).

When enabled, the LTC4091 regulates the HVOUT voltage using a constant frequency, current mode regulator. An external PFET between HVOUT (drain) and OUT (source) is turned on via the $\overline{\text{HVPR}}$ pin allowing OUT to charge the battery and/or supply power to the application. The LTC4091 maintains approximately 100mV between the HVOUT pin and the BAT pin.

An ideal diode function provides power from the battery when input power is removed. Powering the load through the ideal diode instead of connecting the load directly to the battery allows a fully charged battery to remain fully

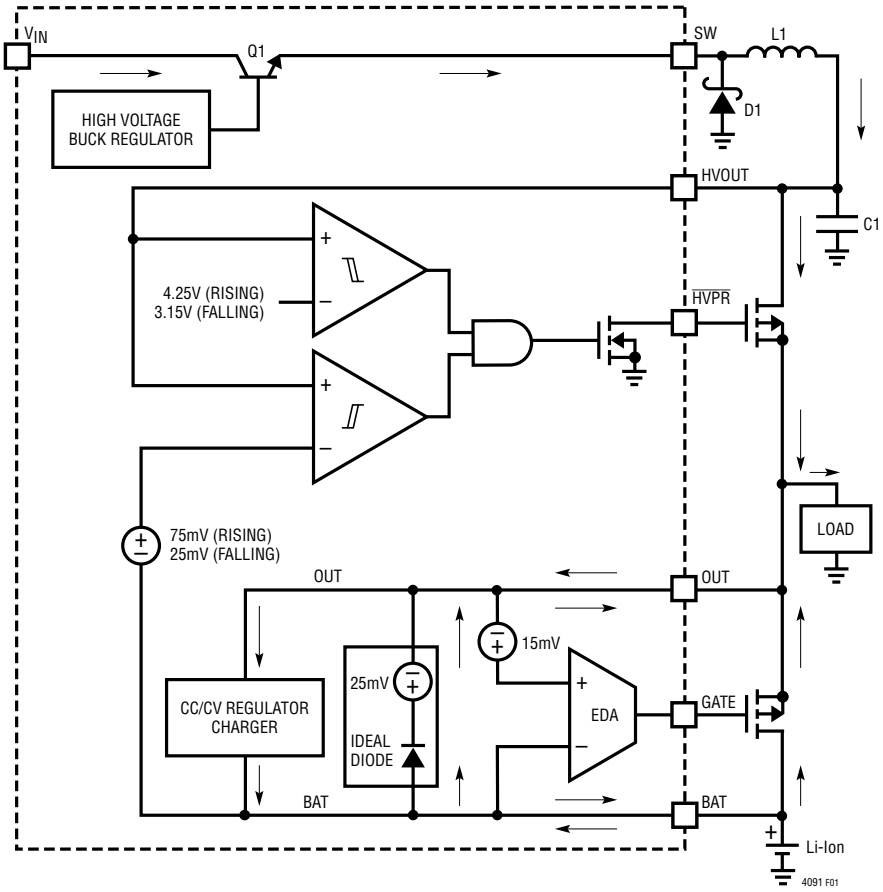


Figure 1. Simplified Block Diagram

OPERATION

charged until external power is removed. Once external power is removed the output drops until the ideal diode is forward biased. The forward biased ideal diode will then provide the output power to the load from the battery.

High Voltage Step-Down Regulator

The power delivered from V_{IN} to HVOUT is controlled by a constant frequency, current mode step down regulator. An external P-channel MOSFET directs this power to OUT and prevents reverse conduction from OUT to HVOUT (and ultimately V_{IN}).

An oscillator, with frequency set by R_T, enables an RS flip-flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C. An error amplifier servos the V_C node to maintain approximately 100mV between HVOUT and BAT. By keeping the voltage across the battery charger low, efficiency is optimized because power lost to the battery charger is minimized and power available to the external load is maximized. If the BAT pin voltage is less than approximately 3.5V, then the error amplifier will servo the V_C node to provide a constant HVOUT output voltage of about 3.6V. An active clamp on the V_C node provides current limit. The V_C node is also clamped to the voltage on the RUN/SS pin: Soft-start is implemented by generating a voltage ramp at the RUN/SS pin using an external resistor and capacitor.

The switch driver operates from either the high voltage input or from the BOOST pin. An external capacitor and internal diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

To further optimize efficiency, the buck regulator automatically switches to Burst Mode® operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current.

The oscillator reduces the switching regulator's operating frequency when the voltage at the HVOUT pin is low (below 3.95V). This frequency foldback helps to control the output current during startup and overload.

The switching regulator contains a V_{IN} good comparator which trips when the switching regulator is enabled via RUN/SS and the input voltage is sufficient to bias internal circuitry. The $\overline{VINGD}$ output is an open-collector transistor that is off when no input is present, allowing an external resistor to pull the $\overline{VINGD}$ pin high.

Ideal Diode from BAT to OUT

The LTC4091 has an internal ideal diode as well as a controller for an optional external ideal diode. If a battery is the only power supply available then the battery will automatically deliver power to the load via an ideal diode circuit between the BAT and OUT pins. The ideal diode circuit (along with the recommended 68µF capacitor on the OUT pin) allows the LTC4091 to handle large transient loads and wall adapter connect/disconnect events without the need for large bulk capacitors. The ideal diode responds within a few microseconds and prevents the OUT pin voltage from dropping significantly below the BAT pin voltage. A comparison of the I-V curve of the ideal diode and a Schottky diode can be seen in Figure 2.

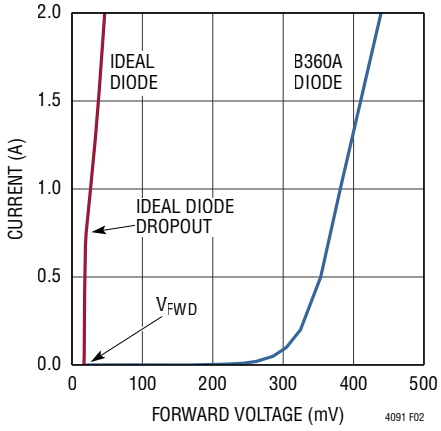


Figure 2. LTC4091 vs Schottky Diode Forward Voltage Drop

OPERATION

If power to V_{IN} (primary input) is removed, then all of the application power will be provided by the battery via the ideal diode. A 68µF capacitor at OUT is sufficient to keep a transition from input power to battery power from causing significant output voltage droop. The ideal diode consists of a precision amplifier that enables a large P-channel MOSFET transistor whenever the voltage at OUT is approximately 25mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 75mΩ.

If this is sufficient for the application then no external components are necessary. However if more conductance is needed, an external P-channel MOSFET can be added from BAT to OUT. The GATE pin of the LTC4091 drives the gate of the PFET for automatic ideal diode control. The source of the external MOSFET should be connected to OUT and the drain should be connected to BAT. In order to help protect the external MOSFET in overcurrent situations, it should be placed in close thermal contact to the LTC4091. It is important to maintain high impedance on this pin and minimize all leakage paths.

Battery Charger

The battery charger circuits of the LTC4091 are designed for charging single cell lithium-ion batteries. Featuring an internal P-channel power MOSFET, the charger uses a constant-current/constant-voltage charge algorithm with programmable current and a programmable timer for charge termination. Charge current can be programmed up to 1.5A. No blocking diode or sense resistor is required. The $\overline{CHRG}$ open-drain status output provides information regarding the charging status of the LTC4091 at all times. An NTC input provides the option of charge qualification using battery temperature.

The charge cycle begins when the voltage at the OUT pin rises above the battery voltage and the battery voltage is below the recharge threshold. No charge current actually flows until the OUT voltage is 100mV above the BAT voltage. At the beginning of the charge cycle, if the battery voltage is below 2.9V, the charger goes into trickle charge mode to bring the cell voltage up to a safe level for charging. The charger goes into the fast charge constant-current mode once the voltage on the BAT pin rises above 2.9V. In constant current mode, the charge current is set by R_{PROG}. When the battery approaches the final charge voltage, the charge current begins to decrease as the LTC4091 switches to constant-voltage mode. When the charge current drops below 10% of the programmed value while in constant-voltage mode the $\overline{CHRG}$ pin assumes a high impedance state.

A 4.2V charge voltage is selected by leaving V4P1 high impedance. It is important to minimize all leakage paths around this pin if it is left open. A 4.1V charge voltage is selected by connecting V4P1 to BAT.

An external capacitor on the TIMER pin sets the total minimum charge time. When this time elapses the charge cycle terminates and the $\overline{CHRG}$ pin assumes a high impedance state, if it has not already done so. While charging in constant current mode, if the charge current is decreased by thermal regulation the charge time is automatically increased. In other words, the charge time is extended inversely proportional to the actual charge current delivered to the battery. For Li-Ion and similar batteries that require accurate final charge potential, the internal bandgap reference, voltage amplifier and the resistor divider provide regulation with accuracy typically better than ±0.5%.

Trickle Charge and Defective Battery Detection

At the beginning of a charge cycle, if the battery voltage is low (below 2.9V) the charger goes into trickle charge reducing the charge current to 10% of the full-scale current. If the low battery voltage persists for one quarter of the total charge time, the battery is assumed to be defective, the charge cycle is terminated and the $\overline{CHRG}$ pin output assumes a high impedance state. If for any reason the battery voltage rises above ~2.9V the charge cycle will be restarted. To restart the charge cycle (i.e., when the dead battery is replaced with a discharged battery), simply remove the input voltage and reapply it or cycle the TIMER pin to 0V. Connecting the TIMER pin to ground disables the battery charger.

OPERATION

Programming Charge Current

The formula for the battery charge current is:

$$I_{CHG} = I_{PROG} \bullet 52,500 = \frac{V_{PROG}}{R_{PROG}} \bullet 52,500$$

where V_{PROG} is the PROG pin voltage and R_{PROG} is the total resistance from the PROG pin to ground.

For example, if typical 500mA charge current is required, calculate:

$$R_{PROG} = \frac{1V}{500mA} \bullet 52,500 = 105k$$

For best stability over temperature and time, 1% metal film resistors are recommended. Under trickle charge conditions, this current is reduced to 10% of the full-scale value.

The Charge Timer

The programmable charge timer is used to terminate the charge cycle. The timer duration is programmed by an external capacitor at the TIMER pin. The charge time is typically:

$$t_{TIMER}(hours) = C_{TIMER}\ (F) \bullet R_{PROG}\ (\Omega) \bullet 300$$

The timer starts when an input voltage is applied or when leaving shutdown and the voltage on the battery is less than the recharge threshold. At power-up or exiting shutdown with the battery voltage less than the recharge threshold the charge time is a full cycle. If the battery is greater than the recharge threshold the timer will not start and charging is prevented. If after power-up the battery voltage drops below the recharge threshold, or if after a charge cycle the battery voltage is still below the recharge threshold, the charge time is set to one-half of a full cycle.

The LTC4091 has a feature that extends charge time automatically. Charge time is extended if the charge current in constant current mode is reduced due to thermal regulation. This change in charge time is inversely proportional to the change in charge current. As the LTC4091 approaches constant voltage mode the charge current begins to drop. This change in charge current is due to normal charging operation and does not affect the timer duration.

Once a time-out occurs and the voltage on the battery is greater than the recharge threshold, the charge current stops, and the $\overline{CHRG}$ output assumes a high impedance state if it has not already done so.

Connecting the TIMER pin to ground disables the battery charger.

$\overline{CHRG}$ Status Output Pin

When the charge cycle starts, the $\overline{CHRG}$ pin is pulled to ground by an internal N-channel MOSFET capable of driving an LED. When the charge current drops below 10% of the programmed full charge current while in constant voltage mode, the pin assumes a high impedance state, but charge current continues to flow until the charge time elapses. If this state is not reached before the end of the programmable charge time, the pin will assume a high impedance state when a time-out occurs. The $\overline{CHRG}$ current detection threshold can be calculated by the following equation:

$$I_{DETECT} = \frac{0.1V}{R_{PROG}} \bullet 52,500 = \frac{5250V}{R_{PROG}}$$

For example, if the full charge current is programmed to 500mA with a 105k PROG resistor the $\overline{CHRG}$ pin will change state at a battery charge current of 50mA.

Note: The end-of-charge (EOC) comparator that monitors the charge current latches its decision. Therefore, the first time the charge current drops below 10% of the programmed full charge current while in constant voltage mode, it will toggle $\overline{CHRG}$ to a high impedance state. If, for some reason the charge current rises back above the threshold, the $\overline{CHRG}$ pin will not resume the strong pull-down state. The EOC latch can be reset by a recharge cycle (i.e., V_{BAT} drops below the recharge threshold).

OPERATION

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.1V or 4V depending on V4P1). To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than a few milliseconds. The charge cycle and safety timer will also restart if the V_{IN} UVLO cycles low and then high (e.g. V_{IN}, is removed and then replaced).

Thermal Regulation

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 105°C. Thermal regulation protects the LTC4091 from excessive temperature due to high power operation or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC4091 or external components. The benefit of the LTC4091 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

Undervoltage Lockout

An internal undervoltage lockout circuit monitors the output voltage (OUT) and can disable the battery charger circuits. The battery charger circuits are disabled until V_{OUT} exceeds V_{BAT} by 80mV. The undervoltage lockout comparator has built-in hysteresis.

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. To use this feature connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, RNOM, from VNTC to NTC. RNOM should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (denoted R_{25C}).

The LTC4091 will pause charging when the resistance of the NTC thermistor drops to 0.41 times the value of R_{25C} or approximately 4.1k (for a Vishay Curve 2 thermistor, this corresponds to approximately 50°C). The safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4091 is also designed to pause charging (and timer) when the value of the NTC thermistor increases to 2.82 times the value of R_{25C}. For a Vishay Curve 2 thermistor this resistance, 28.2k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

APPLICATIONS INFORMATION

Choosing a Charge Voltage for the Battery:

The LTC4091 offers two different charge voltage options: 4.1V and 4.2V. Choosing a higher charge voltage increases the battery capacity to provide a longer product run-time but reduces the battery lifetime, usually measured by the number of charge/discharge cycles. Battery manufacturers usually consider the end of life for a battery to be when the battery capacity drops to 80% of the rated capacity. The curves in Figure 3 show the relationship between cell capacity and cycle life for a typical Li-Ion battery cell. Using 4.2V as the charge voltage, a typical Li-Ion battery is considered at 100% initial capacity but delivers about 500 charge/discharge cycles before the capacity drops to 80%. However, if the same battery uses 4.1V as the charge voltage, it is at 85% initial capacity but the number of charge/discharge cycles can be almost doubled to 1000 before the capacity drops to 80%. Lowering the charge voltage even further to 4V can increase the battery lifetime more than three times to 1800 charge/discharge cycles. Since LTC4091 is a backup product, the battery is likely to spend the majority of its lifetime fully charged. This makes it even more critical to charge at a lower charge voltage to maximize battery lifetime since battery capacity degrades even faster when batteries remain fully charged. Because of the different Li-Ion battery chemistries and other conditions that can affect battery lifetime, the curves shown here are only estimates of the number of charge cycles and battery-capacity levels.

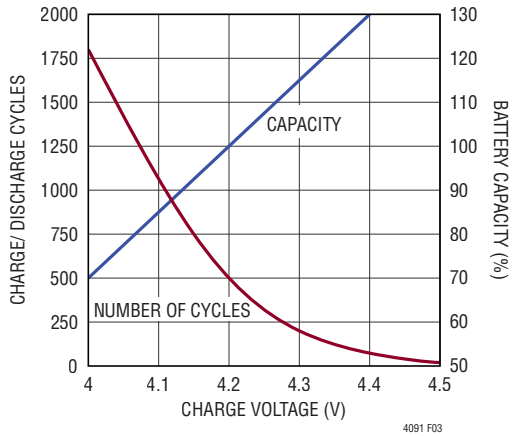


Figure 3. Battery Cycle Life and Capacity as a Function of Charge Voltage

Setting the Switching Frequency

The switching regulator uses a constant-frequency PWM architecture that can be programmed to switch from 200kHz to 2.4MHz by using a resistor tied from the RT pin to ground. The oscillator frequency as a function of R_T follows the expression below:

$$F_{SW}\ (MHz) = \frac{38}{R_T\ (k\Omega) + 7.5}$$

Operating Frequency Trade-Offs

Selection of the operating frequency for the high voltage buck regulator is a trade-off between efficiency, component size, minimum dropout voltage, and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, lower maximum input voltage, and higher dropout voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_D + V_{HVOUT}}{t_{ON(MIN)} \bullet \left(V_D + V_{IN} - V_{SW}\right)}$$

where V_{IN} is the typical high voltage input voltage, V_{HVOUT} is the output voltage of the switching regulator, V_D is the catch diode drop (~0.5V), and V_{SW} is the internal switch drop (~0.5V at max load). This equation shows that slower switching frequency is necessary to safely accommodate high V_{IN}/V_{HVOUT} ratio. Also, as shown in the next section, lower frequency allows a lower dropout voltage. The reason input voltage range depends on the switching frequency is because the high voltage switch has non-zero minimum on and off times. The switch can turn on for a minimum of ~100ns and turn off for a minimum of ~150ns. This means that the minimum and maximum duty cycles are:

$$DC_{MIN} = f_{SW} \bullet t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_{SW} \bullet t_{OFF(MIN)}$$

APPLICATIONS INFORMATION

where f_{SW} is the switching frequency, $t_{ON(MIN)}$ is the minimum switch-on time (~100ns), and $t_{OFF(MIN)}$ is the minimum switch-off time (~150ns). These equations show that duty cycle range increases when switching frequency is decreased.

A good choice of switching frequency should allow adequate input voltage range (see next section) and keep the inductor and capacitor values small.

V_{IN} Input Voltage Range

The maximum input voltage range for LTC4091 applications depends on the switching frequency, the Absolute Maximum Ratings of the V_{IN} and BOOST pins, and the operating mode.

The high voltage switching regulator can operate from input voltages up to 36V, and safely withstand input voltages up to 60V. Note that while V_{IN} > 38V (typical), the LTC4091 will stop switching, allowing the output to fall out of regulation.

While the high voltage regulator output is in start-up, short-circuit, or other overload conditions, the switching frequency should be chosen according to the following discussion.

For safe operation at inputs up to 60V the switching frequency must be low enough to satisfy $V_{IN(MAX)} \geq 40V$ according to the following equation. If lower $V_{IN(MAX)}$ is desired, this equation can be used directly.

$$V_{IN(MAX)} = \frac{V_{HVOUT} + V_D}{f_{SW} \bullet t_{ON(MIN)}} - V_D + V_{SW}$$

where $V_{IN(MAX)}$ is the maximum operating input voltage, V_{HVOUT} is the high voltage regulator output voltage, V_D is the catch diode drop (~0.5V), V_{SW} is the internal switch drop (~0.5V at max load), f_{SW} is the switching frequency (set by R_T), and $t_{ON(MIN)}$ is the minimum switch-on time (~150ns). Note that a higher switching frequency will depress the maximum operating input voltage. Conversely, a lower switching frequency will be necessary to achieve safe operation at high input voltages.

If the output is in regulation and no short-circuit, start-up, or overload events are expected, then input voltage transients of up to 60V are acceptable regardless of the switching frequency. In this mode, the LTC4091 may enter pulse-skipping operation where some switching pulses are skipped to maintain output regulation. In this mode the output voltage ripple and inductor current ripple will be higher than in normal operation.

The minimum input voltage is determined by either the high voltage regulator's minimum operating voltage of ~6V or by its maximum duty cycle (see equation in previous section). The minimum input voltage due to duty cycle is:

$$V_{IN(MIN)} = \frac{V_{HVOUT} + V_D}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_D + V_{SW}$$

where $V_{IN(MIN)}$ is the minimum input voltage, and $t_{OFF(MIN)}$ is the minimum switch-off time (~150ns). Note that higher switching frequency will increase the minimum input voltage. If a lower dropout voltage is desired, a lower switching frequency should be used.

Inductor Selection and Maximum Output Current

A good choice for the inductor value is L = 6.8µH (assuming an 800kHz operating frequency). With this value the maximum load current will be ~2.4A. For details of maximum output current, see Linear Technology Application Note 44. The RMS current rating of the inductor must be greater than the maximum load current and its saturation current should be about 30% higher. Note that the maximum load current will be programmed charge current plus the largest expected application load current. For robust operation in fault conditions, the saturation current should be ~3.5A. To keep efficiency high, the series resistance (DCR) should be less than 0.1Ω. Table 1 lists several vendors and types that are suitable.

APPLICATIONS INFORMATION

Table 1. Inductor Vendors

VENDOR	URL	PART SERIES	TYPE
Murata	www.murata.com	LQH55D	Open
TDK	www.componenttdk.com	SLF7045 SLF10145	Shielded Shielded
Toko	www.toko.com	D62CB D63CB D75C D75F	Shielded Shielded Shielded Open
Sumida	www.sumida.com	CR54 CDRH74 CDRH6D38 CR75	Open Shielded Shielded Open

Catch Diode

The catch diode conducts current only during switch-off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{HVOUT} \bullet \frac{(V_{IN} - V_{HVOUT})}{V_{IN}}$$

where I_{HVOUT} is the output load current. The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the worst-case condition of shorted output. The diode current will then increase to the typical peak switch current. Peak reverse voltage is equal to the regulator input voltage. Use a Schottky diode with a reverse voltage rating greater than the input voltage. The overvoltage protection feature in the high voltage regulator will keep the switch off when V_{IN} > 40V which allows the use of a 40V rated Schottky even when V_{VIN} ranges up to 60V. Table 2 lists several Schottky diodes and their manufacturers.

Table 2. Diode Vendors

PART NUMBER	V_R (V)	I_{AVE} (A)	V_F AT 1A (MV)	V_F AT 2A (MV)
On Semiconductor				
MBRM120E	20	1	530	595
MBRM140	40	1	550	
Diodes Inc.				
B120	20	1	500	
B130	30	1	500	
B220	20	2		500
B230	30	2		500
DFLS240L	40	2		500
International Rectifier				
10BQ030	30	1	420	470
20BQ030	30	2		470

Switching Regulator Capacitor Selection

Ceramic capacitors are small, robust and have very low ESR providing the best ripple performance. However, ceramic capacitors can cause problems when used with the high voltage switching regulator due to their piezoelectric nature. When in Burst Mode operation, the LTC4091's switching frequency depends on the load current, and at very light loads the LTC4091 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LTC4091 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

Only a small amount of capacitance is required on HVOUT – about 3.3µF. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value capacitor if the compensation network is also adjusted to maintain the loop bandwidth. A lower value of output capacitor can be used to save space and cost but transient performance will suffer. See the Switching Regulator Frequency Compensation section to choose an appropriate compensation network.

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor, or one with a higher voltage rating, may be required. Low ESR is important, so choose one that is intended for use in switching regulators. The ESR should be specified by the supplier, and should be 0.05Ω or less.

APPLICATIONS INFORMATION

Switching Regulator Frequency Compensation

The LTC4091 high voltage regulator uses current mode control to regulate the output. This simplifies loop compensation. In particular, the high voltage regulator does not require the ESR of the output capacitor for stability, so you are free to use ceramic capacitors to achieve low output ripple and small circuit size. Frequency compensation is provided by the components tied to the V_C pin as shown in the Block Diagram. Generally a capacitor (C_C) and a resistor (R_C) in series to ground are used. In addition, there may be a lower value capacitor in parallel. This capacitor (C_F) is not part of the loop compensation but is used to filter noise at the switching frequency, and is required only if a phase-lead capacitor is used or if the output capacitor has high ESR.

Loop compensation determines the stability and transient performance. Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with the back page schematic and tune the compensation network to optimize performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load. Figure 4 shows the transient response when the load current is stepped from 500mA to 1500mA and back to 500mA.

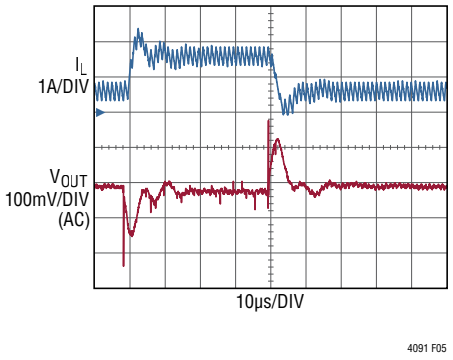


Figure 4. Transient Load Response of the LTC4091 High Voltage Regulator Back Page Application as the Load Current is Stepped from 500mA to 1500mA. V_{HVOUT} = 3.6V

Low Ripple Burst Mode Operation and Pulse-Skipping Mode

The LTC4091 is capable of operating in either low ripple Burst Mode operation or pulse-skipping mode selected by the SYNC pin. Tie the SYNC pin below $V_{SYNC,L}$ (0.3V) for low ripple Burst Mode operation or above $V_{SYNC,H}$ (1V) for pulse-skipping mode.

To enhance efficiency at light loads, the LTC4091 can be operated in low ripple Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTC4091 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. Because the LTC4091 delivers power to the output with single, low current pulses, the output ripple is kept below 15mV for a typical application. As the load current decreases towards a no load condition, the percentage of time that the high voltage regulator operates in sleep mode increases and the average input current is greatly reduced resulting in high efficiency even at very low loads. See Figure 5.

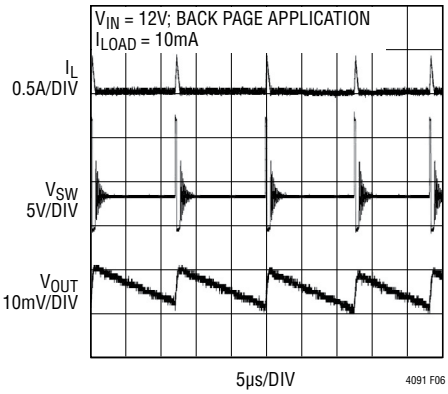


Figure 5. High Voltage Regulator Burst Mode Operation

APPLICATIONS INFORMATION

High Voltage Regulator Burst Mode Operation

At higher output loads (above 90mA for the back page application) the LTC4091 will be running at the frequency programmed by the R_T resistor, and will be operating in standard PWM mode. The transition between PWM and low ripple Burst Mode operation is seamless, and will not disturb the output voltage.

Boost Pin Considerations

Capacitor C2 (see Block Diagram) and an internal diode are used to generate a boost voltage that is higher than the input voltage. In most case, a 0.47µF capacitor will work well. The BOOST pin must be at least 2.3V above the SW pin for proper operation.

High Voltage Regulator Soft-Start

The RUN/SS pin can be used to soft-start the high voltage regulator of the LTC4091, reducing maximum input current during start-up. The RUN/SS pin is driven through an external R_C filter to create a voltage ramp at this pin. Figure 6 shows the start-up and shut-down waveforms with the soft-start circuit. By choosing a large RC time constant the peak start-up current can be reduced to the current that is required to regulate the output with no overshoot. Choose the value of the resistor so that it can supply 20µA when the RUN/SS pin reaches 2.3V.

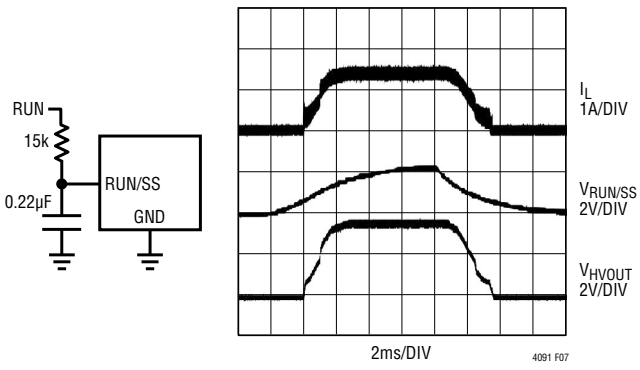


Figure 6. To Soft-Start the High Voltage Regulator, Add a Resistor and Capacitor to the RUN/SS Pin

Automotive Cold-Crank Ride Through

In automotive applications that are expected to experience large dips in supply voltage, such as during a cold-crank event, the high voltage switching regulator can lose regulation resulting in excessive V_C voltage and consequently excessive output overshoot when V_{IN} recovers. To prevent overshoot when recovering from a cold-crank event it is necessary to reset the LTC4091's soft-start circuit via the RUN/SS pin. Figure 7 shows an example of a simple circuit that automatically detects a brown-out condition and resets the RUN/SS pin, re-engaging the soft-start feature and preventing damaging output overshoot.

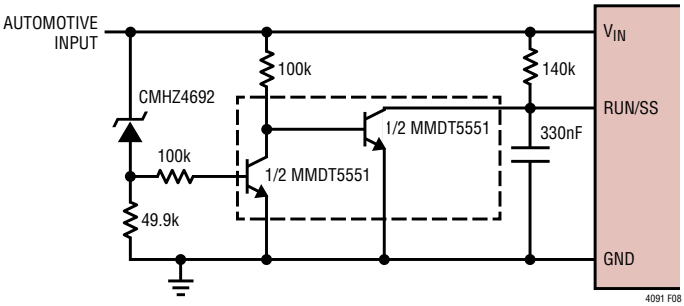


Figure 7. Cold-Crank Ride Through Circuit

Synchronization and Mode

The SYNC pin allows the high voltage regulator to be synchronized to an external clock.

Synchronizing the LTC4091 internal oscillator to an external frequency can be done by connecting a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should be such that the valleys are below 0.3V and the peaks are above 1V (up to 6V). The high voltage regulator may be synchronized over a 300kHz to 2MHz range. The R_T resistor should be chosen such that the LTC4091 oscillates 25% slower than the external synchronization frequency to ensure adequate slope compensation. While synchronized, the high voltage regulator will turn on the power switch on positive going edges of the clock.

APPLICATIONS INFORMATION

When using the SYNC function, there is the potential for inductor current runaway during short-circuit or overload conditions, if the following condition is violated:

$$f_{SW(MAX)} = \frac{V_D + V_{OUT}}{t_{ON(MIN)}\left(V_D + V_{IN} - V_{SW}\right)}$$

where $V_{IN(MAX)}$ is the maximum operating input voltage, V_{HVOUT} is the switching regulator output voltage, V_D is the catch diode drop (~0.5V), V_{SW} is the internal switch drop (~0.5V at max load), f_{SW} is the synchronized switching frequency, and $t_{ON(MIN)}$ is the minimum switch on time (~100ns). Obviously, with a shorted output, it is not difficult to violate this condition.

Alternate NTC Thermistors and Biasing

The LTC4091 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC (see Figure 8). By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R_{25C}) the upper and lower temperatures are pre-programmed to approximately 50°C and 0°C, respectively (assuming a Vishay Curve 2 thermistor).

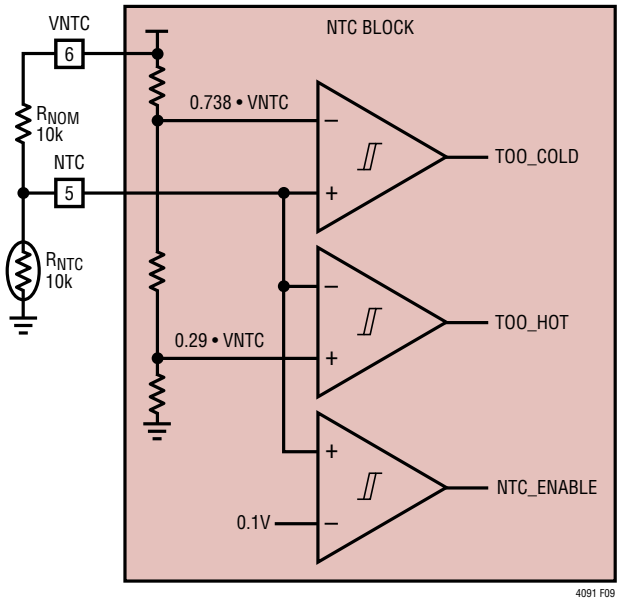


Figure 8. Typical NTC Thermistor Circuit

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N02N1002J, used in the following examples, has a nominal value of 10k and follows the Vishay Curve 2 resistance-temperature characteristic. The LTC4091 trip points were designed to work with thermistors whose resistance-temperature characteristics follow Vishay Dale's R-T Curve 2. The Vishay NTHS0603N02N1002J is an example of such a thermistor. However, Vishay Dale has many thermistor products that follow the R-T Curve 2 characteristic in a variety of sizes. Furthermore, any thermistor whose ratio of R_{COLD} to R_{HOT} is about 7.0 will also work (Vishay Dale R-T Curve 2 shows a ratio of 2.815 / 0.409 = 6.89).

In the explanation below, the following notation is used.

R_{25C} = Value of the Thermistor at 25°C

$R_{NTC|COLD}$ = Value of Thermistor at the Cold Trip Point

$R_{NTC|HOT}$ = Value of the Thermistor at the Hot Trip Point

r_{cold} = Ratio of $R_{NTC|COLD}$ to R_{25C}

r_{HOT}= Ratio of $R_{NTC|HOT}$ to R_{25C}

RNOM = Primary Thermistor Bias Resistor (see Figure 9)

R1 = Optional Temperature Range Adjustment Resistor (see Figure 9)

APPLICATIONS INFORMATION

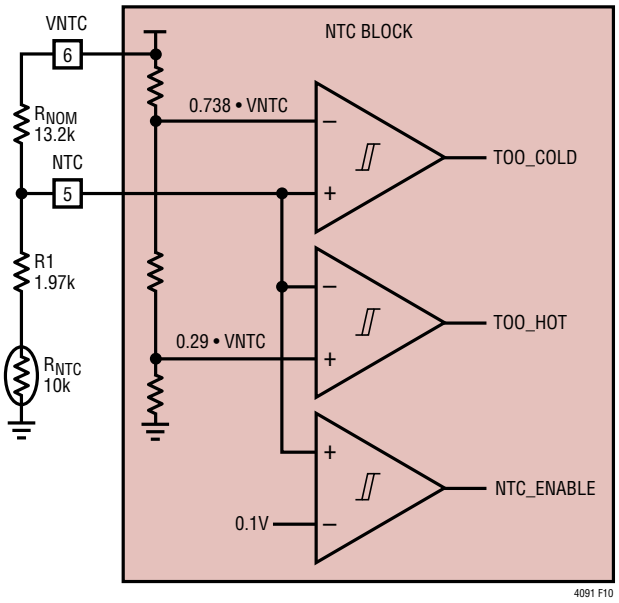


Figure 9. NTC Thermistor Circuit with Additional Dilution Resistor

The trip points for the LTC4091's temperature qualification are internally programmed at 0.29 • VNTC for the hot threshold and 0.74 • VNTC for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{RNOM + R_{NTC|HOT}} \bullet VNTC = 0.29 \bullet VNTC$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{RNOM + R_{NTC|COLD}} \bullet VNTC = 0.74 \bullet VNTC$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$$R_{NTC|HOT} = 0.409 \bullet RNOM$$

and

$$R_{NTC|COLD} = 2.815 \bullet RNOM$$

By setting RNOM equal to R_{25C}, the above equations result in $r_{HOT} = 0.409$ and $r_{COLD} = 2.815$. Referencing these ratios to the Vishay Resistance-Temperature Curve 2 chart gives a hot trip point of about 50°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 50°C.

By using a bias resistor, RNOM, different in value from R_{25C}, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the nonlinear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$RNOM = \frac{r_{HOT}}{0.409} \bullet R_{25C}$$

$$RNOM = \frac{r_{COLD}}{2.815} \bullet R_{25C}$$

where r_{HOT} and r_{COLD} are the resistance ratios at the desired hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 40°C hot trip point is desired.

From the Vishay Curve 2 R-T characteristics, r_{HOT} is 0.5758 at 40°C. Using the above equation, RNOM should be set to 14k. With this value of RNOM, the cold trip point is about –7°C. Notice that the span is now 47°C rather than the previous 50°C. This is due to the increase in temperature gain of the thermistor as absolute temperature decreases.

The upper and lower temperature trip points can be independently programmed by using an additional dilution resistor as shown in Figure 9. The following formulas can be used to compute the values of RNOM and R1:

$$RNOM = \frac{r_{COLD} - r_{HOT}}{2.815} \bullet R_{25C}$$

$$R1 = 0.409 \bullet RNOM - r_{HOT} \bullet R_{25C}$$

For example, to set the trip points to –5°C and 55°C with a Vishay Curve 2 thermistor choose

$$RNOM = \frac{3.532 - 0.3467}{2.815 - 0.409} \bullet 10k = 13.2k$$

APPLICATIONS INFORMATION

the nearest 1% value is 13.3k.

$$R1 = 0.409 \bullet 13.3k - 0.3467 \bullet 10k = 1.97k$$

the nearest 1% value is 1.96k. The final solution is shown in Figure 10 and results in an upper trip point of 55°C and a lower trip point of –5°C.

Power Dissipation and High Temperature Considerations

The die temperature of the LTC4091 must be lower than the maximum rating of 125°C. This is generally not a concern unless the ambient temperature is above 85°C. The total power dissipated inside the LTC4091 depends on many factors, including input voltage, battery voltage, programmed charge current and load current.

When powered from the primary source, the power dissipation can be estimated by calculating the regulator power loss from an efficiency measurement, and subtracting the catch diode loss.

$$P_D = (1-\eta)\bullet\left(V_{HVOUT}\bullet\left(I_{BAT}+I_{OUT}\right)\right)$$
$$-V_D\bullet\left(1-\frac{V_{HVOUT}}{V_{VIN}}\right)\bullet\left(I_{BAT}+I_{OUT}\right)+0.1V\bullet I_{BAT}$$

where η is the efficiency of the high voltage regulator and V_D is the forward voltage of the catch diode at $I = I_{BAT} + I_{OUT}$. The first term corresponds to the power lost in converting V_{VIN} to V_{HVOUT}, the second term subtracts the catch diode loss, and the third term is the power dissipated in the battery charger. For a typical application, an example of this calculation would be:

$$P_D = (1-0.87)\bullet\left(3.8V\bullet\left(1A+0.6A\right)\right)$$
$$-0.4V\bullet\left(1-\frac{4V}{12V}\right)\bullet\left(1A+0.6A\right)+0.1V\bullet 1A = 0.46W$$

This example assumes 87% efficiency, V_{IN} = 12V, V_{BAT} = 3.7V (V_{HVOUT} is about 3.8V), I_{BAT} = 1A, I_{OUT} = 600mA resulting in just under 0.5W total dissipation.

It is important to solder the exposed backside of the package to a ground plane. This ground should be tied to other copper layers below with thermal vias; these layers will spread the heat dissipated by the LTC4091. Additional vias should be placed near the catch diode. Adding more copper to the top and bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. With these steps, the thermal resistance from die (i.e., junction) to ambient can be reduced to θ_{JA} = 40°C/W.

Board Layout Considerations

As discussed in the previous section, it is critical that the exposed metal pad on the backside of the LTC4091 package be soldered to the PC board ground. Furthermore, proper operation and minimum EMI requires a careful printed circuit board (PCB) layout. Note that large, switched currents flow in the power switch (between the V_{IN} and SW pins), the catch diode and the V_{IN} input capacitor. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The loop formed by these components should be as small as possible.

Additionally, the SW and BOOST nodes should be kept as small as possible. Linear Technology demonstration board DC2558A shows an example of a preferred printed circuit board layout. Gerber files can be downloaded at: http://www.linear.com/product/LTC4091#demoboards.

High frequency currents, such as the high voltage input current of the LTC4091, tend to find their way along the ground plane on a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. See Figure 10.

APPLICATIONS INFORMATION

V_{IN} Bypass Capacitor

Many types of capacitors can be used for input bypassing; while recommended, caution must be exercised when using multilayer ceramic capacitors. Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as from connecting the charger input to a hot power source. For more information, refer to Application Note 88.

Battery Charger Stability Considerations

The constant-voltage mode feedback loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, a 100µF capacitor with a 50mΩ series resistor to GND is recommended at the BAT pin to keep ripple voltage low when the battery is disconnected.

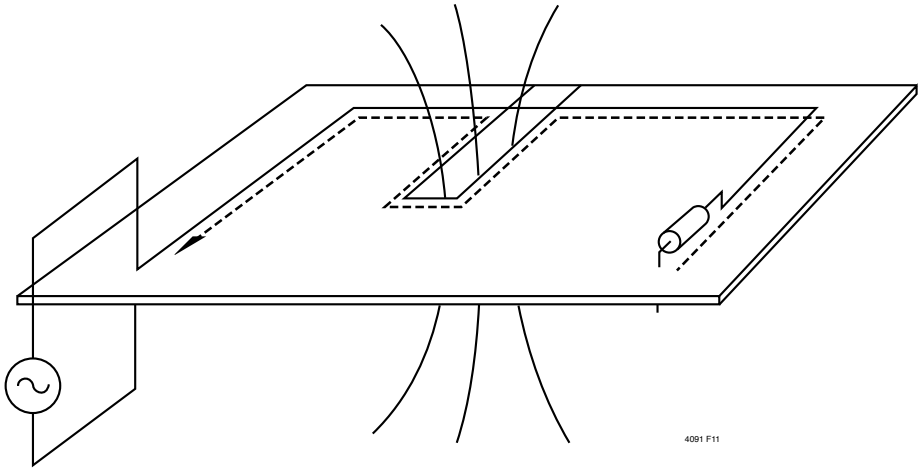
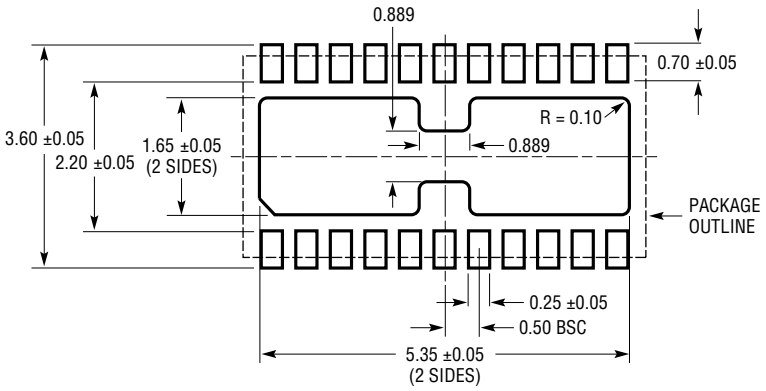


Figure 10. Ground Currents Follow Their Incident Path at High Speed. Slices in the Ground Plane Cause High Voltage and Increased Emissions.

PACKAGE DESCRIPTION

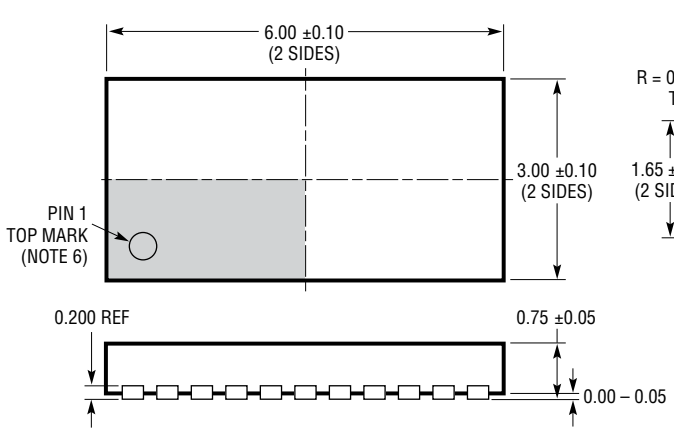
Please refer to http://www.linear.com/product/LTC4091#packaging for the most recent package drawings.

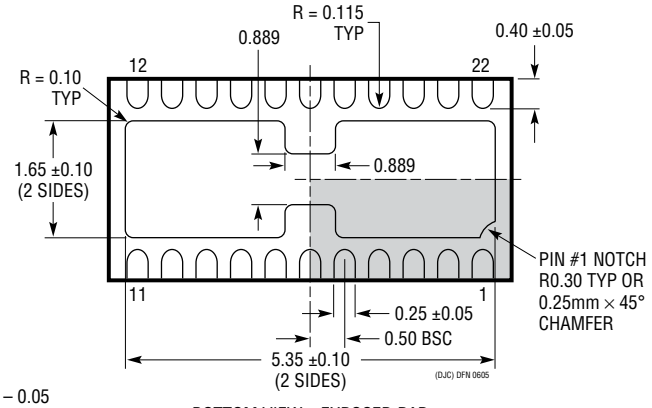
DJC Package
22-Lead Plastic DFN (6mm × 3mm)
(Reference LTC DWG # 05-08-1714 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. APPLY SOLDER MASK TO AREAS THAT
   ARE NOT SOLDERED
3. DRAWING IS NOT TO SCALE





BOTTOM VIEW—EXPOSED PAD

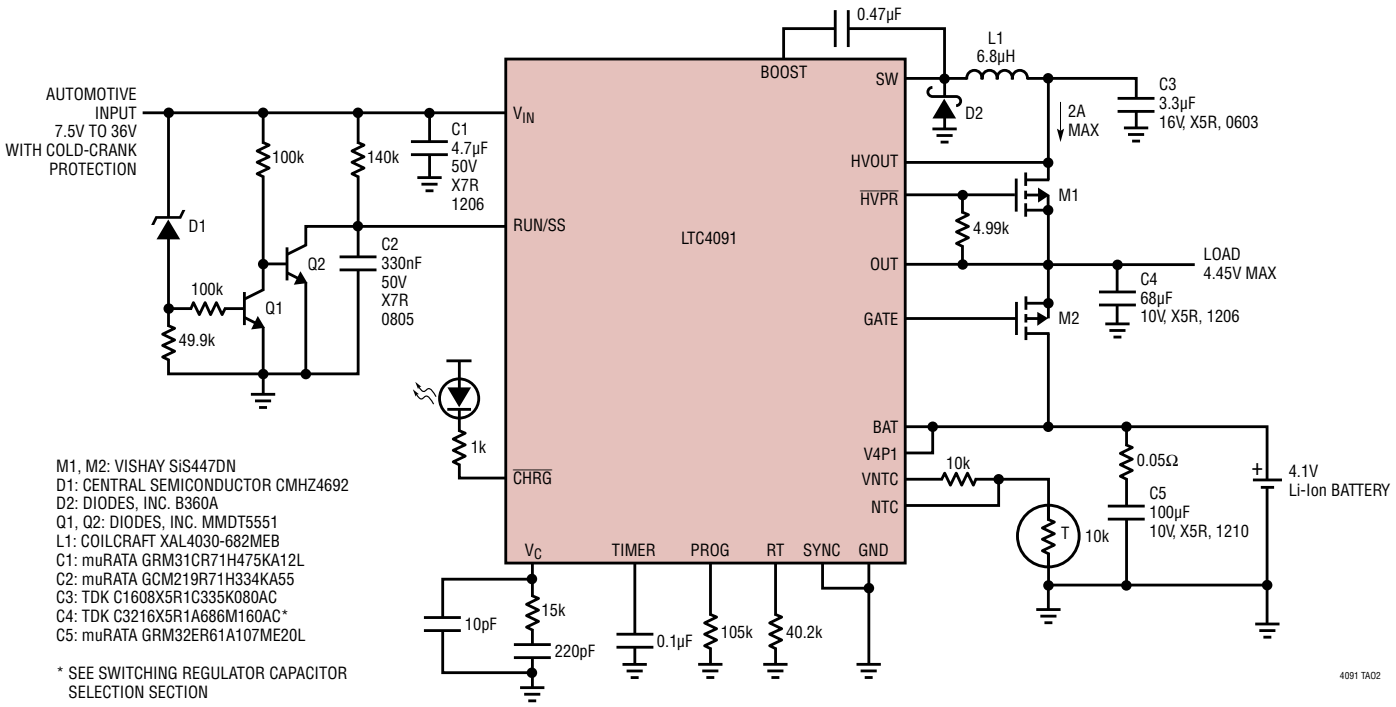
NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX)
   IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/16	Modified I_{VGLK} conditions	4
		Changed θ_{JA} from 40°C/W to 31.8°C/W	4
		Change Minimum On Time from 150ns to 100ns	15
		Change Minimum On Time from 150ns to 100ns	16
		Add approximate symbol "~", to 150ns minimum switch-off time	16
		Correct table numbering	16, 17
		Correct figure numbering	18-23
		Change Minimum On Time from 150ns to 100ns	20
		Correct $R_{NTC|HOT}$ to $R_{NTC|COLD}$	21

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3226	Boost Charge Pump + PowerPath Manager for SCaps	I_{CHARGE}: 0.33A, V_{IN}: 2.5V to 5.5V, V_{OUT}: 2.5V to 5.5V
LTC3355	Buck SCap Charger + Boost Backup	I_{CHARGE}: 1A, V_{IN}: 3V to 20V, V_{OUT}: 2.7V to 5.5V
LTC3110	Bi-Directional Buck-Boost + PowerPath Manager for SCaps	I_{CHARGE}: 2A, V_{IN}: 0.1V to 5.5V, V_{OUT}: 1.8V to 5.5V
LTC3643	Bi-Directional Boost Charger/Buck Backup, Electrolytic Caps	I_{CHARGE}: 2A, V_{IN}: 3V to 17V, V_{OUT}: Up to 40V
LTC4040	Buck Battery Charger + Boost Backup for Li Batteries	I_{CHARGE}: 2.5A, V_{IN}: 3.5V to 5.5V, V_{OUT}: 3.5V to 5V
LTC3128	Buck-Boost SCap Charger	I_{CHARGE}: 3A, V_{IN}: 1.7V to 5.5V, V_{OUT}: 1.8V to 5.5V
LTC4425	Linear/Ideal Diode SCap Charger	I_{CHARGE}: 3A, V_{IN}: 1.7V to 5.5V, V_{OUT}: 2.7V to 5.5V
LTC4110	Bi-Directional Buck-Boost Flyback Controller	I_{CHARGE}: 3A, V_{IN}: 4.5V to 19V, V_{OUT}: 2.7V to 19V
LTC3350	Bi-Directional Controller + Monitor + PowerPath for SCaps	I_{CHARGE}: 10A+, V_{IN}: 4.5V to 35V, V_{OUT}: 4V to 35V
LTC4089	USB Power Manager with High Voltage Switching Charger	Seamless Transition Between Power Sources: Li-Ion Battery, USB and 6V to 36V External Supply, High Efficiency, 1.2A Charger from 6V to 36V Input with Adaptive Output Control
LTC4090	USB Power Manager with 2A High Voltage Bat-Track™ Buck Charger	Seamless Transition Between Power Sources: Li-Ion Battery, USB and 6V to 38V Supply (60V Max), 2A Output High Voltage Back Regulator with Bat-Track Adaptive Output Control

LT 0817 REV A • PRINTED IN USA

© LINEAR TECHNOLOGY CORPORATION 2017

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC4091EDJC#TRPBF on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management