THE DATASHEET OF

LTC2939CMS#TRPBF

Configurable 4- and 6-Supply Monitors with Watchdog Timer

FEATURES

- **Simultaneously Monitors Four (LTC2938) or Six Supplies (LTC2939)**
- **Sixteen User-Selectable Combinations of 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V and/or ± Adjustable Voltage Thresholds**
- **Guaranteed Threshold Accuracy: ±1.5%**
- **Adjustable Reset and Watchdog Timeout**
- Low Supply Current: 80µA Typical
- Power Supply Glitch Immunity
- Guaranteed $\overline{RST}$ for V_{CC} > 1V
- High Temperature Operation to 125°C
- 12-Pin 4mm × 3mm DFN or 12-Lead MSOP (LTC2938) and 16-Lead MSOP Package (LTC2939)

APPLICATIONS

- Desktop and Notebook Computers
- Multivoltage Systems
- Telecom Equipment
- Network Servers
- Automotive Control Systems

DESCRIPTION

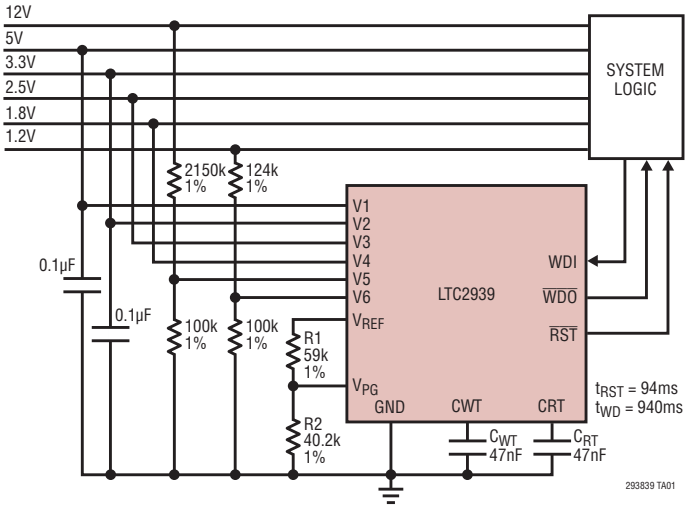
The LTC®2938/LTC2939 are configurable supply monitors for systems with up to four or six supply voltages that need watchdog supervision. One of sixteen preset or adjustable voltage monitor combinations can be selected using an external resistive divider connected to the program input. The preset voltage thresholds are accurate to ±1.5% over temperature. The LTC2938 and LTC2939 also feature adjustable inputs with a 0.5V nominal threshold.

The reset and watchdog timeout periods are adjustable using external capacitors. Tight voltage threshold accuracy and glitch immunity ensure reliable reset operation without false triggering. The $\overline{RST}$ output is guaranteed to be in the correct state for V_{CC} down to 1V. Each status output has a weak internal pull-up and may be externally pulled up to a user-defined voltage.

The 80µA supply current makes the LTC2938 and LTC2939 ideal for power conscious systems. The LTC2939 monitors up to six supplies and the LTC2938 monitors up to four supplies.

TYPICAL APPLICATION

6-Supply Monitor 12V (ADJ), 5V, 3.3V, 2.5V, 1.8V, 1.2V (ADJ)



Voltage Configuration Table

V1 (V)	V2 (V)	V3 (V)	V4 (V)	V5 (V)	V6 (V)
5	3.3	2.5	1.8	ADJ	ADJ
5	3.3	2.5	ADJ	ADJ	ADJ
5	3.3	1.8	ADJ	ADJ	ADJ
5	3.3	ADJ	ADJ	ADJ	ADJ
5	3.3	ADJ	–ADJ	ADJ	ADJ
3.3	2.5	1.8	1.5	ADJ	ADJ
3.3	2.5	1.8	ADJ	ADJ	ADJ
3.3	1.8	1.5	1.2	ADJ	ADJ
3.3	1.8	1.5	ADJ	ADJ	ADJ
3.3	1.8	1.2	ADJ	ADJ	ADJ
3.3	2.5	ADJ	ADJ	ADJ	ADJ
3.3	2.5	ADJ	–ADJ	ADJ	ADJ
3.3	1.8	ADJ	ADJ	ADJ	ADJ
3.3	1.8	ADJ	–ADJ	ADJ	ADJ
3.3	1.5	ADJ	ADJ	ADJ	ADJ
3.3	1.2	ADJ	ADJ	ADJ	ADJ

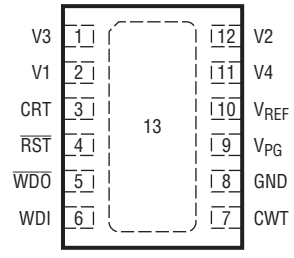
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

V1, V2, V3, V4, V5, V6, V_{PG} ..... –0.3V to 7V
$\overline{RST}$ ..... –0.3V to 7V
CWT, $\overline{WDO}$ ..... –0.3V to 7V
CRT, V_{REF}, WDI ..... –0.3V to (V_{CC} + 0.3V)
Reference Load Current (I_{VREF}) ..... ±1mA
V4 Input Current (–ADJ Mode) ..... –1mA
$\overline{RST}$, $\overline{WDO}$ Currents ..... ±10mA

Operating Temperature Range
LTC2939C ..... 0°C to 70°C
LTC2939I ..... –40°C to 85°C
LTC2939H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec)
MS Package Only ..... 300°C

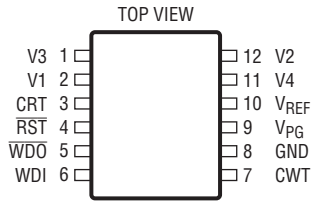
PIN CONFIGURATION

LTC2938



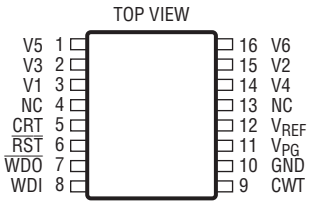
DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) PCB GND CONNECTION OPTIONAL

LTC2938



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 130°C/W

LTC2939



MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2938CDE#PBF	LTC2938CDE#TRPBF	2938	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2938IDE#PBF	LTC2938IDE#TRPBF	2938	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2938HDE#PBF	LTC2938HDE#TRPBF	2938	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC2938CMS#PBF	LTC2938CMS#TRPBF	2938	12-Lead Plastic MSOP	0°C to 70°C
LTC2938IMS#PBF	LTC2938IMS#TRPBF	2938	12-Lead Plastic MSOP	–40°C to 85°C
LTC2938HMS#PBF	LTC2938HMS#TRPBF	2938	12-Lead Plastic MSOP	–40°C to 125°C
LTC2939CMS#PBF	LTC2939CMS#TRPBF	2939	16-Lead Plastic MSOP	0°C to 70°C
LTC2939IMS#PBF	LTC2939IMS#TRPBF	2939	16-Lead Plastic MSOP	–40°C to 85°C
LTC2939HMS#PBF	LTC2939HMS#TRPBF	2939	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Minimum Internal Operating Voltage	$\overline{RST}$ in Correct Logic State	●			1	V
V_{CCMINP}	Minimum Required for Configuration	V_{CC} Rising	●			2.6	V
V_{RT50}	5V, 5% Reset Threshold	V1 Input Threshold	●	4.600	4.675	4.750	V
V_{RT33}	3.3V, 5% Reset Threshold	V1, V2 Input Threshold	●	3.036	3.086	3.135	V
V_{RT25}	2.5V, 5% Reset Threshold	V2, V3 Input Threshold	●	2.300	2.338	2.375	V
V_{RT18}	1.8V, 5% Reset Threshold	V2, V3, V4 Input Threshold	●	1.656	1.683	1.710	V
V_{RT15}	1.5V, 5% Reset Threshold	V2, V3, V4 Input Threshold	●	1.380	1.403	1.425	V
V_{RT12}	1.2V, 5% Reset Threshold	V2, V3, V4 Input Threshold	●	1.104	1.122	1.140	V
V_{RTA}	ADJ Reset Threshold	V3, V4, V5, V6 Input Threshold	●	492.5	500	507.5	mV
V_{RTAN}	–ADJ Reset Threshold	V4 Input Threshold	●	–18	0	18	mV
V_{REF}	Reference Voltage	V_{CC} > 2.3V, I_{VREF} = ±1mA, C_{REF} < 1000pF	●	1.192	1.210	1.228	V
V_{PG}	Configuration Voltage Range	V_{CC} > V_{CCMINP}	●	0		V_{REF}	V
I_{VPG}	V_{PG} Input Current	V_{PG} = V_{REF}	●			±20	nA
I_{V1}	V1 Input Current	V1 = 5V, I_{VREF} = 12µA, (Note 4)	●		80	125	µA
I_{V2}	V2 Input Current	V2 = 3.3V	●		0.8	2	µA
I_{V3}	V3 Input Current	V3 = 2.5V V3 = 0.55V (ADJ Mode)	● ●		0.52	1.2 ±15	µA nA
I_{V4}	V4 Input Current	V4 = 1.8V V4 = 0.55V (ADJ Mode) V4 = -0.02V (–ADJ Mode)	● ● ●		0.34	0.8 ±15 ±15	µA nA nA
I_{V5}, I_{V6}	V5, V6 Input Current (LTC2939)	V5, V6 = 0.55V	●			±15	nA
$I_{CRT(UP)}$	CRT Pull-Up Current	V_{CRT} = GND	●	–1.4	–2	–2.6	µA
$I_{CRT(DN)}$	CRT Pull-Down Current	V_{CRT} = 1.3V	●	10	20	30	µA
t_{RST}	Reset Timeout Period	C_{RT} = 1500pF	●	2	3	4	ms
t_{UV}	V_n Undervoltage Detect to $\overline{RST}$	V_n Less Than Reset Threshold V_{RTX} by More Than 1%			150		µs
V_{OL}	Voltage Output Low $\overline{RST}$	I_{SINK} = 2.5mA; V_{CC} = 3V	●		0.15	0.4	V
		I_{SINK} = 100µA; V_{CC} = 1V	●		0.05	0.3	V
V_{OL}	Voltage Output Low $\overline{WDO}$	I_{SINK} = 2.5mA; V_{CC} = 3.3V	●		0.15	0.4	V
V_{OH}	Voltage Output High $\overline{RST}$, $\overline{WDO}$ (Note 5)	I_{SOURCE} = –1µA; V2 = 3.3V	●	V2 – 1			V
$I_{CWT(UP)}$	CWT Pull-Up Current	V_{CWT} = GND	●	–1.4	–2	–2.6	µA
$I_{CWT(DN)}$	CWT Pull-Down Current	V_{CWT} = 1.3V	●	10	20	30	µA
t_{WD}	Watchdog Timeout Period	C_{WT} = 1500pF	●	20	30	40	ms
V_{WDI}	WDI Input Threshold (V_{CC} = 3.3V to 5.5V)	Logic Low Open Logic High	● ● ●	 0.7 1.4	 0.9	0.4 1.1	V V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{WDI}	WDI Input Current	V_{WDI} = GND	●			–30	µA
		V_{WDI} = 0.7V	●	–10			µA
		V_{WDI} = 1.1V	●	10			µA
		V_{WDI} = 5V	●			30	µA
t_{WP}	WDI Input Pulse Width	V_{CC} = 3.3V or 5.5V	●	2			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

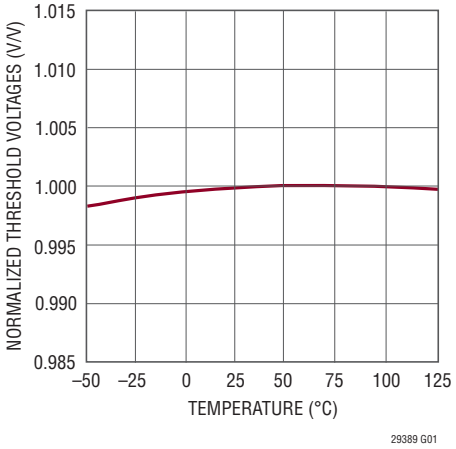
Note 3: The greater of V1, V2 is the internal supply voltage (V_{CC}).

Note 4: Under static no-fault conditions, V1 will necessarily supply quiescent current. If at any time V2 is larger than V1, V2 must be capable of supplying the quiescent current, programming (transient) current and reference load current.

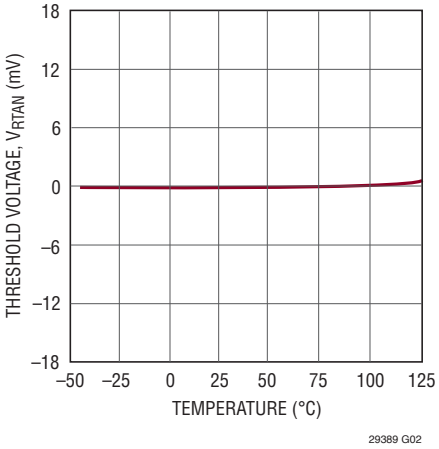
Note 5: The outputs $\overline{RST}$ and $\overline{WDO}$ have internal pull-ups to V2 of typically 6µA. However, external pull-up resistors may be used when faster rise times are required or for V_{OH} voltages greater than V2. For V2 configured to monitor 1.2V, 1.5V, 1.8V and 2.5V supplies, external pull-up resistors are required to ensure that the output voltage, high, is above the V_{IH} input threshold of the external circuit.

TYPICAL PERFORMANCE CHARACTERISTICS

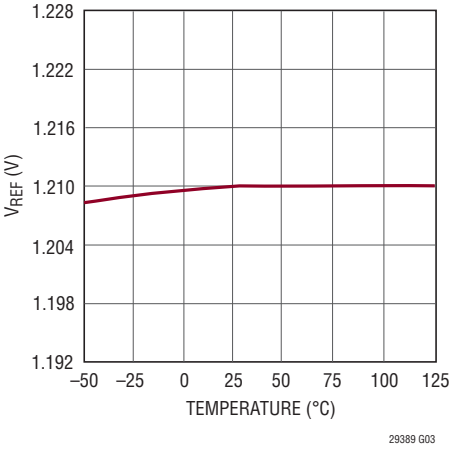
Normalized Threshold Voltages vs Temperature



–ADJ Threshold Voltage vs Temperature

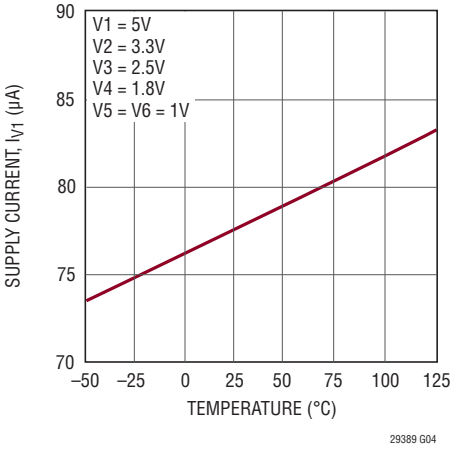


V_{REF} vs Temperature

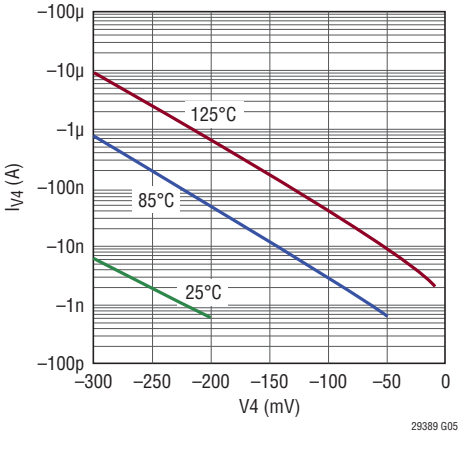


TYPICAL PERFORMANCE CHARACTERISTICS

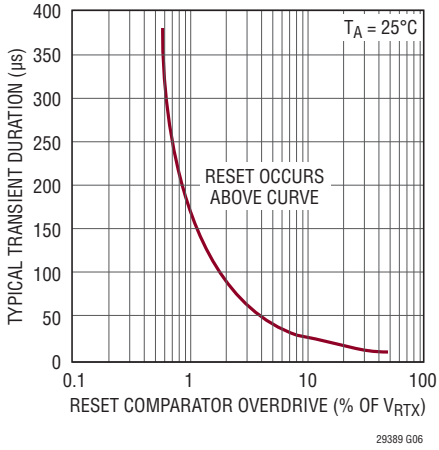
Supply Current vs Temperature



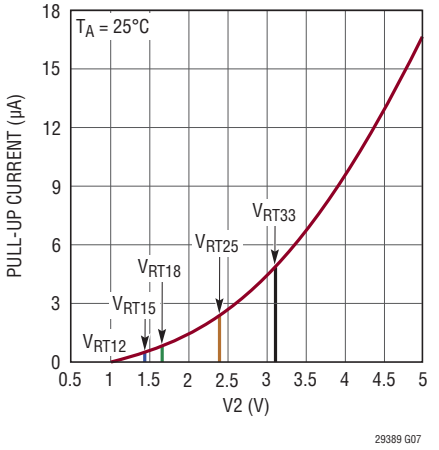
I(V4) vs V4 in –ADJ mode



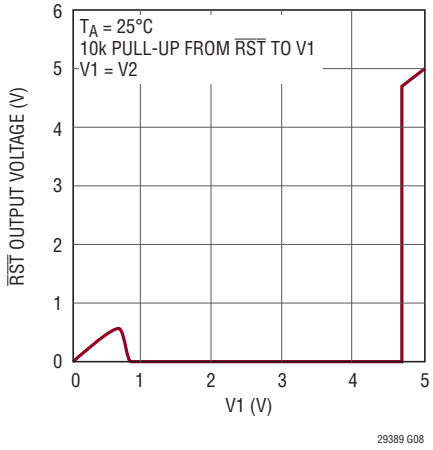
Transient Duration vs Comparator Overdrive



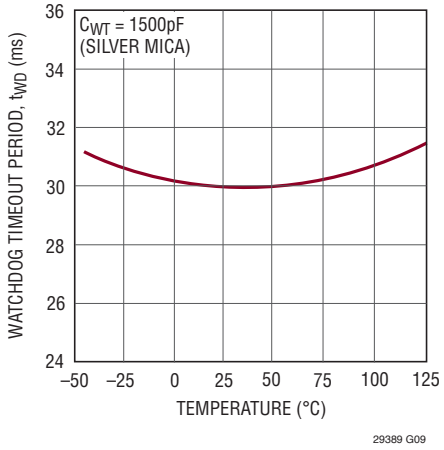
$\overline{RST}$ Pull-Up Current vs V2



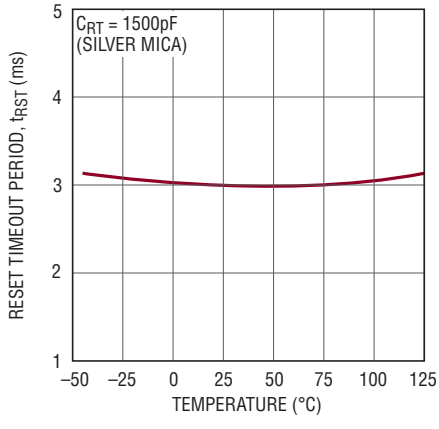
$\overline{RST}$ Output Voltage vs V1, V_{PG} = GND



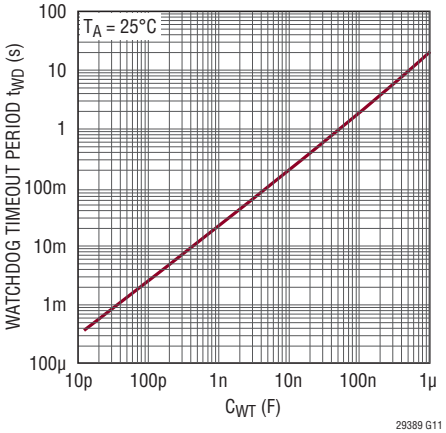
Watchdog Timeout Period vs Temperature



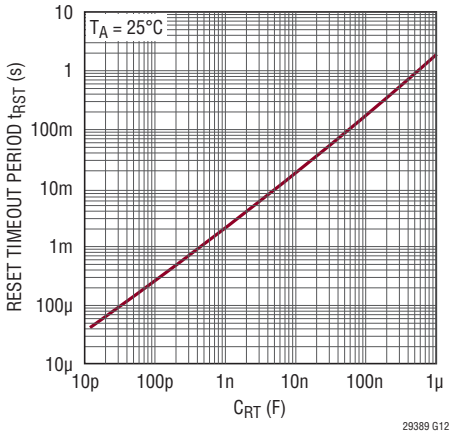
Reset Timeout Period vs Temperature



Watchdog Timeout Period vs C_{WT}

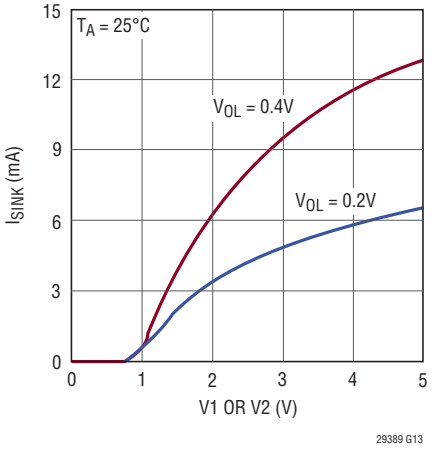


Reset Timeout Period vs C_{RT}



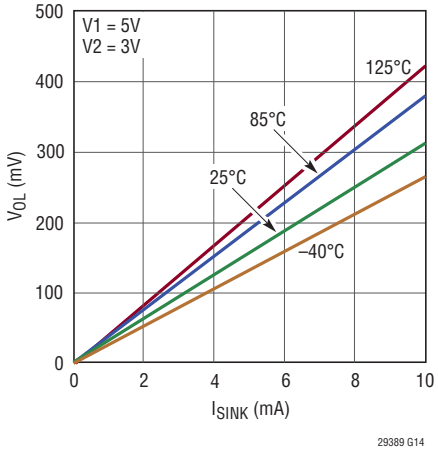
TYPICAL PERFORMANCE CHARACTERISTICS

I_{SINK} vs Supply Voltage ($\overline{RST}$)



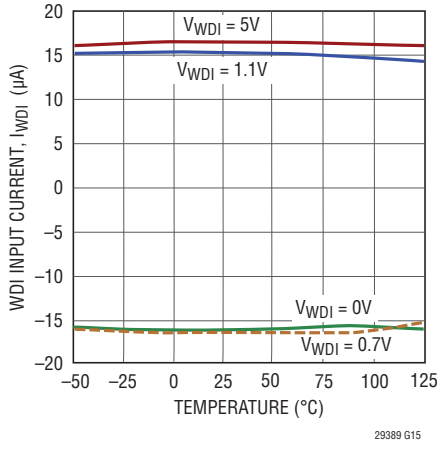
29389 G13

Voltage Output Low vs Sink Current ($\overline{RST}$, $\overline{WDO}$)



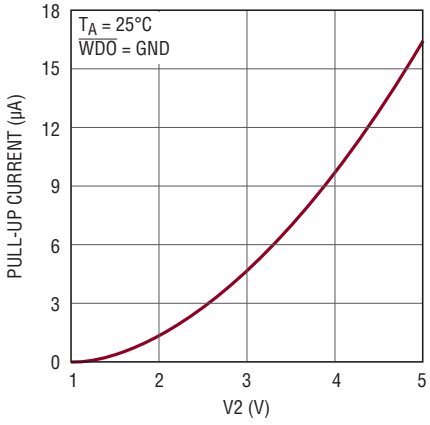
29389 G14

WDI Input Current vs Temperature



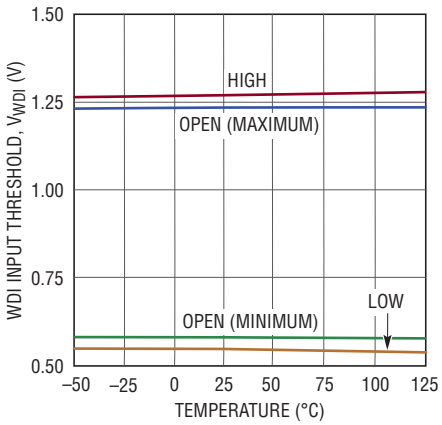
29389 G15

$\overline{WDO}$ Pull-Up Current vs V2



29389 G16

WDI Input Threshold vs Temperature



29389 G17

PIN FUNCTIONS

CRT: Reset Timeout Capacitor. Attach an external capacitor (C_{RT}) to GND to set a reset timeout of 2ms/nF. A 47nF capacitor generates a 94ms reset delay time. Leaving CRT unconnected generates a minimum timeout period of approximately 20µs which will vary depending on parasitic capacitance on the pin.

CWT: Watchdog Timeout Capacitor. Attach a capacitor (C_{WT}) between CWT and GND to set a watchdog timeout period of 20ms/nF. A 47nF capacitor generates a 940ms watchdog timeout period. Leaving CWT unconnected generates a minimum timeout period of approximately 200µs which

PIN FUNCTIONS

will vary depending on parasitic capacitance on the pin. Tie CWT to GND to disable the watchdog function.

GND: Device Ground.

NC: No Internal Connection.

$\overline{RST}$: Reset Output. Logic output with weak 6µA pull-up to V2. Pulls low when any voltage input is below the reset threshold and held low for the configured reset delay time after all voltage inputs are above threshold. When the watchdog timer is enabled but not serviced prior to the configured watchdog timeout period, $\overline{RST}$ pulls low for one reset delay time. May be pulled to greater than V2 using an external pull-up. For V2 configured to monitor 2.5V or below, connect an external pull-up resistor to the interface logic supply to ensure that the output high voltage is above the V_{IH} of the external circuit. Leave open if unused.

V1: Voltage Input 1. Select from 5V or 3.3V. See the Applications Information section for details. The greater of V1 or V2 is also V_{CC} for the device. Bypass this input to ground with a 0.1µF (or greater) capacitor.

V2: Voltage Input 2. Select from 3.3V, 2.5V, 1.8V, 1.5V or 1.2V. See the Applications Information section for details. The greater of V1, V2 is also V_{CC} for the device. Bypass this input to ground with a 0.1µF (or greater) capacitor. All status outputs are weakly pulled up to V2.

V3: Voltage Input 3. Select from 2.5V, 1.8V, 1.5V, 1.2V or ADJ. See the Applications Information section for details. Tie to V1 if unused.

V4: Voltage Input 4. Select from 1.8V, 1.5V, 1.2V, ADJ or –ADJ. See the Applications Information section for details. Tie to V1 if unused and configured for positive voltage.

V5: Adjustable Voltage Input 5 for LTC2939. High impedance comparator input with 0.5V typical threshold. Tie to V1 if unused.

V6: Adjustable Voltage Input 6 for LTC2939. High impedance comparator input with 0.5V typical threshold. Tie to V1 if unused.

V_{PG}: Threshold Select Input. Connect to an external 1% resistive divider between V_{REF} and GND to select one of sixteen combinations of voltage thresholds (see Table 1). Do not add capacitance to the V_{PG} input.

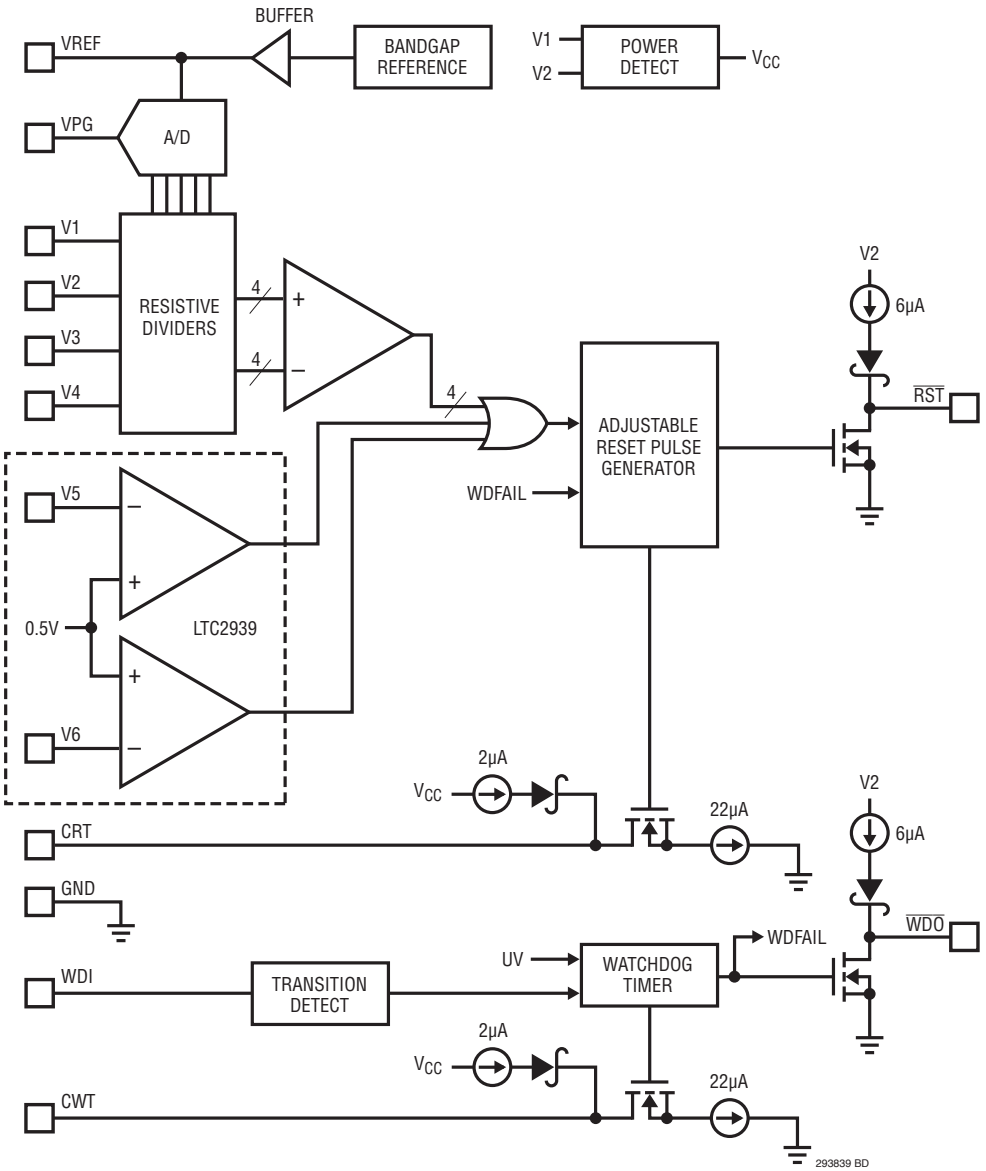
V_{REF}: Buffered Reference Voltage Output. A 1.210V nominal reference used for the mode selection voltage (V_{PG}) and for the offset of negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

WDI: Watchdog Input: A three-state input that controls the operation of the watchdog timer. Leaving the WDI pin unconnected disables the watchdog timer while tying it low or high enables it. While $\overline{RST}$ is high, a transition between low and high logic levels (rising or falling edge) within the watchdog timeout period is required to inhibit $\overline{WDO}$ from pulling low and a watchdog initiated reset. A capacitor attached to CWT sets the watchdog timeout period. A transition between the low and high logic levels on the WDI input clears the voltage on the CWT capacitor, preventing $\overline{WDO}$ from going low. Once $\overline{WDO}$ is latched low, WDI must transition between low and high logic levels to clear $\overline{WDO}$ Transitions between open and logic low or logic high do not clear $\overline{WDO}$.

$\overline{WDO}$: Watchdog Output. Logic output with weak 6µA pull-up to V2. May be pulled greater than V2 using external pull-up. For V2 configured to monitor 2.5V or below, connect an external pull-up resistor to the interface logic supply to ensure that the output high voltage is above the V_{IH} of the external circuit. The watchdog timer is enabled when $\overline{RST}$ is high. The watchdog output pulls low if the watchdog timer expires and the output remains low until set high by the next WDI transition or anytime an undervoltage condition occurs. A watchdog failure also triggers a reset event. Leave open if unused.

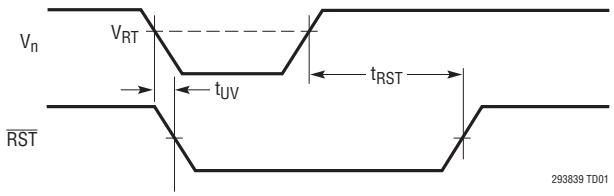
Exposed Pad (DE12 package only): The Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM

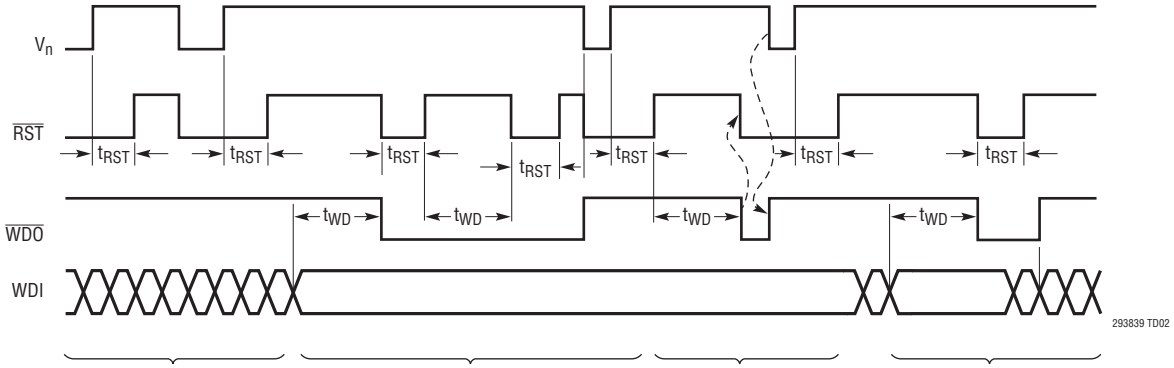


TIMING DIAGRAM

V_n Monitor Timing



Reset and Watchdog Timing



POWER-ON RESET FOLLOWED BY RESET CAUSED BY UNDERVOLTAGE EVENT.

WATCHDOG OUTPUT SET HIGH, WATCHDOG INPUT = DON'T CARE

WATCHDOG INPUT NOT TOGGLED, WATCHDOG TIMER EXPIRES, WATCHDOG OUTPUT PULLS LOW. RESET OUTPUT PULLS LOW FOR ONE RESET TIMEOUT PERIOD.

WATCHDOG INPUT REMAINS UNTOGGLED, WATCHDOG OUTPUT REMAINS LOW, RESET OUTPUT PULLS LOW AGAIN AFTER ONE WATCHDOG TIMEOUT PERIOD. WATCHDOG OUTPUT CLEARED BY UNDERVOLTAGE EVENT.

WATCHDOG INPUT NOT TOGGLED, WATCHDOG TIMER EXPIRES, WATCHDOG OUTPUT PULLS LOW. RESET OUTPUT PULLS LOW.

WATCHDOG OUTPUT LOW TIME SHORTENED BY UNDERVOLTAGE EVENT DURING RESET TIMEOUT.

WATCHDOG INPUT NOT TOGGLED, WATCHDOG TIMER EXPIRES, WATCHDOG OUTPUT PULLS LOW. RESET OUTPUT PULLS LOW.

WATCHDOG OUTPUT NOT CLEARED BY WATCHDOG INPUT DURING RESET TIMEOUT. AFTER RESET COMPLETED, WATCHDOG INPUT CLEARS WATCHDOG OUTPUT.

APPLICATIONS INFORMATION

Supply Monitoring

The LTC2938 and LTC2939 are low power, high accuracy configurable four (LTC2938) and six (LTC2939) supply monitoring circuits with reset output and watchdog functions. Both watchdog and reset timeouts are adjustable using external capacitors. Single-pin configuration selects one of sixteen input voltage monitor combinations. All four (LTC2938) or six (LTC2939) voltage inputs must be above predetermined thresholds for the reset not to be invoked. The LTC2938/LTC2939 assert the reset during power-up, power-down and brownout conditions on any one of the voltage inputs.

Power-Up

The greater of V1 or V2 serves as the internal supply voltage (V_{CC}). On power-up, V_{CC} powers the drive circuits for the $\overline{RST}$ output. This ensures that the $\overline{RST}$ output will be low as soon as V1 or V2 reaches 1V. The $\overline{RST}$ output remains low until the part is configured. After configuration, if any one of the supply monitor inputs is below its configured threshold, $\overline{RST}$ will be at logic low. Once all the monitor inputs rise above their thresholds, an internal timer is started and $\overline{RST}$ is released after the configured delay time.

Threshold Accuracy

Consider a 5V system with ±5% tolerance. The 5V supply may vary between 4.75V to 5.25V. System ICs powered by this supply must operate reliably within this band (and a little more as subsequently explained). A perfectly accurate supervisor for this supply generates a reset at exactly 4.75V. However, no supervisor is perfect. The actual reset threshold of a supervisor varies over a specified band. The LTC2938/LTC2939 varies ±1.5% around its nominal threshold voltage (see Figure 1) over temperature.

The reset threshold band and the power supply tolerance bands should not overlap. This prevents false or nuisance resets when the power supply is actually within its specified tolerance band.

The LTC2938 and LTC2939 have ±1.5% reset threshold accuracy, so a 5% threshold is typically set to 6.5% below the nominal input voltage. Therefore, a typical 5V, 5% threshold is 4.675V.

The threshold is guaranteed to lie in the band between 4.750V and 4.600V over temperature. The powered system must work reliably down to the low end of the threshold band, or risk malfunction before a reset signal is properly issued.

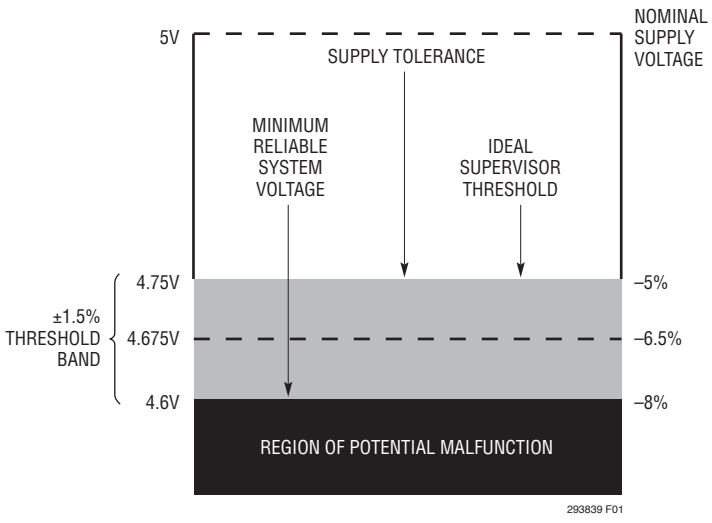


Figure 1. 1.5% Threshold Accuracy Improves System Reliability

APPLICATIONS INFORMATION

A less accurate supervisor increases the required system voltage margin and increases the probability of system malfunction. The LTC2938 and LTC2939 ±1.5% specification improves the reliability of the system over supervisors with wider threshold tolerances.

Monitor Configuration

Select the LTC2938/LTC2939 input voltage combination by placing the recommended resistive divider from V_{REF} to GND and connect the tap point to V_{PG}, as shown in Figure 2.

Table 1 offers recommended 1% resistor values for the various modes. The rightmost column in Table 1 specifies optimum V_{PG}/V_{REF} ratios (±0.01), when configuring with a ratiometric DAC.

Upon power-up, the LTC2938 or LTC2939 enters a configuration period of approximately 150µs during which the voltage on the V_{PG} input is sampled and the monitor is configured to the desired input combination. Do not add capacitance to the V_{PG} input. Immediately after programming, the comparators are enabled and supply monitoring begins.

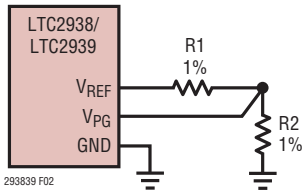


Figure 2. Monitor Programming

Table 1. Voltage Threshold Modes

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (kΩ)	R2 (kΩ)	V_{PG}/V_{REF}
0	5	3.3	ADJ	ADJ	Open	Short	0
1	5	3.3	ADJ	–ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	–ADJ	78.7	22.1	0.219
4	3.3	1.8	1.5	ADJ	71.5	28	0.281
5	5	3.3	2.5	ADJ	66.5	34.8	0.344
6	5	3.3	2.5	1.8	59	40.2	0.406
7	3.3	1.8	1.5	1.2	53.6	47.5	0.469
8	3.3	1.8	1.2	ADJ	47.5	53.6	0.531
9	3.3	1.8	ADJ	ADJ	40.2	59	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28	71.5	0.719
12	3.3	1.8	ADJ	–ADJ	22.1	78.7	0.781
13	3.3	1.5	ADJ	ADJ	16.2	86.6	0.844
14	5	3.3	1.8	ADJ	9.53	93.1	0.906
15	3.3	1.2	ADJ	ADJ	Short	Open	1

APPLICATIONS INFORMATION

Using the Adjustable Thresholds

The reference inputs on the V3 and/or V4 comparators are set to 0.5V when the positive adjustable modes are selected (Figure 3). The LTC2939 V5 and V6 comparators are always in positive adjustable mode with a 0.5V reference. The tap point on an external resistive divider, connected between the positive voltage being sensed and ground, is connected to the high impedance, adjustable inputs (V3, V4, V5 and V6). Calculate the trip voltage from:

$$V_{TRIP} = 0.5V \bullet \left(1 + \frac{R3}{R4}\right)$$

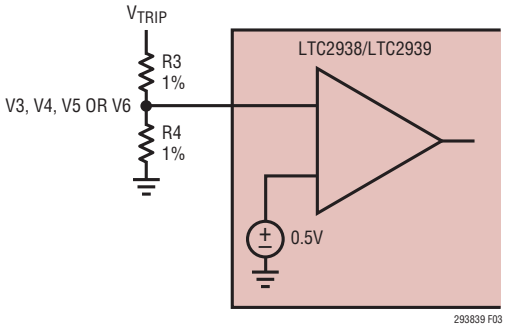


Figure 3. Setting the Positive Adjustable Trip Point

In the negative adjustable mode, the high impedance, adjustable input on the V4 comparator is connected to ground (Figure 4). The tap point on an external resistive divider, connected between the negative voltage being sensed and the V_{REF} output, is connected to the high impedance adjustable input (V4). V_{REF} provides the necessary level shift required to operate at ground. The negative trip voltage is calculated from:

$$V_{TRIP} = -V_{REF} \bullet \frac{R3}{R4};\ V_{REF} = 1.210V\ \text{Nominal}$$

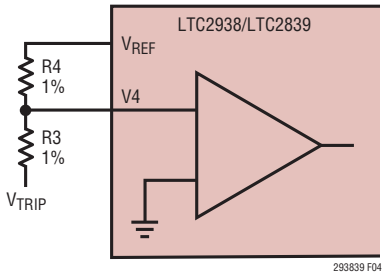


Figure 4. Setting the Negative Adjustable Trip Point

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of V_{REF} (±1mA). With no other load on V_{REF}, R4 (minimum) is:

$$\frac{1.210V}{1mA} = 1.210k$$

Tables 2 and 3 offer suggested 1% resistor values for various adjustable applications assuming 5% monitor thresholds.

Table 2. Suggested 1% Resistor Values for the ADJ Inputs

V_{SUPPLY} (V)	V_{TRIP} (V)	R3 (kΩ)	R4 (kΩ)
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1	0.933	86.6	100
0.9	0.840	68.1	100

Table 3. Suggested 1% Resistor Values for the Negative ADJ Inputs

V_{SUPPLY} (V)	V_{TRIP} (V)	R3 (kΩ)	R4 (kΩ)
–2	–1.87	1.87	121
–5	–4.64	464	121
–5.2	–4.87	487	121
–10	–9.31	931	121
–12	–11.30	1130	121

Although all of the supply monitor comparators have built-in glitch immunity, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the supply for the device. Filter capacitors on the V3, V4, V5 and V6 inputs are allowed.

APPLICATIONS INFORMATION

Power-Down

On power-down, once any of the monitor inputs drops below its threshold, $\overline{RST}$ is held at a logic low. A logic low of 0.4V is guaranteed until both V1 and V2 drop below 1V. If the bandgap reference becomes invalid (V_{CC} < 2V typical), the LTC2938/LTC2939 will reconfigure when V_{CC} rises above 2.4V (max).

Selecting the Reset Timing Capacitor

The reset timeout period is adjustable in order to accommodate a variety of microprocessor applications. The reset timeout period, t_{RST}, is adjusted by connecting a capacitor, C_{RT}, between CRT and ground. The value of this capacitor is determined by:

$$C_{RT} = \frac{t_{RST}}{2M\Omega} = 500\left(\frac{pF}{ms}\right) \bullet t_{RST}$$

Leaving CRT unconnected generates a minimum reset timeout period of approximately 20µs. The maximum reset timeout period is limited by the largest available low leakage capacitor. The accuracy of the timeout period is affected by capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Watchdog Timer

The watchdog circuit typically monitors a microprocessor's activity. The microprocessor is required to change the logic state of the WDI input on a periodic basis in order to clear the watchdog timer. Whenever an undervoltage condition exists, the watchdog timer is cleared and $\overline{WDO}$ is set high. The watchdog timer starts when $\overline{RST}$ pulls high. Subsequent edges received on the WDI input clear the watchdog timer. If uncleared, the watchdog timer continues to run until it times out. Once it times out, internal circuitry brings the $\overline{WDO}$ and $\overline{RST}$ outputs low. $\overline{WDO}$ remains low for at least one reset timeout period and can then be cleared by a new edge on the WDI input or anytime an undervoltage condition occurs.

The watchdog timer may be disabled in three ways. One method is to simply ground CWT. With CWT held at ground, any undervoltage event forces $\overline{WDO}$ high indefinitely. A second method is to leave the WDI input floating or in high impedance. The last method is to continuously drive WDI between the low and high thresholds.

Selecting the Watchdog Timing Capacitor

The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog timeout period, t_{WD}, is adjusted by connecting a capacitor, C_{WT}, between CWT and ground. The value of this capacitor is determined by:

$$C_{WT} = \frac{t_{WD}}{20M\Omega} = 50\left(\frac{pF}{ms}\right) \bullet t_{WD}$$

Leaving CWT unconnected generates a minimum watchdog timeout period of approximately 200µs. The maximum watchdog timeout period is limited by the largest available low leakage capacitor. The accuracy of the timeout period is affected by capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Pull-Up Resistors for $\overline{WDO}$ and $\overline{RST}$

The $\overline{WDO}$ and $\overline{RST}$ pins provide weak pull-up currents to V2. This current is typically greater than 6µA when V2 is greater than 3.3V. The magnitude of the pull-up current decreases as V2 decreases. For V2 configured to monitor 2.5V, 1.8V, 1.5V and 1.2V supplies, external pull-up resistors are required from both pins to the interface logic supply to ensure that the output high voltage is above the V_{OH} input threshold of the external circuit. The $\overline{WDO}$ and $\overline{RST}$ pins can be pulled to voltages higher than V2 by external pull-up resistors.

Watchdog Application

Figure 5 shows a typical application for the LTC2938/LTC2939. The C_{WT} timing capacitor adjusts the watchdog timeout period for optimal software execution. If the software malfunctions and the state of the WDI pin is unchanged before the end of the watchdog timeout period (t_{WD}), the LTC2938/LTC2939 $\overline{WDO}$ pin is latched to a low state. At the same time, $\overline{RST}$ is pulled low to reset the microprocessor. While $\overline{RST}$ is low, the WDI pin does not affect $\overline{RST}$ or $\overline{WDO}$. The system therefore resets for at least t_{RST}.

APPLICATIONS INFORMATION

After $\overline{RST}$ returns high, the microprocessor can poll the state of the $\overline{WDO}$ pin to determine if the reset was caused by an undervoltage condition or by a watchdog timeout. $\overline{WDO}$ high means that the reset was caused by undervoltage since this condition also resets the $\overline{WDO}$ latch (and the watchdog timer). If the $\overline{WDO}$ pin is low, the system reset was caused by watchdog timeout. The microprocessor can then change the state of WDI to clear the $\overline{WDO}$ latch. If the microprocessor fails to do so, the LTC2938/LTC2939 will alternate between t_{RST} and t_{WD} timeout and $\overline{RST}$ will be pulled low for t_{RST} after every watchdog timeout. $\overline{WDO}$ remains low until the microprocessor flips the state of WDI.

Some microprocessors force their I/O pins into high impedance during reset which in turn, floats the WDI pin. This affects the response of the LTC2938/LTC2939. When the WDI pin is floated, the watchdog timer is reset and C_{WT} is discharged towards ground but $\overline{WDO}$ remains unchanged. Putting WDI in high impedance does not affect t_{RST}. Once $\overline{RST}$ goes high again, and WDI is driven from high impedence to a high or low state, the watchdog timer starts a complete t_{WD} timeout period. A high-to-low or low-to-high transition at WDI clears $\overline{WDO}$ if it was previously latched low.

The $\overline{RST}$ and $\overline{WDO}$ pins should not be tied together to generate the master reset signal since a watchdog timeout forces $\overline{RST}$ low together with $\overline{WDO}$ and the master reset signal will remain low indefinitely.

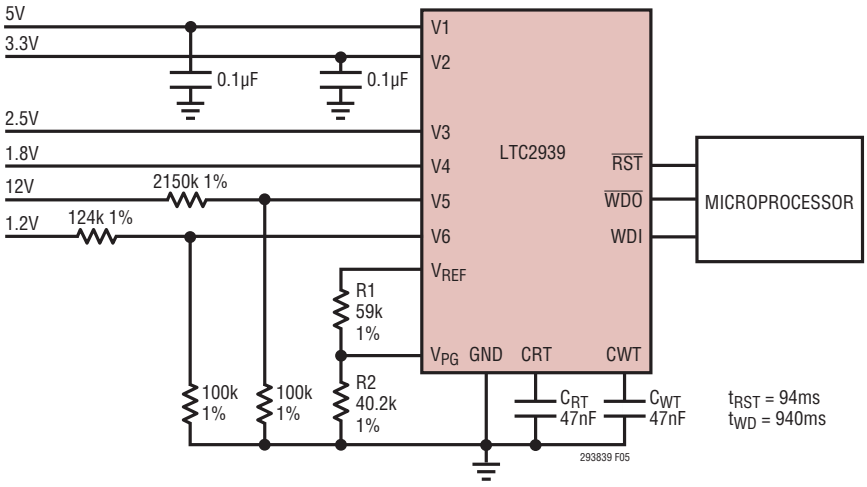
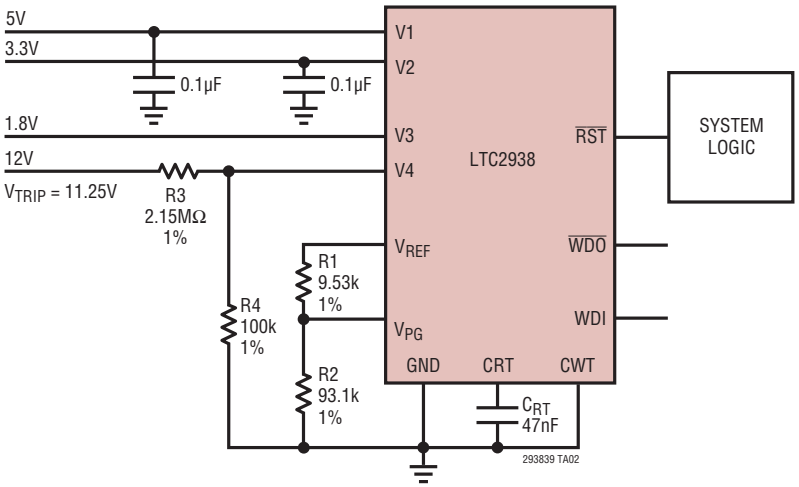


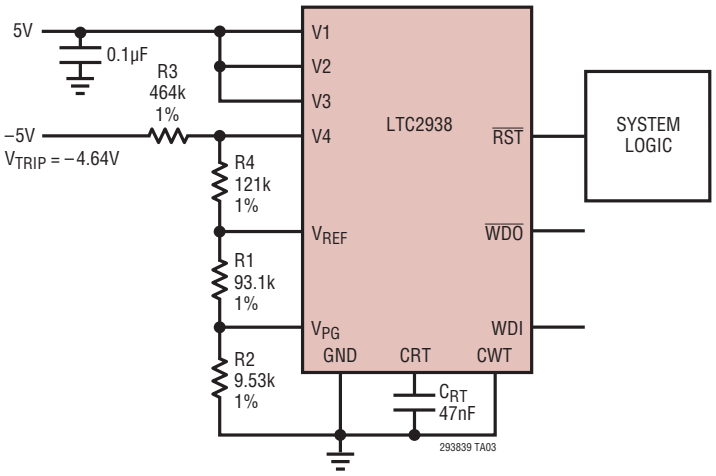
Figure 5. 6-Supply Monitor, 12V (ADJ), 5V, 3.3V, 2.5V, 1.8V, 1.2V (ADJ) with Watchdog Enabled

TYPICAL APPLICATIONS

Quad-Supply Monitor (Mode 14) with Watchdog Disabled

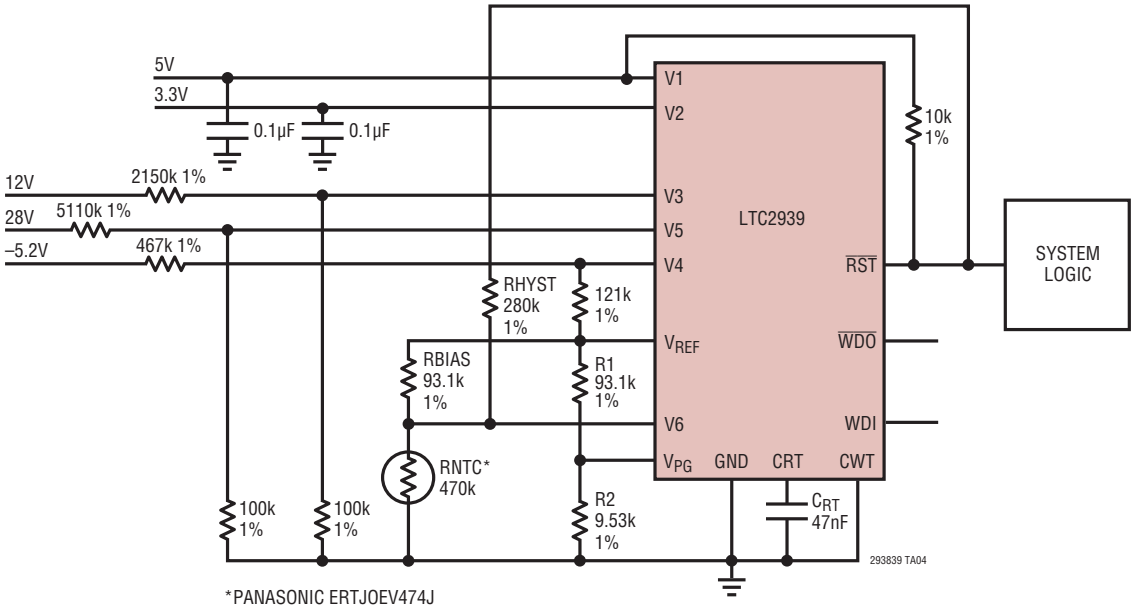


±5V Supply Monitor (Mode 1) with Watchdog Disabled and Unused Inputs Tied High



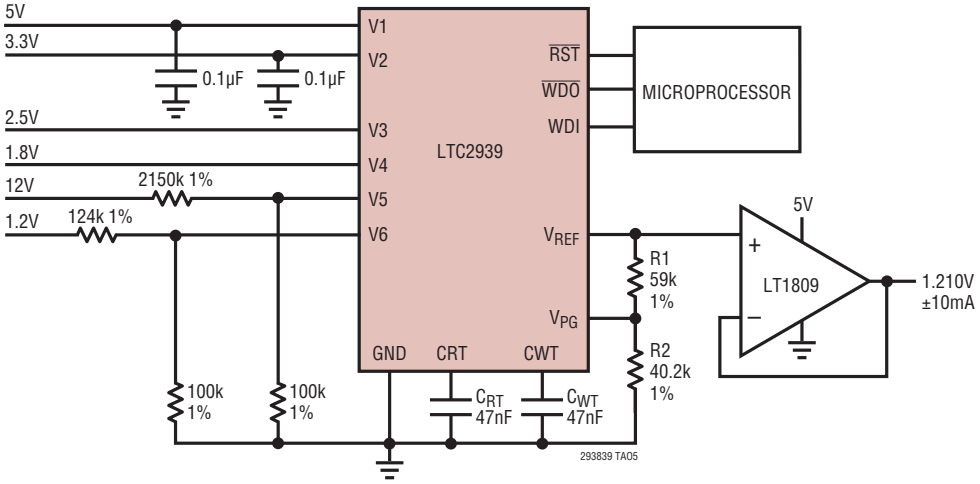
TYPICAL APPLICATIONS

Supply and Temperature Monitor (Mode 1, 5V, 3.3V, 28V, –5.2V, 12V, 100°C)



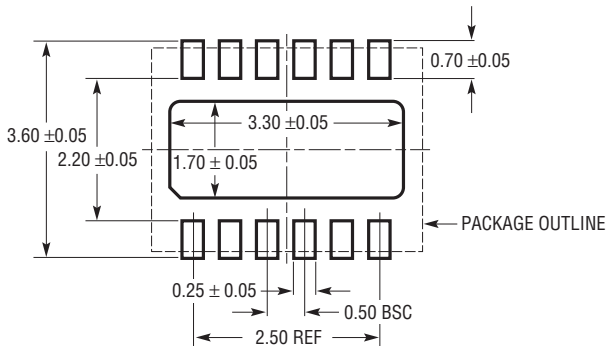
*PANASONIC ERTJOEV474J

Buffered V_{REF} to Power High Current Circuits

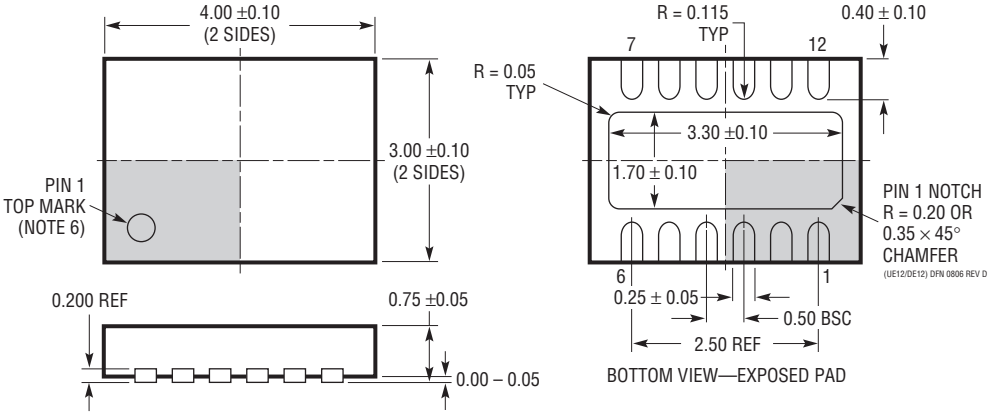


PACKAGE DESCRIPTION

UE/DE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695)



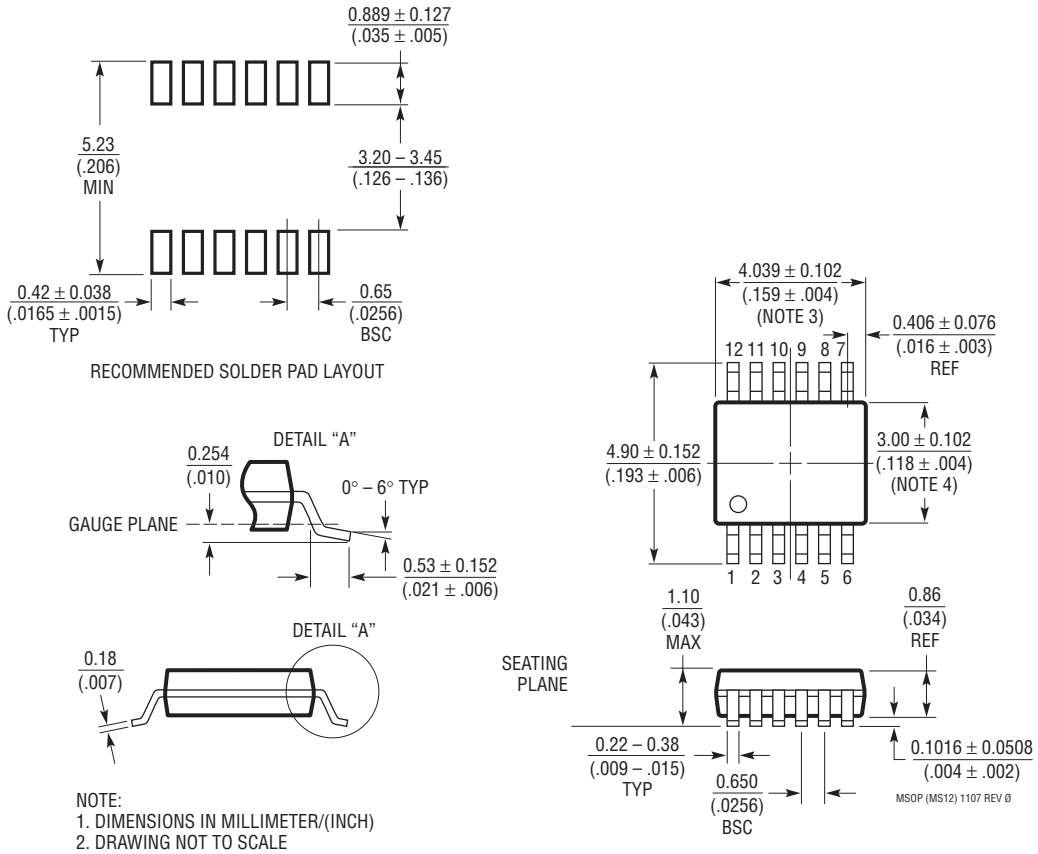
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

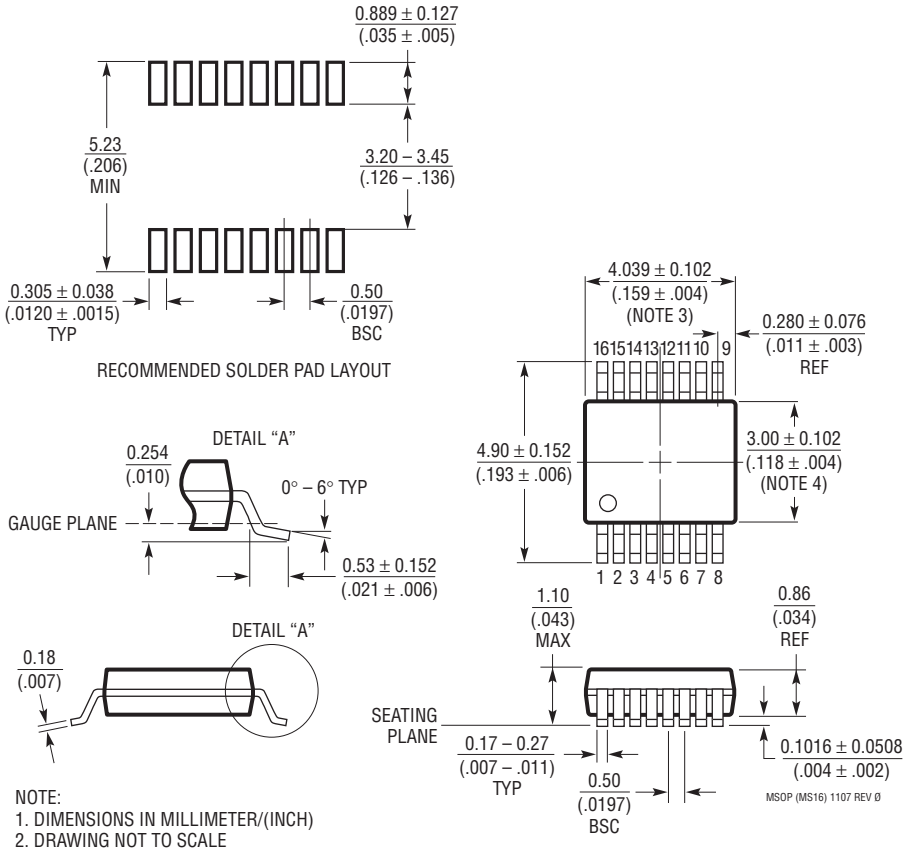
MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev Ø)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

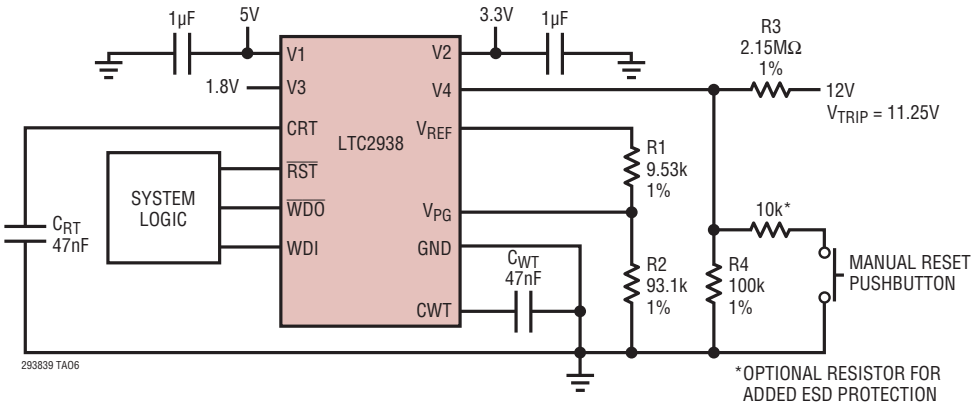
MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Quad-Supply Monitor (Mode 14) with Pushbutton Reset



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2900	Programmable Quad-Supply Monitor	Adjustable Reset, 10-Lead MSOP and DFN Packages
LTC2901	Programmable Quad-Supply Monitor	Adjustable Reset and Watchdog Timer
LTC2902	Programmable Quad-Supply Monitor	Adjustable Reset and Tolerance
LTC2908	Precision 6-Supply Monitor (Four Fixed and Two Adjustable)	8-Lead TSOT-23 and DFN Packages
LTC2930	Configurable 6-Supply Monitor with Adjustable Reset Timer, Manual Reset	H-Grade Temperature Range, 3mm × 3mm DFN-12 Package
LTC2931	Configurable 6-Supply Monitor with Adjustable Reset and Watchdog Timers	H-Grade Temperature Range, Individual Supply Comparator Outputs, TSSOP-20 Package
LTC2932	Configurable 6-Supply Monitor with Individual Comparator Outputs	Adjustable Reset Timer and Tolerance, Pin-Selectable Tolerance (5%, 7.5%, 10% or 12.5%), Reset Disable for Margining, TSSOP-20 Package

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