THE DATASHEET OF

LTC2668IUJ-16#TRPBF

16-Channel 16-/12-Bit ±10V V_{OUT} SoftSpan DACs with 10ppm/°C Max Reference

FEATURES

- **Precision Reference 10ppm/°C Max**
- **Independently Programmable Output Ranges: 0V to 5V, 0V to 10V, ±2.5V, ±5V, ±10V**
- **Full 16-Bit/12-Bit Resolution at All Ranges**
- **Maximum INL Error: ±4LSB at 16 Bits**
- **A/B Toggle via Software or Dedicated Pin**
- **16:1 Analog Multiplexer**
- Guaranteed Monotonic Over Temperature
- Internal or External Reference
- Outputs Drive ±10mA Guaranteed
- 1.8V to 5V SPI Serial interface
- 6mm × 6mm 40-Lead QFN Package

APPLICATIONS

- Optical Networking
- Instrumentation
- Data Acquisition
- Automatic Test Equipment
- Process Control and Industrial Automation

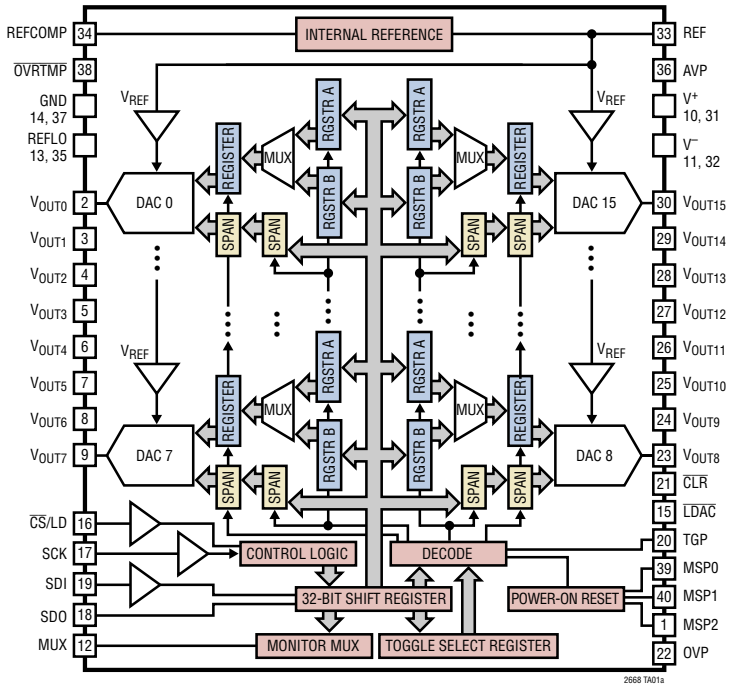
DESCRIPTION

The LTC®2668 is a family of 16-channel, 16-/12-bit ±10V digital-to-analog converters with integrated precision references. They are guaranteed monotonic and have built-in rail-to-rail output buffers. These SoftSpan™ DACs offer five output ranges up to ±10V. The range of each channel is independently programmable, or the part can be hardware-configured for operation in a fixed range.

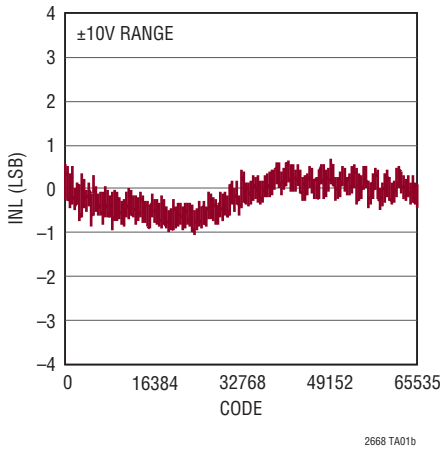
The integrated 2.5V reference is buffered separately to each channel; an external reference can be used for additional range options. The LTC2668 also includes A/B toggle capability via a dedicated pin or software toggle command.

The SPI/Microwire-compatible 3-wire serial interface operates on logic levels as low as 1.71V at clock rates up to 50MHz.

BLOCK DIAGRAM



Integral Nonlinearity (LTC2668-16)

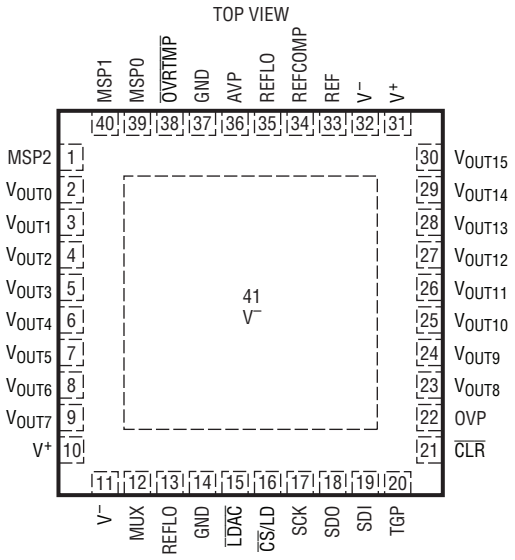


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Analog Supply Voltage (AVP) ..... –0.3V to 6V
Digital I/O Voltage (OVP) ..... –0.3V to 6V
REFLO ..... –0.3V to 0.3V
V^+ ..... –0.3V to 16.5V
V^- ..... –16.5V to 0.3V
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$, TGP ..... –0.3V to 6V
MSP0, MSP1, MSP2 ..... –0.3V to Min (AVP + 0.3V, 6V)
V_{OUT0} to V_{OUT15}, MUX...V^- – 0.3V to V^+ + 0.3V (Max ±16.5V)
REF, REFCOMP ..... –0.3V to Min (AVP + 0.3V, 6V)
SDO ..... –0.3V to Min (OVP + 0.3V, 6V)
$\overline{OVRTMP}$ ..... –0.3V to 6V
Operating Temperature Range
  LTC2668C ..... 0°C to 70°C
  LTC2668I ..... –40°C to 85°C
  LTC2668H ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 33°C/W, θ_{JC} = 2°C/W
EXPOSED PAD IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LTC2668 C UJ 16 #TR PBF

LEAD FREE DESIGNATOR
PBF = Lead Free

TAPE AND REEL
TR = 2000-Piece Tape and Reel

RESOLUTION
16 = 16-Bit
12 = 12-Bit

PACKAGE TYPE
UJ = 40-Lead QFN

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)
H = Automotive Temperature Range (–40°C to 125°C)

PRODUCT PART NUMBER

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

PRODUCT SELECTION GUIDE

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2668CUJ-16#PBF	LTC2668CUJ-16#TRPBF	LTC2668UJ-16	40-Lead (6mm × 6mm) QFN	0°C to 70°C
LTC2668IUJ-16#PBF	LTC2668IUJ-16#TRPBF	LTC2668UJ-16	40-Lead (6mm × 6mm) QFN	–40°C to 85°C
LTC2668HUJ-16#PBF	LTC2668HUJ-16#TRPBF	LTC2668UJ-16	40-Lead (6mm × 6mm) QFN	–40°C to 125°C
LTC2668CUJ-12#PBF	LTC2668CUJ-12#TRPBF	LTC2668UJ-12	40-Lead (6mm × 6mm) QFN	0°C to 70°C
LTC2668IUJ-12#PBF	LTC2668IUJ-12#TRPBF	LTC2668UJ-12	40-Lead (6mm × 6mm) QFN	–40°C to 85°C
LTC2668HUJ-12#PBF	LTC2668HUJ-12#TRPBF	LTC2668UJ-12	40-Lead (6mm × 6mm) QFN	–40°C to 125°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AVP = 5V, OVP = 5V, V^+ = 15V, V^- = –15V, V_{REF} = 2.5V, V_{OUT} unloaded unless otherwise specified.

LTC2668-16/LTC2668-12

SYMBOL	PARAMETER	CONDITIONS		LTC2668-12 MIN	LTC2668-12 TYP	LTC2668-12 MAX	LTC2668-16 MIN	LTC2668-16 TYP	LTC2668-16 MAX	UNITS
DC Performance										
	Resolution		●	12			16			Bits
	Monotonicity	All Ranges (Note 3)	●	12			16			Bits
DNL	Differential Nonlinearity	All Ranges (Note 3)	●		±0.05	±0.5		±0.2	±1	LSB
INL	Integral Nonlinearity All Ranges (Note 3)	V^+/V^- = ±15V	●		±0.2	±1		±2.2	±4	LSB
		V^- = GND (Note 3)								
		C-Grade, I-Grade	●		±0.2	±1		±2.2	±4	LSB
		H-Grade	●		±0.2	±1		±2.2	±5	LSB
V_{OS}	Unipolar Offset Error	0V to 5V Range	●		±1	±2		±1	±2	mV
		0V to 10V Range	●		±2	±4		±2	±4	mV
	V_{OS} Temperature Coefficient	All Unipolar Ranges			1			1		ppm/°C
ZSE	Single-Supply Zero-Scale Error	All Unipolar Ranges, V^- = GND	●		2	4		2	4	mV
BZE	Bipolar Zero Error	All Bipolar Ranges	●		±0.02	±0.08		±0.02	±0.08	%FSR
	BZE Temperature Coefficient	All Bipolar Ranges			1			1		ppm/°C
GE	Gain Error	All Ranges, External Reference	●		±0.02	±0.08		±0.02	±0.08	%FSR
	Gain Temperature Coefficient				2			2		ppm/°C
PSR	Power Supply Rejection All Ranges	AVP = 5V, ±10% V^+/V^- = ±15V, ±5%			0.1 0.001			1 0.01		LSB/V LSB/V

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage Swing	To V^- (Unloaded, V^- = GND)			V^- + 0.004		V
		To V^+ (Unloaded, V^+ = 5V)			V^+ – 0.004		V
		To V^- (–10mA ≤ I_{OUT} ≤ 10mA)	●			V^- + 1.4	V
		To V^+ (–10mA ≤ I_{OUT} ≤ 10mA)	●	V^+ – 1.4			V
	Load Regulation	–10mA ≤ I_{OUT} ≤ 10mA (Note 4)	●		78	150	µV/mA
R_{OUT}	DC Output Impedance	–10mA ≤ I_{OUT} ≤ 10mA (Note 4)	●		0.078	0.15	Ω
	DC Crosstalk (Note 5) 0V to 5V Range	Due to Full-Scale Output Change Due to Load Current Change Due to Powering Down (per Channel)			±1 ±2 ±4		µV µV/mA µV
I_{SC}	V^+/V^- Short-Circuit Output Current (Note 6)	AVP = 5.5V, V^+/V^- = ±15.75V, V_{REF} = 2.5V, ±10V Output Range					
		Code: Zero-Scale; Forcing Output to GND	●	16		42	mA
		Code: Full-Scale; Forcing Output to GND	●	–40		–14.5	mA
Reference							
	Reference Output Voltage			2.495	2.5	2.505	V
	Reference Temperature Coefficient	(Note 7)			±2	±10	ppm/°C
	Reference Line Regulation	AVP ±10%			50		µV/V
	Reference Short-Circuit Current	AVP = 5.5V, Forcing Output to GND	●			5	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AVP = 5V, OVP = 5V, V^+ = 15V, V^- = –15V, V_{REF} = 2.5V, V_{OUT} unloaded unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	REFCOMP Pin Short-Circuit Current	AVP = 5.5V, Forcing Output to GND	●			200	µA
	Reference Load Regulation	AVP = 5V ± 10%, I_{OUT} = 100µA Sourcing			140		mV/mA
	Reference Output Voltage Noise Density	$C_{REFCOMP}$ = C_{REF} = 0.1µF, at f = 10kHz			32		nV/√Hz
	Reference Input Range	External Reference Mode (Note 8)	●	0.5		AVP – 1.75	V
	Reference Input Current	External Reference	●		0.001	1	µA
	Reference Input Capacitance (Note 9)		●		40		pF
Power Supply							
AVP	Analog Supply Voltage		●	4.5		5.5	V
V^+	Analog Positive Supply		●	4.5		15.75	V
V^-	Analog Negative Supply	V^- Not Tied to GND V^- Tied to GND	●	–15.75	 0	–4.5	V V
OVP	Digital I/O Supply Voltage		●	1.71		AVP + 0.3	V
I_{AVP}	Supply Current AVP	AVP = 5V, Unipolar Ranges (Note 10) AVP = 5V, Bipolar Ranges (Note 10)	● ●		5.4 9.4	6.5 12	mA mA
I_S	Supply Current V^+/V^-	Unipolar Ranges (Code = 0) Bipolar Ranges (Note 11)	● ●		4.6 8	6.5 9.5	mA mA
I_{OVP}	Supply Current OVP (Note 12)	OVP = 5V	●		0.02	1	µA
	AVP Shutdown Supply Current	OVP = AVP = 5V, V^+/V^- = ±15V	●		1	3	µA
	V^+ Shutdown Supply Current	OVP = AVP = 5V, V^+/V^- = ±15V	●		35	70	µA
	V^- Shutdown Supply Current	OVP = AVP = 5V, V^+/V^- = ±15V	●	–60	–27		µA
Monitor Mux							
	Monitor Mux DC Output Impedance				2.2		kΩ
	Monitor Mux Leakage Current	Monitor Mux Disabled (High Impedance)	●		0.02	1	µA
	Monitor Mux Output Voltage Range	Monitor Mux Selected to DAC Channel	●	V^-		V^+ – 1.4	V
	Monitor Mux Continuous Current (Note 9)		●			±1	mA
AC Performance							
t_{SET}	Settling Time (Notes 9, 13) 0V to 5V or ±2.5V Span, ±5V Step	±0.024% (±1LSB at 12 Bits) ±0.0015% (±1LSB at 16 Bits)			4.5 9		µs µs
	Settling Time (Notes 9, 13) 0V to 10V or ±5V Span, ±10V Step	±0.024% (±1LSB at 12 Bits) ±0.0015% (±1LSB at 16 Bits)			8 9		µs µs
	Settling Time (Notes 9, 13) ±10V Span, ±20V Step	±0.024% (±1LSB at 12 Bits) ±0.0015% (±1LSB at 16 Bits)			15.5 20.5		µs µs
SR	Voltage Output Slew Rate				5		V/µs
	Capacitive Load Driving				1000		pF
	Glitch Impulse (Note 14)	At Mid-Scale Transition, 0V to 5V Range			8		nV • s
	DAC-to-DAC Crosstalk (Note 15)	Due to Full-Scale Output Change			6		nV • s
e_n	Output Voltage Noise 0V to 5V Output Span, Internal Reference	Density at f = 1kHz Density at f = 10kHz 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, Internal Reference			90 80 1.7 55		nV/√Hz nV/√Hz $µV_{RMS}$ $µV_{RMS}$

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AVP = 5V, OVP = 5V, V^+ = 15V, V^- = –15V, V_{REF} = 2.5V, V_{OUT} unloaded unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital I/O							
V_{OH}	Digital Output High Voltage	SDO Pin. Load Current = –100µA	●	OVP – 0.2			V
V_{OL}	Digital Output Low Voltage	SDO Pin. Load Current = 100µA $\overline{OVRTMP}$ Pin. Load Current = 100µA	● ●			0.2 0.2	V V
I_{OZ}	Digital Hi-Z Output Leakage	SDO Pin Leakage Current ($\overline{CS}$/LD High) $\overline{OVRTMP}$ Pin Leakage Current (Not Asserted)	● ●			±1 1	µA µA
I_{LK}	Digital Input Leakage	V_{IN} = GND to OVP	●			±1	µA
C_{IN}	Digital Input Capacitance (Note 9)		●			8	pF
OVP = 2.7V to AVP							
V_{IH}	Digital Input High Voltage		●	0.8 • OVP			V
V_{IL}	Digital Input Low Voltage		●			0.5	V
OVP = 1.71V to 2.7V							
V_{IH}	Digital Input High Voltage		●	0.8 • OVP			V
V_{IL}	Digital Input Low Voltage		●			0.3	V

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Digital input low and high voltages are 0V and OVP, respectively.

LTC2668-16/LTC2668-12

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AVP = 4.5V to 5.5V, OVP = 2.7V to AVP							
t1	SDI Valid to SCK Setup		●	6			ns
t2	SDI Valid to SCK Hold		●	6			ns
t3	SCK HIGH Time		●	9			ns
t4	SCK LOW Time		●	9			ns
t5	$\overline{CS}$/LD Pulse Width		●	10			ns
t6	LSB SCK High to $\overline{CS}$/LD High		●	7			ns
t7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t8	SDO Propagation Delay from SCK Falling Edge	C_{LOAD} = 10pF OVP = 4.5V to AVP OVP = 2.7V to 4.5V	 ● ●			 20 30	 ns ns
t9	$\overline{CLR}$ Pulse Width		●	20			ns
t10	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
t12	$\overline{LDAC}$ Pulse Width		●	15			ns
t13	$\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition		●	15			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz
t14	TGP High Time (Note 9)		●	1			µs
t15	TGP Low Time (Note 9)		●	1			µs

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Digital input low and high voltages are 0V and OVP, respectively.

LTC2668-16/LTC2668-12

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AVP = 4.5V to 5.5V, OVP = 1.71V to 2.7V							
t1	SDI Valid to SCK Setup		●	7			ns
t2	SDI Valid to SCK Hold		●	7			ns
t3	SCK HIGH Time		●	30			ns
t4	SCK LOW Time		●	30			ns
t5	$\overline{CS}$/LD Pulse Width		●	15			ns
t6	LSB SCK High to $\overline{CS}$/LD High		●	7			ns
t7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t8	SDO Propagation Delay from SCK Falling Edge	C_{LOAD} = 10pF	●			60	ns
t9	$\overline{CLR}$ Pulse Width		●	30			ns
t10	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
t12	$\overline{LDAC}$ Pulse Width		●	15			ns
t13	$\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition		●	15			ns
	SCK Frequency	50% Duty Cycle	●			15	MHz
t14	TGP High Time (Note 9)		●	1			µs
t15	TGP Low Time (Note 9)		●	1			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND

Note 3: For V^- = GND, linearity is defined from code k_L to code $2^N - 1$, where N is the resolution and k_L is the lower end code for which no output limiting occurs. For V_{REF} = 2.5V and N = 16, k_L = 128 and linearity is defined from code 128 to code 65,535. For V_{REF} = 2.5V and N = 12, k_L = 8 and linearity is defined from code 8 to code 4095.

Note 4: $4.5V \le V^+ \le 16.5V$; $-16.5V \le V^- \le -4.5V$ or V^- = GND. V_{OUT} is at least 1.4V below V^+ and 1.4V above V^-.

Note 5: DC crosstalk is measured with AVP = 5V, using the internal reference. The conditions of one DAC channel are changed as specified, and the output of an adjacent channel (at mid-scale) is measured before and after the change.

Note 6: This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: Temperature coefficient is calculated by first computing the ratio of the maximum change in output voltage to the nominal output voltage. The ratio is then divided by the specified temperature range.

Note 8: Gain-error and bipolar zero error specifications may be degraded for reference input voltages less than 1.25V. See the Gain Error vs Reference Input and Bipolar Zero vs Reference Input curves in the Typical Performance Characteristics section.

Note 9: Guaranteed by design and not production tested.

Note 10: Internal reference on.

Note 11: $I(V^+)$ measured in ±10V span; outputs unloaded; all channels at full scale. $I(V^-)$ measured in ±10V span; outputs unloaded; all channels at negative full scale. Each DAC amplifier is internally loaded by a 40kΩ feedback network, so supply currents increase as output voltages diverge from 0V.

Note 12: Digital inputs at 0V or OVP.

Note 13: Internal reference mode. Load is 2k in parallel with 100pF to GND.

Note 14: AVP = 5V, 0V to 5V range, internal reference mode. DAC is stepped ±1LSB between half-scale and half-scale – 1LSB. Load is 2k in parallel with 200pF to GND.

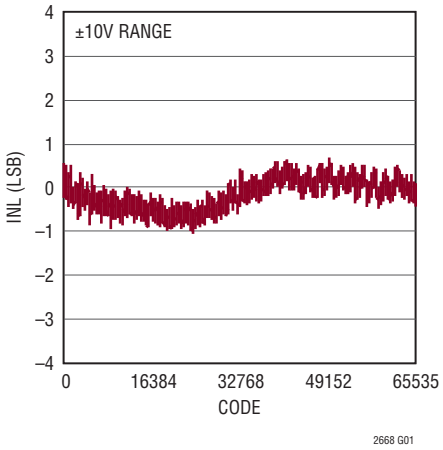
Note 15: DAC-to-DAC crosstalk is the glitch that appears at the output of one DAC due to full-scale change at the output of another DAC. 0V to 10V range with internal reference. The measured DAC is at mid-scale.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

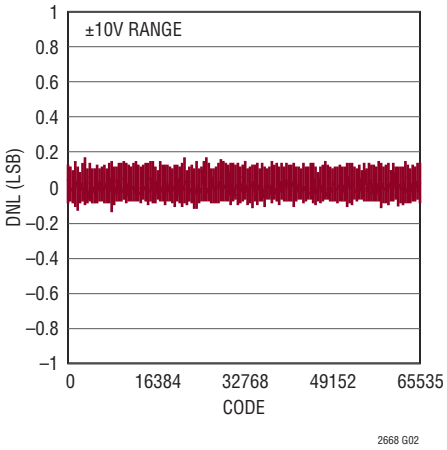
LTC2668-16

Integral Nonlinearity (INL)



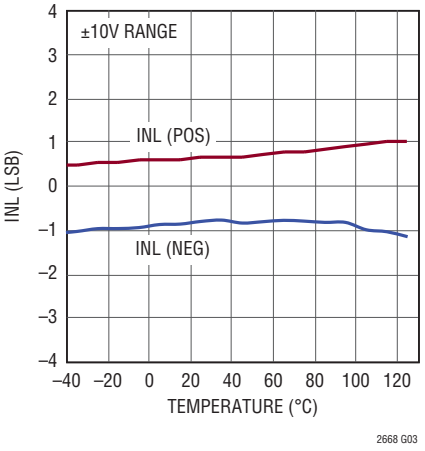
2668 G01

Differential Nonlinearity (DNL)



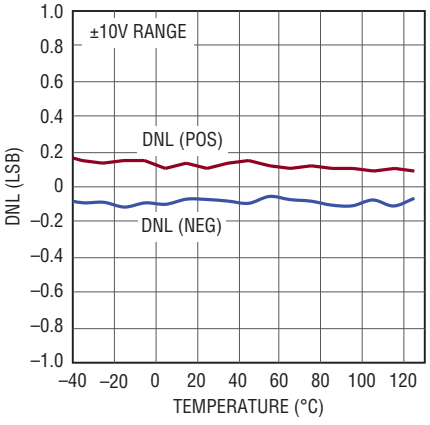
2668 G02

INL vs Temperature



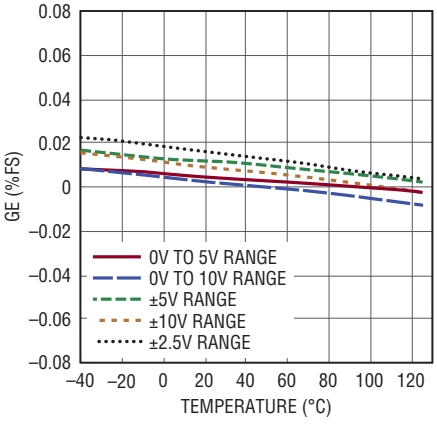
2668 G03

DNL vs Temperature



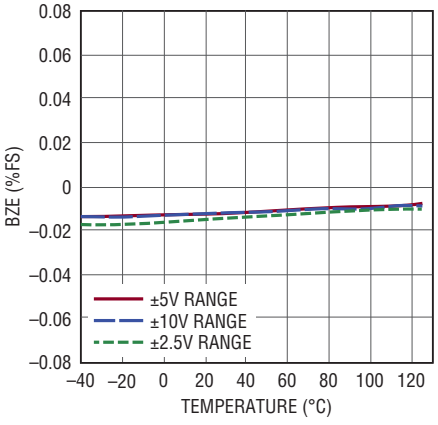
2668 G04

Gain Error vs Temperature



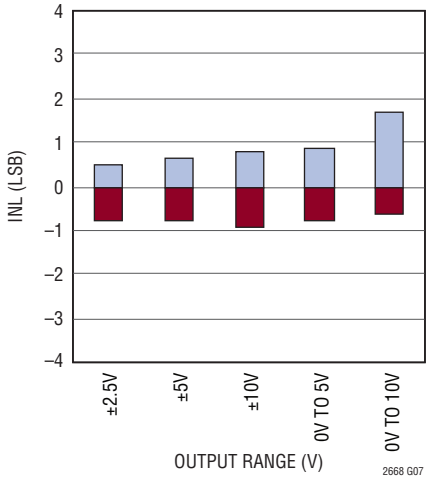
2668 G05

Bipolar Zero Error vs Temperature



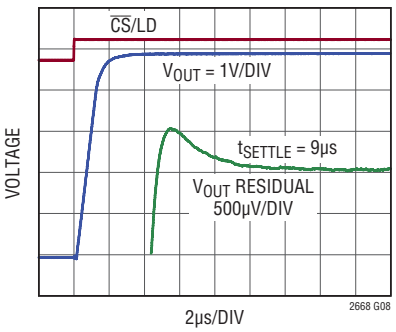
2668 G06

INL vs Output Range



2668 G07

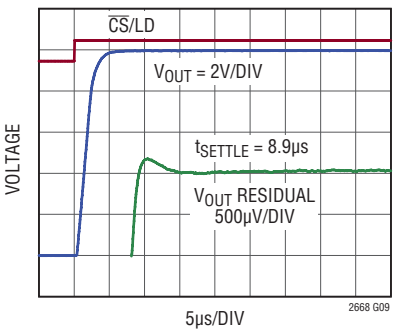
Settling 5V Step



2668 G08

0V to 5V RANGE; INTERNAL REFERENCE
RISING 5V STEP; AVERAGE OF 64 EVENTS.
FALLING SETTLING IS SIMILAR OR BETTER.
SUBTRACT 100ns FIXTURE DELAY FROM
SETTLING WAVEFORM

Settling 10V Step



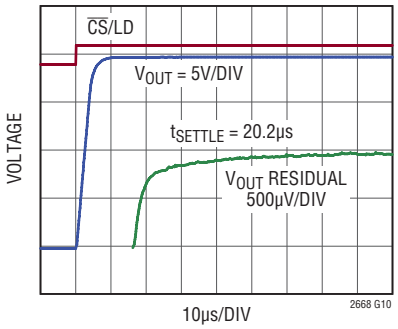
2668 G09

0V to 10V RANGE; INTERNAL REFERENCE
RISING 10V STEP; AVERAGE OF 64 EVENTS.
FALLING SETTLING IS SIMILAR OR BETTER.
SUBTRACT 100ns FIXTURE DELAY FROM
SETTLING WAVEFORM

TYPICAL PERFORMANCE CHARACTERISTICS

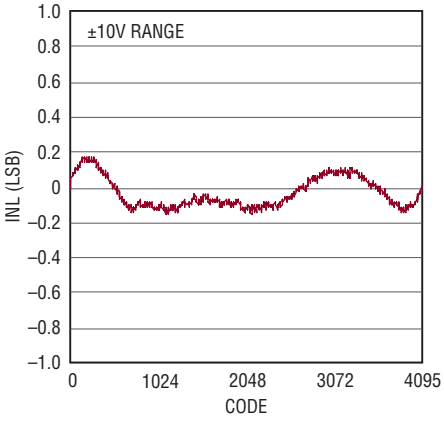
T_A = 25°C, unless otherwise noted.

Settling 20V Step

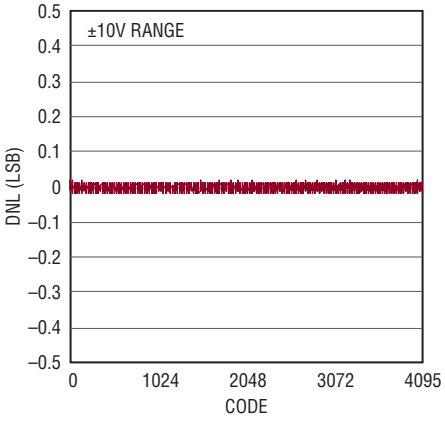


±10V RANGE; INTERNAL REFERENCE
RISING 20V STEP; AVERAGE OF 64 EVENTS.
FALLING SETTLING IS SIMILAR OR BETTER.
SUBTRACT 100ns FIXTURE DELAY FROM
SETTLING WAVEFORM.

Integral Nonlinearity (INL) (LTC2668-12)

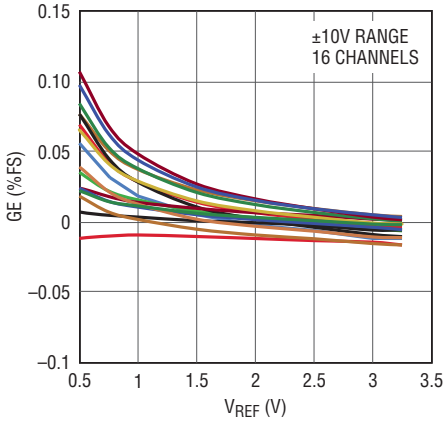


Differential Nonlinearity (DNL) (LTC2668-12)

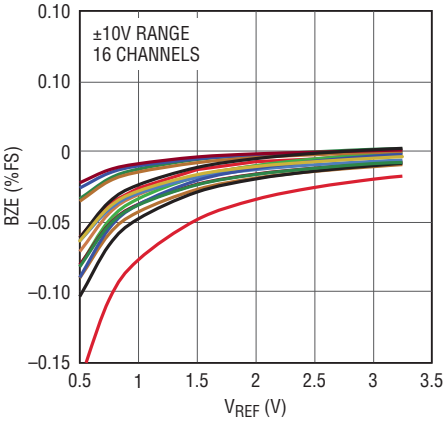


LTC2668-16/LTC2668-12

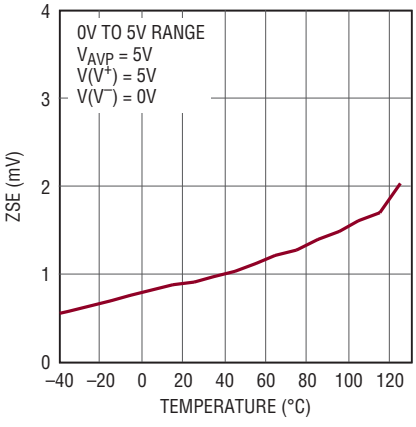
Gain Error vs Reference Input



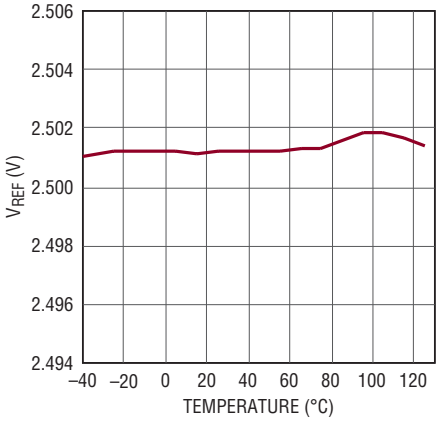
Bipolar Zero Error vs Reference Input



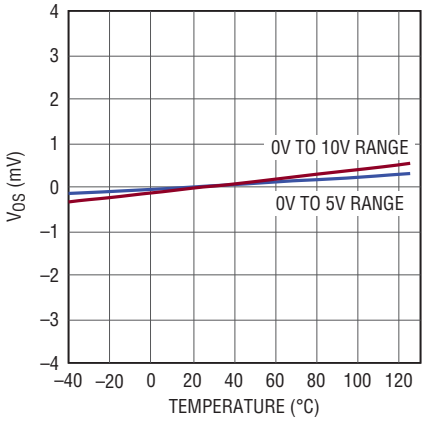
Single-Supply Zero-Scale Error vs Temperature



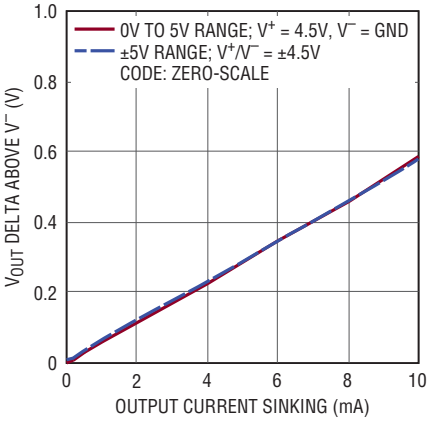
Reference Output vs Temperature



Unipolar Offset vs Temperature



Headroom to V⁻ Rail vs Output Current

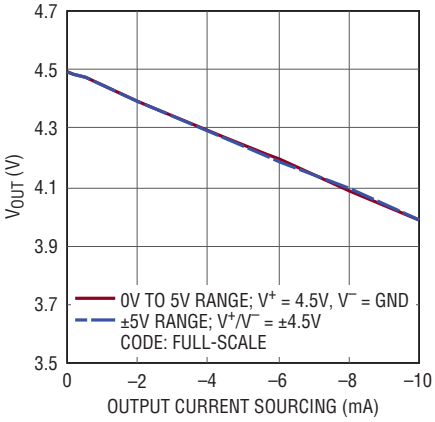


TYPICAL PERFORMANCE CHARACTERISTICS

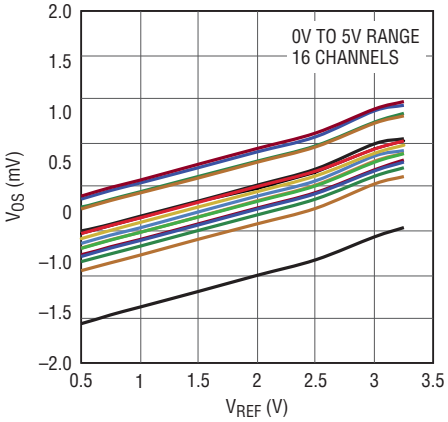
T_A = 25°C, unless otherwise noted.

LTC2668-16/LTC2668-12

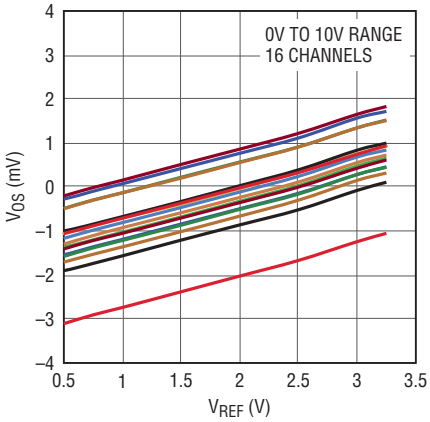
Headroom to V⁺ Rail vs Output Current



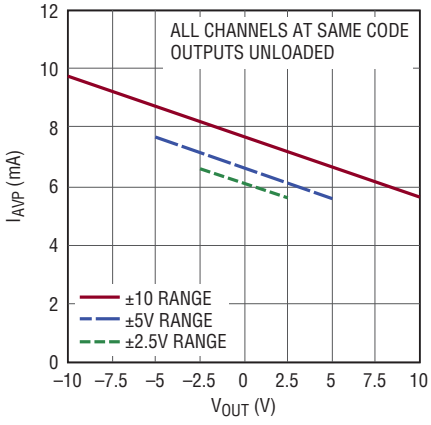
Unipolar Offset vs Reference Input



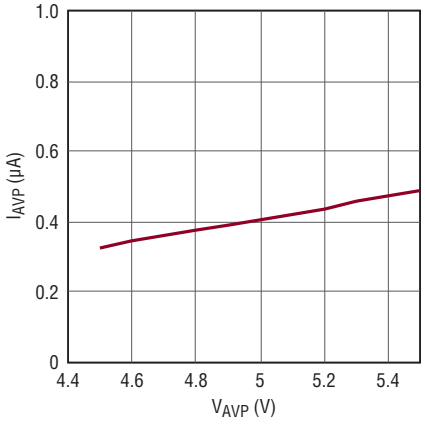
Unipolar Offset vs Reference Input



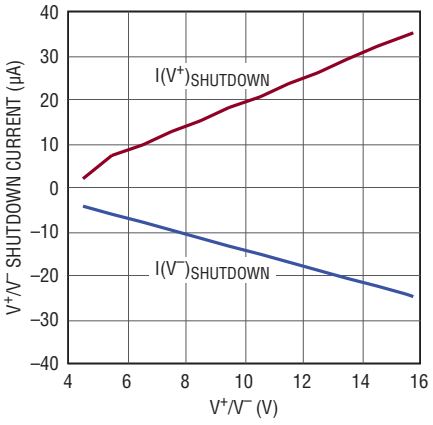
AVP Supply Current vs Bipolar Output Voltage



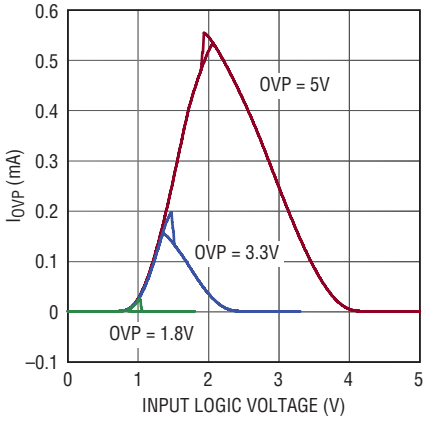
AVP Shutdown Current vs AVP



V⁺/V⁻ Shutdown Current vs Symmetric Supplies

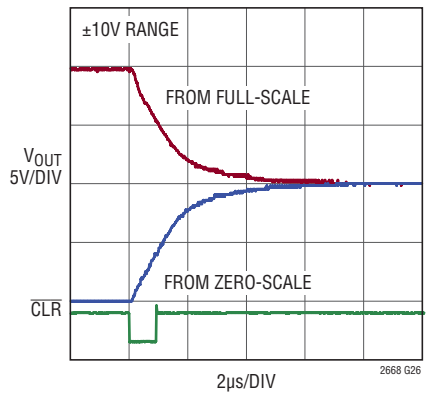


I_{OVP} Supply Current vs Logic Voltage

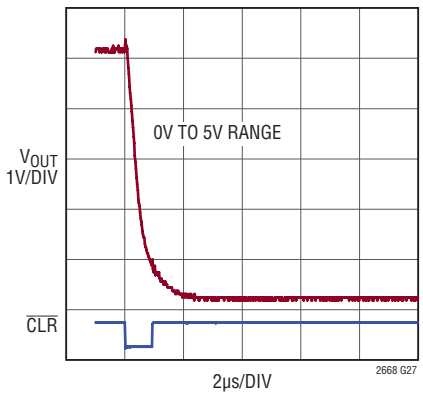


AVP = 5V
SCK, SDI, $\overline{CS}$/LD, $\overline{CLR}$, $\overline{LDAC}$,
TGP TIED TOGETHER

Hardware CLR to Mid-Scale



Hardware CLR to Zero-Scale

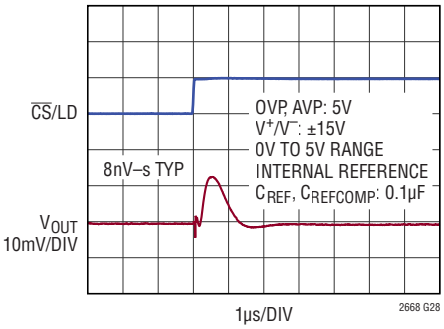


TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

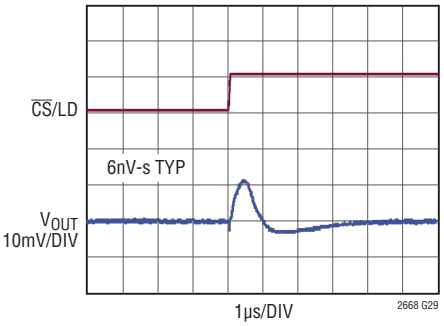
LTC2668-16/LTC2668-12

Mid-Scale Glitch Impulse



FALLING MAJOR CARRY TRANSITION
RISING TRANSITION IS SIMILAR OR BETTER
ALL CHANNELS ARE SIMILAR OR BETTER

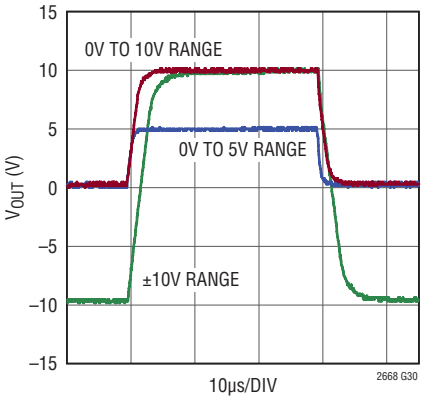
DAC-to-DAC Crosstalk



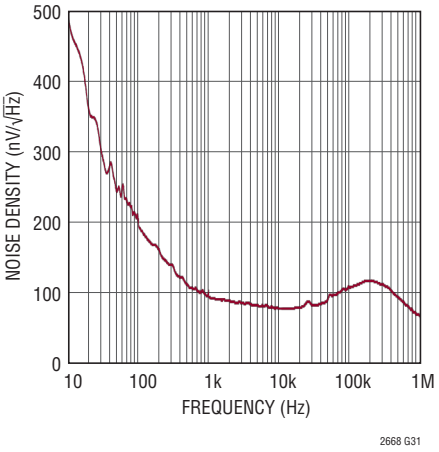
OVP, AVP: 5V
V+, V–: ±15V
0V TO 10V RANGE
INTERNAL REFERENCE
CREF, CREFCOMP: 0.1µF

SUBJECT CHANNEL: VOUT0
AGGRESSOR CHANNEL:
VOUT1 10V TO 0V STEP
VOUT1 RISING IS SIMILAR OR BETTER
ALL CHANNELS ARE SIMILAR OR BETTER

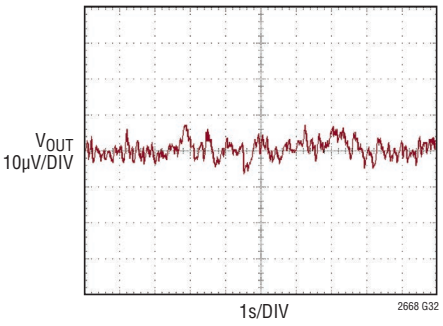
Large Signal Response



Noise Density vs Frequency

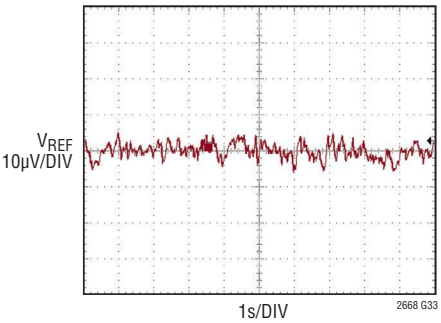


Output 0.1Hz to 10Hz Voltage Noise



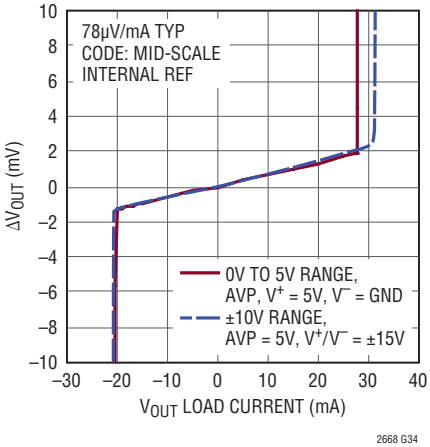
AVP = 5V, V+, V– = ±15V
0V TO 5V RANGE
CODE = MID-SCALE
INTERNAL REFERENCE
CREF = CREFCOMP = 0.1µF

Reference 0.1Hz to 10Hz Voltage Noise



AVP = 5V, V+, V– = ±15V
VREF = 2.5V
CREF = CREFCOMP = 0.1µF

Load Regulation



PIN FUNCTIONS

MSP2 (Pin 1): MSPAN Bit 2. Tie this pin to AVP or GND to select the power-on span and power-on-reset code for all 16 channels (see Table 4).

V_{OUT0} to V_{OUT15} (Pins 2-9, 23-30): DAC Analog Voltage Outputs.

V^+ (Pins 10, 31): Analog Positive Supply. Typically 15V; 4.5V to 15.75V range. Bypass to GND with a 1µF capacitor.

V^- (Pins 11, 32, 41): Analog Negative Supply. Typically –15V; –4.5V to –15.75V range, or can be tied to GND. Bypass to GND with a 1µF capacitor unless V^- is connected to GND.

MUX (Pin 12): Analog Multiplexer Output. Any of the 16 DAC outputs can be internally routed to the MUX pin. When the mux is disabled, this pin becomes high impedance.

REFLO (Pins 13, 35): Reference Low Pins. Signal ground for all DAC channels and internal reference. These pins should be tied to GND.

GND (Pins 14, 37): Analog Ground. Tie to a clean analog ground plane.

$\overline{\text{LDAC}}$ (Pin 15): Active-low Asynchronous DAC Update Pin. If $\overline{\text{CS}}$/LD is high, a falling edge on $\overline{\text{LDAC}}$ immediately updates all DAC registers with the contents of the input registers (similar to a software update). If $\overline{\text{CS}}$/LD is low when $\overline{\text{LDAC}}$ goes low, the DAC registers are updated after $\overline{\text{CS}}$/LD returns high. A low on the $\overline{\text{LDAC}}$ pin powers up the DACs. A software power-down command is ignored if $\overline{\text{LDAC}}$ is low. Logic levels are determined by OVP.

Tie $\overline{\text{LDAC}}$ high (to OVP) if not used. Updates can then be performed through SPI commands (see Table 1).

$\overline{\text{CS}}$/LD (Pin 16): Serial Interface Chip Select/Load Input. When $\overline{\text{CS}}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{\text{CS}}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed. Logic levels are determined by OVP.

SCK (Pin 17): Serial Interface Clock Input. Logic levels are determined by OVP.

SDO (Pin 18): Serial Interface Data Output. The serial output of the 32-bit shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. Can be used for data echo readback or daisy-chain operation (pull-up/down resistor required). The SDO pin becomes high impedance when $\overline{\text{CS}}$/LD is high. Logic levels are determined by OVP.

SDI (Pin 19): Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2668 accepts input word lengths of either 24 or 32 bits. Logic levels are determined by OVP.

TGP (Pin 20): Asynchronous Toggle Pin. A falling edge updates the DAC register with data from input register A. A rising edge updates the DAC register with data from input register B. Toggle operations only affect those DAC channels with their toggle select bit (Tx) set to 1. Tie the TGP pin to OVP if toggle operations are to be done through software. Tie the TGP pin to GND if not using toggle operations. Logic levels are determined by OVP.

$\overline{\text{CLR}}$ (Pin 21): Active-low Asynchronous Clear Input. A logic low at this level-triggered input clears the part to the reset code and range determined by the hardwired option chosen using the MSPAN pins and specified in Table 4. The control registers are cleared to zero. Logic levels are determined by OVP.

OVP (Pin 22): Digital Input/Output Supply Voltage. $1.71V \leq OVP \leq AVP + 0.3V$. Bypass to GND with a 0.1µF capacitor.

REF (Pin 33): Reference In/Out. The voltage at the REF pin sets the full-scale range of all channels. By default, the internal reference is routed to this pin. Must be buffered when driving external DC load currents. If the reference is disabled (see Reference Modes in the Operation section), its output is disconnected and the REF pin becomes a high impedance input to which you may apply a precision external reference. For low noise and reference stability, tie a capacitor from this pin to GND. The value must be $\leq C_{REFCOMP}$, where $C_{REFCOMP}$ is the capacitance tied to the REFCOMP pin. The allowable external reference input voltage range is 0.5V to $V_{AVP} – 1.75V$.

PIN FUNCTIONS

REFCOMP (Pin 34): Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1µF capacitor to GND. Tying REFCOMP to GND causes the part to power up with the internal reference disabled, allowing the use of an external reference at start-up.

AVP (Pin 36): Analog Supply Voltage Input. 4.5V ≤ AVP ≤ 5.5V. Bypass to GND with a 1µF capacitor.

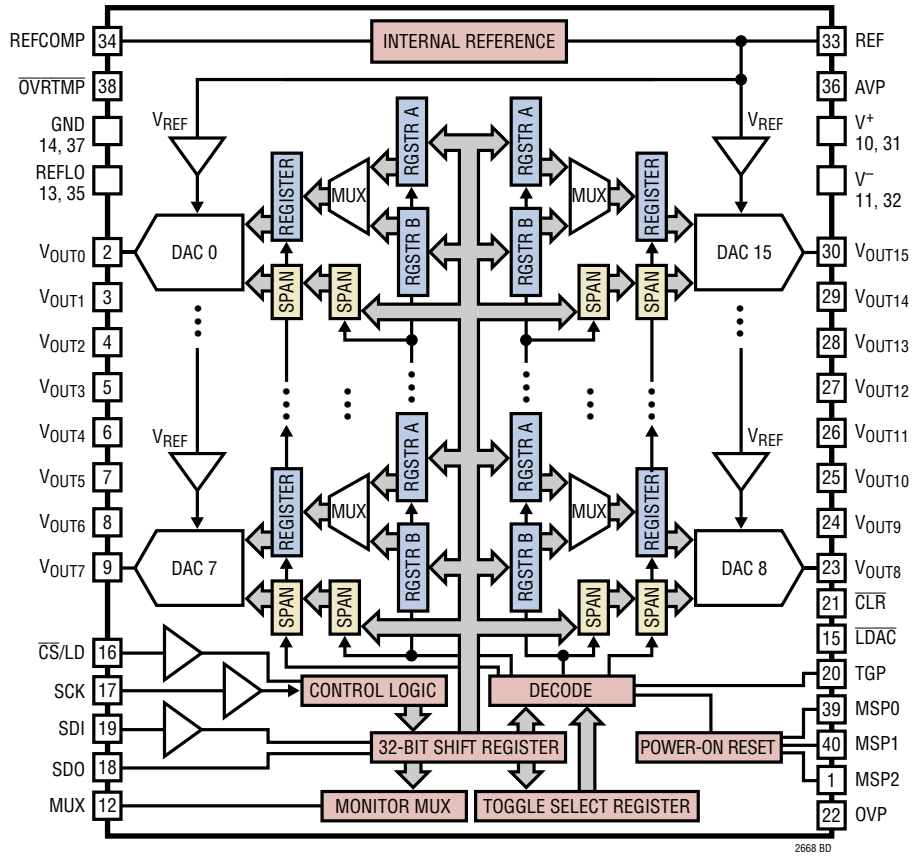
$\overline{\text{OVRTMP}}$ (Pin 38): Thermal Protection Interrupt Pin. This open-drain N-channel output pulls low when chip temperature exceeds 160°C. This pin is released on the next $\overline{\text{CS}}$/LD rising edge. A pull-up resistor is required.

MSP0 (Pin 39): MSPAN Bit 0. Tie this pin to AVP or GND to select the power-on span and power-on-reset code for all 16 channels (see Table 4).

MSP1 (Pin 40): MSPAN Bit 1. Tie this pin to AVP or GND to select the power-on span and power-on-reset code for all 16 channels (see Table 4).

Exposed Pad (Pin 41): Analog Negative Supply (V^-). Must be soldered to PCB.

BLOCK DIAGRAM



TIMING DIAGRAM

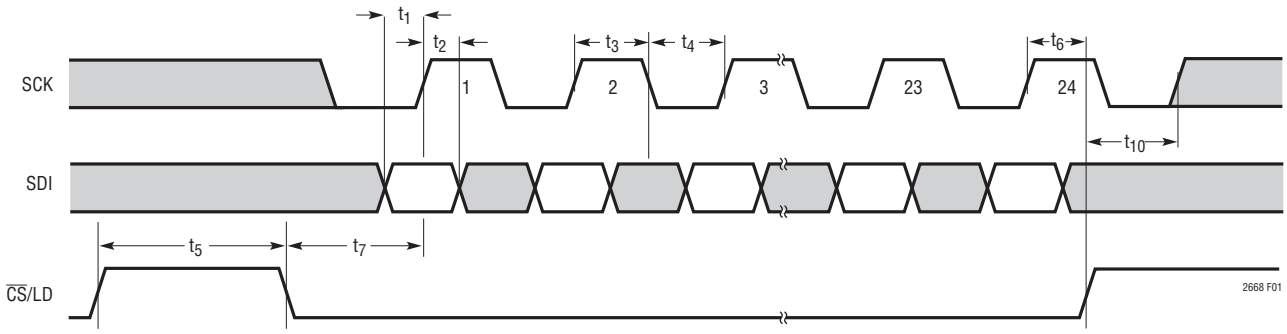


Figure 1. Serial Interface Timing

OPERATION

The LTC2668 is a family of 16-channel, ±10V digital-to-analog converters with selectable output ranges and an integrated precision reference. The DACs operate on positive 5V and bipolar ±15V supplies. The bipolar supplies can operate as low as ±4.5V, and need not be symmetrical. In addition, the negative V^- supply can be operated at ground, making the parts compatible with single-supply systems. The outputs are driven by the bipolar supply rails.

The output amplifiers offer true rail-to-rail operation. When drawing a load current from the V^+ or V^- rail, the output voltage headroom with respect to that rail is limited by the 60Ω typical channel resistance of the output devices. See the graph, Headroom at Rails vs Output Current, in the Typical Performance Characteristics section.

The LTC2668 is controlled using a cascadable 3-wire SPI/Microwire-compatible interface with echo readback.

Power-On Reset

The outputs reset when power is first applied, making system initialization consistent and repeatable. By tying the MSPAN pins (MSP2, MSP1, MSP0) to GND and/or AVP, you can select the initial output range and reset code (zero- or mid-scale), as well as selecting between a manual (fixed) range and SoftSpan operation. See Table 4 for pin configurations and available options.

Power Supply Sequencing and Start-Up

The supplies (AVP, OVP, V^+ and V^-) may be powered up in any convenient order.

If an external reference is used, the voltage at REF should be kept within the range $-0.3V \le V_{REF} \le AVP + 0.3V$ (see the Absolute Maximum Ratings section). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences when the voltage at AVP is in transition.

Supply bypassing is critical to achieving the best possible performance. We recommend at least 1µF to ground on AVP, V^+ and V^- supplies, and at least 0.1µF of low ESR capacitance for each supply, as close to the device as possible. The larger capacitor may be omitted for OVP.

Hot-plugging or hard switching of supplies is not recommended, as power supply cable or trace inductances combined with bypass capacitances can cause supply voltage transients beyond absolute maximum ratings, even if the bench supply has been carefully current-/voltage-limited. During start-up, limit the supply inrush currents to no more than 5A and supply slew rates to no more than 5V/µs. Internal protection circuitry can be damaged and long-term reliability adversely affected if these requirements are not met.

OPERATION

Table 1. Command Codes

COMMAND				
C3	C2	C1	C0	
0	0	0	0	Write Code to *n*
1	0	0	0	Write Code to *All*
0	1	1	0	Write Span to *n*
1	1	1	0	Write Span to *All*
0	0	0	1	Update *n* (Power Up)
1	0	0	1	Update *All* (Power Up)
0	0	1	1	Write Code to *n*, Update *n* (Power Up)
0	0	1	0	Write Code to *n*, Update *All* (Power Up)
1	0	1	0	Write Code to *All*, Update *All* (Power Up)
0	1	0	0	Power Down *n*
0	1	0	1	Power Down Chip (All DACs, Mux and Reference)
1	0	1	1	Monitor Mux
1	1	0	0	Toggle Select
1	1	0	1	Global Toggle
0	1	1	1	Config
1	1	1	1	No Operation

Table 2. DAC Addresses, *n*

ADDRESS				
A3	A2	A1	A0	
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4
0	1	0	1	DAC 5
0	1	1	0	DAC 6
0	1	1	1	DAC 7
1	0	0	0	DAC 8
1	0	0	1	DAC 9
1	0	1	0	DAC 10
1	0	1	1	DAC 11
1	1	0	0	DAC 12
1	1	0	1	DAC 13
1	1	1	0	DAC 14
1	1	1	1	DAC 15

Data Transfer Functions

The DAC input-to-output transfer functions for all output ranges and resolutions are shown in Figures 2a and 2b. The input code is in straight binary format for all ranges.

Serial Interface

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The 4-bit command, C3-C0, is loaded first, followed by the 4-bit DAC address, A3-A0, and finally the 16-bit data word in straight binary format. For the LTC2668-16, the data word comprises the 16-bit input code, ordered MSB-to-LSB. For the LTC2668-12, the data word comprises the 12-bit input code, ordered MSB-to-LSB, followed by four don't-care bits. Data can only be transferred to the LTC2668 when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 3a.

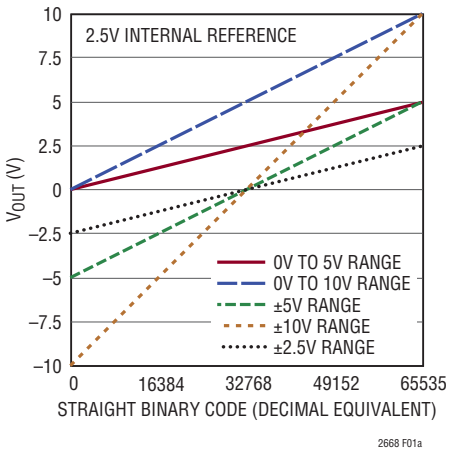


Figure 2a. LTC2668-16 Transfer Function

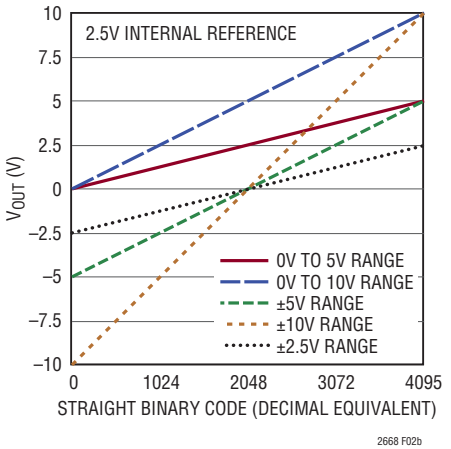
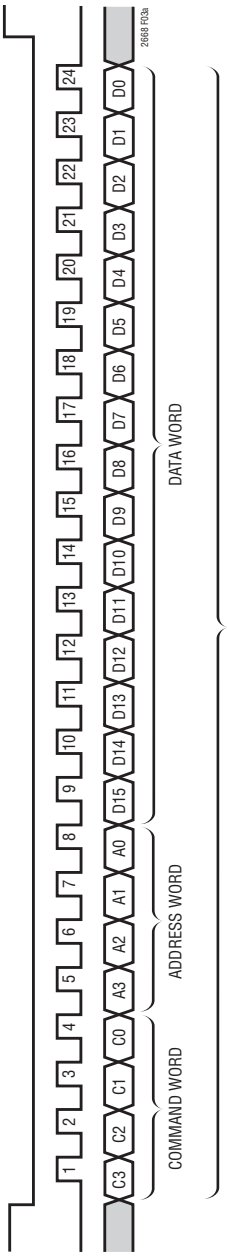
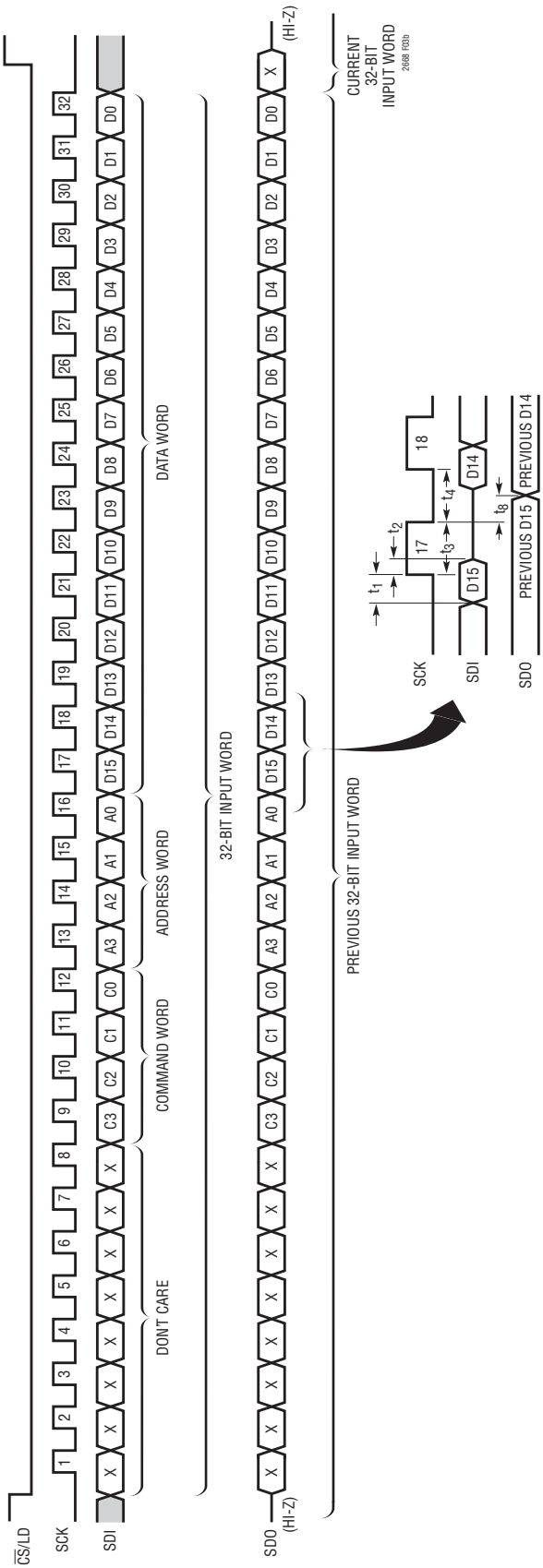


Figure 2b. LTC2668-12 Transfer Function

OPERATION



3a. LTC2668-16 24-Bit Load Sequence (Minimum Input Word). LTC2668-12 SDI Data Word Is 12-Bit Input Code + 4 Don't-Care Bits



3b. LTC2668-16 32-Bit Load Sequence. LTC2668-12 SDI/SDO Data Word Is 12-Bit Input Code + 4 Don't-Care Bits

Figure 3. LTC2668 Load Sequences

OPERATION

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits must be transferred to the device first, followed by the 24-bit word, as just described. Figure 3b shows the 32-bit sequence. The 32-bit word is required for echo readback and daisy-chain operation, and is also available to accommodate processors that have a minimum word width of 16 or more bits.

Input and DAC Registers

The LTC2668 has five internal registers for each DAC, in addition to the main shift register (see the Block Diagram). Each DAC channel has two sets of double-buffered registers: one set for the code data, and one set for the span (output range) of the DAC. Double buffering provides the capability to simultaneously update the span and code, which allows smooth voltage transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an input register and a DAC register:

- **Input Register:** The write operation shifts data from the SDI pin into a chosen input register. The input registers are holding buffers; write operations do not affect the DAC outputs.

  In the code data path, there are two input registers, A and B, for each DAC register. Register B is an alternate input register used only in the toggle operation, while register A is the default input register (see the Block Diagram).

- **DAC Register:** The update operation copies the contents of an input register to its associated DAC register. The content of a DAC register directly controls the DAC output voltage or range. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

  Note that updates always refresh both code and span data, but the values held in the DAC registers remain unchanged unless the associated input register values have been changed via a write operation. For example, if you write a new code and update the channel, the code is updated, while the span is refreshed unchanged. A channel update can come from a serial update command, an $\overline{LDAC}$ negative pulse, or a toggle operation.

Table 3. Write Span Code

S2	S1	S0	OUTPUT RANGE	
			INTERNAL REFERENCE	EXTERNAL REFERENCE
0	0	0	0V TO 5V	0V to $2V_{REF}$
0	0	1	0V to 10V	0V to $4V_{REF}$
0	1	0	±5V	$\pm 2V_{REF}$
0	1	1	±10V	$\pm 4V_{REF}$
1	0	0	±2.5V	$\pm V_{REF}$

Output Ranges

The LTC2668 is a 16-channel DAC with selectable output ranges. Ranges can either be programmed in software or hardwired through pin strapping.

SoftSpan Operation

SoftSpan operation (ranges controlled through the serial interface) is invoked by tying all three MSPAN pins (MSP2, MSP1 and MSP0) to AVP (see Table 4). In SoftSpan configuration, all channels initialize to zero-scale in 0V to 5V range at power-on. The range and code of each channel are then fully programmable.

Each channel has a set of double-buffered registers for range information (see the Block Diagram). Program the span input register using the *Write Span n* or *Write Span All* commands (0110b and 1110b, respectively). Figure 4 shows the syntax, and Table 3 shows the span codes and ranges.

As with the double-buffered code registers, update operations copy the span input registers to the associated span DAC registers.

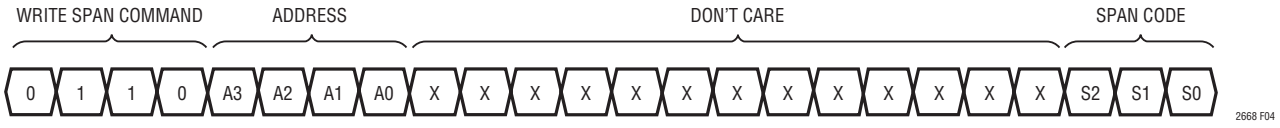


Figure 4. Write Span Syntax

OPERATION

Manual Span Operation

Multiple output ranges are not needed in all applications. By tying the MSPAN pins (MSP2, MSP1 and MSP0) to GND and/or AVP, any output range can be hardware-configured without additional operational overhead. Zero-scale and mid-scale reset options are also available for the unipolar modes (see Table 4).

Table 4. MSPAN Pin Configurations

MSP2	MSP1	MSP0	OUTPUT RANGE	RESET CODE	MANUAL SPAN	SOFT-SPAN
0	0	0	±10V	Mid-Scale	X	
0	0	AVP	±5V	Mid-Scale	X	
0	AVP	0	±2.5V	Mid-Scale	X	
0	AVP	AVP	0V to 10V	Zero-Scale	X	
AVP	0	0	0V to 10V	Mid-Scale	X	
AVP	0	AVP	0V to 5V	Zero-Scale	X	
AVP	AVP	0	0V to 5V	Mid-Scale	X	
AVP	AVP	AVP	0V to 5V	Zero-Scale		X

Monitor Mux

The LTC2668 includes a high voltage multiplexer (mux) for surveying the channel outputs.

The MUX pin is intended for use with high impedance inputs only; the output impedance of the multiplexer is 2.2kΩ. Continuous DC output current at the MUX pin must be limited to ±1mA to avoid damaging internal circuits.

The output voltage range of the multiplexer is from V^- to $V^+ – 1.4V$. The output is disabled (high impedance) at power-up.

The syntax and codes for the *Mux* command are shown in Figure 5 and Table 5.

Table 5. Monitor Mux Control Codes

M4	M3	M2	M1	M0	MUX PIN OUTPUT
0	0	0	0	0	Disabled (Hi-Z)
1	0	0	0	0	V_{OUT0}
1	0	0	0	1	V_{OUT1}
1	0	0	1	0	V_{OUT2}
1	0	0	1	1	V_{OUT3}
1	0	1	0	0	V_{OUT4}
1	0	1	0	1	V_{OUT5}
1	0	1	1	0	V_{OUT6}
1	0	1	1	1	V_{OUT7}
1	1	0	0	0	V_{OUT8}
1	1	0	0	1	V_{OUT9}
1	1	0	1	0	V_{OUT10}
1	1	0	1	1	V_{OUT11}
1	1	1	0	0	V_{OUT12}
1	1	1	0	1	V_{OUT13}
1	1	1	1	0	V_{OUT14}
1	1	1	1	1	V_{OUT15}

Toggle Operations

Some systems require that DAC outputs switch repetitively between two voltage levels. Examples include introducing a small AC bias, or independently switching between 'on' and 'off' states. The LTC2668 toggle function facilitates these kinds of operations by providing two input registers (A and B) per DAC channel.

Toggling between A and B is controlled by three signals. The first of these is the toggle select command, which acts on a data field of 16 bits, each of which controls a single channel (see Figure 6). The second is the global toggle command, which controls all selected channels using the global toggle bit TGB (see Figure 7). Finally, the TGP pin

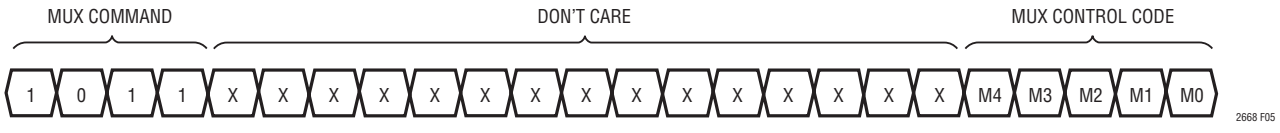


Figure 5. Mux Command

OPERATION

allows the use of an external clock or logic signal to toggle the DAC outputs between A and B. The signals from these controls are combined as shown in Figure 8.

If the toggle function is not needed, tie TGP (Pin 20) to ground and leave the toggle select register in its power-on reset state (cleared to zero). Input registers A then function as the sole input registers, and registers B are not used.

Toggle Select Register (TSR)

The Toggle Select command (1100b) syntax is shown in Figure 6. Each bit in the 16-bit TSR data field controls the DAC channel of the same name: T0 controls channel 0, T1 channel 1,…, and Tx controls channel x.

The toggle select bits (T0, T1,..., T15) have a dual function. First, each toggle select bit controls which input register (A or B) receives data from a write-code operation. When the toggle select bit of a given channel is high, write-code operations are directed to input register B of the addressed channel. When the bit is low, write-code operations are directed to input register A.

Secondly, each toggle select bit enables the corresponding channel for a toggle operation.

Writing to Input Registers A and B

Having chosen channels to toggle, write the desired codes to Input registers A for the chosen channels; then set the channels' toggle select bits using the toggle select command; and finally, write the desired codes to input registers B. Once these steps are completed, the channels are ready to toggle. For example, to set up channel 3 to toggle between codes 4096 and 4200:

1) Write code channel 3 (code = 4096) to register A
   00000011 00010000 00000000
2) Toggle Select (set bit T3)
   11000000 00000000 00001000
3) Write code channel 3 (code = 4200) to register B
   00000011 00010000 01101000

The Write code of step (3) is directed to register B because in step (2), bit T3 was set to 1. Channel 3 now has Input registers A and B holding the two desired codes, and is prepared for the toggle operation.

Toggling Between Registers A and B

Once Input registers A and B have been written to for all desired channels and the corresponding toggle select bits are set high, as in the previous example, the channels are ready for toggling.

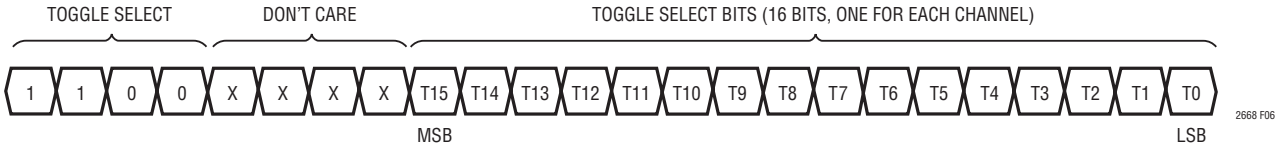


Figure 6. Toggle Select Syntax

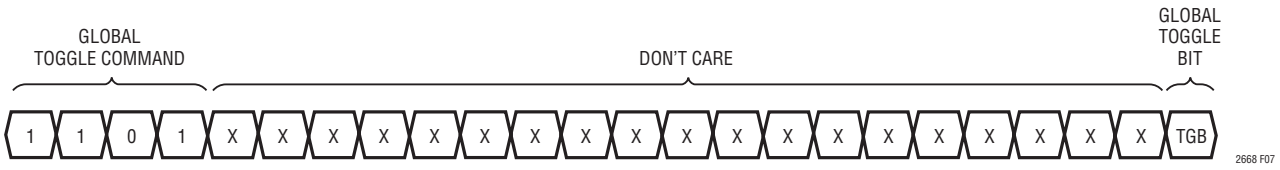


Figure 7. Global Toggle Syntax

OPERATION

The LTC2668 supports three types of toggle operations: a first in which all selected channels are toggled together using the SPI port; a second in which all selected channels are toggled together using an external clock or logic signal; and a third in which any combination of channels can be instructed to update from either input register A or B.

The internal toggle-update circuit is edge triggered, so only transitions (of TGB or TGP) trigger an update from the respective input register.

To toggle all selected channels together using the SPI port, ensure the TGP pin is high and that the bits in the toggle select register corresponding to the desired channels are also high. Use the global toggle command (1101b) to alternate codes, sequentially changing the global toggle bit TGB (see Figure 7). Changing TGB from 1 to 0 updates the DAC registers from their respective input registers A. Changing TGB from 0 to 1 updates the DAC registers from their respective input registers B. Note that in this way up to 16 channels may be toggled with just one serial command.

To toggle all selected channels using an external logic signal, ensure that the TGB bit in the global toggle register is high and that in the toggle select register, the bits corresponding to the desired channels are also high. Apply a clock or logic signal to the TGP pin to alternate codes. TGP falling edges update the DAC registers from their associated input registers A. TGP rising edges update the DAC registers from their associated input registers B. Note that once the input registers are set up, all toggling is triggered by the signal applied to the TGP pin, with no further SPI instructions needed.

To cause any combination of channels to update from either input register A or B, ensure the TGP pin is high and that the TGB bit in the global toggle register is also high. Using the toggle select command, set the toggle select bits as needed to select the input register (A or B) with which each channel is to be updated. Then update all channels, either by using the serial command (1001b) or by applying a negative pulse to the LDAC pin. Any channels whose toggle select bits are 0 update from input register

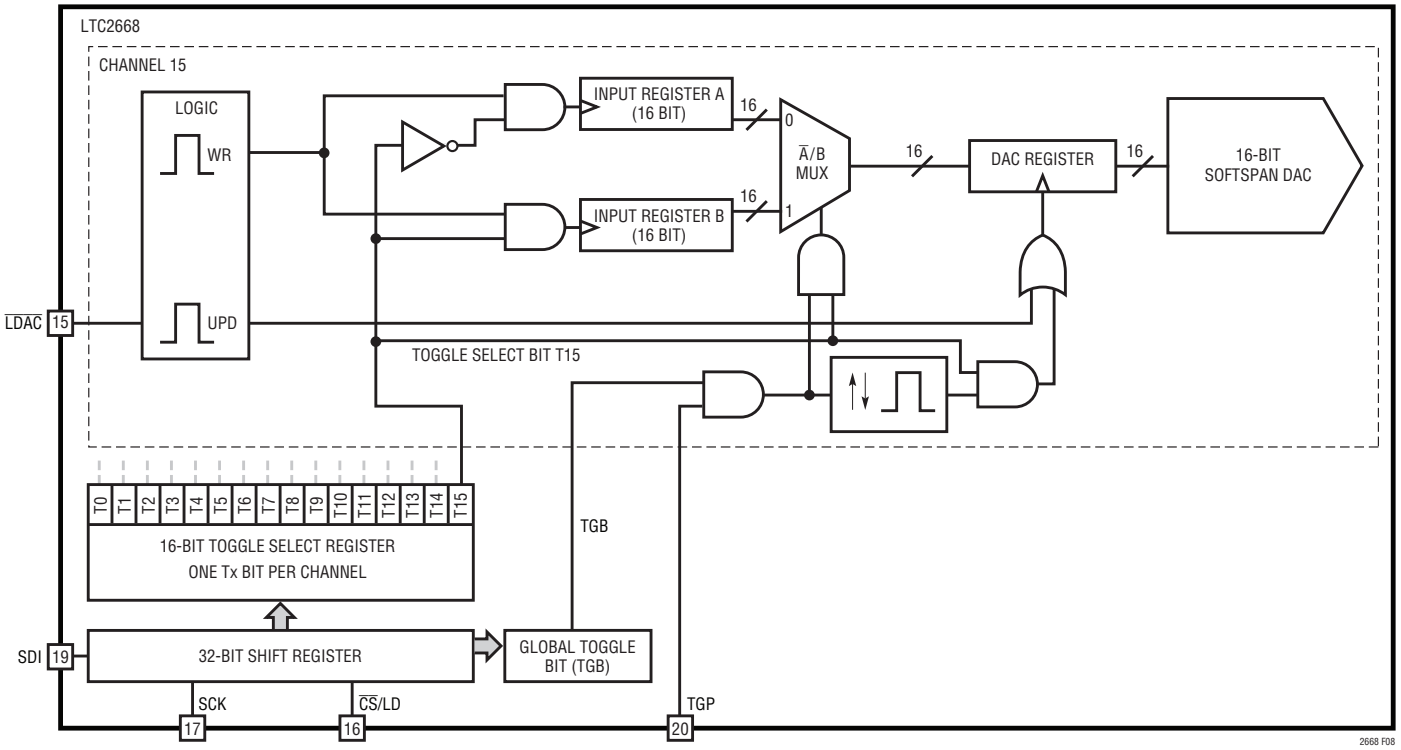


Figure 8. Simplified Toggle Block Diagram. Conceptual Only, Actual Circuit May Differ

OPERATION

A, while channels whose toggle select bits are 1 update from input register B (see Figure 8). By alternating toggle-select and update operations, up to 16 channels can be simultaneously switched to A or B as needed.

Daisy-Chain Operation

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge, suitable for clocking into the microprocessor on the next 32 SCK rising edges.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e., SCK, SDI and $\overline{CS}$/LD). Such a daisy-chain series is configured by connecting the SDO of each upstream device to the SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then, the concatenated input data is transferred to the chain, using the SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the *No-Operation* command (1111) for all other devices in the chain.

When $\overline{CS}$/LD is taken high, the SDO pin presents a high impedance output, so a pull-up resistor is required at the SDO of each device (except the last) for daisy-chain operation.

Echo Readback

The SDO pin can be used to verify data transfer to the device. During each 32-bit instruction cycle, SDO outputs the previous 32-bit instruction for verification.

When $\overline{CS}$/LD is high, SDO presents a high impedance output, releasing the bus for use by other SPI devices.

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than sixteen DAC outputs are needed. When in power-down, the output amplifiers and reference buffers are disabled. The DAC outputs are put into a high impedance state, and the output pins are passively pulled to ground through individual 42k (minimum) resistors. Register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address. In addition, all the DAC channels and the integrated reference together can be put into power-down mode using the *Power-Down Chip* command, 0101b. The 16-bit data word is ignored for all power-down commands.

Normal operation resumes by executing any command which includes a DAC update—either in software, as shown in Table 1, by taking the asynchronous $\overline{LDAC}$ pin low, or by toggling (see the Types of Toggle Operations section). The selected DAC is powered up as its voltage output is updated. When updating a powered-down DAC, add wait time to accommodate the extra power-up delay. If the channels have been powered down (command 0100b) prior to the update command, the power-up delay time is 30µs. If, on the other hand, the chip has been powered down (command 0101b), the power-up delay time is 35µs.

Asynchronous DAC Update Using $\overline{LDAC}$

In addition to the update commands shown in Table 1, the asynchronous, active-low $\overline{LDAC}$ pin updates all 16 DAC registers with the contents of the input registers.

If $\overline{CS}$/LD is high, a low on the $\overline{LDAC}$ pin causes all DAC registers to be updated with the contents of the input registers.

If $\overline{CS}$/LD is low, a low-going pulse on the $\overline{LDAC}$ pin before the rising edge of $\overline{CS}$/LD powers up all DAC outputs, but does not cause the outputs to be updated. If $\overline{LDAC}$ remains low after the rising edge of $\overline{CS}$/LD, then $\overline{LDAC}$ is recognized, the command specified in the 24-bit word is executed and the DAC outputs are updated.

OPERATION

The DAC outputs are powered up when $\overline{LDAC}$ is taken low, independent of the state of $\overline{CS}$/LD.

If $\overline{LDAC}$ is low at the time $\overline{CS}$/LD goes high, any software power-down command (power down *n*, power-down chip, config/select external reference) that was specified in the input word is inhibited.

Reference Modes

The LTC2668 has two reference modes (internal and external) with which the reference source can be selected. In either mode, the voltage at the REF pin and the output range settings determine the full-scale voltage of each of the channels.

The device has a precision 2.5V integrated reference with a typical temperature drift of 2ppm/°C. To use the internal reference, the REFCOMP pin should be left floating (no DC path to ground). In addition, the RD bit in the config register must have a value of 0. This value is reset to 0 at power-up, or it can be reset using the *Config* command, 0111b. Figure 9 shows the command syntax.

A buffer is needed if the internal reference is to drive external circuitry. For reference stability and low noise, a 0.1µF capacitor should be tied between REFCOMP and GND. In this configuration, the internal reference can drive up to 0.1µF with excellent stability. In order to ensure stable operation, the capacitive load on the REF pin should not exceed that on the REFCOMP pin.

To use an external reference, tie the REFCOMP pin to ground. This disables the output of the internal reference at start-up, so that the REF pin becomes a high impedance input. Apply the desired reference voltage at the REF pin after powering up, and set the RD bit to 1 using the *Config* command (0111b). This reduces AVP supply current by approximately 200µA.

The acceptable external reference voltage range is: $0.5V \le V_{REF} \le AVP - 1.75V$.

Integrated Reference Buffers

Each channel has its own integrated high performance reference buffer. The buffers have very high input impedance and do not load the reference voltage source. These buffers shield the reference voltage from glitches caused by DAC switching and, thus, minimize DAC-to-DAC dynamic crosstalk. Typically DAC-to-DAC crosstalk is less than 6nV•s (0V to 10V range). See the DAC-to-DAC Crosstalk graph in the Typical Performance Characteristics section.

Voltage Outputs

An amplifier's ability to maintain its rated voltage accuracy over a wide range of load conditions is characterized in its load regulation specification. The change in output voltage is measured per milliampere of forced load current change. Each of the LTC2668's high voltage, rail-to-rail output amplifiers has guaranteed load regulation when sourcing or sinking up to 10mA with supply headroom as low as 1.4V. Additionally, the amplifiers can drive up to ±14mA if available headroom is increased to 2.2V or more.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from µV/mA to ohms. The amplifier's DC output impedance is typically 0.08Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 60Ω typical channel resistance of the output devices—e.g., when sinking 1mA, the minimum output voltage (above V^-) is 60Ω • 1mA = 60mV. See the Headroom at Rails vs Output Current graphs in the Typical Performance Characteristics section.

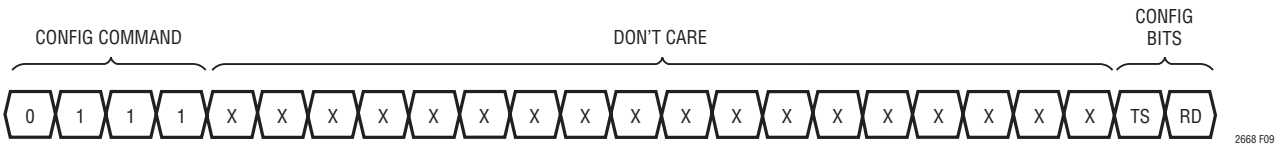


Figure 9. Config Command Syntax—Thermal Shutdown (TS) and Reference Disable (RD)

OPERATION

The amplifiers are stable driving capacitive loads of up to 1000pF.

Thermal Overload Protection

The LTC2668 protects itself if the die temperature exceeds 160°C. All channels power down, and the open-drain $\overline{\text{OVRTMP}}$ interrupt pin pulls low. The reference and bias circuits stay powered on. Once triggered, the device stays in shutdown even after the die cools.

The temperature of the die must fall to approximately 150°C before the channels can be returned to normal operation. Once the part has cooled sufficiently, the shutdown can be cleared with any valid update operation, including $\overline{\text{LDAC}}$ or a toggle operation. A $\overline{\text{CS}}$/LD rising edge releases the $\overline{\text{OVRTMP}}$ pin regardless of the die temperature.

Since the total load current of the device can easily exceed 100mA, die heating potential of the system design should be evaluated carefully. Grounded loads as low as 1k may be used and will not result in excessive heat.

Thermal protection can be disabled by using the *Config* command to set the TS bit (see Figure 9).

Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by minimizing common-mode resistance of signal and power grounds.

As with any high resolution converter, clean board grounding is important. A low impedance analog ground plane is necessary, as are star-grounding techniques. Keep the board layer used for star ground continuous to minimize ground resistances; that is, use the star-ground concept without using separate star traces. Resistance from the REFLO pin to the star point should be as low as possible.

For best performance, stitch the ground plane with arrays of vias on 150 to 200 mil centers connecting it with the ground pours from the other board layers. This reduces overall ground resistance and minimizes ground loop area.

Using LTC2668 in 5V Single-Supply Systems

LTC2668 can be used in single-supply systems simply by connecting the V^- pins to ground along with REFLO and GND, while V^+ and AVP are connected to a 5V supply. OVP can be connected to the 5V supply or to the logic supply voltage if lower than 5V.

With the internal reference, use the 0V to 5V output range. As with any rail-to-rail device, the output is limited to voltages within the supply range. Since the outputs of the device cannot go below ground, they may limit at the lowest codes, as shown in Figure 10b. Similarly, limiting can occur near full-scale if full-scale error (FSE = V_{OS} + GE) is positive, or if $V^+ < 2 \bullet V_{REF}$. See Figure 10c.

The multiplexer can be used and is fully functional. It can pull all the way to ground, but the upper headroom limitation means that it is useful for output voltages of 3.6V or below only (V^+ = 5V).

More flexibility can be afforded by using an external reference. For example, by using a 1.25V reference such as the LTC6655, we can now select between 0x to 2x and 0x to 4x ranges, which give full-scale voltages of 2.5V and 5V, respectively. Furthermore, the part can be configured for reset to zero- or mid-scale codes (see the Output Ranges section).

OPERATION

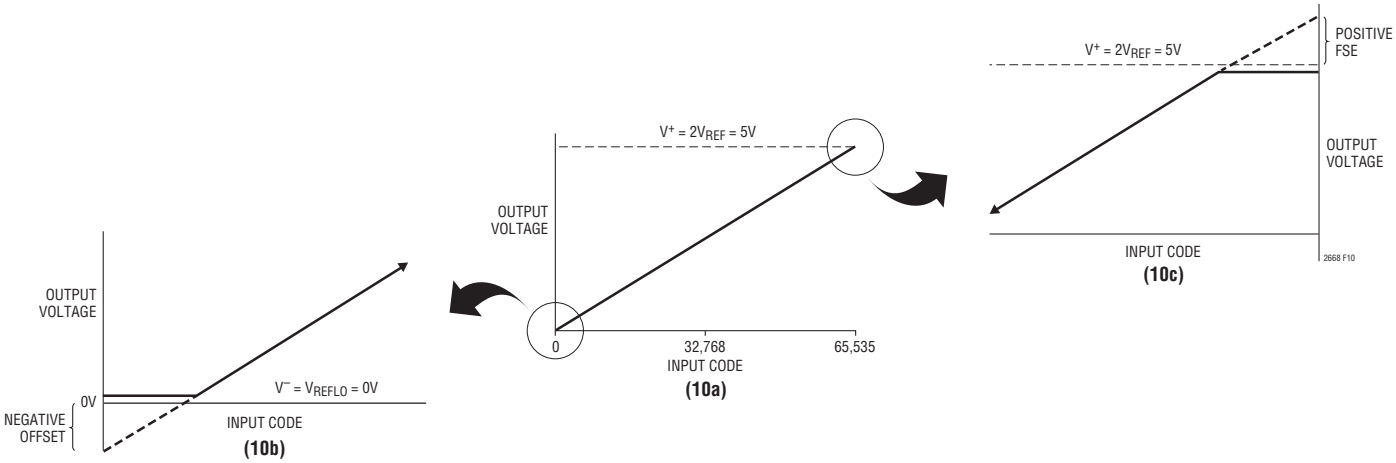
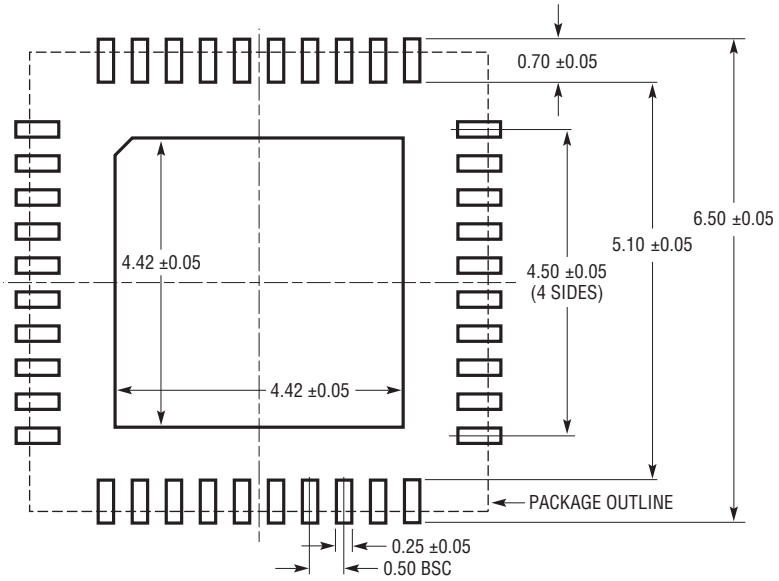


Figure 10. Effects of 0V to 5V Output Range for Single-Supply Operation. (10a) Overall Transfer Function (10b) Effect of Negative Offset for Codes Near Zero-Scale (10c) Effect of Positive Full-Scale Error for Codes Near Full-Scale

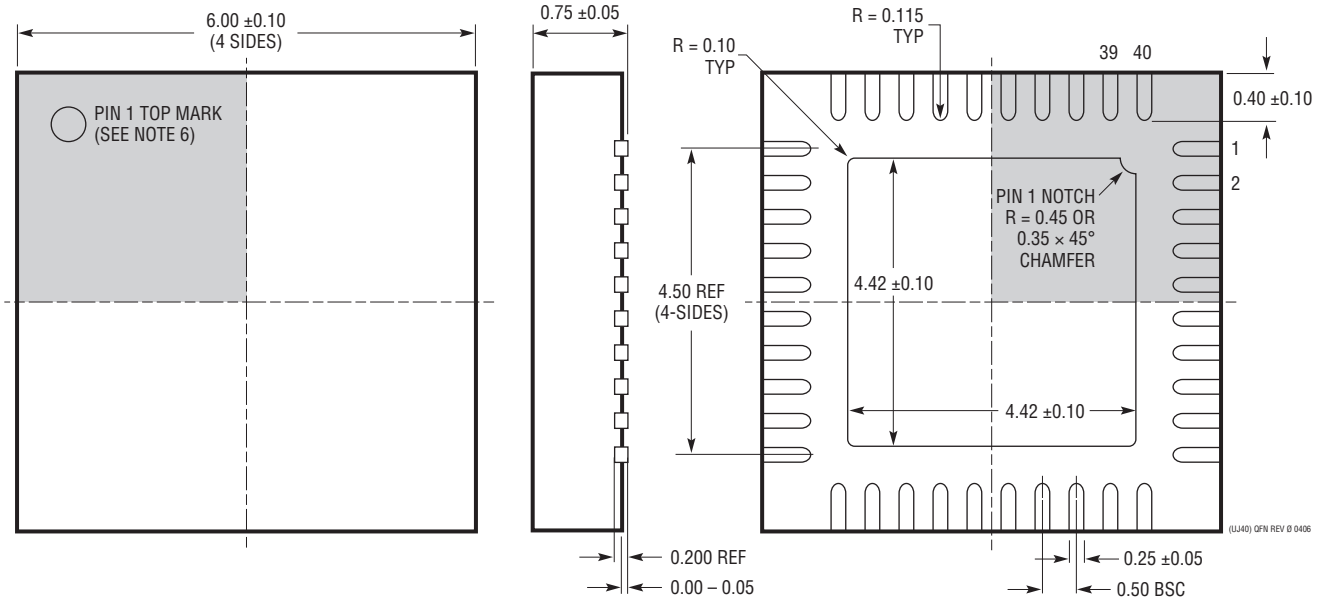
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

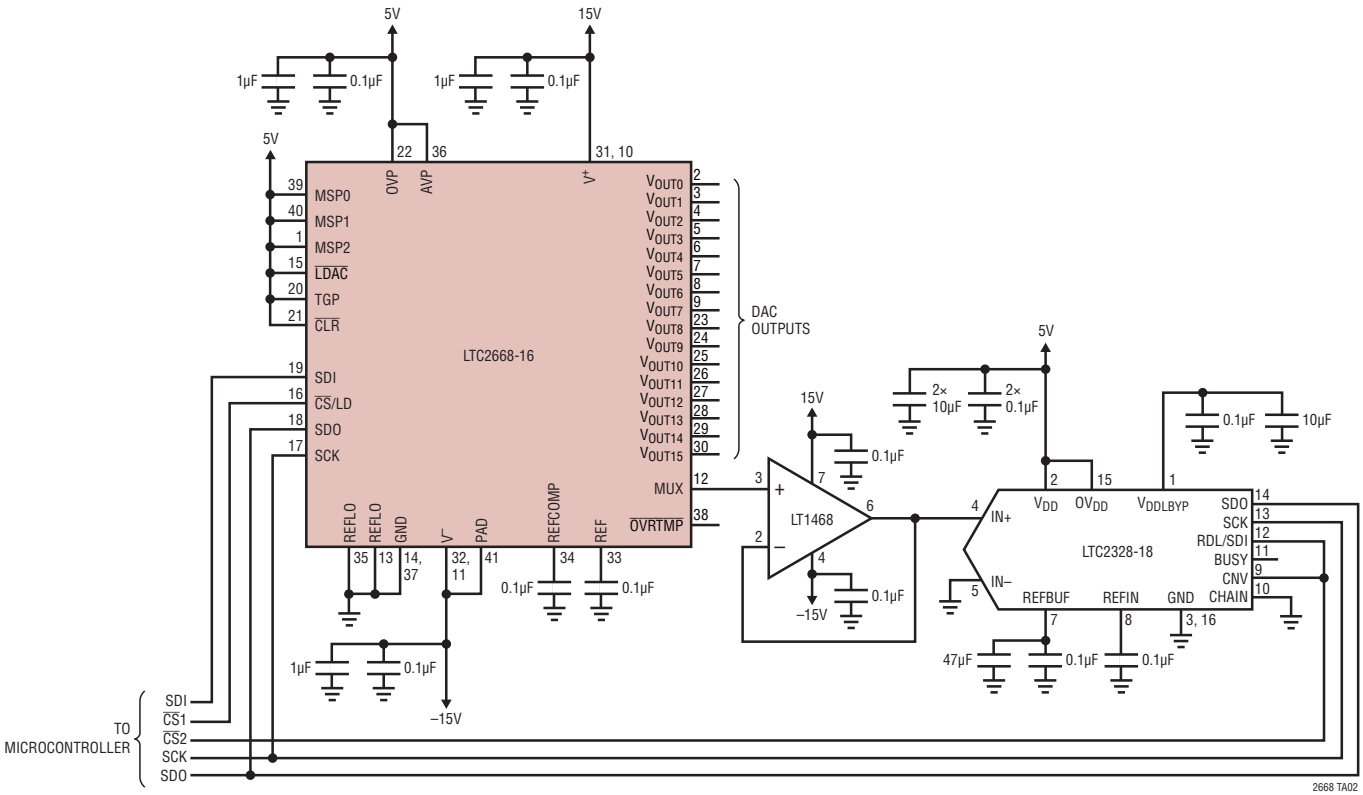
NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/15	Updated V^- and glitch impulse in the Electrical Characteristics section.	5
		Replaced Mid-Scale Glitch Impulse graph.	11
		Edited the Power Supply Sequencing and Start-Up section. Updated V_{OUT} output voltage swing conditions.	15
		Fixed AVP pin on schematic (pin 36).	28

TYPICAL APPLICATION

Using the Analog Multiplexer to Measure DAC Output Voltages Up to ±10.24V. Independent ADC Reference Cross-Checks LTC2668 Internal Reference



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2704	Quad Serial 16-/14-/12-Bit V_{OUT} SoftSpan DACs with ±2LSB INL, ±1LSB DNL	Software Programmable Output Ranges Up to ±10V, SPI Interface, No External Amps Needed
LTC2754	Quad Serial 16-/12-Bit I_{OUT} SoftSpan DACs with ±1LSB INL, ±1LSB DNL	Software Programmable Output Ranges Up to ±10V, SPI Interface, 7mm × 8mm QFN Package
LTC2656	Octal Serial 16-/12- Bit V_{OUT} DACs with Internal Reference	±10ppm/°C Internal Reference, 4mm × 5mm QFN Package
LTC2636	Octal 12-/10-/8-Bit SPI V_{OUT} DACs with Internal Reference	±10ppm/°C Internal Reference, 4mm × 3mm DFN and 16-Lead MSOP Packages
References		
LTC6655A	Low Drift Precision Buffered Reference	0.025% Max Tolerance, 2ppm/°C Max, 0.25ppm$_{P-P}$ 0.1Hz to 10Hz Noise

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- Excess Inventory Management