THE DATASHEET OF

LT4363HMS-2#PBF

High Voltage Surge Stopper with Current Limit

FEATURES

- **Withstands Surges Over 100V with V_{CC} Clamp**
- **Wide Operating Voltage Range: 4V to 80V**
- **Adjustable Output Clamp Voltage**
- **Fast Overcurrent Limit: Less Than 5µs**
- **Reverse Input Protection to –60V**
- Adjustable UV/OV Comparator Thresholds
- Low 7µA Shutdown Current
- Shutdown Pin Withstands –60V to 100V
- Adjustable Fault Timer
- Controls N-Channel MOSFET
- Less Than 1% Retry Duty Cycle During Faults, LT4363-2
- Available in 12-Pin (4mm × 3mm) DFN, 12-Pin MSOP and 16-Pin SO Packages

APPLICATIONS

- Avionic/Industrial Surge Protection
- Hot Swap™/Live Insertion
- High Side Switch for Battery Powered Systems
- Intrinsic Safety Applications

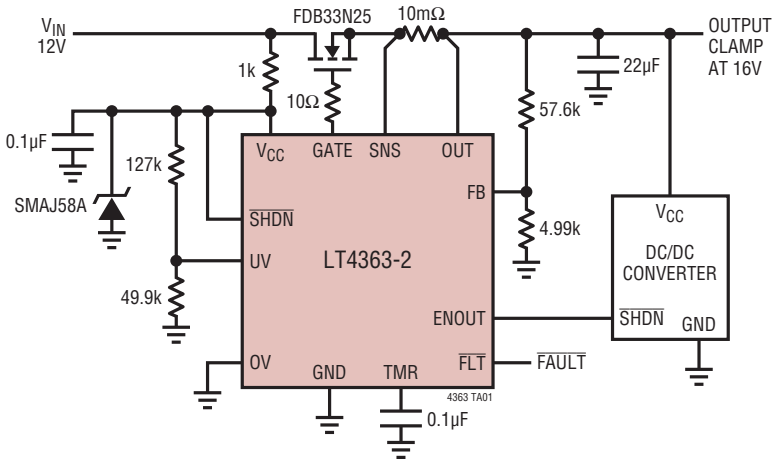
DESCRIPTION

The LT®4363 surge stopper protects loads from high voltage transients. It regulates the output during an overvoltage event, by controlling the gate of an external N-channel MOSFET. The output is limited to a safe value allowing the loads to continue functioning. The LT4363 also monitors the voltage drop between the SNS and OUT pins to protect against overcurrent faults. An internal amplifier limits the voltage across the current sense resistor to 50mV. In either fault condition, a timer is started inversely proportional to MOSFET stress. Before the timer expires, the $\overline{FLT}$ pin pulls low to warn of an impending power down. If the condition persists, the MOSFET is turned off. The LT4363-1 remains off until reset whereas the LT4363-2 restarts after a cool down period.

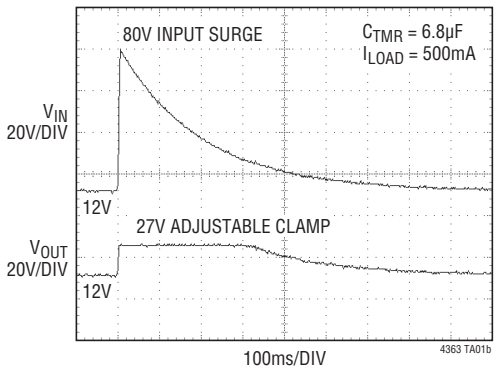
Two precision comparators can monitor the input supply for overvoltage (OV) and undervoltage (UV) conditions. When the potential is below the UV threshold, the external MOSFET is kept off. If the input supply voltage is above the OV threshold, the MOSFET is not allowed to turn back on. Back-to-back MOSFETs can be used in lieu of a Schottky diode for reverse input protection, reducing voltage drop and power loss. A shutdown pin reduces the quiescent current to less than 7µA during shutdown.

TYPICAL APPLICATION

4A, 12V Overvoltage Output Regulator with 150V Surge Protection



Overvoltage Protector Regulates Output at 27V During Transient



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

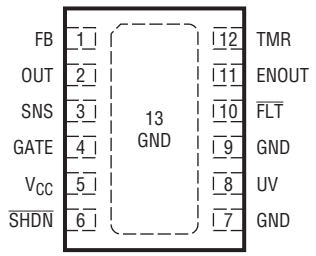
V_{CC}, $\overline{SHDN}$, UV, OV ..... –60V to 100V
SNS, OUT ..... –0.3V to 100V
SNS to OUT ..... –30V to 30V
GATE (Note 3) ..... –0.3V to SNS + 10V
ENOUT, $\overline{FLT}$ ..... –0.3V to 100V
FB ..... –0.3V to 5.5V
TMR 0.5mA

Operating Temperature Range
LT4363C ..... 0°C to 70°C
LT4363I ..... –40°C to 85°C
LT4363H ..... –40°C to 125°C
LT4363MP ..... –55°C to 125°C
Storage Temperature Range
DE12 ..... –65°C to 125°C
MS, SO ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS, SO ..... 300°C

PIN CONFIGURATION

LT4363-1

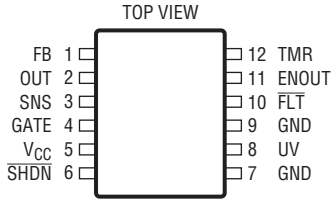
TOP VIEW



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, CONNECTION TO PCB OPTIONAL

LT4363-1

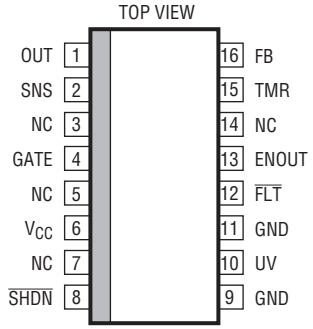
TOP VIEW



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 135°C/W

LT4363-1

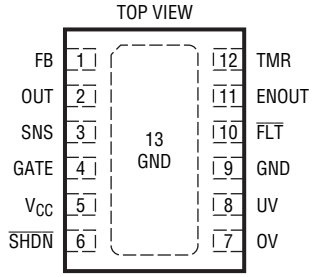
TOP VIEW



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 80°C/W

LT4363-2

TOP VIEW



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
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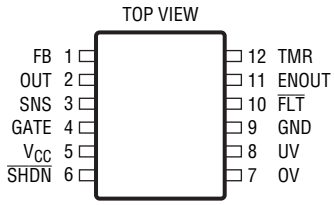
EXPOSED PAD (PIN 13) IS GND, CONNECTION TO PCB OPTIONAL

LT4363-2

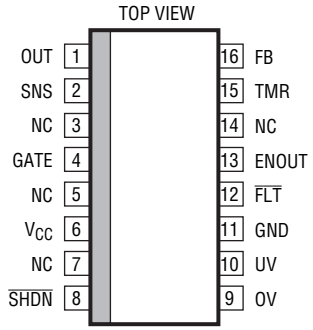
TOP VIEW



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 135°C/W

LT4363-2

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 80°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4363CDE-1#PBF	LT4363CDE-1#TRPBF	43631	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LT4363IDE-1#PBF	LT4363IDE-1#TRPBF	43631	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LT4363HDE-1#PBF	LT4363HDE-1#TRPBF	43631	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT4363CDE-2#PBF	LT4363CDE-2#TRPBF	43632	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LT4363IDE-2#PBF	LT4363IDE-2#TRPBF	43632	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LT4363HDE-2#PBF	LT4363HDE-2#TRPBF	43632	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT4363CMS-1#PBF	LT4363CMS-1#TRPBF	43631	12-Lead Plastic MSOP	0°C to 70°C
LT4363HMS-1#PBF	LT4363HMS-1#TRPBF	43631	12-Lead Plastic MSOP	–40°C to 125°C
LT4363IMS-1#PBF	LT4363IMS-1#TRPBF	43631	12-Lead Plastic MSOP	–40°C to 85°C
LT4363MPMS-1#PBF	LT4363MPMS-1#TRPBF	43631	12-Lead Plastic MSOP	–55°C to 125°C
LT4363CMS-2#PBF	LT4363CMS-2#TRPBF	43632	12-Lead Plastic MSOP	0°C to 70°C
LT4363HMS-2#PBF	LT4363HMS-2#TRPBF	43632	12-Lead Plastic MSOP	–40°C to 125°C
LT4363IMS-2#PBF	LT4363IMS-2#TRPBF	43632	12-Lead Plastic MSOP	–40°C to 85°C
LT4363MPMS-2#PBF	LT4363MPMS-2#TRPBF	43632	12-Lead Plastic MSOP	–55°C to 125°C
LT4363CS-1#PBF	LT4363CS-1#TRPBF	LT4363S-1	16-Lead Plastic SO	0°C to 70°C
LT4363HS-1#PBF	LT4363HS-1#TRPBF	LT4363S-1	16-Lead Plastic SO	–40°C to 125°C
LT4363IS-1#PBF	LT4363IS-1#TRPBF	LT4363S-1	16-Lead Plastic SO	–40°C to 85°C
LT4363MPS-1#PBF	LT4363MPS-1#TRPBF	LT4363S-1	16-Lead Plastic SO	–55°C to 125°C
LT4363CS-2#PBF	LT4363CS-2#TRPBF	LT4363S-2	16-Lead Plastic SO	0°C to 70°C
LT4363HS-2#PBF	LT4363HS-2#TRPBF	LT4363S-2	16-Lead Plastic SO	–40°C to 125°C
LT4363IS-2#PBF	LT4363IS-2#TRPBF	LT4363S-2	16-Lead Plastic SO	–40°C to 85°C
LT4363MPS-2#PBF	LT4363MPS-2#TRPBF	LT4363S-2	16-Lead Plastic SO	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: https://www.analog.com/en/about-adi/quality-reliability/material-declarations.html
For more information on tape and reel specifications, go to: https://www.analog.com/media/en/package-pcb-resources/package/tape-reel-rev-o.pdf

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Operating Voltage Range	LT4363	●	4		80	V
I_{CC}	V_{CC} Supply Current	$\overline{SHDN}$ Open, OUT = SNS = 12V $\overline{SHDN}$ = 0V, OUT = SNS = 0V	● ●		0.7 7	1.2 20 40	mA µA µA
I_R	Reverse Input Current	V_{CC} = –60V, $\overline{SHDN}$, UV, OV Open V_{CC} = $\overline{SHDN}$ = UV = OV = –60V	● ●		–0.5 –3	–4 –10	mA mA
ΔV_{GATE}	GATE Drive	ΔV_{GATE} = (GATE – SNS); V_{CC} = OUT V_{CC} = 4V; I_{GATE} = –0.5µA, 0µA 9V ≤ V_{CC} ≤ 80V; I_{GATE} = –1µA, 0µA	 ● ●	 4.5 10	 13	 16	 V V
$I_{GATE(UP)}$	GATE Pull-Up Current	V_{CC} = GATE = OUT = 12V V_{CC} = GATE = OUT = 48V	● ●	–15 –20	–30 –40	–45 –65	µA µA
$I_{GATE(DN)}$	GATE Pull-Down Current	Overvoltage: FB = 1.5V, GATE = 12V, OUT = 5V Overcurrent: ΔV_{SNS} = 150mV, V_{GATE} = 10V, OUT = 0V Shutdown/UV Mode: $\overline{SHDN}$ = 0V, GATE = 10V UV = 1V, GATE = 10V	● ● ● ●	75 50 50 200	150 100 1000 1000	 	mA mA µA µA
V_{FB}	FB Servo Voltage	GATE = 12V; OUT = 8V	●	1.25	1.275	1.3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{FB}	FB Input Current	V_{FB} = 1.275V	●		±0.2	±1	µA
ΔV_{SNS}	Current Limit Sense Voltage ΔV_{SNS} = (SNS – OUT)	V_{CC} = 12V, OUT = 3V to 12V V_{CC} = 48V, OUT = 3V to 48V	● ●	45 48	50 53	55 58	mV mV
	Current Limit Foldback	V_{CC} = 12V, OUT = 0V to 1V V_{CC} = 48V, OUT = 0V to 1V	● ●	15 16	25 27	35 36	mV mV
I_{SNS}	SNS Input Current	OUT = SNS = 3V to 80V OUT = SNS = 0V	● ●		20 –10	40 –15	µA µA
I_{TMR}	TMR Pull-up Current, Overvoltage	TMR = 1V, FB = 1.5V, ΔV_{DS} = 0.5V TMR = 1V, FB = 1.5V, ΔV_{DS} = 75V	● ●	–1.7 –42	–4 –50	–6 –58	µA µA
	TMR Pull-up Current, OV Warning	TMR = 1.325V, FB = 1.5V, ΔV_{DS} = 0.5V	●	–3	–5	–7	µA
	TMR Pull-up Current, Overcurrent	TMR = 1V, ΔV_{SNS} = 100mV, ΔV_{DS} = 0.5V TMR = 1V, ΔV_{SNS} = 100mV, ΔV_{DS} = 80V	● ●	–5 –190	–9 –250	–13 –310	µA µA
	TMR Pull-up Current, Cool Down	TMR = 3V, FB = 1.5V, ΔV_{SNS} = 0V, ΔV_{DS} = 0V	●	–1	–2.3	–3.5	µA
	TMR Pin Pull-down Current, Cool Down	V_{TMR} = 3V, FB = 1.5V, ΔV_{SNS} = 0V, ΔV_{DS} = 0V	●	1	2	4	µA
$V_{TMR(F)}$ $V_{TMR(G)}$ $V_{TMR(R)}$	TMR Fault Threshold TMR Gate Off Threshold TMR Restart Threshold	TMR Rising TMR Rising TMR Falling, LT4363-2	● ● ●	1.235 1.335 0.47	1.275 1.375 0.5	1.31 1.41 0.53	V V V
ΔV_{TMR}	Early Warning Window	$V_{TMR(G)} – V_{TMR(F)}$	●	80	100	120	mV
$V_{TMR(H)}$	TMR Cool Down High Threshold	V_{CC} = 7V to 80V, TMR Rising	●	3.5	4.3	5.4	V
V_{UV}	UV Input Threshold	UV Rising	●	1.24	1.275	1.31	V
$V_{UV(HYST)}$	UV Input Hysteresis				12		mV
V_{OV}	OV Input Threshold	OV Rising	●	1.24	1.275	1.31	V
$V_{OV(HYST)}$	OV Input Hysteresis				7.5		mV
I_{IN}	UV, OV Input Current	UV = 1.275V UV = –60V	● ●		±0.2 –1	±1 –2	µA mA
I_{LEAK}	$\overline{FLT}$, ENOUT Leakage Current	$\overline{FLT}$, ENOUT = 80V	●		±0.5	±2.5	µA
V_{OL}	$\overline{FLT}$, ENOUT Output Low	I_{SINK} = 0.1mA I_{SINK} = 2mA	● ●		300 2	800 9	mV V
$\Delta V_{OUT(TH)}$	OUT High Threshold	$\Delta V_{OUT} = V_{CC} – V_{OUT}$, ENOUT From Low to High	●	0.25	0.5	0.75	V
$\Delta V_{OUT(RST)}$	OUT Reset Threshold	ENOUT From High to Low	●	1.8	2.7	3.6	V
I_{OUT}	OUT Input Current	V_{CC} = OUT = 12V, $\overline{SHDN}$ Open V_{CC} = OUT = 12V, $\overline{SHDN}$ = 0V	● ●		0.25 0.25	0.5 1	mA mA
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Threshold	V_{CC} = 4V to 80V	 ●	0.6 0.4	1.4	1.7 2.1	V V
$V_{\overline{SHDN}(Z)}$	$\overline{SHDN}$ Open Voltage	V_{CC} = 4V to 80V	●			2.2	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Current	$\overline{SHDN}$ = 0.4V	●	–1	–4	–8	µA
t_{RESET}	$\overline{SHDN}$ Reset Time	$\overline{SHDN} \le$ 0.4V; LT4363-1	●			100	µs
D	Retry Duty Cycle; Overvoltage	V_{CC} = 80V, OUT = 16V, FB = 1.5V; LT4363-2	●		1	2	%
	Retry Duty Cycle; Output Short	V_{CC} = 12V, OUT = 0V, ΔV_{SNS} = 100mV; LT4363-2	●		0.76	1	%
$t_{OFF(UV)}$	Undervoltage Turn Off Propagation Delay	UV Steps from 1.5V to 1V	●		2	5	µs
$t_{OFF(OV)}$	Overvoltage Turn Off Propagation Delay	FB Steps from 0V to 1.5V; OUT = 0V	●		0.25	1	µs
$t_{OFF(OC)}$	Overcurrent Turn Off Propagation Delay	ΔV_{SNS} Steps from 0V to 150mV; OUT = 0V	●		1	2.5	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

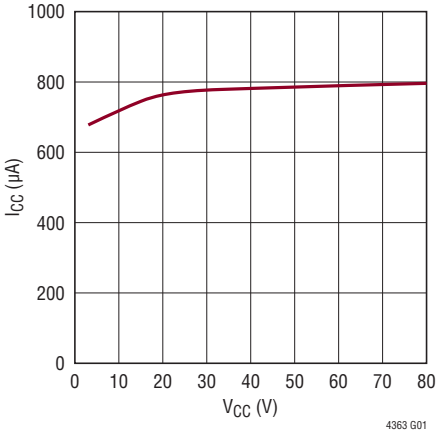
Note 2: All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a minimum of 10V above the OUT pin. Driving this pin to voltages beyond the clamp may damage the device.

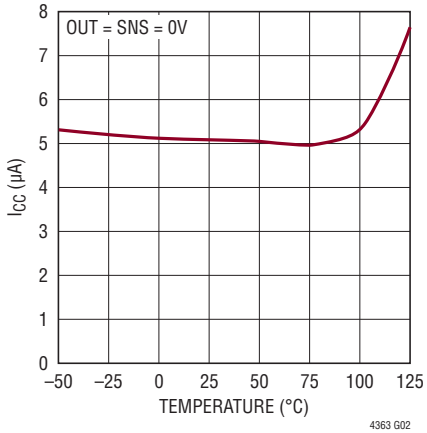
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at V_{CC} = 12V, T_A = 25°C, unless otherwise noted.

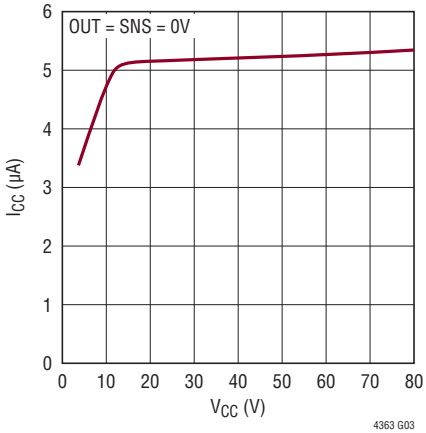
Supply Current vs Supply Voltage (I_{CC} vs V_{CC})



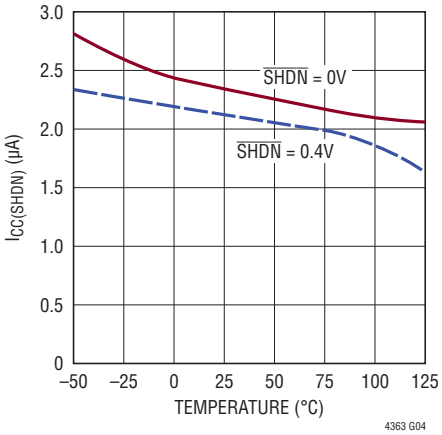
Supply Current During Shutdown vs Temperature ($I_{CC(SHDN)}$ vs Temperature)



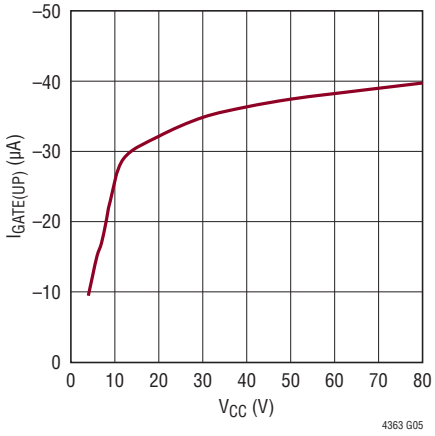
Supply Current During Shutdown vs Supply Voltage ($I_{CC(SHDN)}$ vs V_{CC})



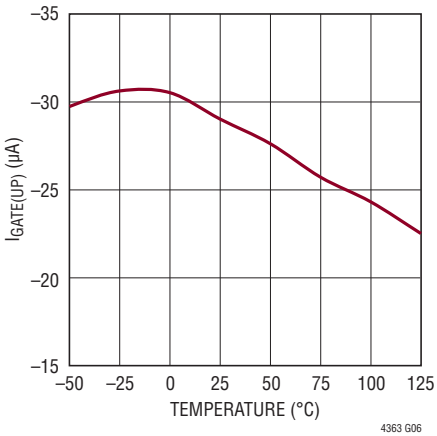
$\overline{SHDN}$ Current vs Temperature



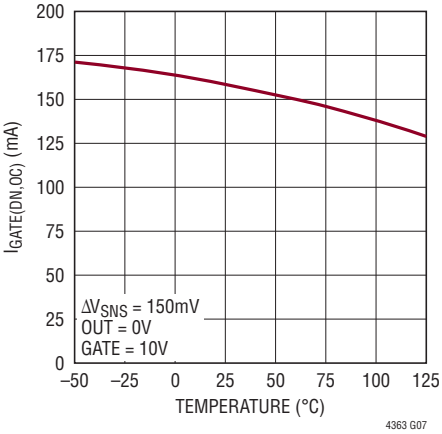
GATE Pull-Up Current vs V_{CC}



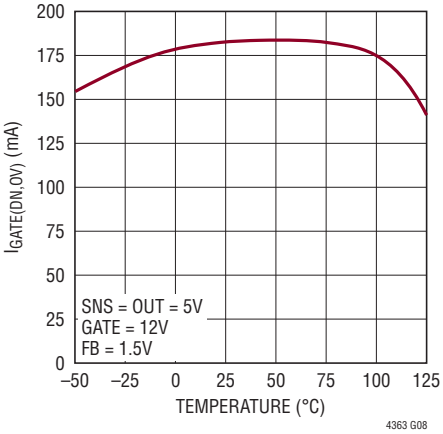
GATE Pull-Up Current vs Temperature



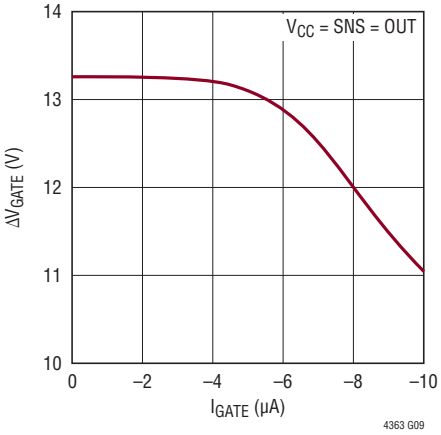
GATE Pull-Down Current vs Temperature: Overcurrent



GATE Pull-Down Current vs Temperature: Overvoltage



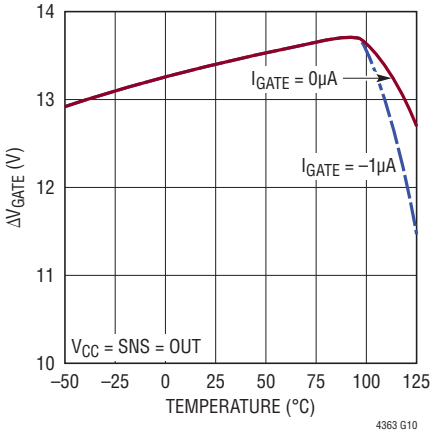
Gate Drive Voltage vs Gate Pull-Down Current ΔV_{GATE} vs I_{GATE}



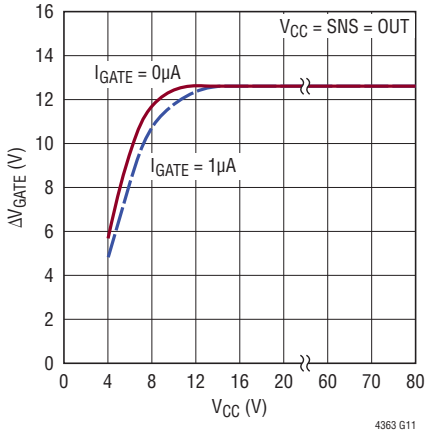
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at V_{CC} = 12V, T_A = 25°C, unless otherwise noted.

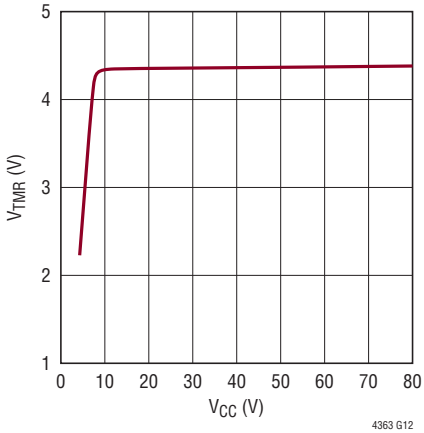
Gate Drive vs Temperature (ΔV_{GATE} vs Temperature)



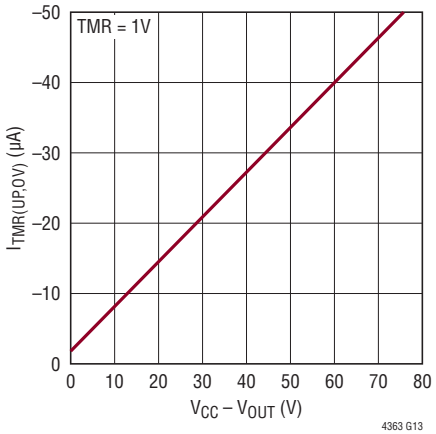
Gate Drive vs Supply Voltage (ΔV_{GATE} vs V_{CC})



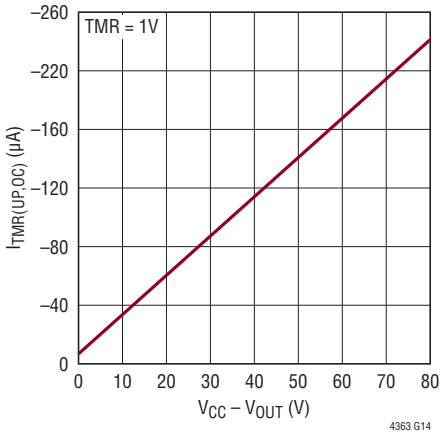
TMR High Threshold vs Supply Voltage



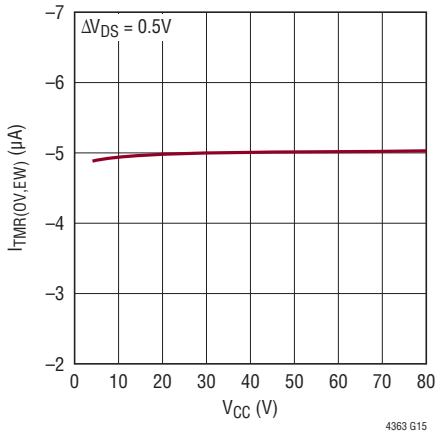
Overvoltage TMR Current vs (V_{CC} – V_{OUT})



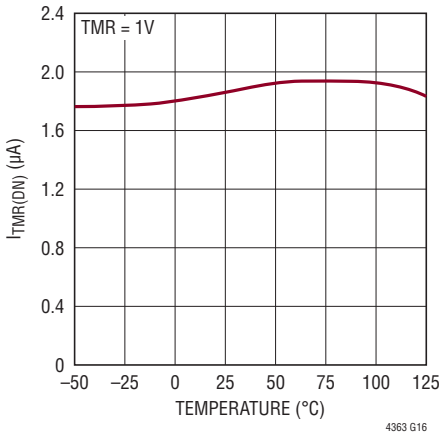
Overcurrent TMR Current vs (V_{CC} – V_{OUT})



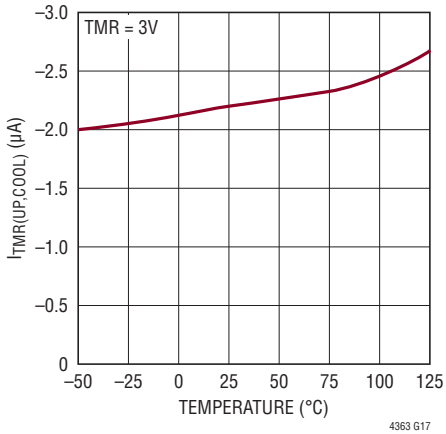
Warning Period TMR Current vs V_{CC}



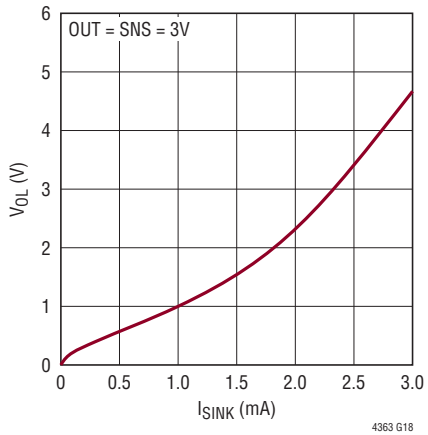
TMR Pull-Down Current vs Temperature



TMR Pull-Up Current (Cool Down) vs Temperature



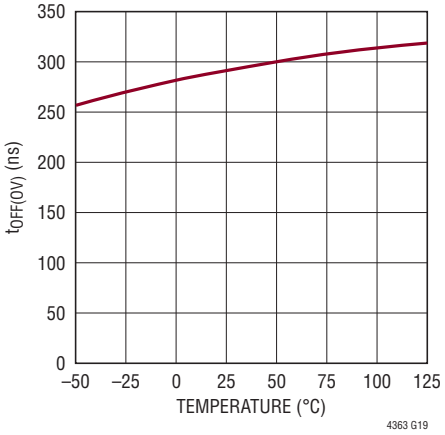
Output Low Voltage vs Current



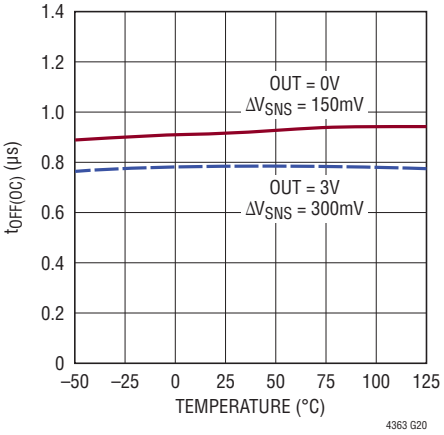
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at V_{CC} = 12V, T_A = 25°C, unless otherwise noted.

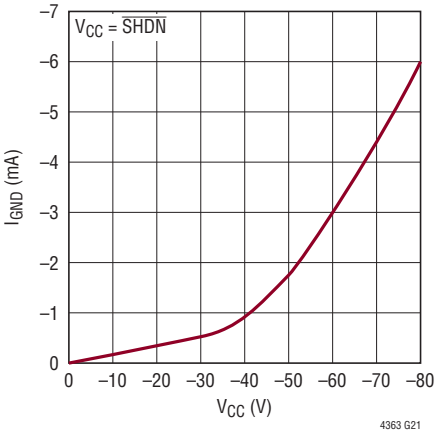
Overvoltage Turn-Off Time vs Temperature



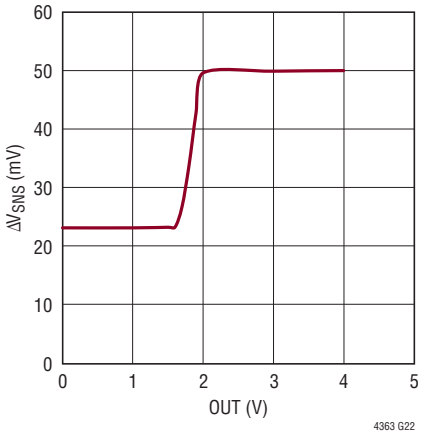
Overcurrent Turn-Off Time vs Temperature



Reverse Current vs Reverse Voltage



Current Limit Foldback (ΔV_{SNS} vs OUT)



PIN FUNCTIONS

ENOUT: Open Collector Enable Output. The ENOUT pin goes high impedance when the voltage at the OUT pin is within 0.5V of V_{CC} and 3V above GND, indicating the external MOSFET is fully on. The state of the pin is latched until the OUT pin voltage drops below 2V, resetting the latch. The internal NPN is capable of sinking up to 2mA of current.

Exposed Pad (DFN Package Only): Exposed pad may be left open or connected to device ground (GND).

FB: Voltage Regulator Feedback Input. Connect this pin to the center tap of the resistive divider connected between the OUT pin and ground. During an overvoltage condition, the GATE pin is controlled to maintain a 1.275V threshold at the FB pin. Connect to GND to disable the OV clamp.

$\overline{\text{FLT}}$: Open Collector Fault Output. This pin pulls low after the voltage at the TMR pin has reached the fault threshold of 1.275V. It indicates the pass transistor is about to turn off because either the supply voltage has stayed at an elevated level for an extended period of time (voltage fault) or the device is in an overcurrent condition (current fault). The internal NPN is capable of sinking up to 2mA of current.

GATE: N-Channel MOSFET Gate Drive Output. The GATE pin is pulled up by an internal charge pump current source to 13V above the OUT pin. A 14V protection clamp limits this voltage during faults. Both voltage and current amplifiers control the GATE pin to regulate the output voltage and limit the current through the MOSFET.

GND: Device Ground.

OUT: Output Voltage Sense Input. This pin senses the voltage at the source of the external N-channel MOSFET. The voltage difference between V_{CC} and OUT sets the fault timer current. When this difference drops below 0.5V, the EN pin goes high impedance.

OV (LT4363-2): Overvoltage Comparator Input. When OV is above its threshold of 1.275V, the fault retry function is inhibited even when the TMR pin voltage has reached its retry threshold. As soon as the voltage at OV pin falls below its lower threshold the GATE pin is allowed to turn back on. Connect to GND if unused.

$\overline{\text{SHDN}}$: Shutdown Control Input. The LT4363 can be shutdown to a low current mode by pulling the $\overline{\text{SHDN}}$ pin below the threshold of 0.4V. Pull this pin above 2.1V or disconnect it to allow the internal current source to turn the part back on. The leakage current to ground at the pin should be limited to no more than 1µA if no external pull up is used to turn the part on. The $\overline{\text{SHDN}}$ pin can be pulled up to 100V or below GND by 60V without damage.

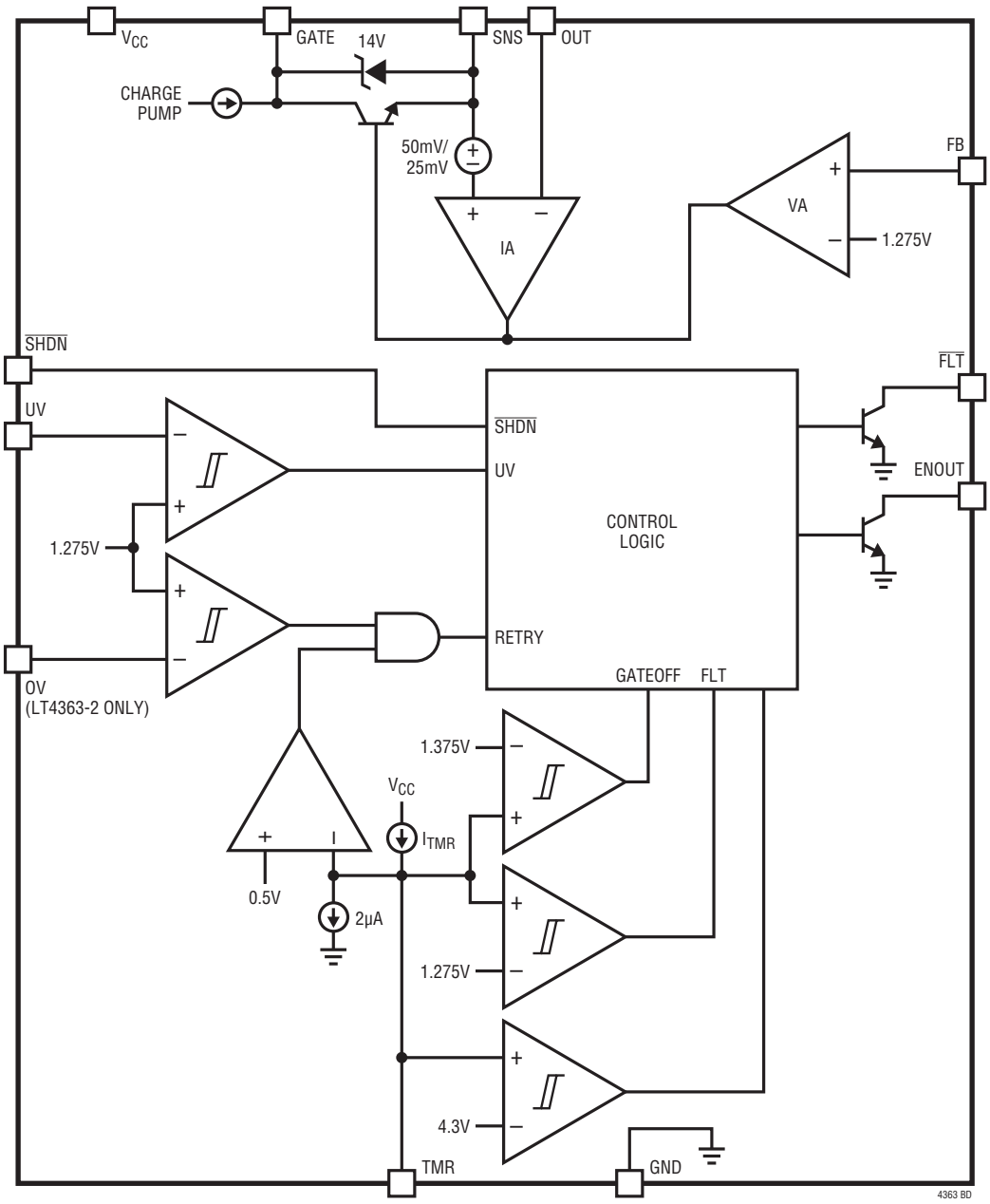
SNS: Current Sense Input. Connect this pin to the input of the current sense resistor. The current limit circuit controls the GATE pin to limit the sense voltage between SNS and OUT pins to 50mV. This is reduced to 25mV in a severe fault when OUT is below 2V. When in current limit mode, a current source charges up the TMR pin. The voltage difference with the OUT pin must be limited to less than 30V. Connect to OUT pin if unused.

TMR: Fault Timer Input. Connect a capacitor between this pin and ground to set the times for early fault warning, fault turn-off, and cool down periods. The current charging up this pin during fault conditions depends on the voltage difference between the V_{CC} and OUT pins. When TMR reaches 1.275V, the $\overline{\text{FLT}}$ pin pulls low to indicate the detection of a fault condition. If the condition persists, the pass transistor turns off when TMR reaches the threshold of 1.375V. A 2µA current source then continues to pull the TMR up. When TMR reaches 4.3V, the 2µA current reverses direction and starts to pull the TMR pin low. When TMR reaches the retry threshold of 0.5V, the GATE pin pulls high turning back on the pass transistor for the LT4363-2 version. The GATE pin latches low after fault time out for the LT4363-1. A minimum of 10nF capacitor is needed to compensate the loop.

UV: Undervoltage Comparator Input. When UV falls below its threshold of 1.275V, the GATE is pulled down with a 1mA current. When UV rises above 1.275V plus the hysteresis, the pull down current disappears and the GATE pin is pulled up by the internal charge pump. If unused, connect to V_{CC}.

V_{CC}: Positive Supply Voltage Input. The positive supply input ranges from 4V to 80V for normal operation. It can also be pulled below ground by up to 60V during a reverse battery condition, without damaging the part. Shutting down the LT4363 by pulling the $\overline{\text{SHDN}}$ pin to ground will reduce the supply current to 7µA.

BLOCK DIAGRAM



OPERATION

Some power systems must cope with high voltage surges of short duration such as those in vehicles. Load circuitry must be protected from these transients, yet high availability systems must continue operating during these events.

The LT4363 is an overvoltage protection regulator that drives an external N-channel MOSFET as the pass transistor. It operates from a wide supply voltage range of 4V to 80V. It can also be pulled below ground potential by up to 60V without damage. The internal charge pump turns on the N-channel MOSFET to supply current to the loads with very little power loss. Two MOSFETs can be connected back to back to replace an inline Schottky diode for reverse input protection. This improves the efficiency and increases the available supply voltage level to the load circuitry.

Normally, the pass transistor is fully on, powering the loads with very little voltage drop. When the supply voltage surges too high, the voltage amplifier (VA) controls the gate of the MOSFET and regulates the voltage at the OUT pin to a level that is set by the external resistive divider from the OUT pin to ground and the internal 1.275V reference. A current source starts charging up the capacitor connected at the TMR pin to ground. If the TMR voltage reaches 1.275V, the $\overline{FLT}$ pin pulls low to indicate impending turn-off due to the overvoltage condition. The pass transistor stays on until TMR reaches 1.375V, at which point the GATE pin pulls low turning off the MOSFET.

A current continues to pull the TMR pin up until it reaches about 4.3V, at which point the current reverses direction and pulls the TMR pin down. For the LT4363-2 version, when the voltage at the TMR pin reaches 0.5V the GATE pin begins rising, turning on the MOSFET. The $\overline{FLT}$ pin will then return to a high impedance state. For the latch-off version, LT4363-1, both the GATE and $\overline{FLT}$ pins remain low even after TMR has reached the 0.5V threshold. Allow sufficient time for TMR to discharge to 0.5V and for the MOSFET to cool before attempting to reset the part. To reset, pull the $\overline{SHDN}$ pin low for at least 100µs, then pull high with a slew rate of at least 10V/ms.

The fault timer allows the load to continue functioning during short transient events while protecting the MOSFET from being damaged by a long period of supply overvoltage. The timer period varies with the voltage across the MOSFET. A higher voltage corresponds to a shorter fault timer period, helping to keep the MOSFET within its safe operating area (SOA).

The LT4363 senses an overcurrent condition by monitoring the voltage across an optional sense resistor placed between the SNS and OUT pins. An active current limit circuit (IA) controls the GATE pin to limit the sense voltage to 50mV, if the OUT pin potential is above 2V. In the case of a severe output short that brings OUT below 2V, the servo sense voltage is reduced to 25mV to reduce the stress on the pass transistor. During current limit, the current charging the TMR capacitor is about 5 times the current during an overvoltage event. The $\overline{FLT}$ pin pulls low when the TMR voltage reaches 1.275V and the MOSFET is turned off when it reaches 1.375V. The MOSFET turns back on and the $\overline{FLT}$ pin returns to a high impedance state after TMR has reached the 0.5V threshold for the LT4363-2 version. For the latch-off version, LT4363-1, both the GATE and $\overline{FLT}$ pins remain low even after TMR has reached the 0.5V threshold. Reset the part in the same way as in overvoltage time-out case.

An accurate undervoltage comparator keeps the GATE pin low until the voltage at the UV pin is above the 1.275V threshold. An overvoltage comparator prevents the MOSFET from turning on after fault time-out while the voltage at the OV pin is still above 1.275V for the LT4363-2. The $\overline{SHDN}$ pin turns off the pass transistor and all the internal circuitry, reducing the supply current to a mere 7µA.

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The LT4363 limits the voltage and current delivered to the load during supply transient or output overload events. The total fault timer period is set to ride through short-duration faults, while longer events cause the output to shut off and protect the MOSFET pass device from damage. The MOSFET provides a low resistance path from the input to the load during normal operation, while in fault conditions it operates as a series regulator.

Overvoltage Fault

The LT4363 limits the voltage at the output during an overvoltage at the input. An internal amplifier regulates the GATE pin to maintain 1.275V at the FB pin. During this interval the MOSFET is on and supplies current to the load. This allows uninterrupted operation during short overvoltage events. If the overvoltage condition persists, the timer causes the MOSFET to turn off.

Overcurrent Fault

The LT4363 features and adjustable current limit that protects against output short circuits or excessive load current. During an overcurrent event, the GATE pin is regulated to limit the current sense voltage across the SNS and OUT pins to 50mV. In the case of a severe short at the output, where OUT is less than 2V, the current sense voltage is reduced to 25mV to further reduce power dissipation in the MOSFET. If the overcurrent condition persists, the timer causes the MOSFET to turn off.

Fault Timer Overview

Overvoltage and overcurrent conditions are limited in duration by an adjustable timer. A capacitor at the TMR pin sets the delay time before a fault condition is reported at the $\overline{FLT}$ pin as well as the overall delay before the MOSFET is turned off. The same capacitor also sets the cool down time before the MOSFET is allowed to turn back on.

When either an overvoltage or overcurrent fault condition occurs, a current source charges the TMR pin capacitor. The exact current level varies as a function of the type of fault and the V_{DS} voltage drop across the MOSFET. This scheme takes better advantage of the MOSFET's available Safe Operating Area (SOA) than would a fixed timer current.

The TMR pin is biased to 0.5V under normal operating conditions. In the presence of a fault the timer first charges to 1.275V, and then enters the early warning phase of operation. At this point the $\overline{FLT}$ pin pulls low and after charging to 1.375V, the timer shuts off the MOSFET. The warning phase is indicated by $\overline{FLT}$ low and gives time for the load to perform house-keeping chores such as data storage in anticipation of impending power loss. After faulting off, the timer enters the cool down phase. At the end of the cool down period the LT4363-1 remains off until reset, while the LT4363-2 automatically restarts. For the LT4363-2 retry is inhibited if the OV pin is greater than 1.275V. This prevents motorboating in the event there is a sustained input overvoltage condition.

Fault Timer Operation in Overvoltage

In the presence of an overvoltage condition when the LT4363 regulates the output voltage, the timer charges from 0.5V to 1.275V with a current that varies as a function of V_{DS} (see Figure 1). V_{DS} is inferred from the drop across V_{CC} and OUT. The timer current increases linearly from around 4µA with $V_{DS} \leq 0.5V$, to 50µA with $V_{DS} = 75V$. Because V_{DS} is measured indirectly, clamping or filtering at the V_{CC} pin affects the timer current response. A graph of Overvoltage TMR Current vs ($V_{CC} – V_{OUT}$) is shown in the Typical Performance Characteristics.

When TMR reaches 1.275V, the $\overline{FLT}$ pin is latched low as an early warning of impending shutdown. The timer current is cut to a fixed value of 6µA and continues to run until TMR reaches 1.375V, producing a fixed early warning period given by:

$$C_{TMR} = t_{WARNING} \bullet \frac{6\mu A}{100mV}$$

When TMR reaches 1.375V, the MOSFET is turned off and allowed to cool for an extended period. The total elapsed time between the onset of output regulation and turn-off is given by:

$$t_{REG} = C_{TMR} \bullet \left(\frac{0.775V}{I_{TMR}} + \frac{100mV}{6\mu A} \right)$$

Because I_{TMR} is a function of $V_{CC} – V_{OUT}$, the exact time in regulation depends upon the input waveform and the time required for the output voltage to come into regulation.

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Fault Timer Operation in Overcurrent

TMR pin behavior in overcurrent is substantially the same as in overvoltage. In the presence of an overcurrent condition when the LT4363 regulates the output current, the timer charges from 0.5V to 1.275V with a current that varies as a function of V_{DS} (see Figure 2). The current is about 5 times the value produced in overvoltage, under similar conditions V_{DS}, increasing linearly from 8µA with V_{DS} < 0.5V to 260µA with V_{DS} = 80V. V_{DS} is inferred from the drop across V_{CC} and OUT. Because V_{DS} is measured indirectly, clamping or filtering at the V_{CC} pin affects the timer current response. A graph of Overcurrent TMR Current vs (V_{CC} – V_{OUT}) is shown in the Typical Performance Characteristics.

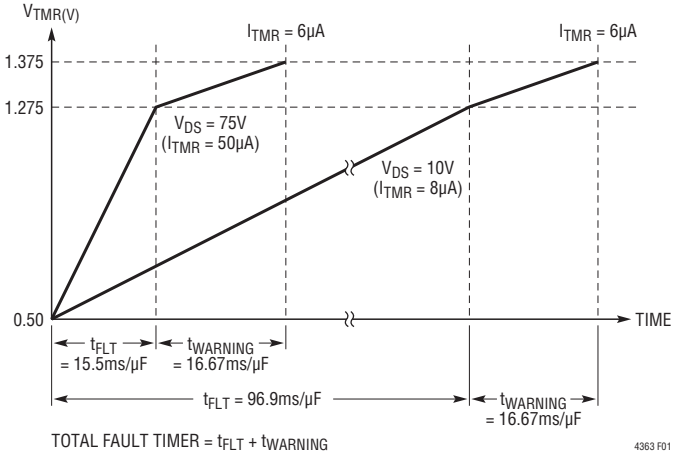

Figure 1. Overvoltage Fault Timer Current

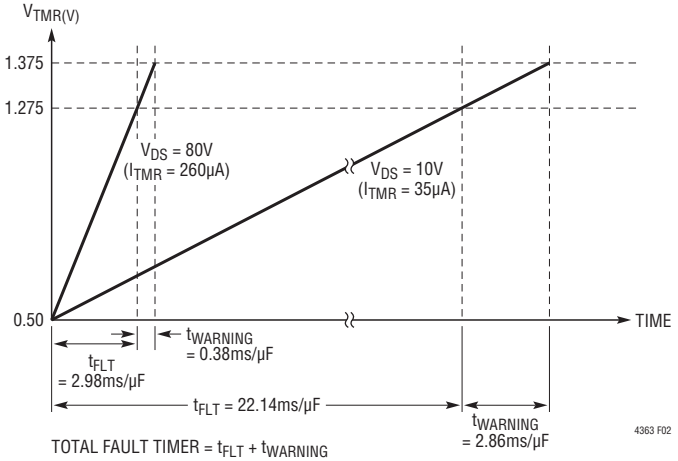

Figure 2. Overcurrent Fault Timer Current

When TMR reaches 1.275V, the $\overline{FLT}$ pin is latched low as an early warning of impending shutdown. But unlike the overvoltage case, the timer current is not reduced and instead continues unabated until TMR reaches 1.375V, producing an early warning period given by:

$$C_{TMR} = t_{WARNING} \bullet \frac{I_{TMR}}{100mV}$$

When TMR reaches 1.375V, the MOSFET is turned off and allowed to cool for an extended period. The total elapsed time between the onset of current limiting and turn-off is given by:

$$t_{LIM} = C_{TMR} \bullet \frac{0.875V}{I_{TMR}}$$

Because I_{TMR} is a function of V_{CC} – V_{OUT}, the exact time in current limit depends upon the input waveform and the time required for the output current to come into regulation.

Cool Down Phase

Cool Down behavior is the same whether initiated by overvoltage or overcurrent. During the cool down phase, the timer continues to charge from 1.375V to 4.3V with 2µA, and then discharges back down to 0.5V with 2µA, for a total equivalent voltage swing of 6.725V. The cool down time is given by:

$$t_{COOL} = C_{TMR} \bullet \frac{2.925V + 3.8V}{2\mu A}$$

Up to this point the operation of the LT4363-1 and LT4363-2 is the same. Behavior at the end of the cool down phase and in response to the $\overline{SHDN}$ pin is entirely different.

At the end of the cool down phase the LT4363-1 remains latched off and $\overline{FLT}$ remains low. It may be restarted by pulling the $\overline{SHDN}$ pin low for at least 100µs or by cycling power. The cool down phase may be interrupted at anytime by pulling $\overline{SHDN}$ low for at least 1s/µF of C_{TMR}; the LT4363-1 will restart when $\overline{SHDN}$ goes high.

The LT4363-2 will automatically retry at the end of the cool down phase. Retry is inhibited if the OV pin is above 1.275V; this prevents repetitive retries while the input is held in a sustained overvoltage condition. Retry is auto-

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matically initiated once the OV pin falls below 1.268V. OV has no effect on initial start-up when power is first applied and upon exiting shutdown. The cool down phase may be interrupted in the LT4363-2 by pulling $\overline{SHDN}$ low for at least 1s/µF of C_{TMR}.

For both the LT4363-1 and LT4363-2 the $\overline{FLT}$ pin goes high in shutdown and is cleared high when power is first applied to V_{CC}. If $\overline{FLT}$ is set low, it can be reset during the cool down phase by pulling $\overline{SHDN}$ low for at least 1s/µF of C_{TMR}.

Intermittent Fault Conditions

Brief overvoltage or overcurrent conditions interrupt the operation of the timer. If the TMR pin has not yet reached 1.275V when the input falls below the regulation value or drops out of current limit, the timer capacitor is discharged back to 0.5V with a 2µA current sink. If the TMR voltage crosses 1.275V $\overline{FLT}$ is set low. If the overvoltage or overcurrent abates before reaching 1.375V, the timer capacitor discharges with 2µA back to 0.5V, whereupon $\overline{FLT}$ resets high. If several short overvoltage or overcurrent events occur in rapid succession, the timer capacitor will integrate the charging and discharging currents.

MOSFET Selection

The LT4363 drives an N-channel MOSFET to conduct the load current. The important features of the MOSFET are on-resistance $R_{DS(ON)}$, the maximum drain-source voltage $V_{(BR)DSS}$, the threshold voltage, and the SOA.

The maximum allowable drain-source voltage must be higher than the supply voltage. If the output is shorted to ground or during an overvoltage event, the full supply voltage will appear across the MOSFET.

The gate drive for the MOSFET is guaranteed to be more than 10V and less than 16V for those applications with V_{CC} higher than 9V. This allows the use of standard threshold voltage N-channel MOSFETs. For systems with V_{CC} less than 9V, a logic level MOSFET is required since the gate drive can be as low as 4.5V.

The SOA of the MOSFET must encompass all fault conditions. In normal operation the pass transistor is fully on, dissipating very little power. But during either overvoltage or overcurrent faults, the GATE pin is controlled to regulate either the output voltage or the current through the MOSFET. Large current and high voltage drop across the MOSFET can coexist in these cases. The SOA curves of the MOSFET must be considered carefully along with the selection of the fault timer capacitor.

Transient Stress in the MOSFET

During an overvoltage event, the LT4363 drives a series pass MOSFET to regulate the output voltage at an acceptable level. The load circuitry may continue operating throughout this interval, but only at the expense of dissipation in the MOSFET pass device. MOSFET dissipation or stress is a function of the input voltage waveform, regulation voltage and load current. The MOSFET must be sized to survive this stress.

Most transient event specifications use the prototypical waveshape shown in Figure 3, comprising a linear ramp of rise time t_r, reaching a peak voltage of V_{PK} and exponentially decaying back to V_{IN} with a time constant of τ.

MOSFET stress is the result of power dissipated within the device. For long duration surges of 100ms or more, stress is increasingly dominated by heat transfer; this is a matter of device packaging and mounting, and heat sink thermal mass. This is best analyzed by simulation, using the MOSFET thermal model.

For short duration transients of less than 100ms, MOSFET survival is increasingly a matter of safe operating area

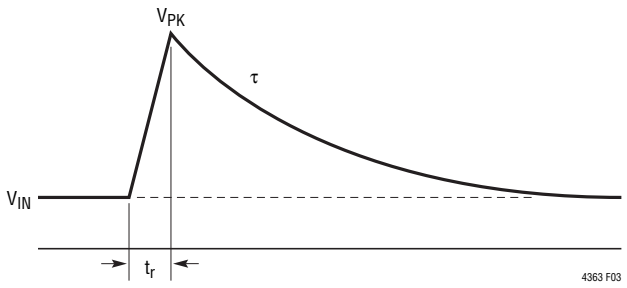

Figure 3. Prototypical Transient Waveform

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(SOA), an intrinsic property of the MOSFET. SOA quantifies the time required at any given condition of V_{DS} and I_D to raise the junction temperature of the MOSFET to its rated maximum. MOSFET SOA is expressed in units of watt-squared-seconds (P^2t). This figure is essentially constant for intervals of less than 100ms for any given device type, and rises to infinity under DC operating conditions. Destruction mechanisms other than bulk die temperature distort the lines of an accurately drawn SOA graph so that P^2t is not the same for all combinations of I_D and V_{DS}. In particular P^2t tends to degrade as V_{DS} approaches the maximum rating, rendering some devices useless for absorbing energy above a certain voltage.

When a fast input voltage step occurs, the current through the pass transistor to supply the load and charge up the output capacitor can be high enough to trigger an overcurrent event. The gate pulls low to 1V above the OUT pin, turning off the MOSFET momentarily. The internal charge pump will then start to pull the GATE pin high and turn on the MOSFET to support the load current and charge up the OUT pin. The fault timer may not start yet because the current level is below the overcurrent limit threshold and the output voltage has not reached the servo voltage. This extra stress needs to be included in calculating the overall stress level of the MOSFET.

Calculating Transient Stress

To select a MOSFET suitable for any given application, the SOA stress must be calculated for each input transient which shall not interrupt operation. It is then a simple matter to choose a device which has adequate SOA to survive the maximum calculated stress. P^2t for a prototypical transient waveform is calculated as follows (Figure 4):

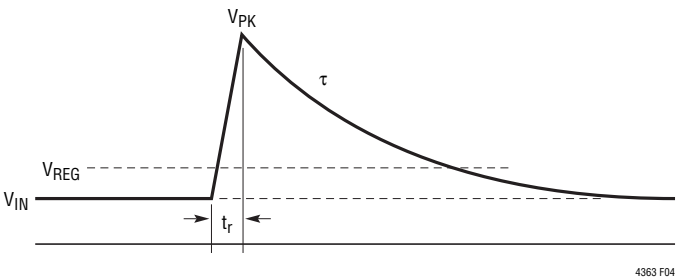

Figure 4. Safe Operating Area Required to Survive Prototypical Transient Waveform

Let

$a = V_{REG} - V_{IN}$

$b = V_{PK} - V_{IN}$

(V_{IN} = Nominal Input Voltage)

Then

$$P^2t = I_{LOAD}^2 \bullet \left[\frac{1}{3} t_r \frac{(b-a)^3}{b} + \frac{1}{2}\tau\left(2a^2 \ln\frac{b}{a} + 3a^2 + b^2 - 4ab\right)\right]$$

Typically $V_{REG} \approx V_{IN}$ and $\tau \gg t_r$ simplifying the above to

$$P^2t = \frac{1}{2} I_{LOAD}^2 \left(V_{PK} - V_{REG}\right)^2 \tau \qquad [W^2s]$$

For the transient conditions of V_{PK} = 80V, V_{IN} = 12V, V_{REG} = 16V, t_r = 10µs and τ = 1ms, and a load current of 3A, P^2t is 18.4W^2s – easily handled by a MOSFET in a DPAK package. The P^2t of other transient waveshapes is evaluated by integrating the square of MOSFET power over time. LTSpice can be used to simulate timer behavior for more complex transients and cases where overvoltage and overcurrent faults coexist.

Calculating Short-Circuit Stress

SOA stress must also be calculated for short-circuit conditions. Short-circuit P^2t is given by:

$$P^2t = \left(\Delta V_{DS} \bullet \frac{\Delta V_{SNS}}{R_{SNS}}\right)^2 \bullet t_{TMR} \qquad [W^2s]$$

Where ΔV_{DS} is the voltage across the MOSFET, and ΔV_{SNS} is the SNS pin threshold, and t_{TMR} is the overcurrent timer interval.

For V_{IN} = 15V, ΔV_{DS} = 13V (V_{OUT} = 2V), ΔV_{SNS} = 50mV, R_{SNS} = 12mΩ and C_{TMR} = 100nF, P^2t is 6.3W^2s – less than the transient SOA calculated in the previous example. Nevertheless, to account for circuit tolerances this figure should be doubled to 12.6W^2s.

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Limiting Inrush Current and GATE Pin Compensation

The LT4363 limits the inrush current to any load capacitance by controlling the GATE pin voltage slew rate. An external capacitor can be connected from GATE to ground to reduce the inrush current at the expense of slower turn-off time. The gate capacitor is set at:

$$C1 = \frac{I_{GATE(UP)}}{I_{INRUSH}} \bullet C_L$$

The LT4363 does not need extra compensation components at the GATE pin for stability during an overvoltage or overcurrent event. With transient input voltage slew rates faster than 5V/µs, a gate capacitor, C1, to ground is needed to prevent self enhancement of the N-channel MOSFET.

The extra gate capacitance slows down the turn off time during fault conditions and may allow excessive current during an output short event. An extra resistor, R1, in series with the gate capacitor can improve the turn off time. A diode, D1, should be placed across R1 with the cathode connected to C1 as shown in Figure 5.

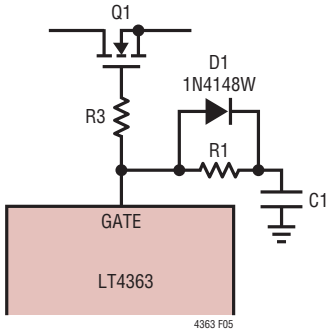


Figure 5. External GATE network

Undervoltage/Overvoltage Comparators

The LT4363 has both undervoltage and overvoltage comparators that can be used to sense the input supply voltage. When the voltage at the UV pin is below the 1.275V threshold, the GATE pin is held low to keep the external MOSFET off. The supply voltage at the V_{CC} pin should be at least 4V for the UV comparator to function.

The overvoltage comparator prevents the LT4363-2 from restarting if the voltage at the OV pin is above the 1.275V threshold during a fault. The pass transistor is not allowed to turn back on even after the cool down period has finished. This prevents the pass transistor from cycling between ON and OFF states when the input voltage stays at an elevated level for a long period of time, reducing the stress on the N-channel MOSFET. For the latch-off version, LT4363-1, the overvoltage comparator function is not available.

Reverse Input Protection

A blocking diode is commonly employed to protect the load when reverse input is possible. This diode causes extra power loss, generates heat, and reduces the available supply voltage range.

The LT4363 is designed to withstand reverse voltage without damage to itself. The V_{CC}, $\overline{SHDN}$, UV, and OV pins can withstand up to 60V of DC voltage below the GND potential. Back-to-back MOSFETs must be used to block the current path through Q1's body diode (Figure 6). Figure 7 shows the approach with a P-channel MOSFET in place of Q2.

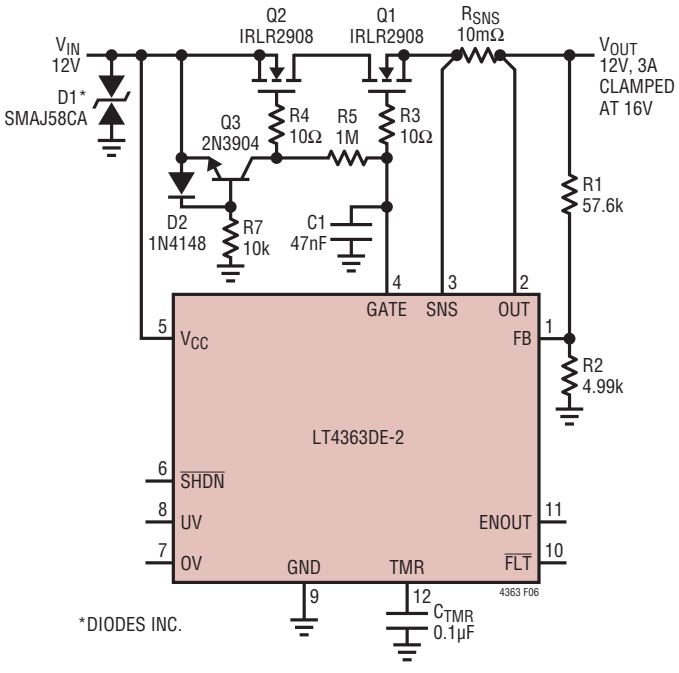


Figure 6. Overvoltage Regulator with N-channel MOSFET Reverse Input Protection

APPLICATIONS INFORMATION

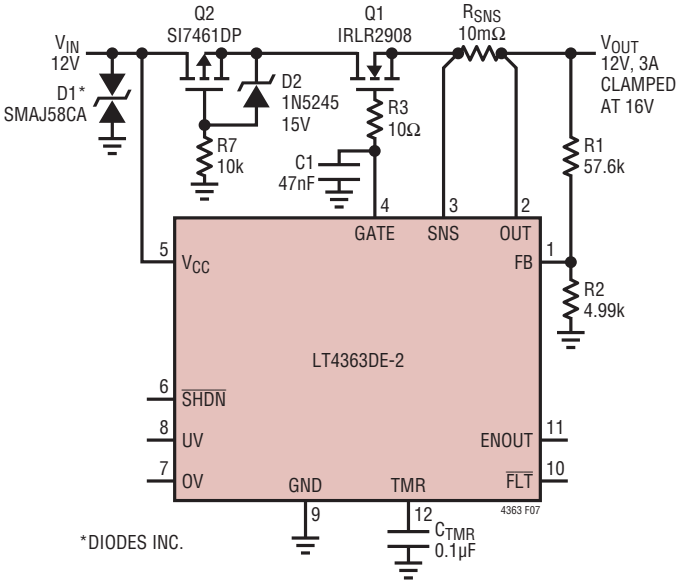


Figure 7. Overvoltage Regulator with P-channel MOSFET Reverse Input Protection

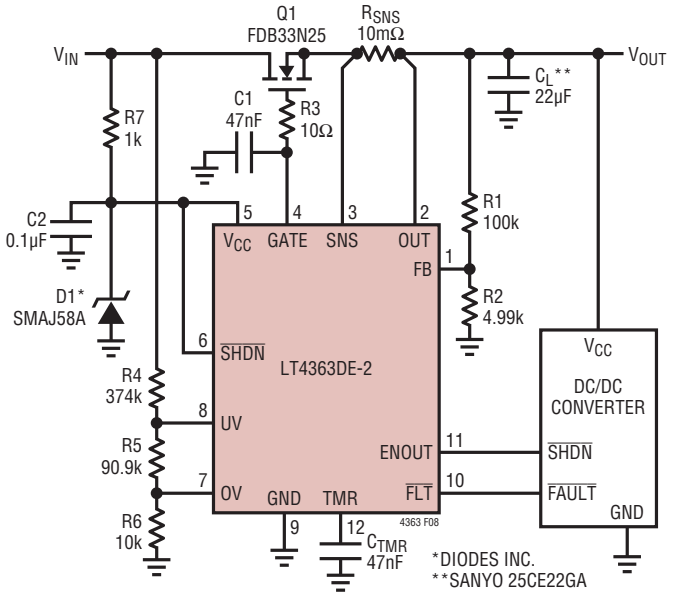


Figure 8. Overvoltage Regulator with Input Voltage Detection

Shutdown

The LT4363 can be shut down to a low current mode when the voltage at the $\overline{SHDN}$ pin is pulled below the shutdown threshold of 0.4V. The quiescent current drops down to 7µA with internal circuitry turned off.

The $\overline{SHDN}$ pin can be pulled up to 100V or below GND by up to 60V without damage. Leaving the pin open allows an internal current source to pull it up and turn on the part while clamping the pin to 2.2V. The leakage current at the pin should be limited to no more than 1µA if no pull up device is used to help turn it on.

Supply Transient Protection

The LT4363 is tested to operate to 80V and guaranteed to be safe from damage up to 100V. Nevertheless, voltage transients above 100V may cause permanent damage. During a short-circuit condition, the large change in current flowing through power supply traces and associated wiring can cause inductive voltage transients which could exceed 100V. To minimize the voltage transients, the power trace parasitic inductance should be minimized by using wide traces. A small RC filter, in Figure 8, at the V_{CC} pin will clamp the voltage spikes.

Another way to limit transients above 100V at the V_{CC} pin is to use a Zener diode and a resistor, D1 and R7 in Figure 8. The Zener diode limits the voltage at the pin while the resistor limits the current through the diode to a safe level during the surge. However, D1 can be omitted if the filtered voltage, due to R7 and C1, at the V_{CC} pin is below 100V. The inclusion of R7 in series with the V_{CC} pin will increase the minimum required voltage at V_{IN} due to the extra voltage drop across it. This voltage drop is due to the supply current of the LT4363 and the leakage current of D1.

A total bulk capacitance of at least 22µF low ESR electrolytic is required close to the source pin of MOSFET Q1. In addition, the bulk capacitance should be at least 10 times larger than the total ceramic bypassing capacitor on the input of the DC/DC converter.

Layout Considerations

To achieve accurate current sensing, Kelvin connection to the current sense resistor (R_{SNS} in Figure 8) is recommended. The minimum trace width for 1 oz copper foil is 0.02" per amp to ensure the trace stays at a reasonable temperature. 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/square. Small resistances can cause large errors in high current applications. Noise immunity will be improved

APPLICATIONS INFORMATION

significantly by locating resistive dividers close to the pins with short V_{CC} and GND traces.

Design Example

As a design example, take an application with the following specifications: V_{CC} = 8V to 14V DC with a transient of 150V and decay time constant (τ) of 400ms, $V_{OUT} \leq 27V$, current limit (I_{LIM}) at 5A, low battery detection of 6V, input overvoltage level at 60V, and 1ms of overvoltage early warning (Figure 8).

Selection of SMAJ58A for D1 will limit the voltage at the V_{CC} pin to less than 71V during 150V surge. The minimum required voltage at the V_{CC} pin is 4V when V_{IN} is at 8V; the supply current for LT4363 is 1.5mA. The maximum value for R7 to ensure proper operation is:

$$R7 = \frac{8V - 4V}{1.5mA} = 2.67k\Omega$$

Select 1kΩ for R7 to accommodate all conditions.

The maximum current through R7 into D1 is then calculated as:

$$I_{D1} = \frac{150V - 64V}{1k\Omega} = 86mA$$

which is easily handled by the SMAJ58A for more than 500ms.

With 0.1µF of bypass capacitance, C2, along with 1k of R7, high voltage transients up to 200V with a pulse width less than 10µs are filtered out at the V_{CC} pin.

Next, calculate the resistive divider value to limit V_{OUT} to 27V during an overvoltage event:

$$V_{REG} = \frac{1.275V \bullet (R1+R2)}{R2} = 27V$$

Set the current through R1 and R2 during the overvoltage condition to 250µA.

$$R2 = \frac{1.275V}{250\mu A} = 5k\Omega$$

Choose 4.99kΩ for R2.

$$R1 = \frac{(27V - 1.275V) \bullet R2}{1.275V} = 100.7k\Omega$$

The nearest standard value for R1 is 100kΩ.

Next calculate the sense resistor, R_{SNS}, value:

$$R_{SNS} = \frac{50mV}{I_{LIM}} = \frac{50mV}{5A} = 10m\Omega$$

C_{TMR} is then chosen for 1ms of early warning time:

$$C_{TMR} = \frac{1ms \bullet 6\mu A}{100mV} = 60nF$$

The nearest standard value for C_{TMR} is 47nF.

Finally, calculate R4, R5, and R6 for 6V low battery detection and 60V input overvoltage level:

$$6V \bullet \frac{R5+R6}{R4+R5+R6} = 1.275V$$

$$60V \bullet \frac{R6}{R4+R5+R6} = 1.275V$$

Choose 10kΩ for R6.

$$R4+R5 = \frac{60V \bullet 10k\Omega}{1.275V} - 10k\Omega = 460.6k\Omega$$

$$R5 = 1.275V \bullet \frac{460.6k\Omega + 10k\Omega}{6V} - 10k\Omega = 90k\Omega$$

R4 = 460.6kΩ – 90kΩ = 370.6kΩ

Select 90.9kΩ for R5 and 374kΩ for R4.

The pass transistor, Q1, should be chosen to withstand a short-circuit with V_{CC} = 14V. In the case of a severe output short where V_{OUT} = 0V, the total overcurrent fault time is:

$$t_{OC} = \frac{47nF \bullet 0.875V}{45.5\mu A} = 0.904ms$$

APPLICATIONS INFORMATION

The power dissipation in Q1 is:

$$P = \frac{14V \bullet 25mV}{10m\Omega} = 35W$$

During an output overload or soft short, the voltage at the OUT pin could stay at 2V or higher. The total overcurrent fault time when V_{OUT} = 2V is:

$$t_{OC} = \frac{47nF \bullet 0.875V}{40\mu A} = 1.028ms$$

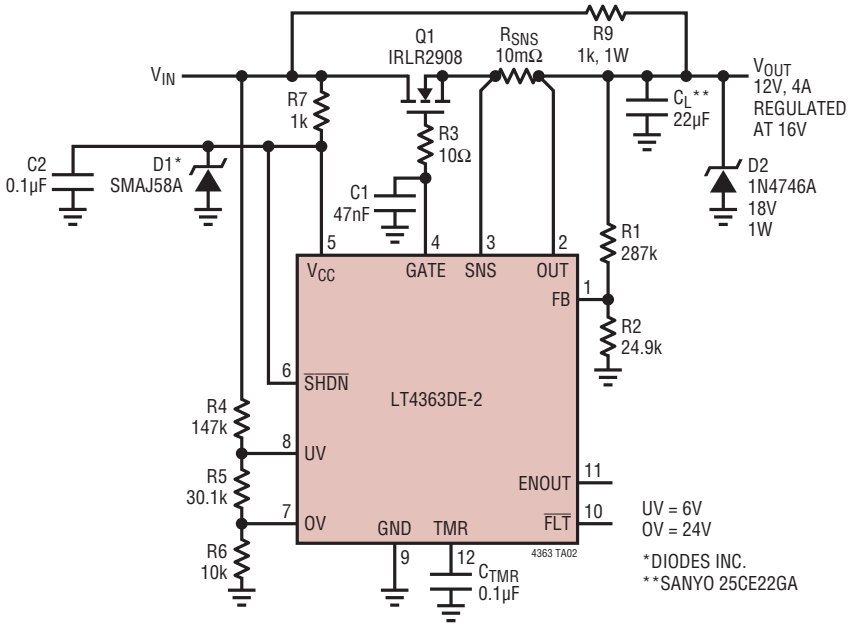
The power dissipation in Q1 is:

$$P = \frac{(14V - 2V) \bullet 50mV}{10m\Omega} = 60W$$

These conditions are well within the Safe Operating Area of the FDB33N25.

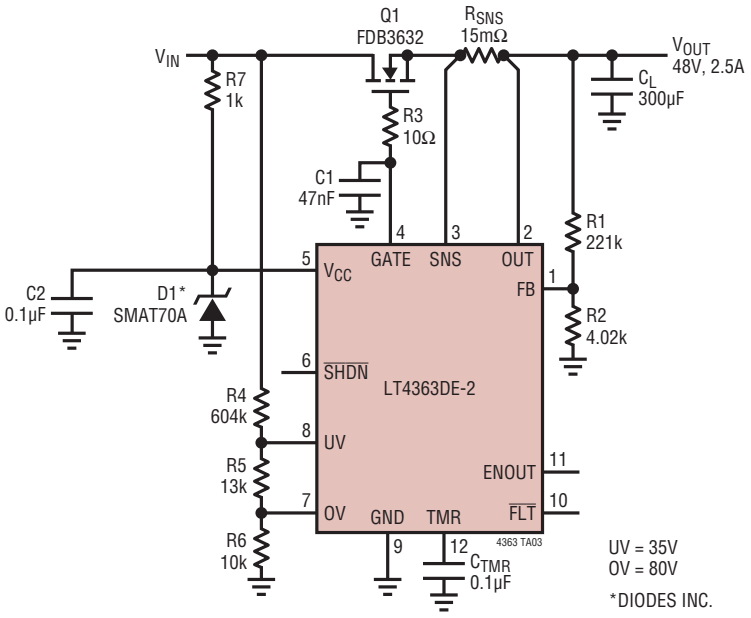
TYPICAL APPLICATIONS

Overvoltage Regulator with Output Keep Alive During Shutdown

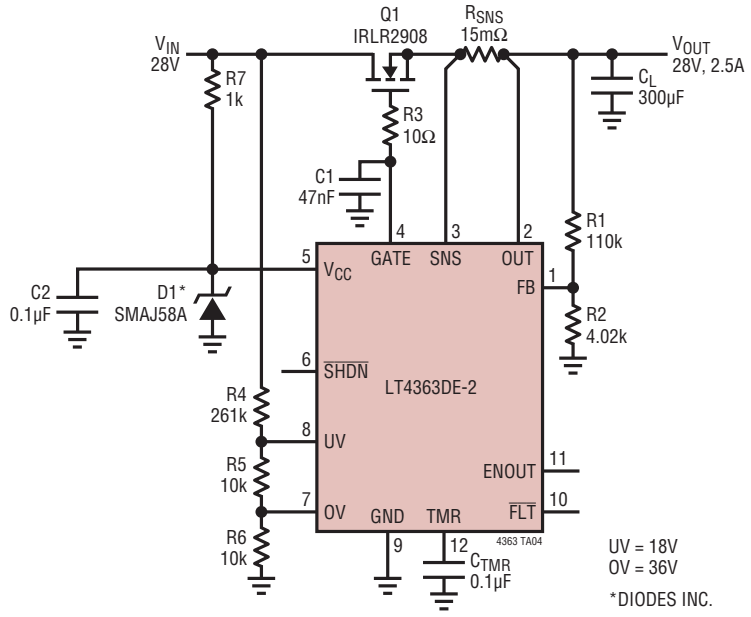


TYPICAL APPLICATIONS

2.5A, 48V Hot Swap with Overvoltage Output Regulation at 72V

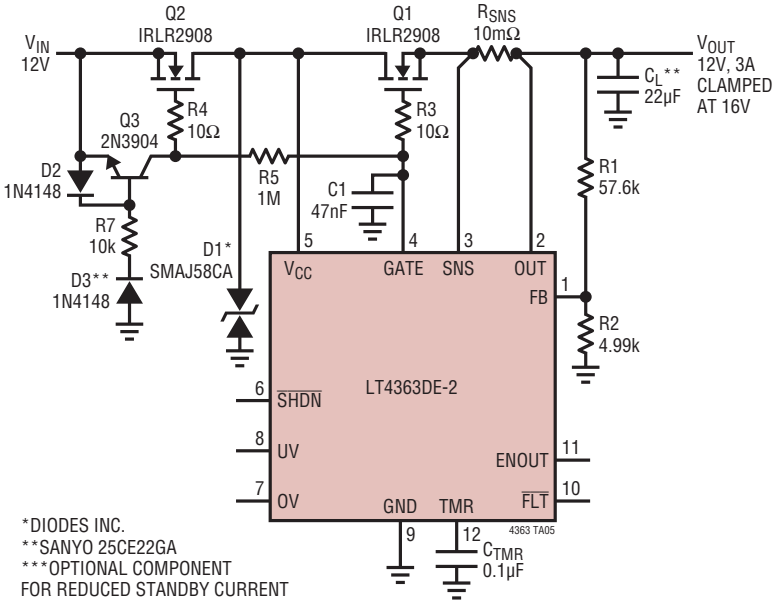


2.5A, 28V Hot Swap with Overvoltage Output Regulation at 36V

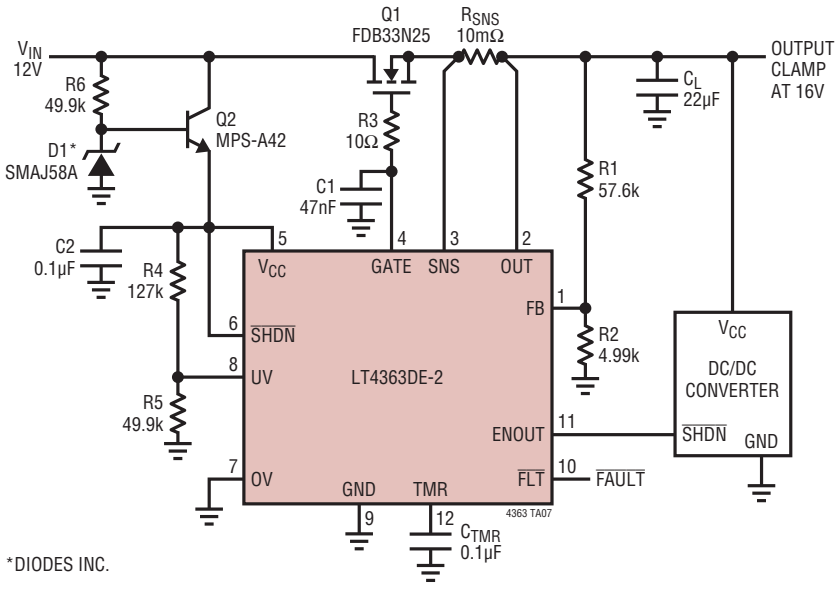


TYPICAL APPLICATIONS

Overvoltage Regulator with Reverse Input Protection Up to –80V



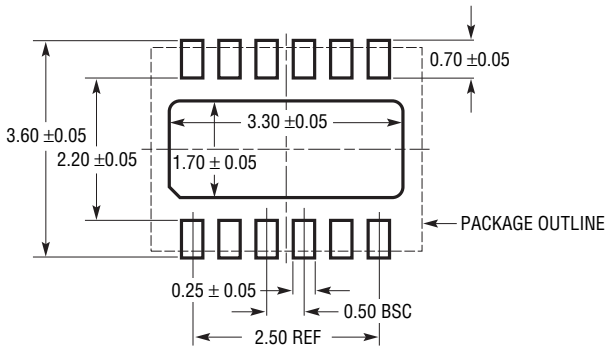
Overvoltage Regulator with 250V Surge Protection



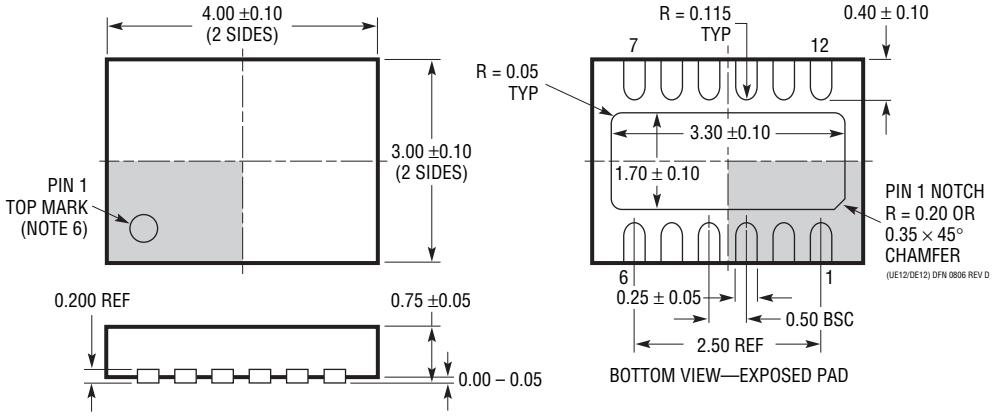
PACKAGE DESCRIPTION

Refer to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints.html for the most recent package drawings.

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

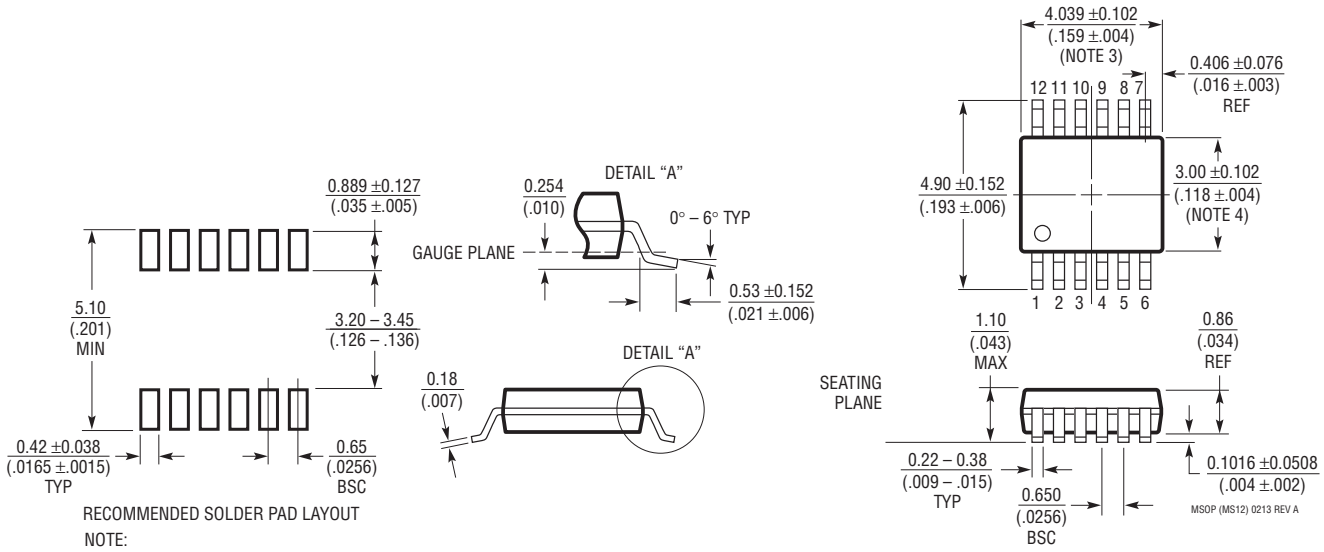


NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION
   (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Refer to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints.html for the most recent package drawings.

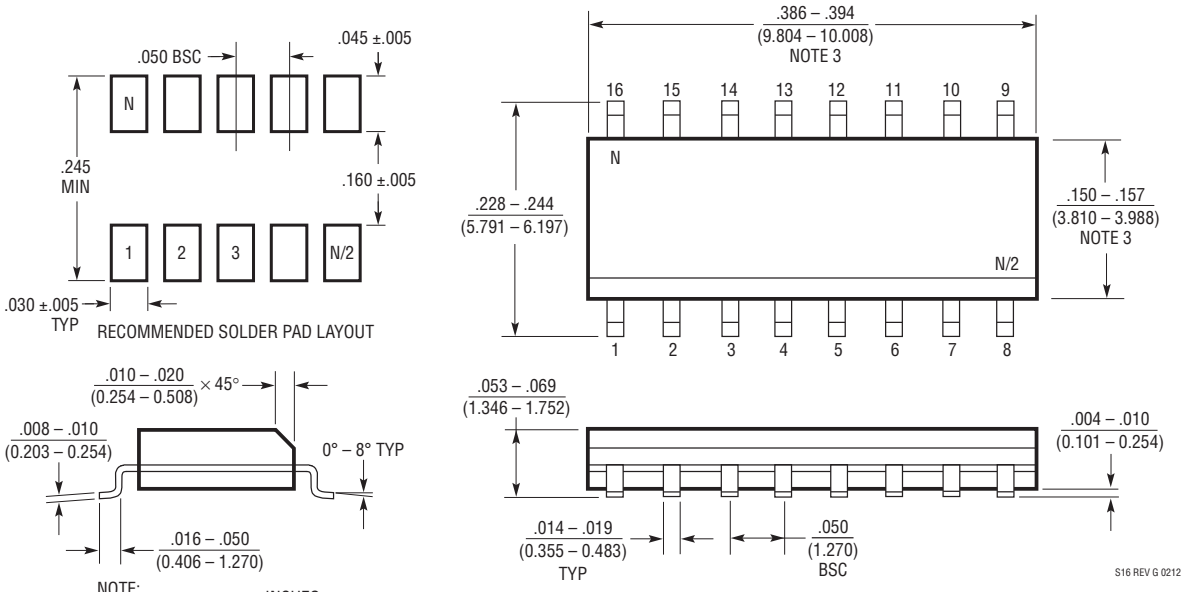
MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev A)



RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

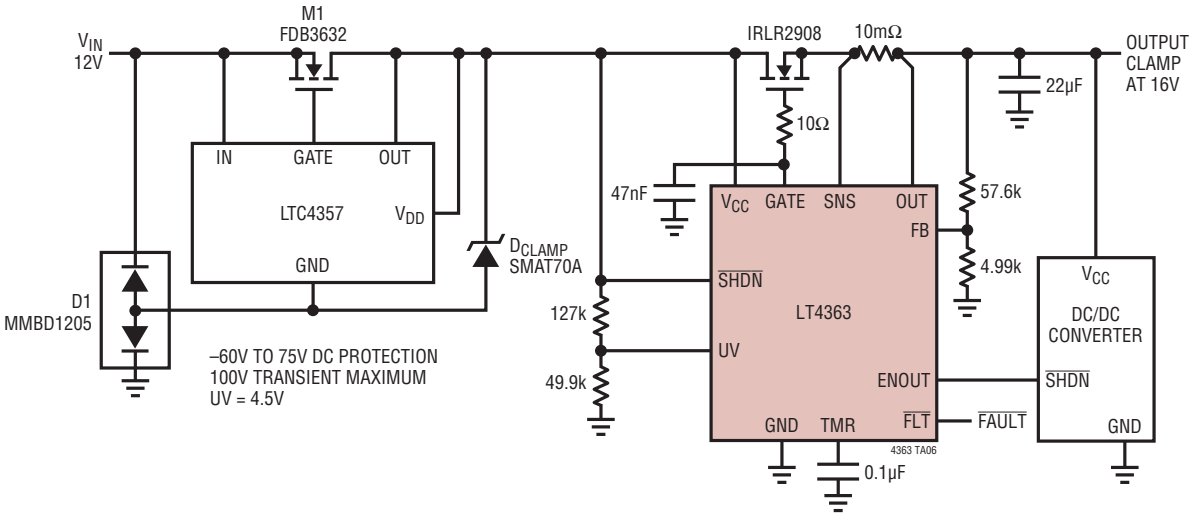
Rev. C

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/12	Add 57.6k resistor to Typical Application	24
B	6/13	Added H and MP temperature grades to Order Information	3
		Operating Voltage Range for all temperature grades is 4V to 80V	3
		Reverse Input Current maximum changed to –4mA from –3mA	3
		$I_{GATE(UP)}$: At 12V, changed from [–10, –20, –35]µA to [–15, –30, –45]µA. At 48V, changed from [–10, –25, –40]µA to [–20, –40, –65]µA	3
		Current Limit Sense Voltage: At 12V, improved from 43mV — 58mV to 45mV — 55mV. At 48V, improved from 45mV — 59mV to 48mV — 58mV	4
		I_{SNS} maximum changed from 30µA to 40µA	4
		$V_{TMR(H)}$ range changed from 3.7V — 5V to 3.5V — 5.4V	4
		OUT Reset Threshold minimum changed from 1.9V to 1.8V	4
		Updated curves in graphs G05, G06 and G09	5
		Corrected Y-axis numbers in Warning Period TMR Current, graph G15	6
		Replaced Current Limit at Supply Voltage graph with Current Limit Foldback	7
		GATE Pin Description: Added information on 14V protection clamp	8
		TMR Pin Description: Added 10nF minimum capacitor requirement	8
		Changed GATE to SNS clamp in Block Diagram to 14V from 13V	9
		Added 0.1µF C2 to Typical Application circuits	18, 19
C	1/24	Updated Applications Section	1
		Updated Description Section	1
		Updated Operation Section	10
		Updated Applications Information Section	13, 15

TYPICAL APPLICATION

Overvoltage Regulator with Ideal Diode Reverse Voltage Protection



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1696	Overvoltage Protection Controller	ThinSOT™ Package, 2.7V to 27V
LTC2909	Triple/Dual Inputs UV/OV Negative Monitor	Pin Selectable Input Polarity Allows Negative and OV Monitoring
LTC2912/LTC2913	Single/Dual UV/OV Voltage Monitor	Ads UV and OV Trip Values, ±1.5% Threshold Accuracy
LTC2914	Quad UV/OV Monitor	For Positive and Negative Supplies
LTC3827/LTC3827-1	Low I_Q, Dual, Synchronous Controller	$4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$, 80µA Quiescent Current
LTC3835/LTC3835-1	Low I_Q, Synchronous Step-Down Controller	Single Channel LTC3827/LTC3827-1
LT3845	Low I_Q, Synchronous Step-Down Controller	$4V \le V_{IN} \le 60V$, $1.23V \le V_{OUT} \le 36V$, 120µA Quiescent Current
LT3850	Dual, 550kHz, 2-Phase Synchronous Step-Down Controller	Dual 180° Phased Controllers, V_{IN} 4V to 24V, 97% Duty Cycle, 4mm × 4mm QFN-28, SSOP-28 Packages
LTC3890	Low I_Q, Dual 2-Phase, Synchronous Step-Down Controller	$4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, 50µA Quiescent Current
LT4256-1	Positive 48V Hot Swap Controller with Open-Circuit Detect	Foldback Current Limiting, Open-Circuit and Overcurrent Fault Output, Up to 80V Supply
LTC4260	Positive High Voltage Hot Swap Controller with 8-Bit ADC and I^2C	Wide Operating Range 8.5V to 80V
LTC4352	Ideal MOSFET ORing Diode	External N-Channel MOSFETs Replace ORing Diodes, 0V to 18V
LTC4354	Negative Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 1µs Turn-Off, 80V Operation
LTC4355	Positive Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 0.3µs Turn-Off, 80V Operation
LT4356-1	High Voltage Surge Stopper	100V Overvoltage and Overcurrent Protection, Latch-Off and Auto-Retry Options
LTC4364	Surge Stopper with Ideal Diode	4V to 80V Operation; –40V Reverse Input, –20V Reverse Output Protection
LTC4365	Window Passer - OV, UV and Reverse Supply Protection Controller	2.5V to 34V Operation, Protects 60V to –40V

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- Shortage Management
- Alternative Solution
- Excess Inventory Management