



**THE DATASHEET OF
LMS1487ECNA/NOPB**



LMS1487

LMS1487 5V Low Power RS-485 / RS-422 Differential Bus Transceiver



Literature Number: SNOSA34E

5V Low Power RS-485 / RS-422 Differential Bus Transceiver

General Description

The LMS1487 is a low power differential bus/line transceiver designed for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines. It meets ANSI Standards TIA/EIA RS422-B, TIA/EIA RS485-A and ITU recommendation and V.11 and X.27. The LMS1487 combines a TRI-STATE® differential line driver and differential input receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active high and active low, respectively, that can be externally connected to function as a direction control. The driver and receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to bus whenever the driver is disabled or when $V_{CC} = 0V$. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments. The LMS1487 is available in a 8-Pin SOIC and 8-pin DIP packages. It is a drop-in socket replacement to Maxim's MAX1487

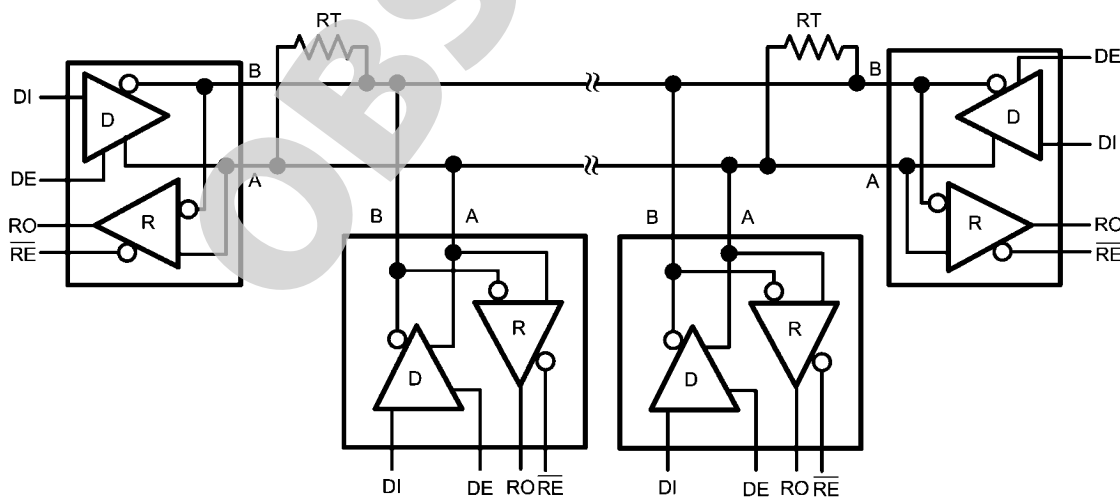
Features

- Meet ANSI standard RS-485-A and RS-422-B
- Data rate 2.5 Mbps
- Single supply voltage operation, 5V
- Wide input and output voltage range
- Thermal shutdown protection
- Short circuit protection
- Low quiescent current 320µA
- Allows up to 128 transceivers on the bus
- Open circuit fail-safe for receiver
- Extended operating temperature range $-40^{\circ}C$ to $85^{\circ}C$
- Drop-in replacement to MAX1487
- Available in 8-pin SOIC and 8-pin DIP package

Applications

- Low power RS-485 systems
- Network hubs, bridges, and routers
- Point of sales equipment (ATM, barcode scanners,...)
- Local area networks (LAN)
- Integrated service digital network (ISDN)
- Industrial programmable logic controllers
- High speed parallel and serial applications
- Multipoint applications with noisy environment

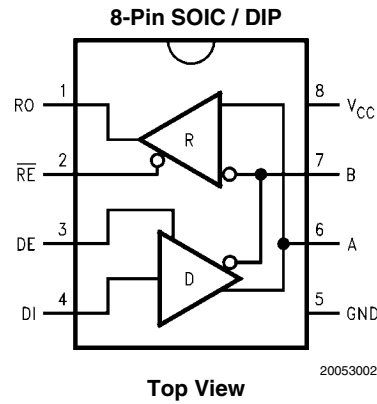
Typical Application



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A Typical multipoint application is shown in the above figure. Terminating resistors, RT, are typically required but only located at the two ends of the cable. Pull up and pull down resistors maybe required at the end of the bus to provide fail-safe biasing. The biasing resistors provide a bias to the cable when all drivers are in TRI-STATE, See National Application Note, AN-847 for further information.

Connection Diagram



Truth Table

| DRIVER SECTION | | | | |
|------------------|----|--------------|----|---|
| \overline{RE} | DE | DI | A | B |
| X | H | H | H | L |
| X | H | L | L | H |
| X | L | X | Z | Z |
| RECEIVER SECTION | | | | |
| \overline{RE} | DE | A-B | RO | |
| L | L | $\geq +0.2V$ | H | |
| L | L | $\leq -0.2V$ | L | |
| H | X | X | Z | |
| L | L | OPEN * | H | |

Note: * = Non Terminated, Open Input only

X = Irrelevant
 Z = TRI-STATE
 H = High level
 L = Low level

Pin Descriptions

| Pin # | I/O | Name | Function |
|-------|-----|-----------------|---|
| 1 | O | RO | Receiver Output: If $A > B$ by 200 mV, RO will be high; If $A < B$ by 200mV, RO will be low. RO will be high also if the inputs (A and B) are open (non-terminated) |
| 2 | I | \overline{RE} | Receiver Output Enable: RO is enabled when \overline{RE} is low; RO is in TRI-STATE when \overline{RE} is high |
| 3 | I | DE | Driver Output Enable: The driver outputs (A and B) are enabled when DE is high; they are in TRI-STATE when DE is low. Pins A and B also function as the receiver input pins (see below) |
| 4 | I | DI | Driver Input: A low on DI forces A low and B high while a high on DI forces A high and B low when the driver is enabled |
| 5 | N/A | GND | Ground |
| 6 | I/O | A | Non-inverting Driver Output and Receiver Input pin. Driver Output levels conform to RS-485 signaling levels |
| 7 | I/O | B | Inverting Driver Output and Receiver Input pin. Driver Output levels conform to RS-485 signaling levels |
| 8 | N/A | V_{CC} | Power Supply: $4.75V \leq V_{CC} \leq 5.25V$ |

Ordering Information

| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|------------|-------------|-----------------|--------------------------|-------------|
| 8-Pin SOIC | LMS1487CM | LMS1487CM | 95 Units/Rail | M08A |
| | LMS1487CMX | | 2.5k Units Tape and Reel | |
| | LMS1487IM | LMS1487IM | 95 Units/Rail | |
| | LMS1487IMX | | 2.5k Units Tape and Reel | |
| 8-Pin DIP | LMS1487CNA | LMS1487CNA | 40 Units/Rail | N08E |
| | LMS1487INA | LMS1487INA | 40 Units/Rail | |

OBSOLETE

Absolute Maximum Ratings *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| | |
|---|--------------------------|
| Supply Voltage, V_{CC} <i>(Note 2)</i> | 7V |
| Input Voltage, V_{IN} (DI, DE, or \overline{RE}) | -0.3V to $V_{CC} + 0.3V$ |
| Voltage Range at Any Bus Terminal (AB) | -7V to 12V |
| Receiver Outputs | -0.3V to $V_{CC} + 0.3V$ |
| Package Thermal Impedance, θ_{JA} | |
| SOIC | 125°C/W |
| DIP | 88°C/W |
| Junction Temperature <i>(Note 3)</i> | 150°C |
| Operating Free-Air Temperature Range, T_A | |
| Commercial | 0°C to 70°C |
| Industrial | -40°C to 85°C |
| Storage Temperature Range | -65°C to 150°C |
| Soldering Information | |
| Infrared or Convection (20 sec.) | 235°C |

| | |
|----------------------------|-------|
| Lead Temperature | 260°C |
| ESD Rating <i>(Note 4)</i> | 7kV |

Operating Ratings

| | Min | Nom | Max | |
|--|------|-----|------|----|
| Supply Voltage, V_{CC} | 4.75 | 5.0 | 5.25 | V |
| Voltage at any Bus Terminal (Separately or Common Mode) V_{IN} or V_{IC} | -7 | | 12 | V |
| High-Level Input Voltage, V_{IH} <i>(Note 5)</i> | 2 | | | V |
| Low-Level Input Voltage, V_{IL} <i>(Note 5)</i> | | | 0.8 | V |
| Differential Input Voltage, V_{ID} <i>(Note 6)</i> | | | ±12 | V |
| High-Level Output Driver, I_{OH} | | | -15 | mA |
| | | | 0 | |
| Receiver, I_{OH} | | | -42 | mA |
| Low-Level Output Driver, I_{OL} | | | 80 | mA |
| Receiver, I_{OL} | | | 26 | mA |

Electrical Characteristics

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------|---|--|------|-----|------|-------|
| Driver Section | | | | | | |
| $ V_{OD1} $ | Differential Output Voltage | $R = \infty$ <i>(Figure 1)</i> | | | 5.25 | V |
| $ V_{OD2} $ | Differential Output Voltage | $R = 50\Omega$ <i>(Figure 1)</i> , RS-422 | 2.0 | | | V |
| | | $R = 27\Omega$ <i>(Figure 1)</i> , RS-485 | 1.5 | | 5.0 | |
| ΔV_{OD} | Change in Magnitude of Driver Differential Output Voltage for Complementary Output States | $R = 27\Omega$ or 50Ω <i>(Figure 1)</i> , <i>(Note 7)</i> | | | 0.2 | V |
| V_{OC} | Common-Mode Output Voltage | $R = 27\Omega$ or 50Ω <i>(Figure 1)</i> | | | 3.0 | V |
| ΔV_{OC} | Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States | $R = 27\Omega$ or 50Ω <i>(Figure 1)</i> , <i>(Note 7)</i> | | | 0.2 | V |
| V_{IH} | CMOS Input Logic Threshold High | DE, DI, \overline{RE} | 2.0 | | | V |
| V_{IL} | CMOS Input Logic Threshold Low | DE, DI, \overline{RE} | | | 0.8 | V |
| I_{IN1} | Logic Input Current | DE, DI, \overline{RE} | | | ±2 | µA |
| Receiver Section | | | | | | |
| I_{IN2} | Input Current (A, B) | DE = 0V, $V_{CC} = 0V$ or 5.25V $V_{IN} = 12V$ | | | 0.25 | mA |
| | | $V_{IN} = -7V$ | | | -0.2 | |
| V_{TH} | Differential Input Threshold Voltage | $-7V \leq V_{CM} \leq +12V$ | -0.2 | | +0.2 | V |
| ΔV_{TH} | Input Hysteresis Voltage ($V_{TH+} - V_{TH-}$) | $V_{CM} = 0$ | | 95 | | mV |
| V_{OH} | CMOS High-level Output Voltage | $I_{OH} = -4mA$, $V_{ID} = 200mV$ | 3.5 | | | V |
| V_{OL} | CMOS Low-level | $I_{OL} = 4mA$, $V_{ID} = -200mV$ | | | 0.40 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------------------|---------------------------------------|--|-----|-----|---------|-----------|
| I_{OZR} | Tristate Output Leakage Current | $0.4V \leq V_O \leq +2.4V$ | | | ± 1 | μA |
| R_{IN} | Input Resistance | $-7V \leq V_{CM} \leq +12V$ | 48 | | | $k\Omega$ |
| Power Supply Current | | | | | | |
| I_{CC} | Supply Current | $DE = V_{CC}, \overline{RE} = GND \text{ or } V_{CC}$ | | 320 | 500 | μA |
| | | $DE = 0V, \overline{RE} = GND \text{ or } V_{CC}$ | | 315 | 400 | |
| I_{OSD1} | Driver Short-circuit Output Current | $V_O = \text{high}, -7V \leq V_{CM} \leq +12V$ (Note 8) | 35 | | 250 | mA |
| I_{OSD2} | Driver Short-circuit Output Current | $V_O = \text{low}, -7V \leq V_{CM} \leq +12V$ (Note 8) | 35 | | 250 | mA |
| I_{OSR} | Receiver Short-circuit Output Current | $0V \leq V_O \leq V_{CC}$ | 7 | | 95 | mA |
| Switching Characteristics | | | | | | |
| Driver | | | | | | |
| $T_{PLH},$ T_{PHL} | Propagation Delay Input to Output | $R_L = 54\Omega, C_L = 100pF$ (Figure 3, Figure 7) | 10 | 35 | 60 | nS |
| T_{SKEW} | Driver Output Skew | $R_L = 54\Omega, C_L = 100 pF$ (Figure 3, Figure 7) | | 5 | 10 | nS |
| $T_R,$ T_F | Driver Rise and Fall Time | $R_L = 54\Omega, C_L = 100 pF$ (Figure 3, Figure 7) | 3 | 8 | 40 | nS |
| $T_{ZH},$ T_{ZL} | Driver Enable to Output Valid Time | $C_L = 100 pF, R_L = 500\Omega$ (Figure 4, Figure 8) | | 25 | 70 | nS |
| $T_{HZ},$ T_{LZ} | Driver Output Disable Time | $C_L = 15 pF, R_L = 500\Omega$ (Figure 4, Figure 8) | | 30 | 70 | nS |
| Receiver | | | | | | |
| $T_{PLH},$ T_{PHL} | Propagation Delay Input to Output | $R_L = 54\Omega, C_L = 100 pF$ (Figure 5, Figure 7) | 20 | 50 | 200 | nS |
| T_{SKEW} | Receiver Output Skew | $R_L = 54\Omega, C_L = 100 pF$ (Figure 5, Figure 7) | | 5 | | nS |
| $T_{ZH},$ T_{ZL} | Receiver Enable Time | $C_L = 15 pF, R_L = 1 k\Omega$ (Figure 6, Figure 10) | | 20 | 50 | nS |
| | Receiver Disable Time | | | 20 | 50 | nS |
| F_{MAX} | Maximum Data Rate | | 2.5 | | | $Mbps$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics

Note 2: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}, \theta_{JA},$ and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: ESD rating based upon human body model, 100pF discharged through 1.5k Ω .

Note 5: Voltage limits apply to DI, DE, RE pins.

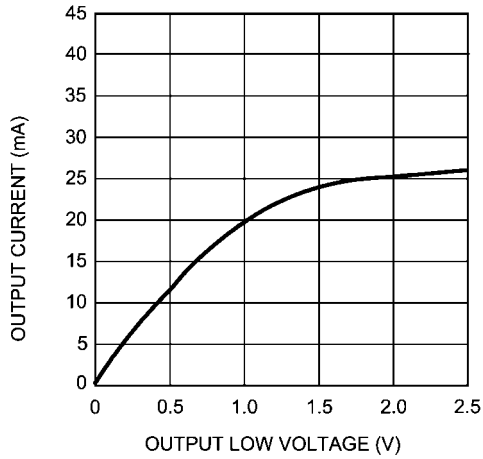
Note 6: Differential input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

Note 7: $|\Delta V_{OD}|$ and $|\Delta V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC} , respectively when the input changes from high to low levels.

Note 8: Peak current

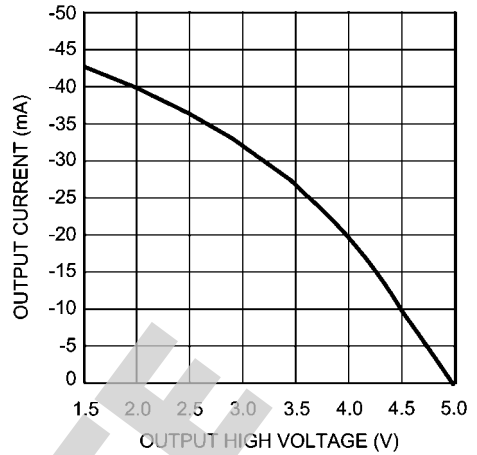
Typical Performance Characteristics

Output Current vs. Receiver Output Low Voltage



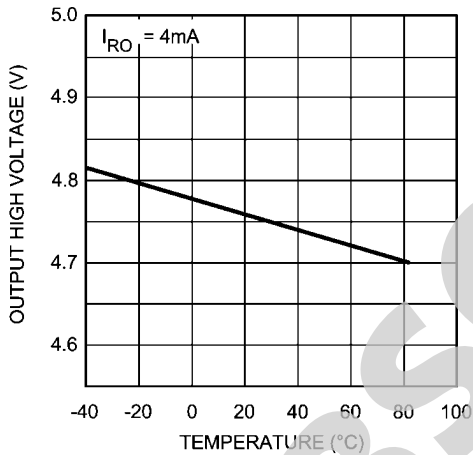
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Output Current vs. Receiver Output High Voltage



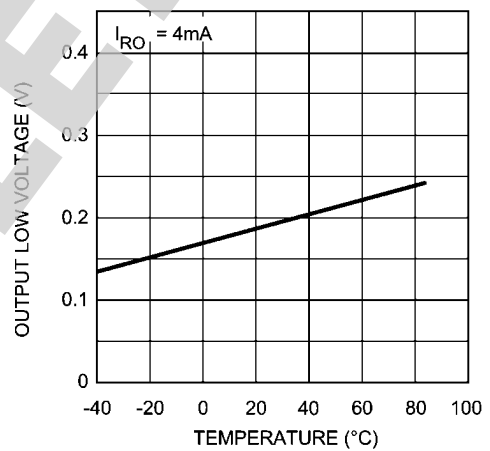
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Receiver Output High Voltage vs. Temperature



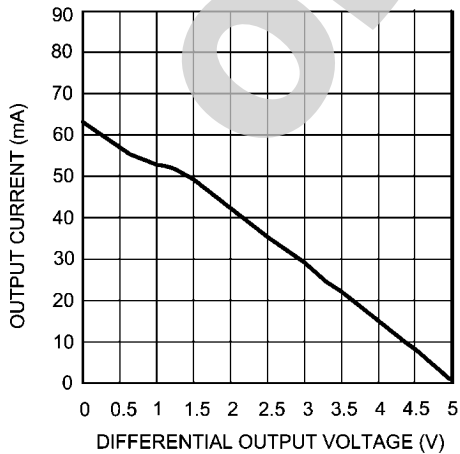
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Receiver Output Low-Voltage vs. Temperature



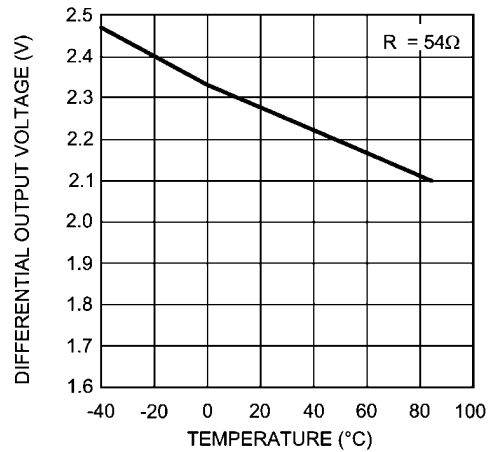
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Driver Output Current vs. Differential Output Voltage



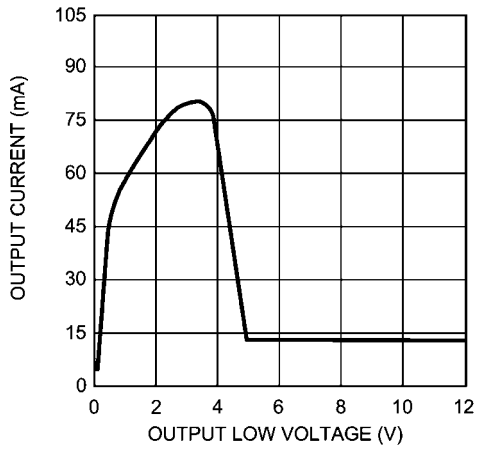
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Driver Differential Output Voltage vs. Temperature



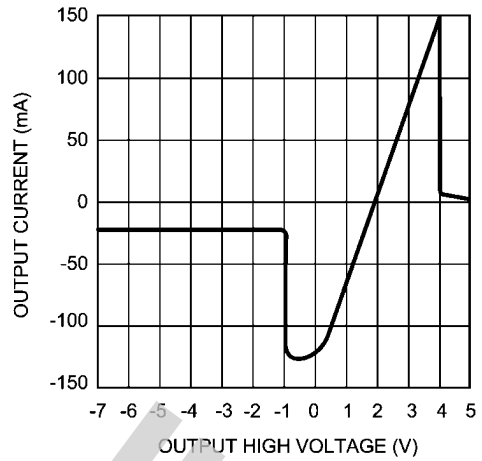
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Output Current vs. Driver Output Low Voltage



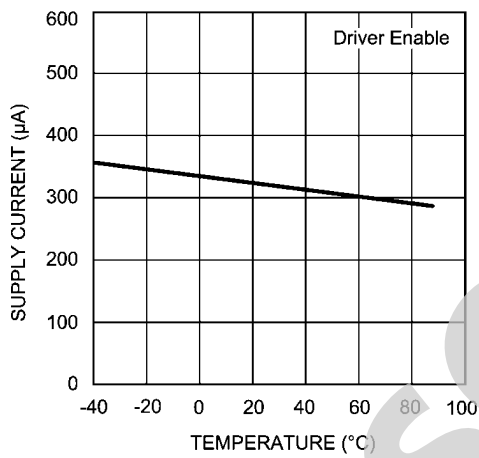
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Output Current vs. Driver Output High Voltage



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Supply Current vs. Temperature



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Parameter Measuring Information

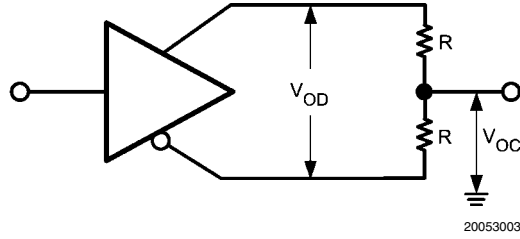


FIGURE 1. Test Circuit for V_{OD} and V_{OC}

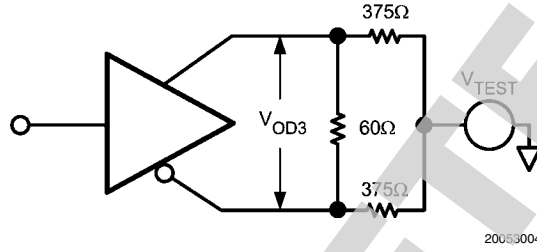


FIGURE 2. Test Circuit for V_{OD3}

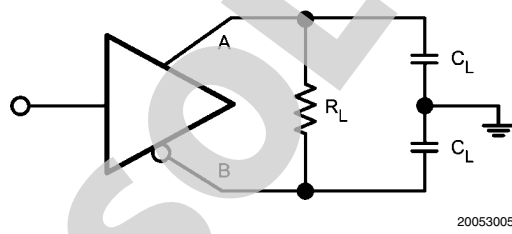


FIGURE 3. Test Circuit for Driver Propagation Delay

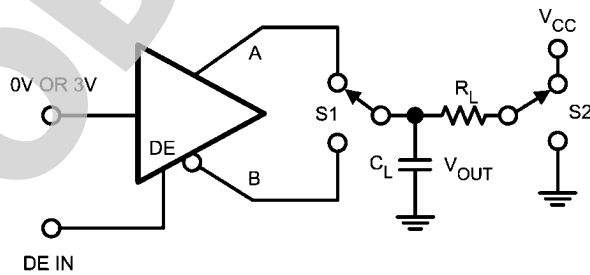


FIGURE 4. Test Circuit for Driver Enable / Disable

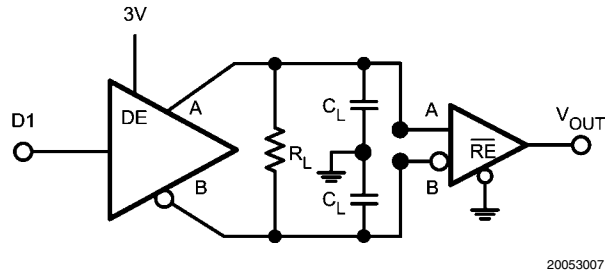


FIGURE 5. Test Circuit for Receiver Propagation Delay

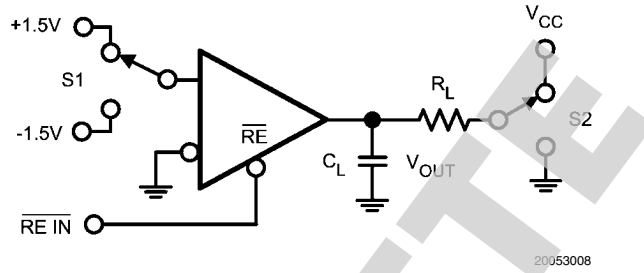
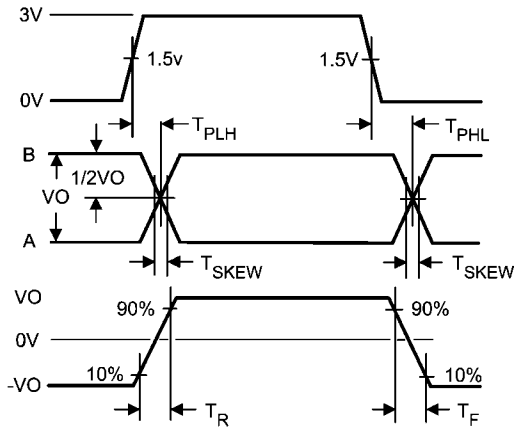


FIGURE 6. Test Circuit for Receiver Enable / Disable

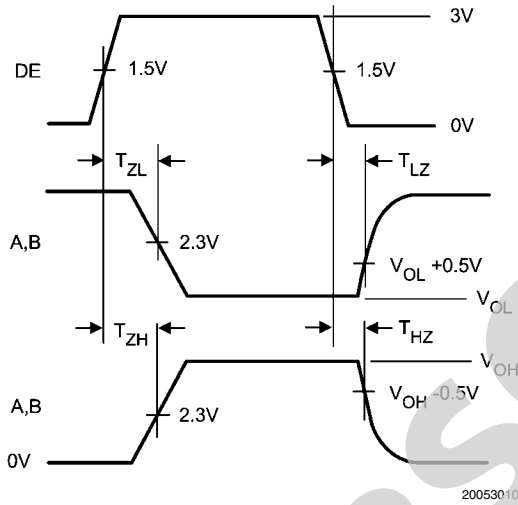
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Switching Characteristics



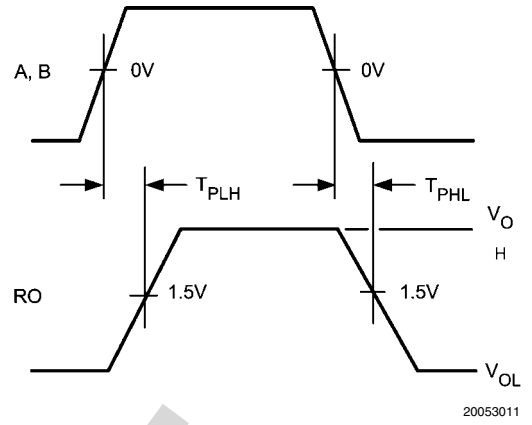
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FIGURE 7. Driver Propagation Delay, Rise / Fall Time



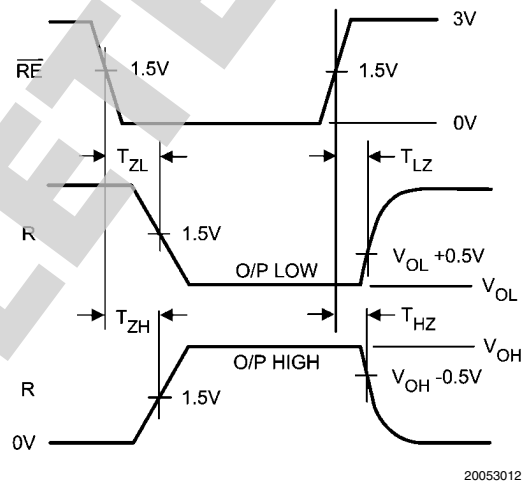
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FIGURE 8. Driver Enable / Disable Time



20053011

FIGURE 9. Receiver Propagation Delay



20053012

FIGURE 10. Receiver Enable / Disable Time

Application Information

POWER LINE NOISE FILTERING

A factor to consider in designing power and ground is noise filtering. A noise filtering circuit is designed to prevent noise generated by the integrated circuit (IC) as well as noise entering the IC from other devices. A common filtering method is to place by-pass capacitors (C_{bp}) between the power and ground lines.

Placing a by-pass capacitor (C_{bp}) with the correct value at the proper location solves many power supply noise problems. Choosing the correct capacitor value is based upon the desired noise filtering range. Since capacitors are not ideal, they

may act more like inductors or resistors over a specific frequency range. Thus, many times two by-pass capacitors may be used to filter a wider bandwidth of noise. It is highly recommended to place a larger capacitor, such as $10\mu\text{F}$, between the power supply pin and ground to filter out low frequencies and a $0.1\mu\text{F}$ to filter out high frequencies.

By-pass capacitors must be mounted as close as possible to the IC to be effective. Long leads produce higher impedance at higher frequencies due to stray inductance. Thus, this will reduce the by-pass capacitor's effectiveness. Surface mounted chip capacitors are the best solution because they have lower inductance.

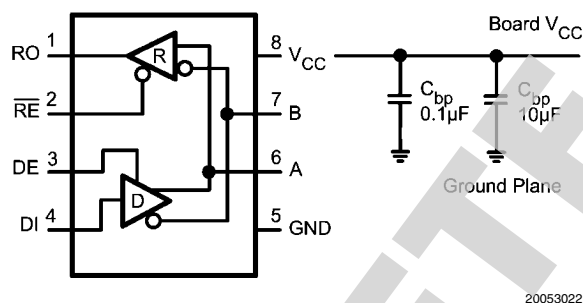
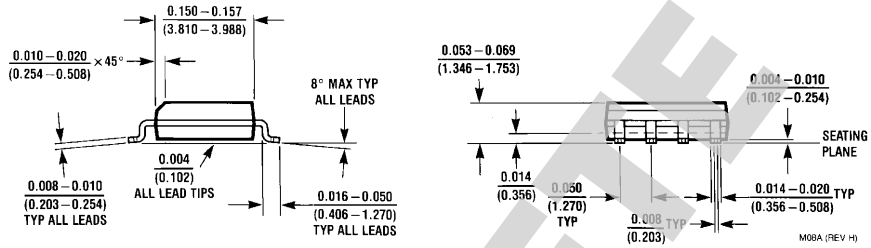
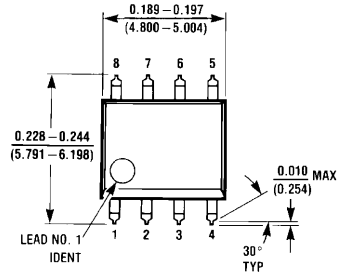
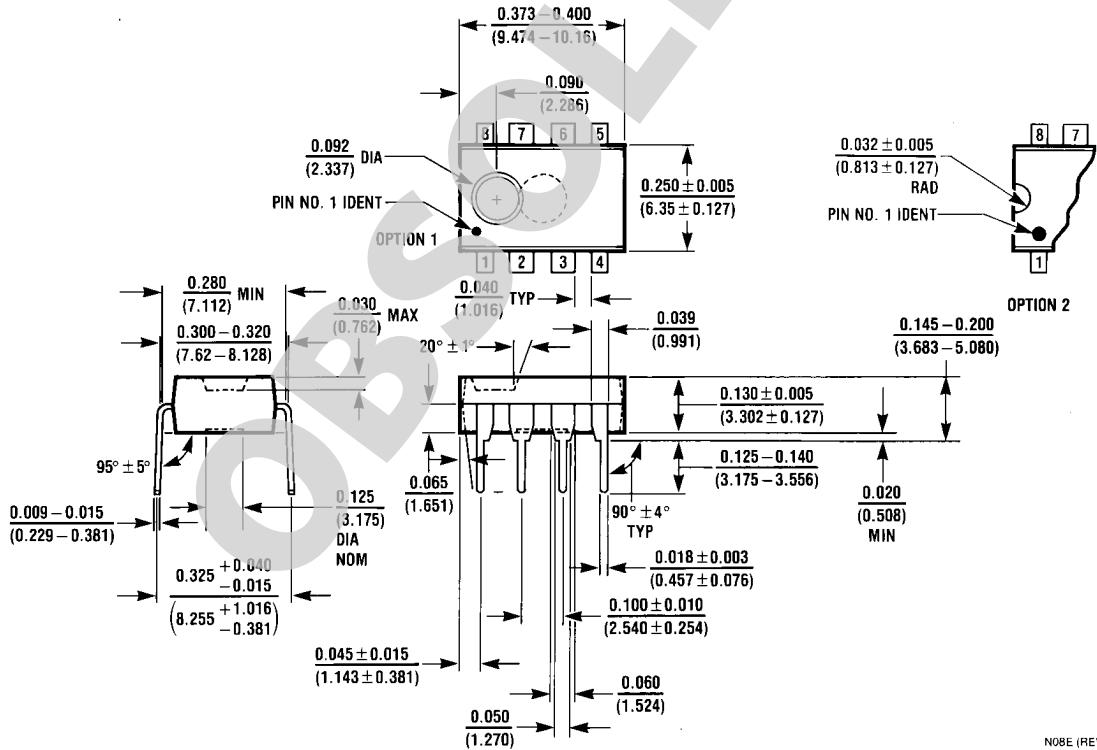


FIGURE 11. Placement of by-pass Capacitors, C_{bp}

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin DIP
NS Package Number N08E

N08E (REV F)

Notes

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Notes

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