



**THE DATASHEET OF  
LM5100CMY/NOPB**



## LM5100A/B/C, LM5101A/B/C 3-A, 2-A, and 1-A High-Voltage, High-Side and Low-Side Gate Drivers

### 1 Features

- Drives Both a High-Side and Low-Side N-Channel MOSFETs
- Independent High- and Low-Driver Logic Inputs
- Bootstrap Supply Voltage up to 118 V DC
- Fast Propagation Times (25-ns Typical)
- Drives 1000-pF Load With 8-ns Rise and Fall Times
- Excellent Propagation Delay Matching (3-ns Typical)
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- Pin Compatible With HIP2100/HIP2101

### 2 Applications

- Current-Fed Push-Pull Converters
- Half and Full Bridge Power Converters
- Synchronous Buck Converters
- Two Switch Forward Power Converters
- Forward with Active Clamp Converters

### 3 Description

The LM5100A/B/C and LM5101A/B/C high-voltage gate drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100 V. The A versions provide a full 3-A of gate drive, while the B and C versions provide 2 A and 1 A, respectively. The outputs are independently controlled with CMOS input thresholds (LM5100A/B/C) or TTL input thresholds (LM5101A/B/C).

An integrated high-voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout is provided on both the low-side and the high-side power rails. These devices are available in the standard SOIC-8 pin, SO PowerPAD-8 pin, and the WSON-10 pin packages. The LM5100C and LM5101C are also available in MSOP-PowerPAD-8 package. The LM5101A is also available in WSON-8 pin package.

#### Device Information<sup>(1)</sup>

PART NUMBER	INPUT THRESHOLD	PEAK OUTPUT CURRENT
LM5100A	CMOS	3 A
LM5101A	TTL	3 A
LM5100B	CMOS	2 A
LM5101B	TTL	2 A
LM5100C	CMOS	1 A
LM5101C	TTL	1 A

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Block Diagram



## Table of Contents

<b>1 Features</b> .....	1	8.3 Feature Description .....	14
<b>2 Applications</b> .....	1	8.4 Device Functional Modes .....	15
<b>3 Description</b> .....	1	<b>9 Application and Implementation</b> .....	16
<b>4 Revision History</b> .....	2	9.1 Application Information .....	16
<b>5 Device Comparison Table</b> .....	3	9.2 Typical Application .....	16
<b>6 Pin Configuration and Functions</b> .....	3	<b>10 Power Supply Recommendations</b> .....	20
<b>7 Specifications</b> .....	5	<b>11 Layout</b> .....	21
7.1 Absolute Maximum Ratings .....	5	11.1 Layout Guidelines .....	21
7.2 ESD Ratings .....	5	11.2 Layout Example .....	21
7.3 Recommended Operating Conditions .....	5	<b>12 Device and Documentation Support</b> .....	22
7.4 Thermal Information .....	6	12.1 Documentation Support .....	22
7.5 Electrical Characteristics .....	6	12.2 Related Links .....	22
7.6 Switching Characteristics .....	8	12.3 Community Resources .....	22
7.7 Typical Characteristics .....	10	12.4 Trademarks .....	22
<b>8 Detailed Description</b> .....	14	12.5 Electrostatic Discharge Caution .....	22
8.1 Overview .....	14	12.6 Glossary .....	22
8.2 Functional Block Diagram .....	14	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	22

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (March 2013) to Revision Q	Page
<ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....</li> </ul>	1

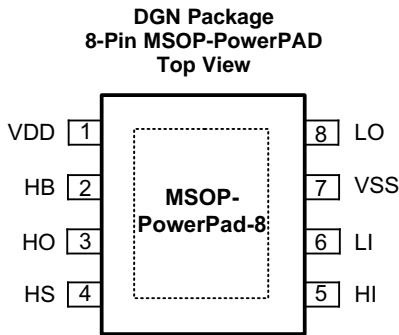
Changes from Revision O (March 2013) to Revision P	Page
<ul style="list-style-type: none"> <li>Changed layout of National Data Sheet to TI format .....</li> </ul>	19

## 5 Device Comparison Table

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5100A, LM5100C	WSON (10)	4.00 mm × 4.00 mm
	SO PowerPAD™ (8)	3.90 mm × 4.89 mm
	SOIC (8)	3.91 mm × 4.90 mm
LM5100B, LM5101B	WSON (10)	4.00 mm × 4.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
LM5101A	WSON (8)	4.00 mm × 4.00 mm
	WSON (10)	4.00 mm × 4.00 mm
	SO PowerPAD (8)	3.90 mm × 4.89 mm
	SOIC (8)	3.91 mm × 4.90 mm
LM5101C	MSOP PowerPAD (8)	3.00 mm × 3.00 mm
	WSON (10)	4.00 mm × 4.00 mm
	SOIC (8)	3.91 mm × 4.90 mm

## 6 Pin Configuration and Functions





### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	8 PINS	10 PINS <sup>(1)</sup>		
HB	2	2	I	High-side gate driver bootstrap supply. Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
HI	5	7	I	High-side driver control input. The LM5100A/B/C inputs have CMOS type thresholds. The LM5101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
HO	3	3	O	High-side gate driver output. Connect to the gate of high-side MOSFET with a short, low inductance path.
HS	4	4	—	High-side MOSFET source connection. Connect to the bootstrap capacitor negative terminal and the source of the high-side MOSFET.
LI	6	8	I	Low-side driver control input. The LM5100A/B/C inputs have CMOS type thresholds. The LM5101A/B/C inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
LO	8	10	O	Low-side gate driver output. Connect to the gate of the low-side MOSFET with a short, low inductance path.
VDD	1	1	I	Positive gate drive supply. Locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
VSS	7	9	—	Ground return. All signals are referenced to this ground.
EP <sup>(2)</sup>			—	TI recommends that the exposed pad on the bottom of the package is soldered to ground plane on the PC board, and that ground plane should extend out from beneath the IC to help dissipate heat.

(1) For WSON-10 package, pins 5 and 6 have no connection.

(2) Exposed pad is not available on the 8-pin SOIC package.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 See <sup>(1)(2)</sup>

	MIN	MAX	UNIT
VDD to VSS	-0.3	18	V
HB to HS	-0.3	18	V
LI or HI input	-0.3	$V_{DD} + 0.3$	V
LO output	-0.3	$V_{DD} + 0.3$	V
HO output	$V_{HS} - 0.3$	$V_{HB} + 0.3$	V
HS to VSS <sup>(3)</sup>	-5	100	V
HB to VSS		118	V
Junction temperature		150	°C
Storage temperature	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military or Aerospace specified devices are required, contact the Texas Instruments Sales Office or Distributors for availability and specifications.
- (3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed  $-1$  V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than  $V_{DD} - 15$  V. For example if  $V_{DD} = 10$  V, the negative transients at HS must not exceed  $-5$  V.

### 7.2 ESD Ratings

		VALUE	UNIT	
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$	V	
	Machine Model (MM) <sup>(2)</sup>	Option A		50
		Option B and C		100

- (1) The Human Body Model (HBM) is a 100-pF capacitor discharged through a 1.5-k $\Omega$  resistor into each pin. 2 kV for all pins except Pin 2, Pin 3 and Pin 4 which are rated at 1000 V for HBM.
- (2) Machine Model (MM) ratings are: 100 V(MM) for Options B and C; 50 V(MM) for Option A.

### 7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
VDD	9		14	V
HS	-1		100	V
HB	$V_{HS} + 8$		$V_{HS} + 14$	V
HS slew rate			< 50	V/ns
Junction temperature	-40		125	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM5100A, LM5100C, LM5101A	LM5101C	LM5101A	LM5100x, LM5101x		UNIT
		SO PowerPAD	MSOP- PowerPAD <sup>(2)</sup>	WSON <sup>(2)</sup>	WSON <sup>(2)</sup>	SOIC	
		8 PINS	8 PINS	8 PINS	10 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(3)</sup>	40	80	37.8	40	170	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	—	—	36.7	—	—	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	—	—	14.9	—	—	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	—	—	0.3	—	—	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	—	—	15.2	—	—	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	4.4	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) 4-layer board with Cu finished thickness 1.5, 1, 1, 1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50-mm x 50-mm ground and power planes embedded in PCB. See Application Note AN-1187 ([SNOA401](#)).
- (3) The R<sub>θJA</sub> is not a given constant for the package and depends on the printed circuit board design and the operating environment.

## 7.5 Electrical Characteristics

unless otherwise specified, limits are for T<sub>J</sub> = 25°C, V<sub>DD</sub> = V<sub>HB</sub> = 12 V, V<sub>SS</sub> = V<sub>HS</sub> = 0 V, no load on LO or HO<sup>(1)</sup>.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENTS</b>							
I <sub>DD</sub>	VDD quiescent current, LM5100A/B/C	LI = HI = 0 V	T <sub>J</sub> = 25°C	0.1		0.2	mA
			T <sub>J</sub> = -40°C to 125°C				
	VDD quiescent current, LM5101A/B/C	LI = HI = 0 V	T <sub>J</sub> = 25°C	0.25		0.4	mA
			T <sub>J</sub> = -40°C to 125°C				
I <sub>DDO</sub>	VDD operating current	f = 500 kHz	T <sub>J</sub> = 25°C	2		3	mA
			T <sub>J</sub> = -40°C to 125°C				
I <sub>HB</sub>	Total HB quiescent current	LI = HI = 0 V	T <sub>J</sub> = 25°C	0.06		0.2	mA
			T <sub>J</sub> = -40°C to 125°C				
I <sub>HBO</sub>	Total HB operating current	f = 500 kHz	T <sub>J</sub> = 25°C	1.6		3	mA
			T <sub>J</sub> = -40°C to 125°C				
I <sub>HBS</sub>	HB to VSS current, quiescent	HS = HB = 100 V	T <sub>J</sub> = 25°C	0.1		10	μA
			T <sub>J</sub> = -40°C to 125°C				
I <sub>HBSO</sub>	HB to VSS current, operating	f = 500 kHz		0.4			mA
<b>INPUT PINS</b>							
V <sub>IL</sub>	Input voltage threshold LM5100A/B/C	Rising Edge	T <sub>J</sub> = 25°C	5.4		6.3	V
			T <sub>J</sub> = -40°C to 125°C	4.5			
V <sub>IL</sub>	Input voltage threshold LM5101A/B/C	Rising Edge	T <sub>J</sub> = 25°C	1.8		2.3	V
			T <sub>J</sub> = -40°C to 125°C	1.3			
V <sub>IHYS</sub>	Input voltage hysteresis LM5100A/B/C			500			mV
V <sub>IHYS</sub>	Input voltage hysteresis LM5101A/B/C			50			mV
R <sub>I</sub>	Input pulldown resistance		T <sub>J</sub> = 25°C	200		400	kΩ
			T <sub>J</sub> = -40°C to 125°C	100			

- (1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

## Electrical Characteristics (continued)

unless otherwise specified, limits are for  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{SS} = V_{HS} = 0\text{ V}$ , no load on LO or HO <sup>(1)</sup>.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>UNDER VOLTAGE PROTECTION</b>							
$V_{DDR}$	VDD rising threshold	$T_J = 25^\circ\text{C}$		6.9		7.4	V
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		6			
$V_{DDH}$	VDD threshold hysteresis			0.5			V
$V_{HBR}$	HB rising threshold	$T_J = 25^\circ\text{C}$		6.6		7.1	V
		$T_J = -40^\circ\text{C to } 125^\circ\text{C}$		5.7			
$V_{HBH}$	HB threshold hysteresis			0.4			V
<b>BOOT STRAP DIODE</b>							
$V_{DL}$	Low-current forward voltage	$I_{VDD-HB} = 100\ \mu\text{A}$	$T_J = 25^\circ\text{C}$	0.52		0.85	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
$V_{DH}$	High-current forward voltage	$I_{VDD-HB} = 100\ \text{mA}$	$T_J = 25^\circ\text{C}$	0.8		1	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
$R_D$	Dynamic resistance LM5100A/B/C, LM5101A/B/C	$I_{VDD-HB} = 100\ \text{mA}$	$T_J = 25^\circ\text{C}$	1.0		1.65	$\Omega$
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
<b>LO AND HO GATE DRIVER</b>							
$V_{OL}$	Low-level output voltage LM5100A/LM5101A	$I_{HO} = I_{LO} = 100\ \text{mA}$	$T_J = 25^\circ\text{C}$	0.12		0.25	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
	Low-level output voltage LM5100B/LM5101B		$T_J = 25^\circ\text{C}$	0.16		0.4	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
	Low-level output voltage LM5100C/LM5101C		$T_J = 25^\circ\text{C}$	0.28		0.65	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
$V_{OH}$	High-level output voltage LM5100A/LM5101A	$I_{HO} = I_{LO} = 100\ \text{mA}$ $V_{OH} = V_{DD} - LO$ or $V_{OH} = HB - HO$	$T_J = 25^\circ\text{C}$	0.24		0.45	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
	High-level output voltage LM5100B/LM5101B		$T_J = 25^\circ\text{C}$	0.28		0.60	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
	High-level output voltage LM5100C/LM5101C		$T_J = 25^\circ\text{C}$	0.6		1.10	V
			$T_J = -40^\circ\text{C to } 125^\circ\text{C}$				
$I_{OHL}$	Peak pullup current LM5100A/LM5101A	HO, LO = 0 V	$T_J = 25^\circ\text{C}$	3		A	
	Peak pullup current LM5100B/LM5101B			2			
	Peak pullup current LM5100C/LM5101C			1			
$I_{OLL}$	Peak pulldown current LM5100A/LM5101A	HO, LO = 12 V	$T_J = 25^\circ\text{C}$	3		A	
	Peak pulldown current LM5100B/LM5101B			2			
	Peak pulldown current LM5100C/LM5101C			1			

## 7.6 Switching Characteristics

Limits in standard type are for  $T_J = 25^\circ\text{C}$  only; limits in boldface type apply over the junction temperature ( $T_J$ ) range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{SS} = V_{HS} = 0\text{ V}$ , No Load on LO or HO <sup>(1)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LPHL}$	LO turnoff propagation delay LM5100A/B/C	LI Falling to LO Falling		20	45	ns
	LO turnoff propagation delay LM5101A/B/C			22	56	ns
$t_{LPLH}$	LO turnon propagation delay LM5100A/B/C	LI Rising to LO Rising		20	45	ns
	LO turnon propagation delay LM5101A/B/C			26	56	ns
$t_{HPHL}$	HO turnoff propagation delay LM5100A/B/C	HI Falling to HO Falling		20	45	ns
	HO turnoff propagation delay LM5101A/B/C			22	56	ns
$t_{HPLH}$	LO turnon propagation delay LM5100A/B/C	HI Rising to HO Rising		20	45	ns
	LO turnon propagation delay LM5101A/B/C			26	56	ns
$t_{MON}$	Delay matching: LO on and HO off LM5100A/B/C			1	10	ns
	Delay matching: LO on and HO off LM5101A/B/C			4	10	ns
$t_{MOFF}$	Delay matching: LO off and HO on LM5100A/B/C			1	10	ns
	Delay matching: LO on and HO off LM5101A/B/C			4	10	ns
$t_{RC}, t_{FC}$	Either output rise and fall time	$C_L = 1000\text{ pF}$		8		ns
$t_R$	Output rise time (3 V to 9 V) LM5100A/LM5101A	$C_L = 0.1\text{ }\mu\text{F}$		430		ns
	Output rise time (3 V to 9 V) LM5100B/LM5101B			570		ns
	Output rise time (3 V to 9 V) LM5100C/LM5101C			990		ns
$t_F$	Output fall time (3 V to 9 V) LM5100A/LM5101A	$C_L = 0.1\text{ }\mu\text{F}$		260		ns
	Output fall time (3 V to 9 V) LM5100B/LM5101B			430		ns
	Output fall time (3 V to 9 V) LM5100C/LM5101C			715		ns
$t_{PW}$	Minimum input pulse width that changes the output			50		ns
$t_{BS}$	Bootstrap diode reverse recovery time	$I_F = 100\text{ mA}$ , $I_R = 100\text{ mA}$		37		ns

(1) Minimum and maximum limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).



**Figure 1. Timing Diagram**

## 7.7 Typical Characteristics

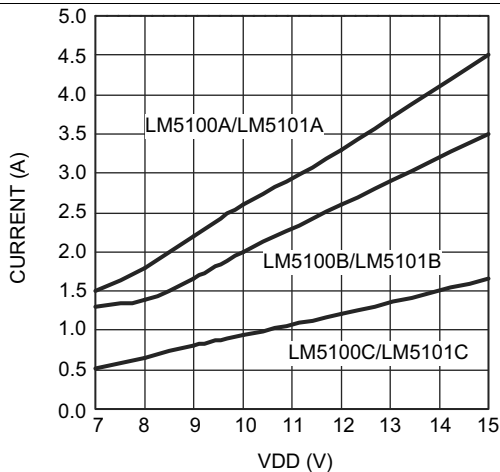


Figure 2. Peak Sourcing Current vs VDD

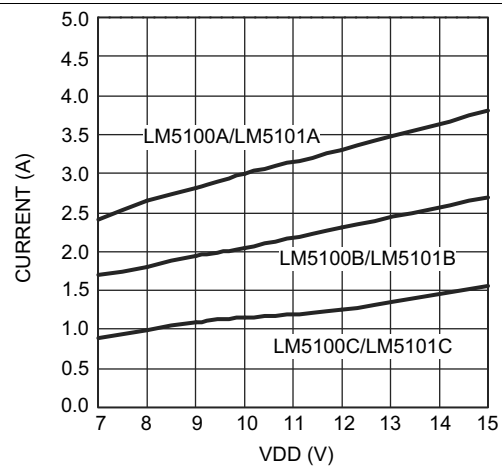


Figure 3. Peak Sinking Current vs VDD

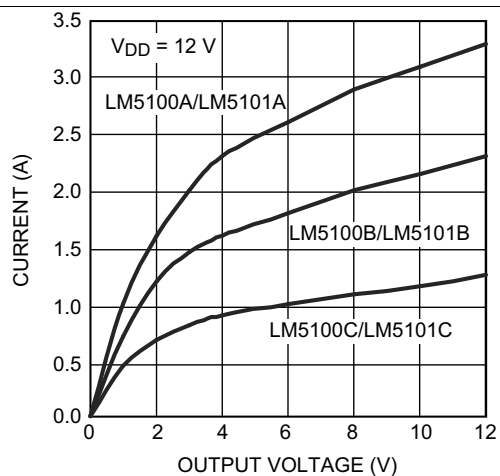


Figure 4. Sink Current vs Output Voltage

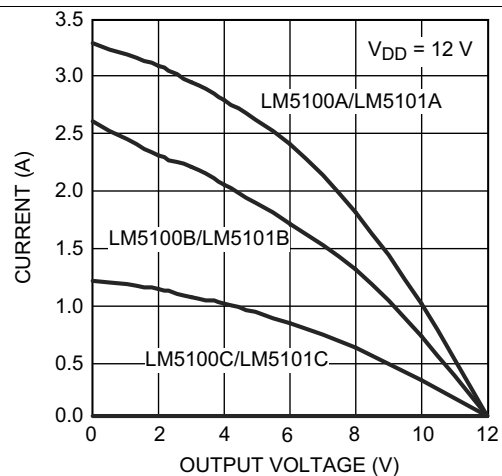


Figure 5. Source Current vs Output Voltage

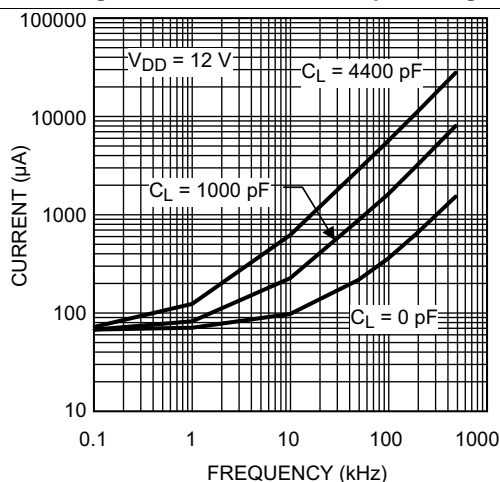


Figure 6. LM5100A/B/C  $I_{DD}$  vs Frequency

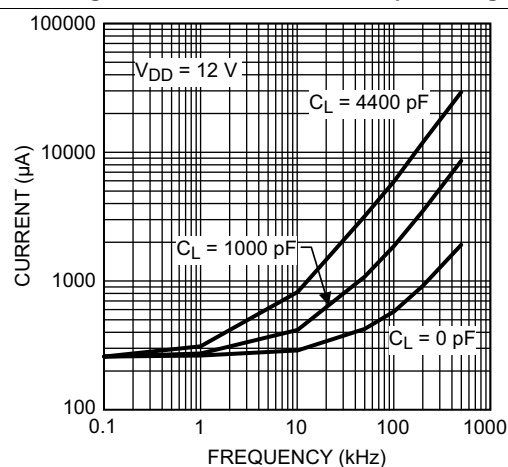


Figure 7. LM5101A/B/C  $I_{DD}$  vs Frequency

Typical Characteristics (continued)

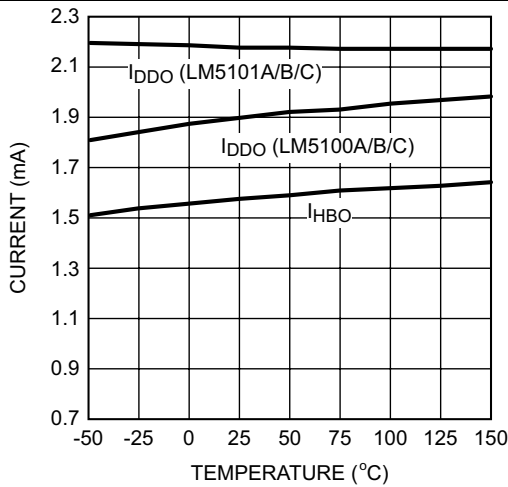


Figure 8. Operating Current vs Temperature

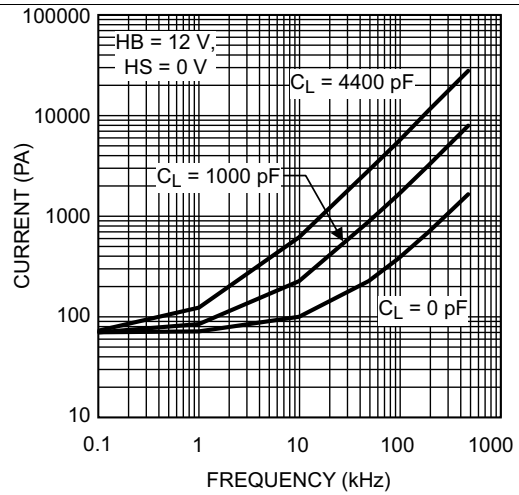


Figure 9.  $I_{HB}$  vs Frequency

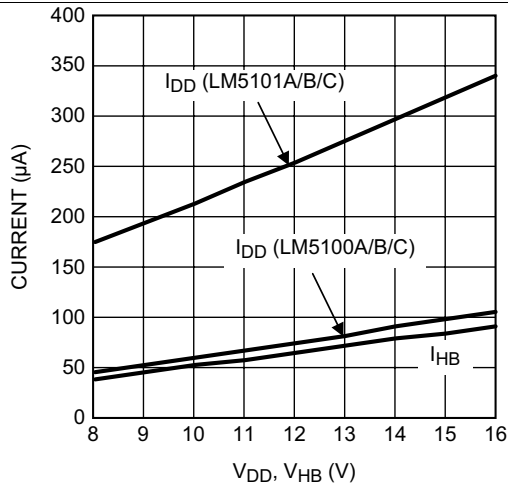


Figure 10. Quiescent Current vs Supply Voltage

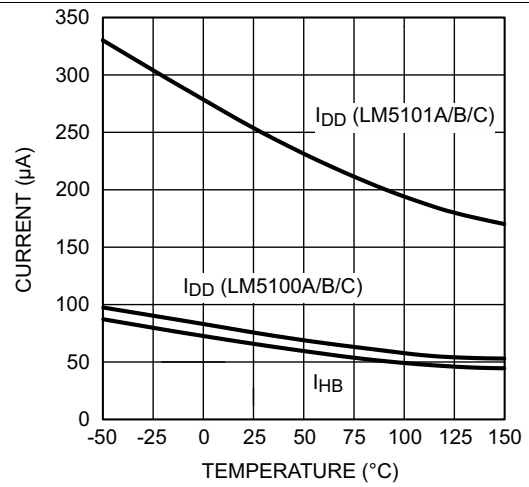


Figure 11. Quiescent Current vs Temperature

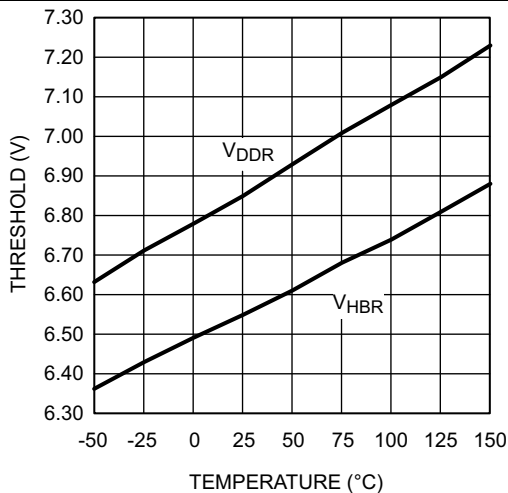


Figure 12. Undervoltage Rising Thresholds vs Temperature

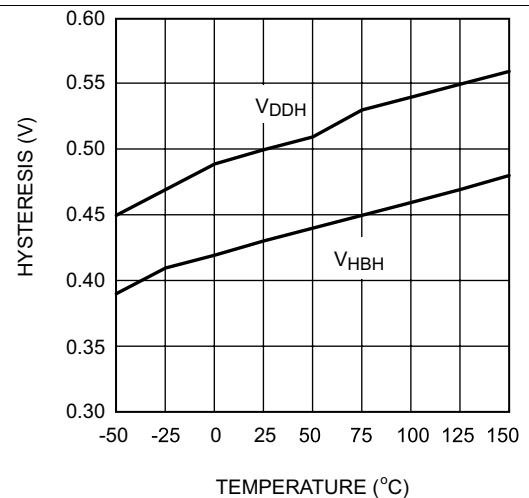


Figure 13. Undervoltage Threshold Hysteresis vs Temperature

Typical Characteristics (continued)

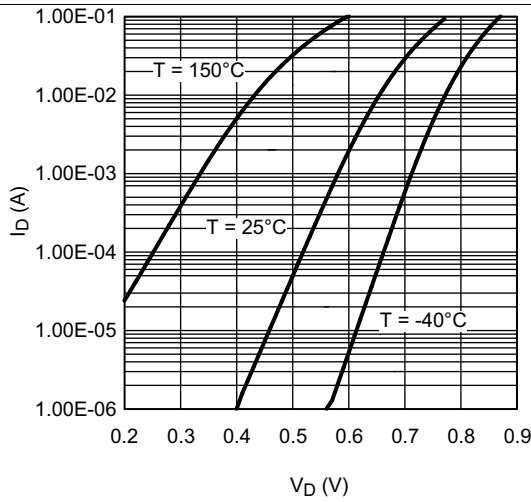


Figure 14. Bootstrap Diode Forward Voltage

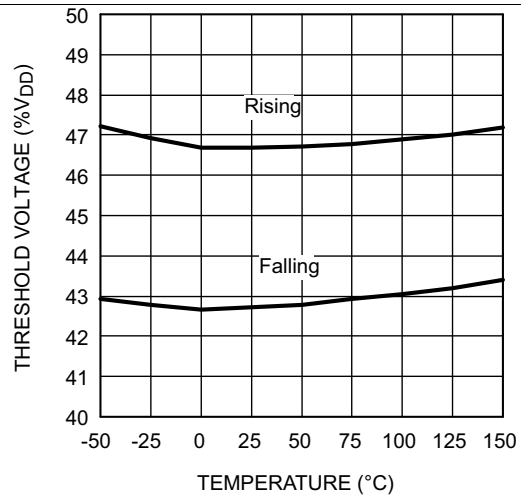


Figure 15. LM5100A/B/C Input Threshold vs Temperature

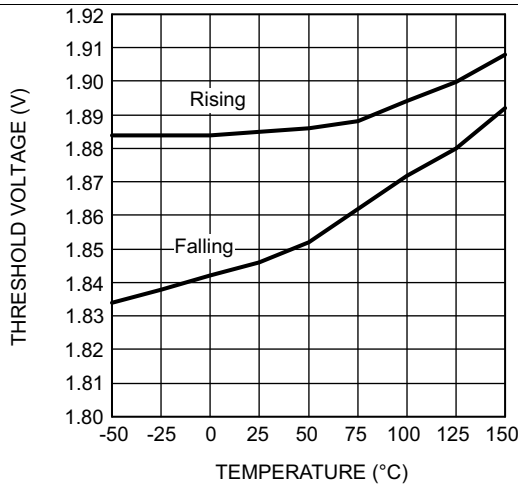


Figure 16. LM5101A/B/C Input Threshold vs Temperature

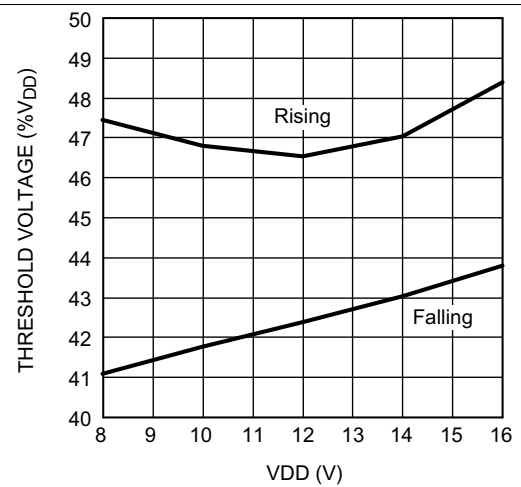


Figure 17. LM5100A/B/C Input Threshold vs VDD

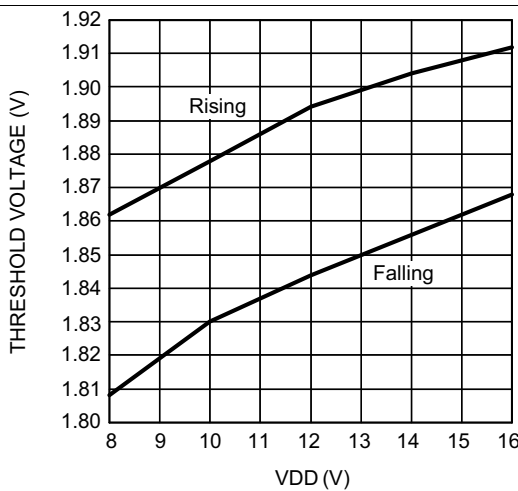


Figure 18. LM5101A/B/C Input Threshold vs VDD

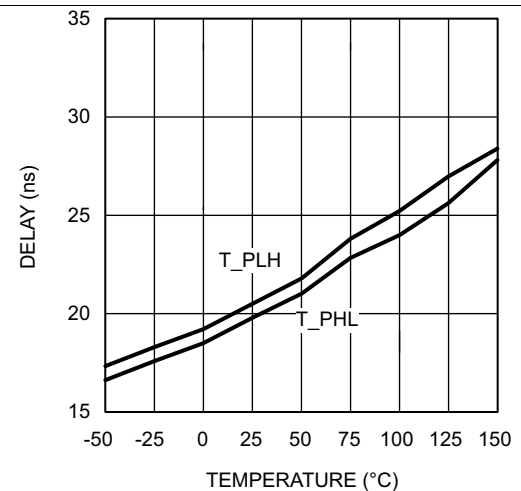


Figure 19. LM5100A/B/C Propagation Delay vs Temperature

Typical Characteristics (continued)

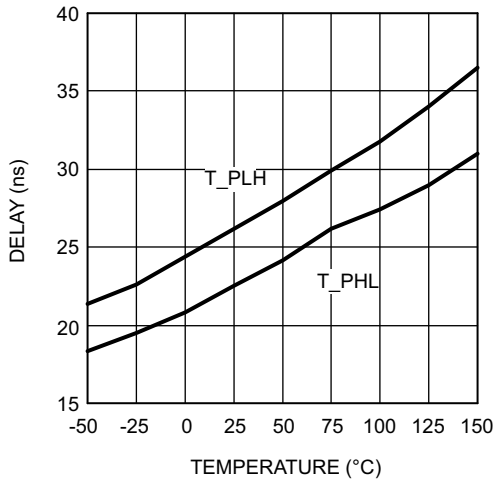


Figure 20. LM5101A/B/C Propagation Delay vs Temperature

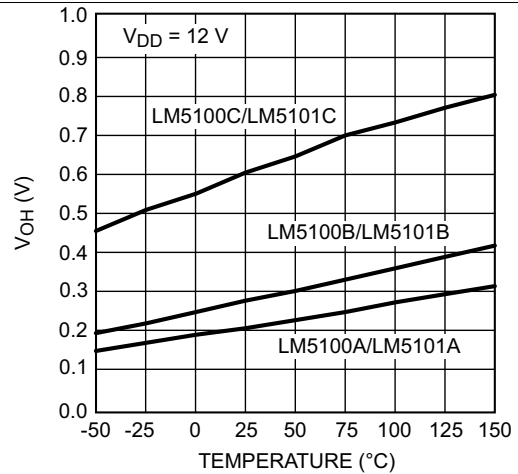


Figure 21. LO and HO Gate Drive - High Level Output Voltage vs Temperature

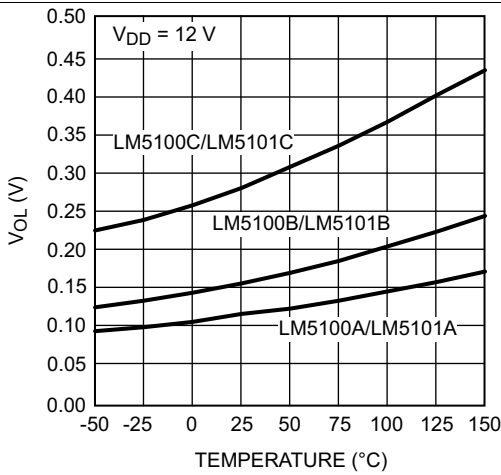


Figure 22. LO and HO Gate Drive - Low Level Output Voltage vs Temperature

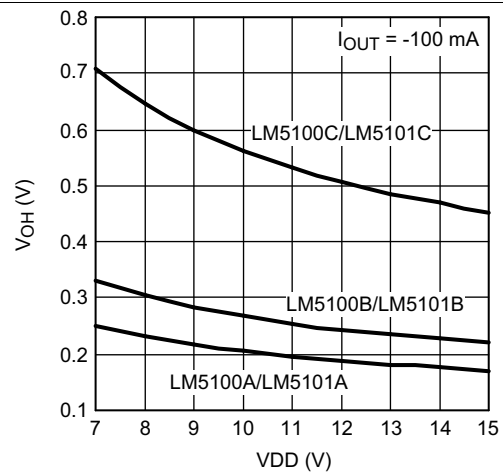


Figure 23. LO and HO Gate Drive - Output High Voltage vs VDD

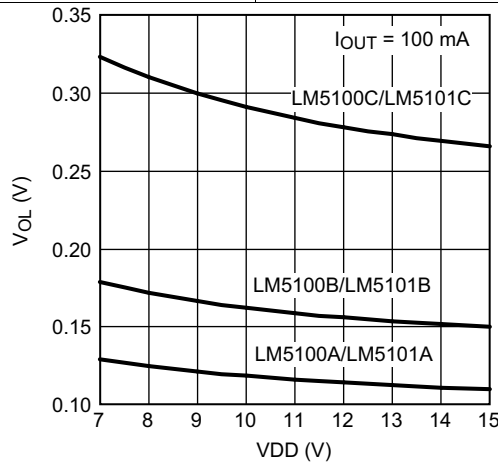


Figure 24. LO and HO Gate Drive - Output Low Voltage vs VDD

## 8 Detailed Description

### 8.1 Overview

The LM5100A/B/C and LM5101A/B/C are designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The outputs are independently controlled with CMOS input thresholds (LM5101A/B/C) or TTL input thresholds (LM5101A/B/C). The floating high-side driver is capable of working with supply voltages up to 100 V. An integrated high voltage diode is provided to charge high side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Start-up and UVLO

Both high and low-side drivers include under voltage lockout (UVLO) protection circuitry which monitors the supply voltage ( $V_{DD}$ ) and bootstrap capacitor voltage ( $V_{HB-HS}$ ) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the  $V_{DD}$  pin of the LM5100A/B/C and LM5101A/B/C, the outputs of the low-side and high-side are held low until  $V_{DD}$  exceeds the UVLO threshold, typically about 6.6 V. Any UVLO condition on the bootstrap capacitor will disable only the high-side output (HO).

#### 8.3.2 Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

## Feature Description (continued)

### 8.3.3 Bootstrap Diode

The bootstrap diode necessary to generate the high-side bias is included in the LM5100/1 family. The diode anode is connected to  $V_{DD}$  and cathode connected to  $V_{HB}$ . With the  $V_{HB}$  capacitor connected to HB and the HS pins, the  $V_{HB}$  capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

### 8.3.4 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from  $V_{DD}$  to  $V_{SS}$  and the high-side is referenced from  $V_{HB}$  to  $V_{HS}$ .

## 8.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See [Start-up and UVLO](#) for more information on UVLO operation mode. In normal mode, the output stage is dependent on the states of the HI and LI pins.

**Table 1. Input/Output Logic Table**

HI	LI	HO <sup>(1)</sup>	LO <sup>(2)</sup>
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
x <sup>(3)</sup>	x	L	L

- (1) HO is measured with respect to the HS.
- (2) LO is measured with the respect to the VSS.
- (3) x is floating condition



## Typical Application (continued)

### 9.2.1 Design Requirements

See [Table 2](#) for the parameter and values.

**Table 2. Operating Parameters**

PARAMETER	VALUE
Gate Driver	LM5101A
MOSFET	CSD18531Q5A
VDD	10 V
Qgmax	43 nC
Fsw	100 kHz
Dmax	95%
I <sub>HBS</sub>	10 μA
V <sub>DH</sub>	1.0 V
V <sub>HBR</sub>	7.1 V
V <sub>HBH</sub>	0.4 V

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Select Bootstrap and VDD capacitor

The bootstrap capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit in any circumstances during normal operation. Calculate the maximum allowable drop across the bootstrap capacitor with [Equation 1](#).

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = 10 \text{ V} - 1.0 \text{ V} - 6.7 \text{ V} = 2.3 \text{ V}$$

where

- V<sub>DD</sub> = Supply voltage of the gate drive IC
- V<sub>DH</sub> = Bootstrap diode forward voltage drop
- V<sub>HBL</sub> = V<sub>HBR</sub> - V<sub>HBH</sub> = 6.7 V, HB falling threshold

The quiescent current of the bootstrap circuit is 10 μA, which is negligible compared to the Q<sub>gs</sub> of the MOSFET (see [Equation 2](#) and [Equation 3](#)).

$$Q_{TOTAL} = Q_{gmax} + I_{HBS} \frac{D_{MAX}}{F_{SW}} = 43 \text{ nC} + 10 \mu\text{A} \frac{0.95}{100 \text{ kHz}} = 43.01 \text{ nC} \quad (2)$$

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{HB}} = \frac{43.01 \text{ nC}}{2.3 \text{ V}} = 18.7 \text{ nF} \quad (3)$$

In practice the value for the C<sub>BOOT</sub> capacitor should be greater than that calculated to allow for situations where the power stage may skip pulse due to load transients. It is recommended to place the bootstrap capacitor as close to the HB and HS pins as possible.

$$C_{BOOT} = 100 \text{ nF} \quad (4)$$

As a general rule the local VDD bypass capacitor should be 10 times greater than the value of C<sub>BOOT</sub>.

$$C_{VDD} = 10 \times C_{BOOT} = 1 \mu\text{F} \quad (5)$$

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum VDD to allow for loss of capacitance once the devices have a DC bias voltage across them and to ensure long-term reliability of the devices.

### 9.2.2.2 Select External Bootstrap Diode and Resistor

The bootstrap capacitor is charged by the VDD through the internal bootstrap diode every cycle when low side MOSFET turns on. The charging of the capacitor involves high peak currents, and therefore transient power dissipation in the internal bootstrap diode may be significant and dependent on its forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver and need to be considered in the gate driver IC power dissipation.

For high frequency and high capacitive loads, it may be necessary to consider using an external bootstrap diode placed in parallel with internal bootstrap diode to reduce power dissipation of the driver. For the selection of external bootstrap diodes for LM510x device, please refer to the application note [SNVA083](#).

Bootstrap resistor  $R_{BOOT}$  is selected to reduce the inrush current in  $D_{BOOT}$  and limit the ramp up slew rate of voltage of HB-HS. It is recommended that  $R_{BOOT}$  is between 2  $\Omega$  and 10  $\Omega$ . For this design, a current limiting resistor of 2.2  $\Omega$  is selected to limit inrush current of bootstrap diode.

$$I_{D_{BOOT}(pk)} = \frac{V_{DD} - V_{D_{BOOT}}}{R_{BOOT}} = \frac{10\text{ V} - 0.6\text{ V}}{2.2\ \Omega} = 4.27\text{ A} \quad (6)$$

### 9.2.2.3 Select Gate driver Resistor

Resistor  $R_{GATE}$  is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver. For this design 4.7- $\Omega$  resistors were selected for this design. Maximum HO and LO drive current are calculated by [Equation 7](#) through [Equation 10](#).

$$I_{HOH} = \frac{V_{DD} - V_{DH} - V_{OH}}{R_{GATE}} = \frac{10\text{ V} - 1.0\text{ V} - 0.45\text{ V}}{4.7\ \Omega} = 1.819\text{ A} \quad (7)$$

$$I_{LOH} = \frac{V_{DD} - V_{OH}}{R_{GATE}} = \frac{10\text{ V} - 0.45\text{ V}}{4.7\ \Omega} = 2.032\text{ A} \quad (8)$$

$$I_{HOL} = \frac{V_{DD} - V_{DH} - V_{OL}}{R_{GATE}} = \frac{10\text{ V} - 1.0\text{ V} - 0.25\text{ V}}{4.7\ \Omega} = 1.862\text{ A} \quad (9)$$

$$I_{LOL} = \frac{V_{DD} - V_{OH}}{R_{GATE}} = \frac{10\text{ V} - 0.25\text{ V}}{4.7\ \Omega} = 2.074\text{ A}$$

where

- $I_{HOH}$  = Maximum HO source current
  - $I_{LOH}$  = Maximum LO source current
  - $I_{HOL}$  = Maximum HO sink current
  - $I_{LOH}$  = Maximum HO sink current
  - $V_{OH}$  = High-Level output voltage drop across HB to HO or VDD to LO
  - $V_{OL}$  = Low-Level output voltage drop across HO to HS or LO to GND
- (10)

### 9.2.2.4 Estimate the Driver Power Losses

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency ( $f_{sw}$ ), output load capacitance on LO and HO ( $C_L$ ), and supply voltage (VDD). The gate charge losses can be calculated by [Equation 11](#).

$$P_{DGATES} = 2 \times V_{DD}^2 \times C_L \times f_{sw} \quad (11)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with [Equation 11](#). [Figure 26](#) can be used to approximate the power losses due to the gate drivers.



**Figure 26. Gate Driver Power Dissipation (LO + HO)**  
**V<sub>DD</sub> = 12 V, Neglecting Diode Losses**

The internal bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages ( $V_{IN}$ ) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculation and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the internal diode power dissipation. If the diode losses can be significant, an external diode placed in parallel with the internal bootstrap diode can be helpful to reduce power dissipation within the IC.



**Figure 27. Diode Power Dissipation V<sub>IN</sub> = 50 V**

The total IC power dissipation can be estimated from the plots shown in [Figure 26](#) and [Figure 27](#) by summing the gate drive losses with the internal bootstrap diode losses for the intended application. For a given ambient temperature, the maximum allowable power loss of the IC can be defined as equation [Equation 12](#).

$$P_{\text{loss}} = \frac{T_J - T_A}{R_{\theta JA}}$$

where

- $P_{\text{loss}}$  = The total power dissipation of the driver
- $T_J$  = Junction temperature
- $T_A$  = Ambient temperature
- $R_{\theta JA}$  = Junction-to-ambient thermal resistance

(12)

The thermal metrics for the driver package is summarized in the *Thermal Information* table. For detailed information regarding the thermal information table, refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* [SPRA953](#).

### 9.2.3 Application Curves



Figure 28. H/LI to HO/LO Turnon Propagation Delay



Figure 29. H/LI to HO/LO Turnoff Propagation Delay

## 10 Power Supply Recommendations

The bias supply voltage range for which the device is rated to operate is from 9 V to 14 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the VDDR supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 18-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 4-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 14 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDDH. Therefore, ensuring that, while operating at or near the 9-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the VDD pin voltage has dropped below the threshold ( $V_{DDR} - V_{DDH}$ ), which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start up, the device does not begin operation until the VDD pin voltage has exceeded above the  $V_{DDR}$  threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Keep in mind that the charge for source current pulses delivered by the LO pin is also supplied through the same VDD pin. As a result, every time a current is sourced out of the LO pin a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that a local bypass capacitor is provided between the VDD and GND pins and located as close as possible to the device for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is necessary. TI recommends using two capacitors between VDD and GND: a 100-nF ceramic surface-mount capacitor that can be nudged very close to the pins of the device and another surface-mount capacitor in the range 0.22  $\mu$ F to 10  $\mu$ F added in parallel. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore, a 0.022- $\mu$ F to 1- $\mu$ F local decoupling capacitor is recommended between the HB and HS pins.

## 11 Layout

### 11.1 Layout Guidelines

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. Low-ESR/ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turnon of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
  - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
  - The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

A recommended layout pattern for the driver is shown in [Figure 30](#). If possible a single layer placement is preferred.

### 11.2 Layout Example



**Figure 30. PCB Layout Recommendation**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

- *AN-1187 Leadless Leadframe Package (LLP)* ([SNOA401](#))
- *AN-1317 Selection of External Bootstrap Diode for LM510X Devices* ([SNVA083](#))
- *Semiconductor and IC Package Thermal Metrics* ([SPRA953](#))

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM5100A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM5100B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM5100C	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM5101A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM5101B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM5101C	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5100AM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 AM	<a href="#">Samples</a>
LM5100AMR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L5100 AMR	<a href="#">Samples</a>
LM5100AMRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L5100 AMR	<a href="#">Samples</a>
LM5100AMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 AM	<a href="#">Samples</a>
LM5100ASD	NRND	WSON	DPR	10	1000	TBD	Call TI	Call TI	-40 to 125	5100ASD	
LM5100ASD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5100ASD	<a href="#">Samples</a>
LM5100BMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 BMA	<a href="#">Samples</a>
LM5100BMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 BMA	<a href="#">Samples</a>
LM5100BSD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5100BSD	<a href="#">Samples</a>
LM5100CMA/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	L5100 CMA	
LM5100CMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5100 CMA	<a href="#">Samples</a>
LM5100CMY/NOPB	OBSOLETE	MSOP- PowerPAD	DGN	8		TBD	Call TI	Call TI		SXCB	
LM5100CMYE/NOPB	OBSOLETE	MSOP- PowerPAD	DGN	8		TBD	Call TI	Call TI		SXCB	
LM5100CMYX/NOPB	OBSOLETE	MSOP- PowerPAD	DGN	8		TBD	Call TI	Call TI		SXCB	
LM5100CSD/NOPB	OBSOLETE	WSON	DPR	10		TBD	Call TI	Call TI	-40 to 125	5100CSD	
LM5101AM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 AM	<a href="#">Samples</a>
LM5101AMR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L5101 AMR	<a href="#">Samples</a>
LM5101AMRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L5101 AMR	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5101AMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 AM	<a href="#">Samples</a>
LM5101ASD	NRND	WSON	DPR	10	1000	TBD	Call TI	Call TI	-40 to 125	5101ASD	
LM5101ASD-1/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM		5101A-1	<a href="#">Samples</a>
LM5101ASD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	5101ASD	<a href="#">Samples</a>
LM5101ASDX	NRND	WSON	DPR	10	4500	TBD	Call TI	Call TI	-40 to 125	5101ASD	
LM5101ASDX-1/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		5101A-1	<a href="#">Samples</a>
LM5101ASDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	5101ASD	<a href="#">Samples</a>
LM5101BMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 BMA	<a href="#">Samples</a>
LM5101BMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 BMA	<a href="#">Samples</a>
LM5101BSD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	(5101ASD ~ 5101BSD)	<a href="#">Samples</a>
LM5101BSDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5101BSD	<a href="#">Samples</a>
LM5101CMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 CMA	<a href="#">Samples</a>
LM5101CMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5101 CMA	<a href="#">Samples</a>
LM5101CMY/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXDB	<a href="#">Samples</a>
LM5101CMYE/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXDB	<a href="#">Samples</a>
LM5101CMYX/NOPB	ACTIVE	MSOP-PowerPAD	DGN	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		SXDB	<a href="#">Samples</a>
LM5101CSD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	5101CSD	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

---

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

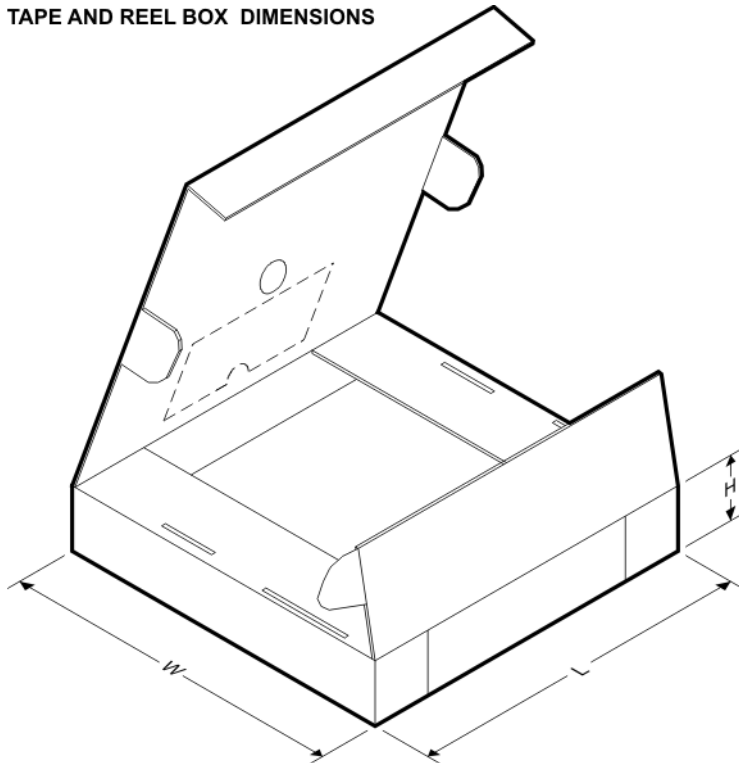
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5100AMRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100ASD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100ASD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5100BSD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5100CMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101AMRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101ASD	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASD-1/NOPB	WSON	NGT	8	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5101ASD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5101ASDX	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASDX-1/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101ASDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5101BMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101BSD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1
LM5101BSDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5101CMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5101CMY/NOPB	MSOP-Power PAD	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CMYE/NOPB	MSOP-Power PAD	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CMYX/NOPB	MSOP-Power PAD	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5101CSD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

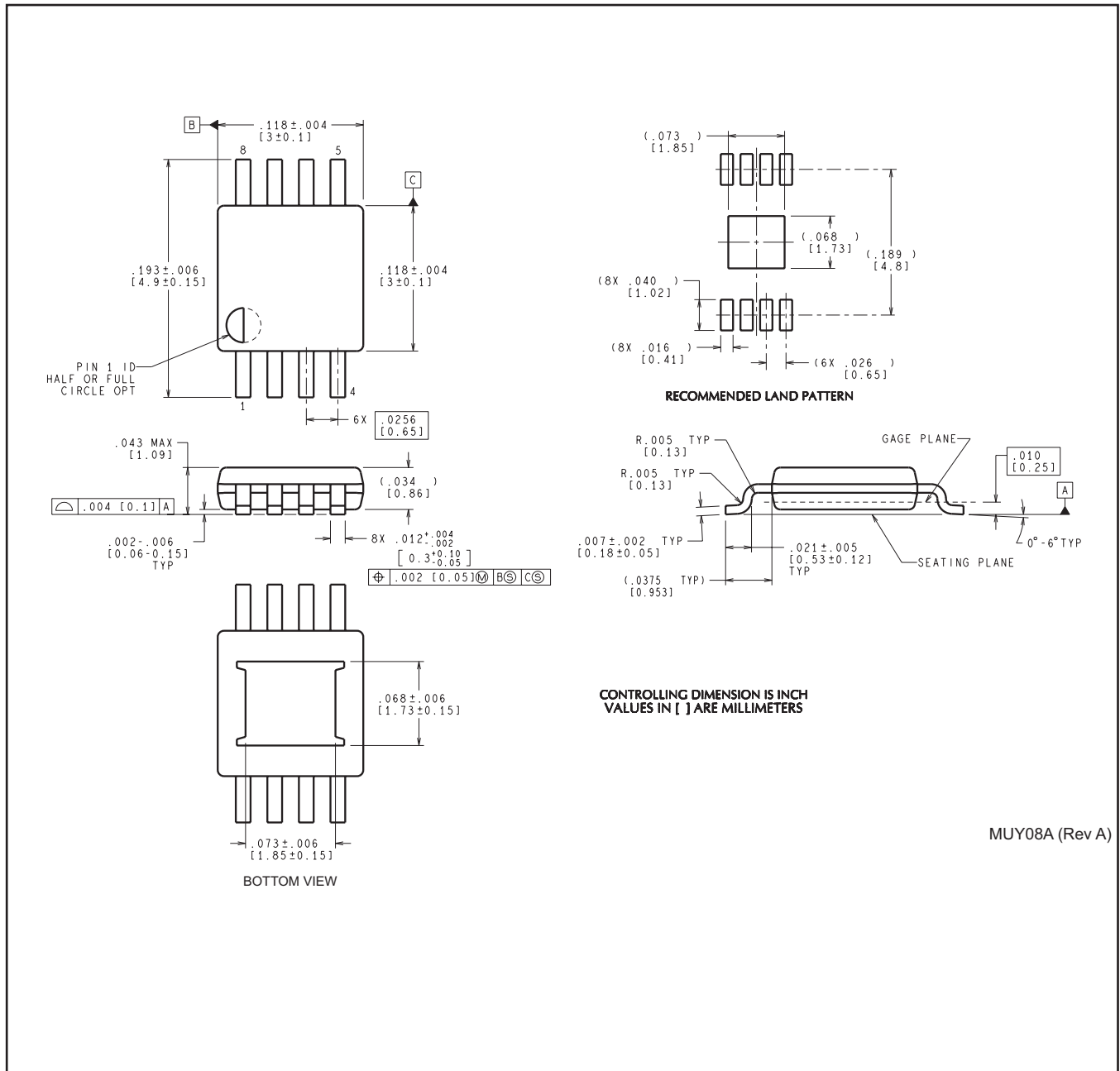
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5100AMRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM5100AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5100ASD	WSON	DPR	10	1000	210.0	185.0	35.0
LM5100ASD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5100BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

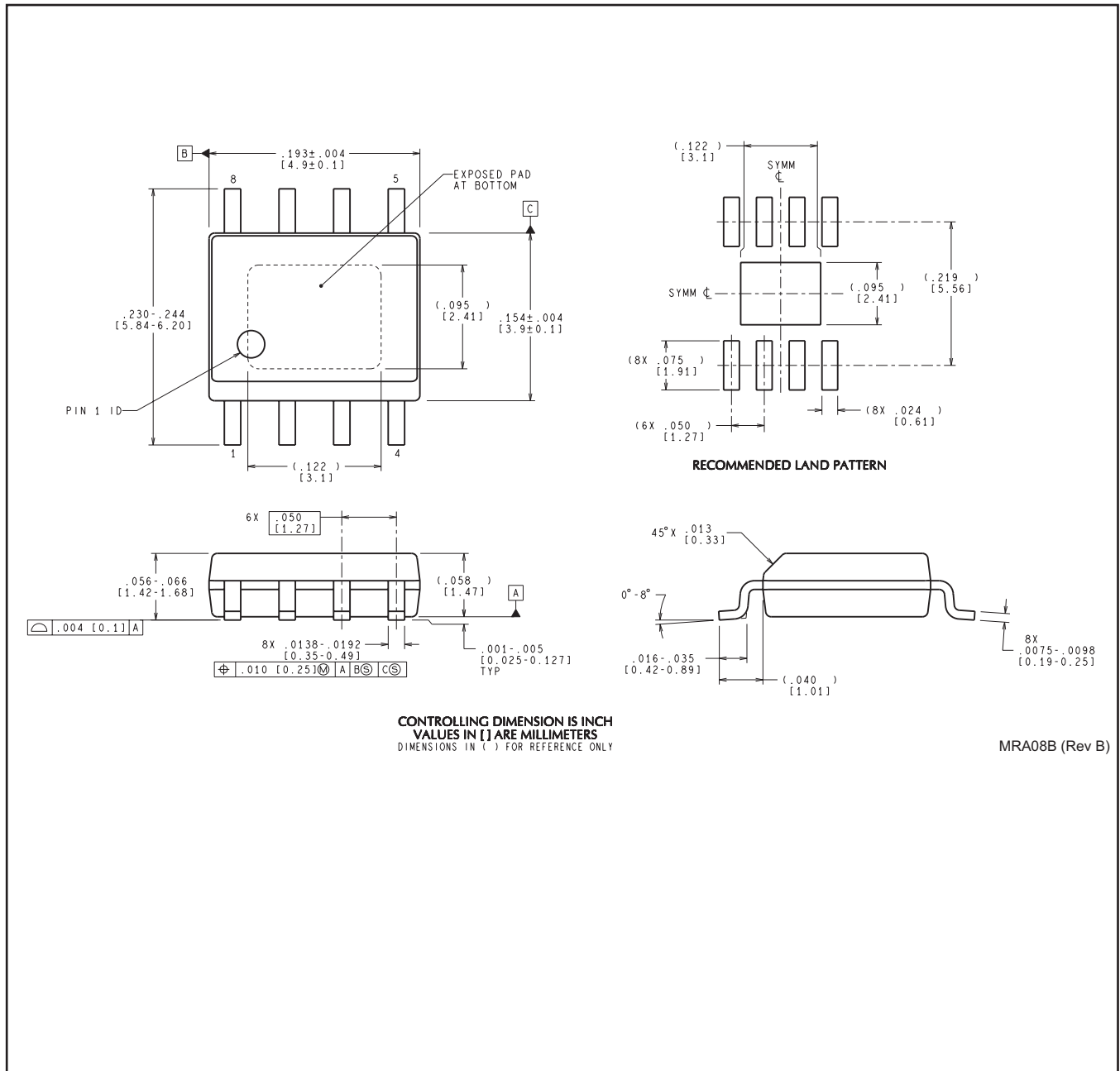
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5100BSD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5100CMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101AMRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM5101AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101ASD	WSON	DPR	10	1000	210.0	185.0	35.0
LM5101ASD-1/NOPB	WSON	NGT	8	1000	203.0	203.0	35.0
LM5101ASD/NOPB	WSON	DPR	10	1000	203.0	203.0	35.0
LM5101ASDX	WSON	DPR	10	4500	367.0	367.0	35.0
LM5101ASDX-1/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LM5101ASDX/NOPB	WSON	DPR	10	4500	346.0	346.0	35.0
LM5101BMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101BSD/NOPB	WSON	DPR	10	1000	203.0	203.0	35.0
LM5101BSDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0
LM5101CMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5101CMY/NOPB	MSOP-PowerPAD	DGN	8	1000	210.0	185.0	35.0
LM5101CMYE/NOPB	MSOP-PowerPAD	DGN	8	250	210.0	185.0	35.0
LM5101CMYX/NOPB	MSOP-PowerPAD	DGN	8	3500	367.0	367.0	35.0
LM5101CSD/NOPB	WSON	DPR	10	1000	203.0	203.0	35.0

DGN0008A



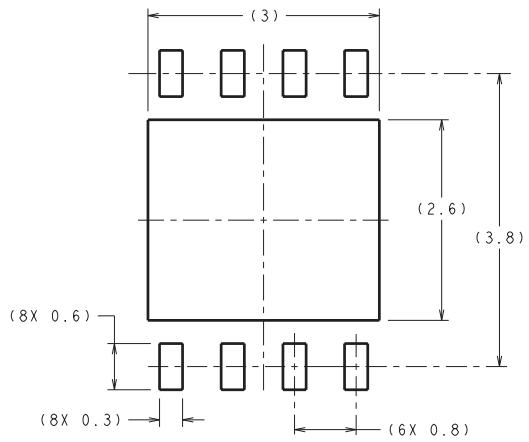
MUY08A (Rev A)

DDA0008B

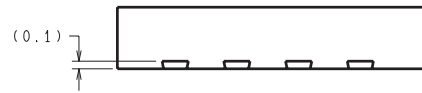


MRA08B (Rev B)

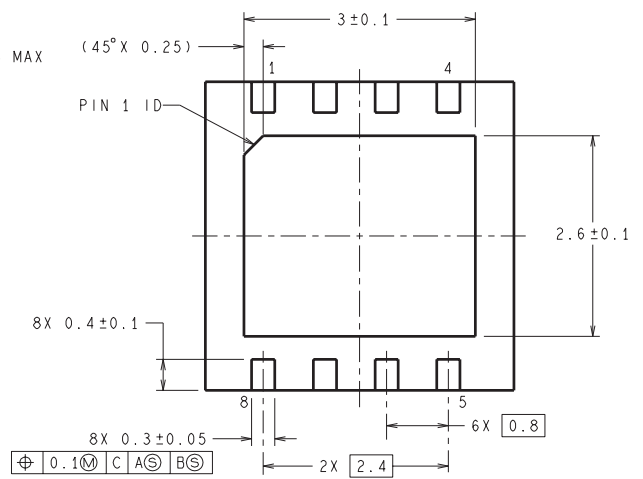
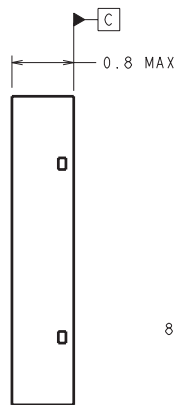
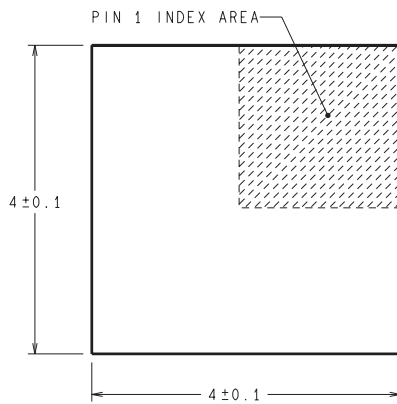
NGT0008A



DIMENSIONS ARE IN MILLIMETERS  
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN



SDC08A (Rev A)

## THERMAL PAD MECHANICAL DATA

DPR (S-PWSON-N10)

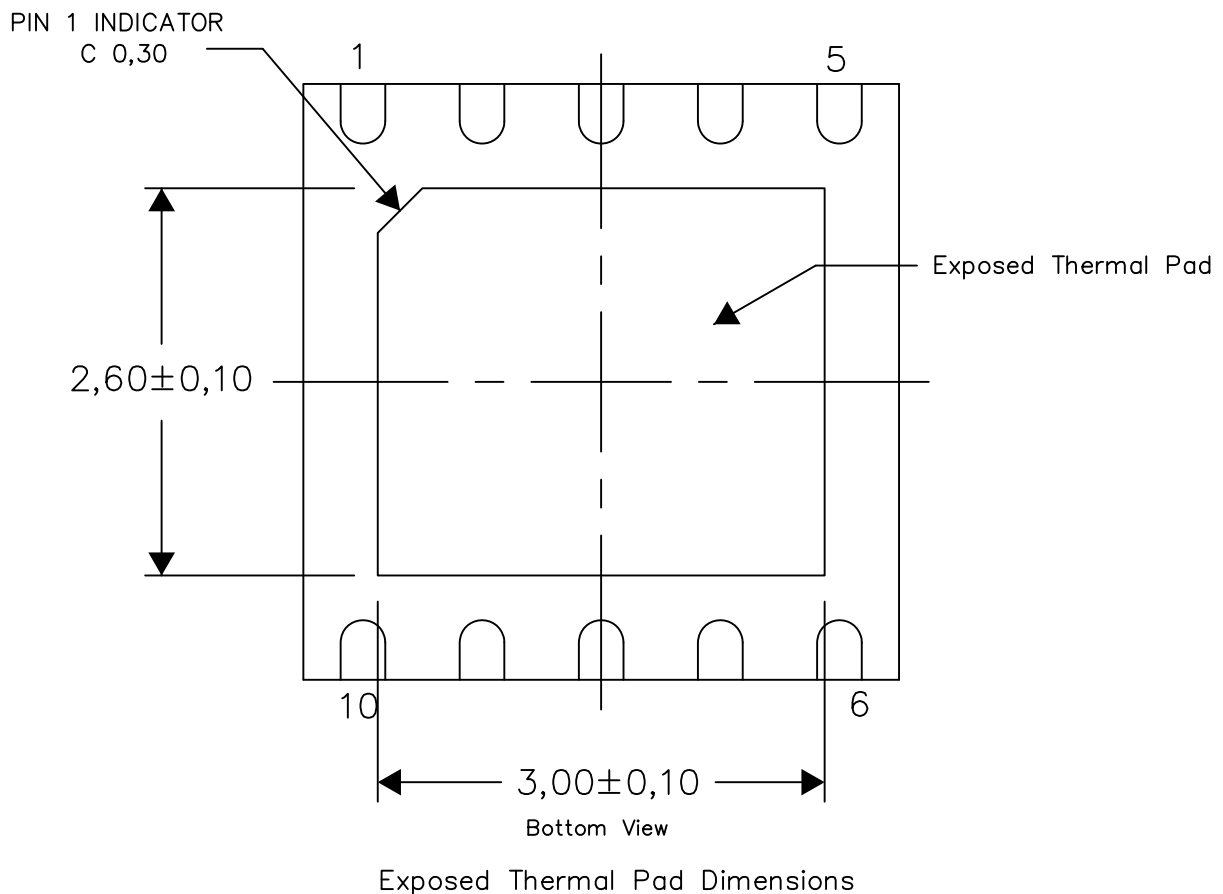
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

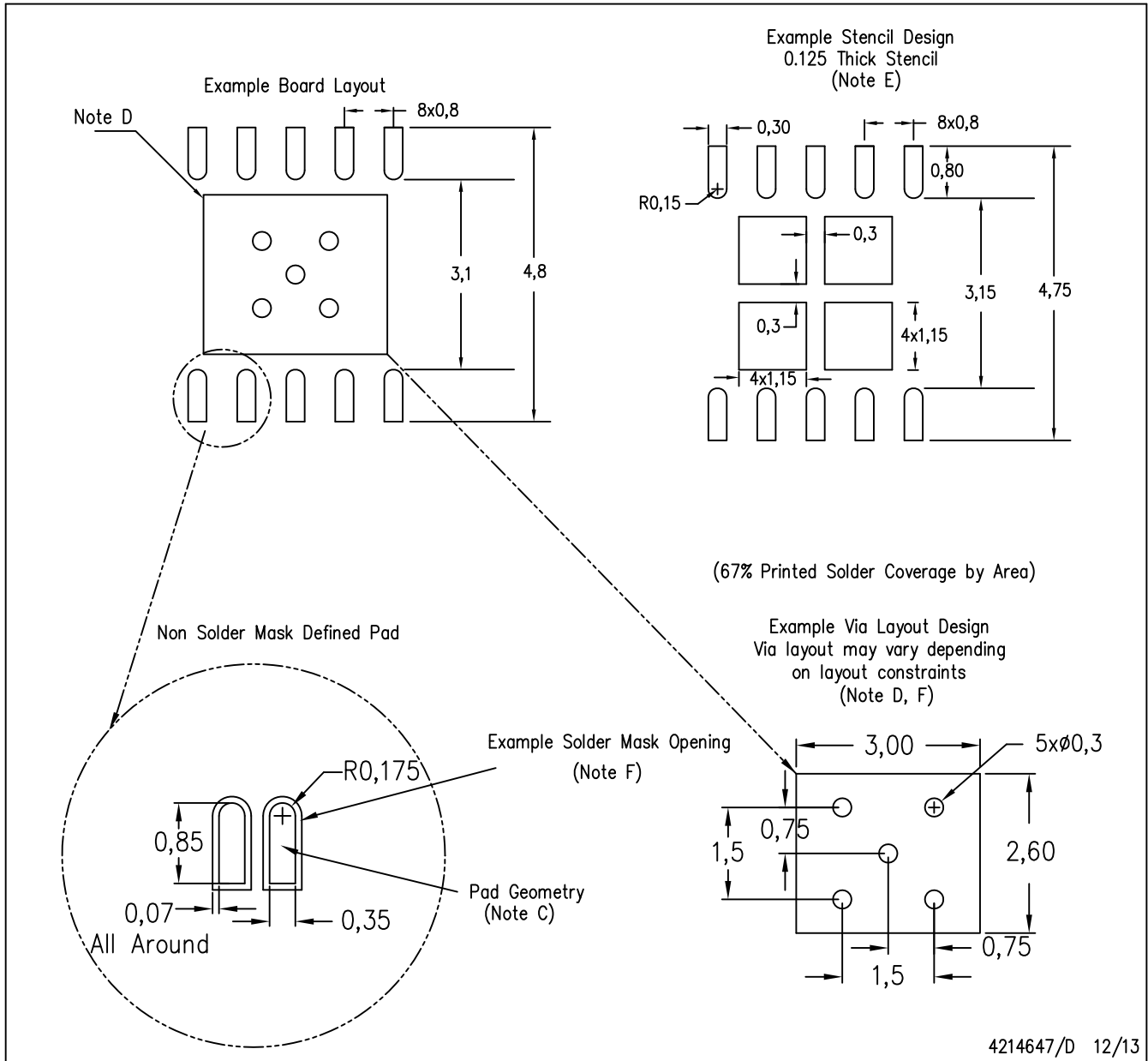


4211551/C 12/13

NOTES: All linear dimensions are in millimeters

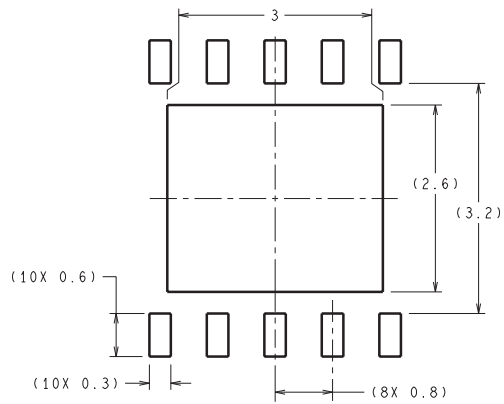
DPR (S-PWSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD

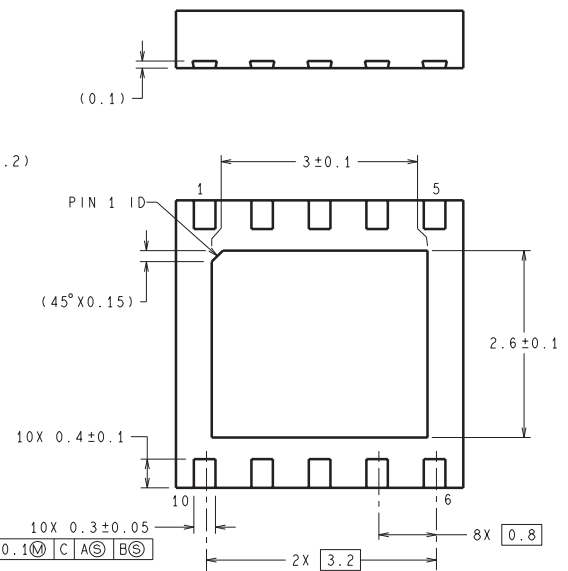
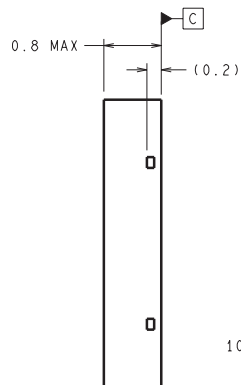
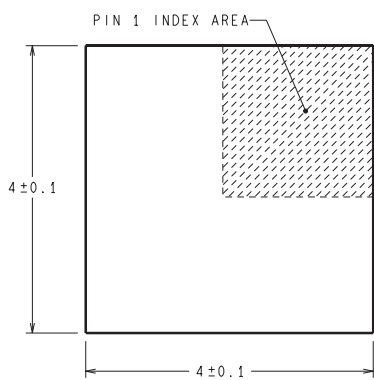


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DPR0010A



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS

SDC10A (Rev A)



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LM5100CMY/NOPB on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management