



**THE DATASHEET OF  
ISL59960IRZ-T7**



ISL59960

960MegaQ™: An Automatic 960H and Composite Video Equalizer, Fully-Adaptive to 4000 Feet

FN8358  
Rev 0.00  
December 18, 2012

The ISL59960 is a single-channel adaptive equalizer for 960H (WD1) or 720H (D1) composite video designed to automatically compensate for long runs of CAT 5/CAT 6 or RG-59 cable, producing high quality video output with no user interaction. The ISL59960 equalizes up to 4000 feet (1200 meters) of CAT 5/CAT 6 cable.

960MegaQ™ compensates for high frequency cable losses of up to 70dB at 9MHz, as well as source amplitude variations up to ±3dB.

The ISL59960 operates from a single +5V supply. Inputs are AC-coupled and internally DC-restored. The output can drive 2V<sub>P-P</sub> into two source-terminated 75Ω loads (AC-coupled or DC-coupled).

Related Literature

- [AN1780](#) “ISL59605-Catx-EVZ/ISL59960-Catx-EVZ Evaluation Board” (Stand-Alone Evaluation Board)
- [AN1776](#) “ISL59603-Coax-EVZ/ISL59960-Coax-EVZ Evaluation Board” (Stand-Alone Evaluation Board)
- [AN1775](#) “ISL59605-SPI-EVALZ/ISL59960-SPI-EVALZ Evaluation Board (with Serial Interface) Operation (Rev 5.0)” (Evaluation Board with USB Serial Interface)

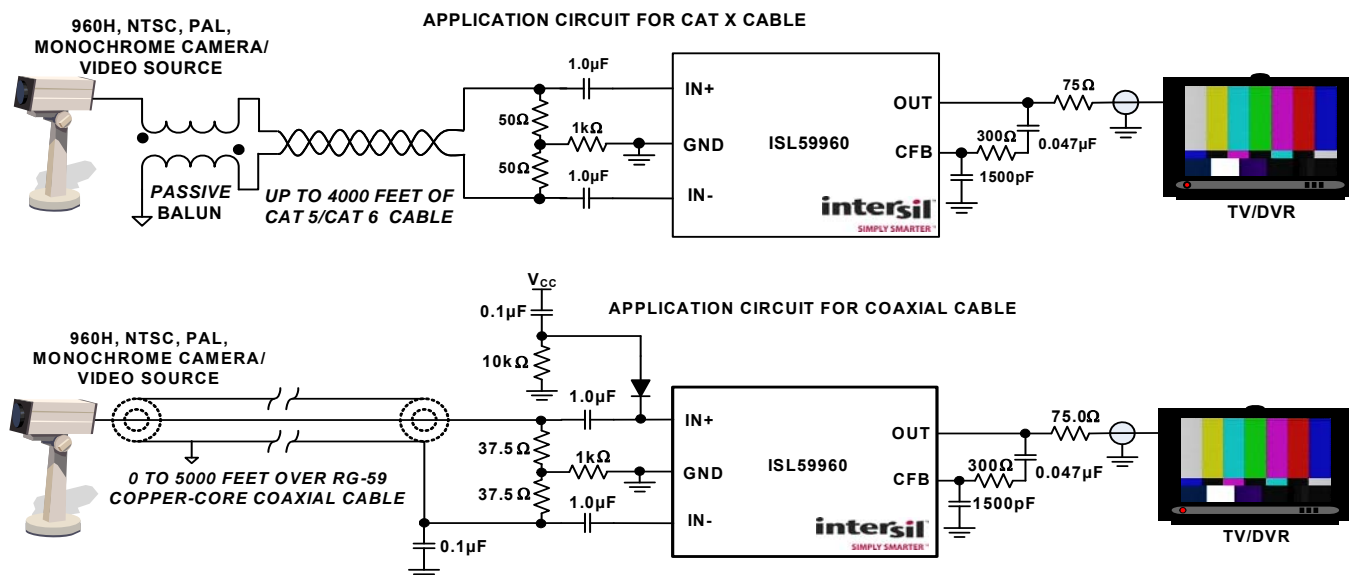
Features

- Equalizes both 960H and 720H video
- Equalizes up to 4000 feet of Cat 5/Cat 6 and up to 5000 feet (1500m) of RG-59
- Fully automatic, stand-alone operation - no user adjustment required
- 13MHz -3dB bandwidth
- ±8kV ESD protection on all inputs
- Automatic cable type compensation
- Compatible with color or monochrome, 960H, NTSC or PAL signals
- Automatic polarity detection and inversion
- Compensates for ±3dB source variation (in addition to cable losses)
- Optional serial interface adds additional functionality
- Works with single-ended or differential inputs
- Output drives up to two 150Ω video loads

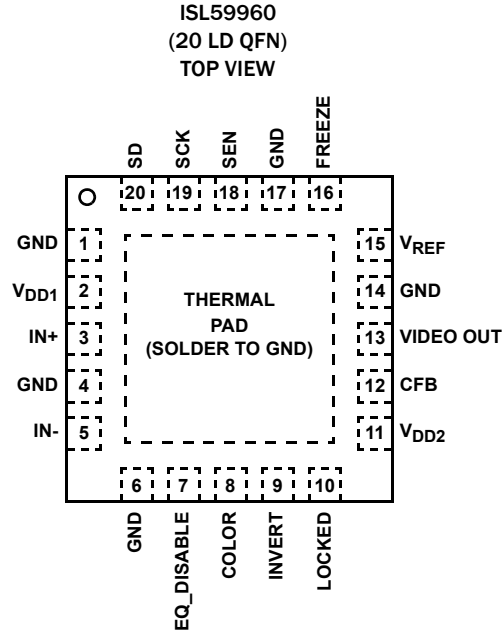
Applications

- Surveillance video
- Video distribution

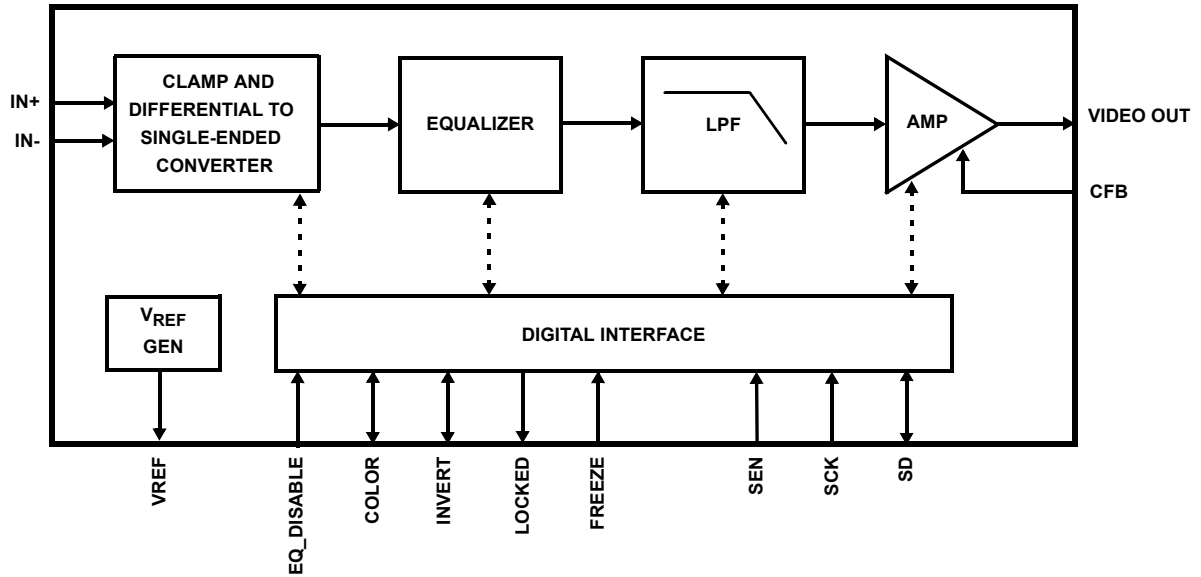
Typical Application



# Pin Configuration



# Block Diagram



## Pin Descriptions

| PIN NUMBER              | PIN NAME   | DESCRIPTION  |
|-------------------------|------------|--|
| <b>INPUTS</b>           |            |  |
| 3                       | IN+        | High impedance analog input. This is the positive differential video input. Input signals are externally AC-coupled with an external 1.0 $\mu$ F capacitor. See "Application Information" on page 10 for information regarding input network for Cat x and coax cables.  |
| 5                       | IN-        | High impedance analog input. This is the negative differential video input. Input signals are externally AC-coupled with an external 1.0 $\mu$ F capacitor. See "Application Information" on page 10 for information regarding input network for Cat x and coax cables.  |
| 12                      | CFB        | Analog input. Bypass to ground with a 1500pF capacitor and connect to VIDEO OUT via a 0.047 $\mu$ F capacitor in series with a 300 $\Omega$ resistor.  |
| <b>OUTPUTS</b>          |            |  |
| 13                      | VIDEO OUT  | Single-ended video output. The internal AGC sets this level to 2V <sub>p,p</sub> for a nominal 1V <sub>p,p</sub> (pre-cable) video source.   |
| <b>DIGITAL I/O</b>      |            |  |
| 7                       | EQ_DISABLE | Digital Input. Equalizer Disable.<br>0: Normal Operation<br>1: Disables the equalizer to allow for insertion of upstream data onto the signal path, e.g., RS-485.<br>This pin must be asserted high or low. Do not float this pin.   |
| 8                       | COLOR      | Digital I/O. Color Indicator/Override.<br>0: Monochrome<br>1: Color<br>When used as an output, this pin indicates whether the incoming signal does or does not have a colorburst. When used as an input, this pin forces the state machine to into monochrome or color mode. See Figure 13 and associated text for more information on functionality.<br>When COLOR is not externally driven, it is an output pin with a 13k $\Omega$ (typical) output impedance. It is capable of driving 5V, high-impedance CMOS logic.<br>Note: The COLOR indicator may be invalid for monochrome signals over greater than ~3500 feet. The device will still equalize properly if this occurs. |
| 9                       | INVERT     | Digital I/O. Polarity Indicator/Override.<br>0: Nominal Polarity.<br>1: Inverted Polarity.<br>When used as an output, this pin indicates the polarity of the incoming signal. When used as an input, this pin controls whether or not the input signal is inverted in the signal chain. See Figure 12 and associated text for more information on functionality.<br>When INVERT is not externally driven, it is an output pin with a 13k $\Omega$ (typical) output impedance. It is capable of driving 5V, high-impedance CMOS logic.<br>In stand-alone mode, toggling this pin high-low-high or low-high-low will make the equalizer reacquire the signal.                        |
| 10                      | LOCKED     | Digital Output.<br>0: Signal is not equalized (or not present).<br>1: Signal is equalized and settled.<br>Note: The LOCKED indicator may be invalid for monochrome signals over greater than ~3500 feet. The device will still equalize properly if this occurs.   |
| 16                      | FREEZE     | Digital Input. Freezes equalizer in its current EQ state.<br>0: Continuous Update<br>1: Freeze EQ in current state.<br>For stand-alone operations, connect FREEZE to the LOCKED pin to enter the recommended <b>Lock Until Reset</b> mode. Tie this pin low if unused.   |
| <b>SERIAL INTERFACE</b> |            |  |
| 18                      | SEN        | Digital Input. Serial Interface Enable. This pin should be tied to ground when not in use.   |
| 19                      | SCK        | Digital Input. Serial Interface Clock Signal. This pin should be tied to ground when not in use.   |
| 20                      | SD         | Digital I/O. Serial Interface Data Signal. This pin should be tied to ground when not in use.  |

## Pin Descriptions (Continued)

| PIN NUMBER      | PIN NAME         | DESCRIPTION  |
|-----------------|------------------|--|
| POWER           |                  |  |
| 2               | V <sub>DD1</sub> | +5V power supply for analog equalizer. Isolate from +5V source with a ferrite bead and bypass to ground with a 0.1 $\mu$ F capacitor in parallel with a 4.7 $\mu$ F capacitor. |
| 11              | V <sub>DD2</sub> | +5V power supply for output amplifier. Bypass to ground with a 0.1 $\mu$ F capacitor.  |
| 15              | V <sub>REF</sub> | Internally generated 2.5V reference. Bypass to ground with a low-ESR 0.47 $\mu$ F capacitor. Do not attach anything else to this pin.  |
| 1, 4, 6, 14, 17 | GND              | Ground   |
| THERMAL PAD     |                  |  |
| EP              | PAD              | Solder the exposed thermal PAD to ground for best thermal and electrical performance.  |

## Ordering Information

| PART NUMBER<br>(Notes 2, 3) | PART<br>MARKING                           | MAX EQ LENGTH | TEMP RANGE<br>(°C) | PACKAGE<br>(Pb-free) | PKG.<br>DWG. # |
|-----------------------------|---|---------------|--------------------|----------------------|----------------|
| ISL59960IRZ                 | 599 60IRZ                                 | 4000 feet     | -40 to +85         | 20 Ld QFN (4x4mm)    | L20.4x4C       |
| ISL59960IRZ-T7 (Note 1)     | 599 60IRZ                                 | 4000 feet     | -40 to +85         | 20 Ld QFN (4x4mm)    | L20.4x4C       |
| ISL59960IRZ-T7A (Note 1)    | 599 60IRZ                                 | 4000 feet     | -40 to +85         | 20 Ld QFN (4x4mm)    | L20.4x4C       |
| ISL59960-Catx-EVZ           | Stand-alone (no USB I/O) evaluation board |               |                    |                      |                |
| ISL59960-Coax-EVZ           | Stand-alone (no USB I/O) evaluation board |               |                    |                      |                |
| ISL59960-SPI-EVZ            | Evaluation board with serial interface    |               |                    |                      |                |

### NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL59960](#). For more information on MSL please see techbrief [TB363](#).

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

|   |                               |
|---|-------------------------------|
| Supply Voltage between $V_{DD}$ and GND         | 5.75V                         |
| Maximum Continuous Output Current               | 50mA                          |
| Maximum Voltage on any Pin                      | GND - 0.3V to $V_{DD} + 0.3V$ |
| <b>ESD Rating</b>                               |                               |
| Human Body Model (tested per JESD22-A114)       | 8,000V                        |
| Machine Model (Tested per JESD22-A115)          | 600V                          |
| CDM Model (Tested per JESD22-C101)              | 2,000V                        |
| Latch Up (Tested per JESD78; Class II, Level A) | 100mA                         |

**Thermal Information**

|                                |   |   |
|--------------------------------|---|---|
| Thermal Resistance (Typical)   | $\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )   | $\theta_{JC}$ ( $^\circ\text{C}/\text{W}$ ) |
| 20 Ld QFN Package (Notes 4, 5) | 40  | 3.7   |
| Storage Temperature            | -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$   |   |
| Ambient Operating Temperature  | -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$  |   |
| Die Junction Temperature       | +150 $^\circ\text{C}$   |   |
| Pb-Free Reflow Profile         | see link below<br><a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |   |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#).
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

**Electrical Specifications**  $V_{DD} = V_{DD1} = V_{DD2} = +5V$ , source video amplitude before any cable loss =  $1V_{P-P}$ , cable type = Cat 5, cable length = 0 feet,  $R_L = 150\Omega$  (75 $\Omega$  series + 75 $\Omega$  load to ground),  $T_A = +25^\circ\text{C}$ , exposed die plate = 0V, unless otherwise specified. Max Cat 5 cable length = 4000 feet.

| PARAMETER                    | DESCRIPTION  | CONDITIONS  | MIN<br>(Note 6) | TYP  | MAX<br>(Note 6) | UNIT          |
|------------------------------|--|---|-----------------|------|-----------------|---------------|
| <b>SUPPLY</b>                |  |   |                 |      |                 |               |
| $V_{DD}$                     | $V_{DD}$ Operating Range                                   |   | 4.5             | 5.0  | 5.5             | V             |
| $I_{S1}$                     | $V_{DD1}$ Supply Current                                   | No input, no load   |                 | 45   | 60              | mA            |
| $I_{S2}$                     | $V_{DD2}$ Supply Current                                   | No input, no load   |                 | 25   | 45              | mA            |
| $PSRR_{DC}$                  | Power Supply Rejection Ratio                               |   |                 | 60   |                 | dB            |
| <b>AC PERFORMANCE</b>        |  |   |                 |      |                 |               |
| BW                           | -3dB Bandwidth   | Cable length = 0 feet                                       |                 | 13   |                 | MHz           |
| DG                           | Differential Gain  | Cable length = 3200 feet,<br>20IRE Sub Carrier on 100% ramp |                 | .75  |                 | %             |
| DP                           | Differential Phase   | Cable length = 3200 feet,<br>20IRE Sub Carrier on 100% ramp |                 | .5   |                 | $^\circ$      |
| <b>DC PERFORMANCE</b>        |  |   |                 |      |                 |               |
| $V_{BL}$                     | Output Blanking/Backporch Level                            | Measured at VIDEO OUT pin                                   | 0.82            | 0.95 | 1.07            | V             |
| <b>INPUT CHARACTERISTICS</b> |  |   |                 |      |                 |               |
| $V_{INDIFF\_MIN}$            | Minimum Correctable Peak-to-Peak Signal Swing              | Measured at the source-end of cable, before cable losses    |                 | 0.7  |                 | $V_{P-P}$     |
| $V_{INDIFF\_MAX}$            | Maximum Correctable Peak-to-Peak Signal Swing              | Measured at the source-end of cable, before cable losses    |                 | 1.4  |                 | $V_{P-P}$     |
| $V_{CM-MIN}$                 | Min Common Mode Input Voltage                              |   |                 | 1    |                 | V             |
| $V_{CM-MAX}$                 | Max Common Mode Input Voltage                              |   |                 | 4    |                 | V             |
| SNR                          | Signal-to-Noise Ratio,<br>NTC-7 Weighted Filter            | EQ = 0 feet   |                 | -68  |                 | dB rms        |
|                              |  | EQ = 1,000 feet   |                 | -67  |                 | dB rms        |
|                              |  | EQ = 2,000 feet   |                 | -66  |                 | dB rms        |
|                              |  | EQ = 3,000 feet   |                 | -65  |                 | dB rms        |
|                              |  | EQ = 4,000 feet   |                 | -61  |                 | dB rms        |
| CMRR                         | Common-mode Rejection Ratio at<br>$f_{IN} = 100\text{kHz}$ | 0 feet cable  |                 | -50  |                 | dB            |
|                              |  | 1600 feet cable   |                 | -41  |                 | dB            |
| $I_{Clamp}$                  | Input Clamp Current  |   |                 | 25   |                 | $\mu\text{A}$ |

**Electrical Specifications**  $V_{DD} = V_{DD1} = V_{DD2} = +5V$ , source video amplitude before any cable loss =  $1V_{p-p}$ , cable type = Cat 5, cable length = 0 feet,  $R_L = 150\Omega$  (75 $\Omega$  series + 75 $\Omega$  load to ground),  $T_A = +25^\circ C$ , exposed die plate = 0V, unless otherwise specified. Max Cat 5 cable length = 4000 feet. (Continued)

| PARAMETER                     | DESCRIPTION                      | CONDITIONS                                       | MIN (Note 6) | TYP  | MAX (Note 6) | UNIT |
|-------------------------------|----------------------------------|--|--------------|------|--------------|------|
| <b>OUTPUT CHARACTERISTICS</b> |                                  |  |              |      |              |      |
| A <sub>GC-ACC</sub>           | AGC Accuracy                     | Accuracy of sync tip amplitude relative to 600mV |              | ±0.5 |              | dB   |
| I <sub>OUT</sub>              | Output Drive Current             |  |              | 40   |              | mA   |
| t <sub>EN-EQ</sub>            | Enable-to-Equalization On Time   |  |              | 500  |              | ns   |
| t <sub>DIS-EQ</sub>           | Disable-to-Equalization Off Time |  |              | 500  |              | ns   |
| <b>LOGIC CONTROL PINS</b>     |                                  |  |              |      |              |      |
| V <sub>IH</sub>               | Logic High Level                 |  | 2.0          |      |              | V    |
| V <sub>IL</sub>               | Logic Low Level                  |  |              |      | 0.8          | V    |
| I <sub>LOGIC</sub>            | Logic Input Current              | EQ_DISABLE, FREEZE, SD, SCK, SEN                 |              | ±10  |              | µA   |
|                               |                                  | INVERT, COLOR                                    |              | ±500 |              | µA   |

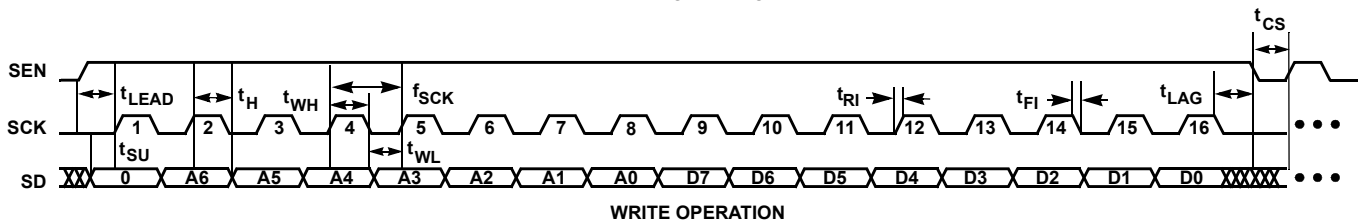
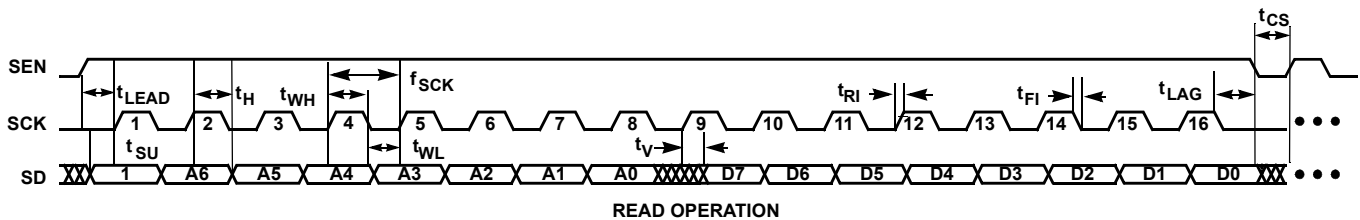
**Serial Timing**

| PARAMETER         | DESCRIPTION                      | CONDITIONS     | MIN (Note 6) | TYP | MAX (Note 6) | UNIT |
|-------------------|----------------------------------|----------------|--------------|-----|--------------|------|
| t <sub>CS</sub>   | Serial Enable Deselect Time      |                | 10           |     |              | ns   |
| t <sub>LEAD</sub> | Lead Time                        |                | 10           |     |              | ns   |
| t <sub>SU</sub>   | SD, SCK Setup Time               |                | 10           |     |              | ns   |
| t <sub>H</sub>    | SD, SEN, SCK Hold Time           |                | 10           |     |              | ns   |
| t <sub>WH</sub>   | SCK High Time                    |                | 100          |     |              | ns   |
| t <sub>WL</sub>   | SCK Low Time                     |                | 100          |     |              | ns   |
| t <sub>RI</sub>   | SD, SEN, SCK Rise Time           |                | 10           |     |              | ns   |
| t <sub>FI</sub>   | SD, SEN, SCK Fall Time           |                | 10           |     |              | ns   |
| t <sub>LAG</sub>  | Lag Time                         |                | 10           |     |              | ns   |
| t <sub>v</sub>    | SCK Rising Edge to SD Data Valid | Read Operation |              |     | 10           | ns   |
| f <sub>SCK</sub>  | SCK Frequency                    |                |              |     | 5            | MHz  |

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

**Serial Timing Diagram**



A6:A0 = REGISTER ADDRESS, D7:D0 = DATA TO BE READ/WITTEN

## Typical Performance Over 2000 Feet of Cat 5 with 960H (WD1) Video

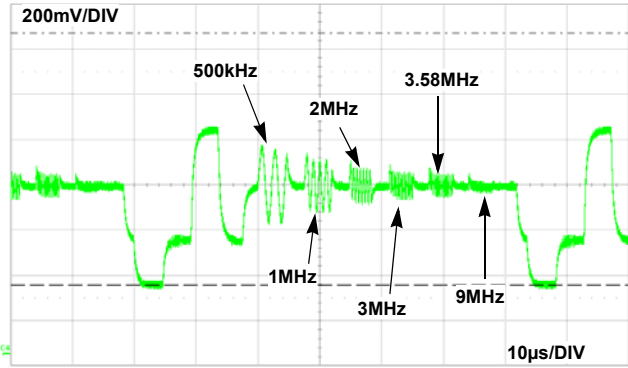


FIGURE 1. MULTIBURST WAVEFORM AFTER 2000 FEET OF UNCOMPENSATED CAT 5

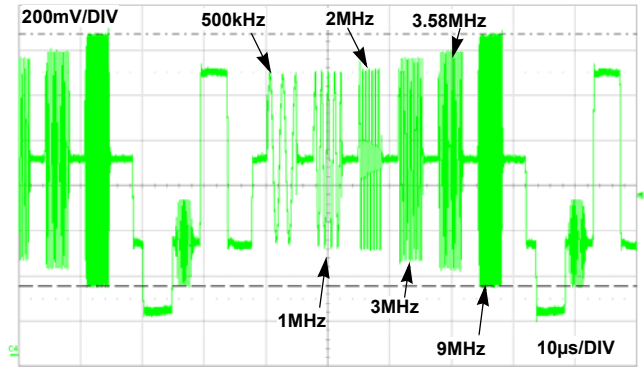


FIGURE 2. MULTIBURST WAVEFORM AFTER 2000 FEET OF CAT 5

## Typical Performance Over 4000 Feet of Cat 5 with 960H (WD1) Video

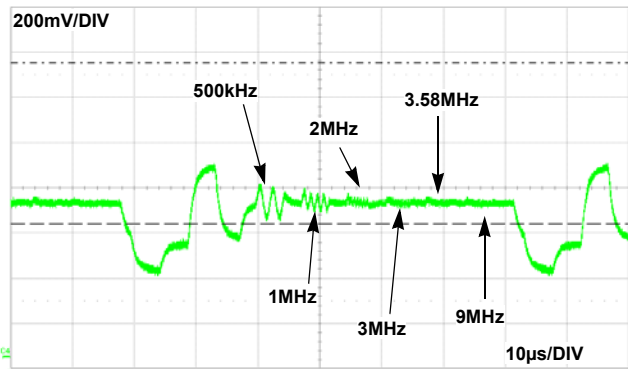


FIGURE 3. MULTIBURST WAVEFORM AFTER 4000 FEET OF UNCOMPENSATED CAT 5

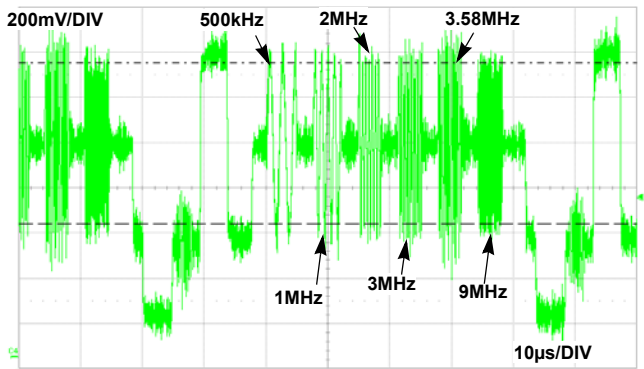


FIGURE 4. MULTIBURST WAVEFORM AFTER 4000 FEET OF CAT 5 WITH ISL59960

## Typical Performance Over 2500 Feet of Bare Copper RG-59 with 960H (WD1) Video

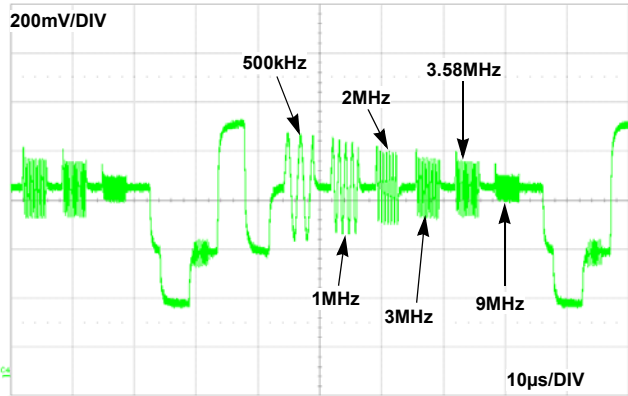


FIGURE 5. MULTIBURST WAVEFORM AFTER 2500 FEET OF UNCOMPENSATED RG-59 COAX

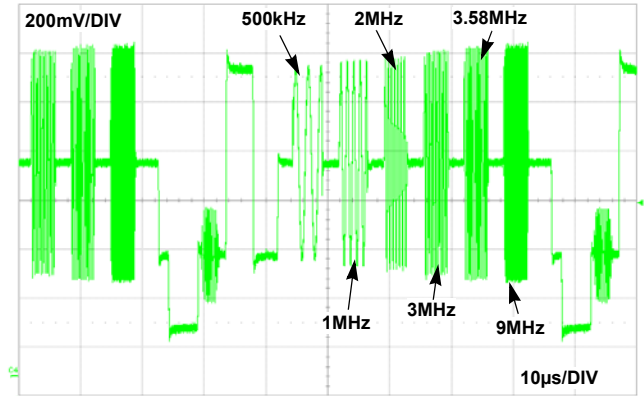


FIGURE 6. MULTIBURST WAVEFORM AFTER 2500 FEET OF RG-59 COAX WITH ISL59960

## Typical Performance Over 5000 Feet of Bare Copper RG-59 with 960H (WD1) Video

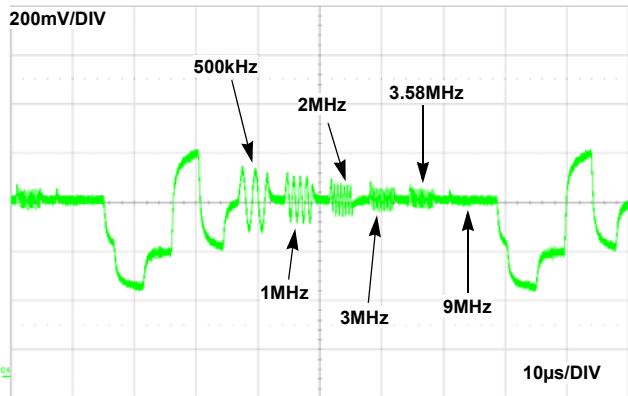


FIGURE 7. MULTIBURST WAVEFORM AFTER 5000 FEET OF UNCOMPENSATED RG-59 COAX

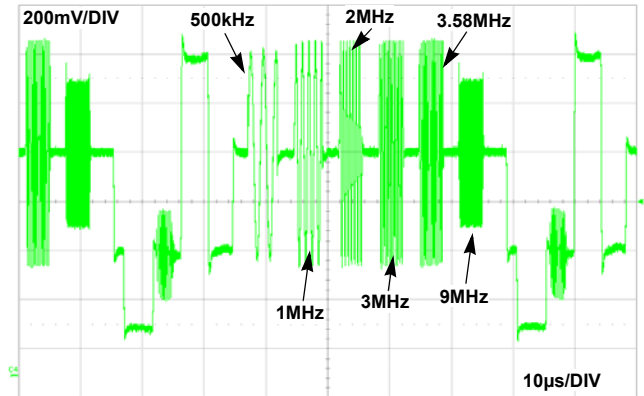


FIGURE 8. MULTIBURST WAVEFORM AFTER 5000 FEET OF RG-59 COAX WITH ISL59960

# Functional Description

## 960MegaQ™ Overview

960MegaQ™ is a fully automated, stand-alone equalizer for both 960H (WD1) and 720H (D1) composite video resolutions transmitted over UTP (Unshielded Twisted Pair, i.e., Cat 5, Cat 6, etc.) or coaxial (RG-59) cables.

Differential video signals sent over long distances of twisted pair wire exhibit large high frequency attenuation, resulting in loss of high frequency detail/blurring. The exact loss characteristic is a complex function of wire gauge, length, composition, and coupling to adjacent conductors.

The video signal can be restored by applying a filter with the exact inverse transfer function to the far end signal. 960MegaQ™ is designed to compensate for the losses due to long cables, and incorporates the functionality and flexibility to match a wide variety of cable types and loss characteristics.

While 960MegaQ™ was designed and optimized for stand-alone operation, with no need for any external control of any kind, it has an optional SPI serial interface with some additional features. See "Additional Equalization Modes Available With the Serial Interface" on page 11 for more information on the features and operation of the serial interface.

## Equalization for Various Cable Types

TABLE 1. CABLE TYPES AND LENGTHS

| CABLE TYPE                                     | MAXIMUM LENGTH SUPPORTED |
|--|--------------------------|
| Copper-Core                                    |                          |
| Cat 5/Cat 5e                                   | 4000 feet                |
| Cat 6  | 4000 feet                |
| Coaxial - RG-59                                | 5000 feet                |
| Non-Copper-Core (Note)                         |                          |
| Cat 5/Cat 5e CCA (Copper-Coated Aluminum Core) | 2000 feet                |
| Coaxial - RG-59 CCS (Copper-Coated Steel Core) | 1500 feet                |

NOTE: Image quality will be significantly improved over unequalized cable, but there will still be some image smearing due to the high resistance of the core material.

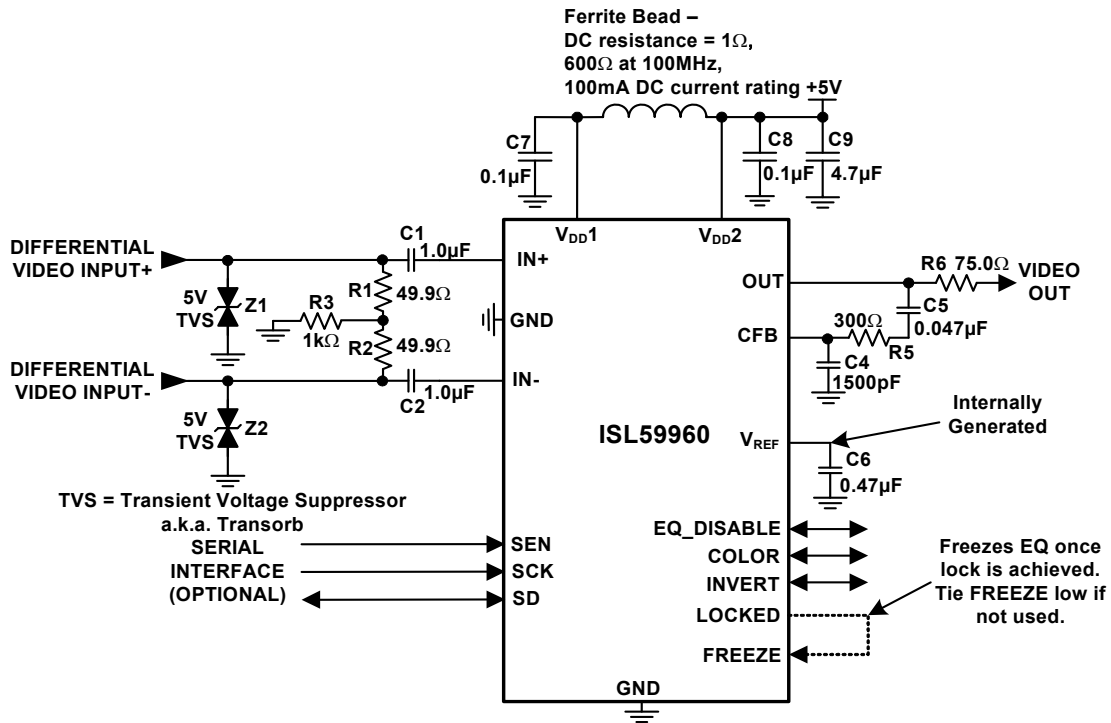


FIGURE 9. APPLICATION CIRCUIT FOR UTP CABLE

## Application Information

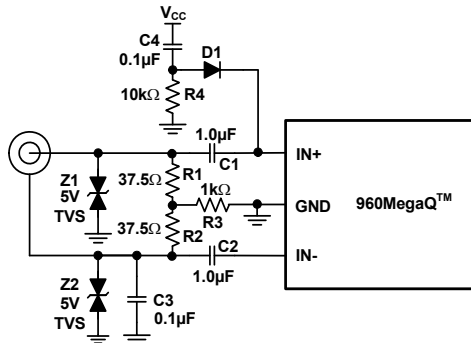
### Unshielded Twisted Pair (UTP) Application Circuit

Figure 9 shows the complete schematic for a 960MegaQ™ equalizer configured for unshielded twisted pair (UTP) cable. The input signal is terminated into the network formed by R1, R2, and R3. C1 and C2 AC-couple the signal into 960MegaQ™. To protect the front-end circuitry, 5V transorbs (Z1 and Z2) should be used instead of diodes because the signals on either differential input may swing far enough below ground to turn on a diode and distort the video.

On the output side, C5, R5, and C4 form a compensation network, while R6 provides 75Ω source-termination for the video output. 960MegaQ™ has a native gain of 6dB, so when VIDEO OUT is terminated into 75Ω (the input to a DVR, TV, etc.), R6 and the 75Ω terminator form a 2:1 divider, producing standard video amplitude across the 75Ω terminator.

### Coax Input Circuit

Figure 10 shows the input termination recommended for coaxial cables. The differential termination resistance is now 75Ω to match the characteristic impedance of the RG-59 coax cable. C3 bypasses high-frequency noise on the coax ground line to system ground. This allows the coax ground to be independent of the system at low frequencies (DC to 50/60Hz) to accommodate differences in the ground potential of the remote video source(s). The coax startup network (D1, R4, C4) prevents a rare start-up condition that can occur when a high average-picture-level (e.g., white screen) video signal is present on the inputs before the power has been applied.



TVS = Transient Voltage Suppressor  
a.k.a. Transorb

FIGURE 10. APPLICATION CIRCUIT FOR COAX CABLE

### Dual UTP/Coax Input Circuit

If desired, it is also possible to support both UTP and coax cables with the same PCB layout using two SPST switches that are closed when in coax mode (Figure 11). Since UTP requires a 100Ω termination network while coax requires 75Ω, a switch to introduce a shunt 300Ω resistor when in coax mode will change the termination from 100Ω to 75Ω. A second switch is required to engage C3. The addition of the coax startup circuit (D1, R4, C4) can unbalance the capacitance of the differential pair and degrade the CMRR in UTP applications. This in turn could cause excess noise at long lengths of UTP. In UTP applications, if the output signal is too noisy at long distances, an optional capacitor

Cx may be used to balance the capacitance of the differential inputs. The value of Cx should be determined by calculating how much trace capacitance is added by the coax startup circuit. A typical value for a good layout is ~5pF. Note that only coax or UTP should be connected at any one time - this circuit does not multiplex between them.

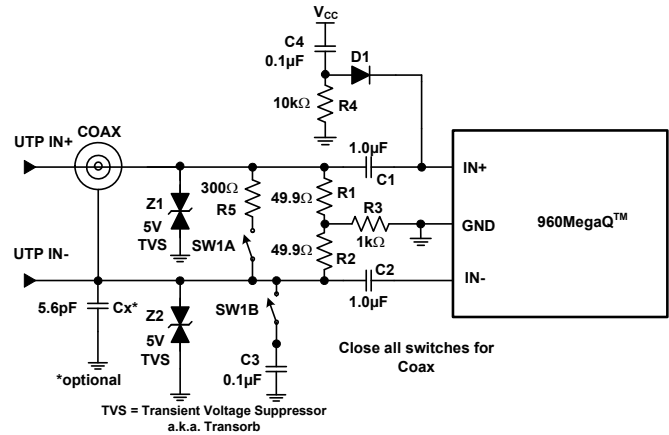


FIGURE 11. APPLICATION CIRCUIT FOR UTP/COAX CABLE

### Using the ISL59960 with Steel Core Coax

Although the ISL59960 was designed for copper based cables, it is capable of equalizing signals for coaxial applications that use steel core cabling. Due to the higher DC and low-band resistance of this cable type, the ISL59960 will not equalize to the same distance as copper based cables. See Table 1 on page 9 for maximum equalization distances.

### Input Multiplexing

Placing a semiconductor multiplexer in front of this part may increase high frequency attenuation and noise. However, a low-capacitance mechanical relay may be acceptable. Note that changing from one channel to another in **Lock Until Reset** mode will require a reset (INVERT toggle) to trigger equalization of the new channel (see "Lock Until RESET" on page 10).

For best performance, do not multiplex the inputs to the equalizer - this can further degrade the signal. Instead, multiplex at the output after equalization has been performed.

### Stand-Alone Operation and Configuration

In its default stand-alone configuration, 960MegaQ™ features two modes of automatic cable equalization: **Lock Until Reset** and **Continuous Update**. **Lock Until Reset** is the recommended mode for most applications.

### LOCK UNTIL RESET

In the **Lock Until Reset** mode, once 960MegaQ™ finds the optimum equalization and the LOCKED signal goes high, the equalization is frozen and will not change until either the power is cycled or the INVERT signal is toggled, which initiates a re-equalization of the input signal. Re-equalization is usually only necessary during device/system evaluation - in normal operation 960MegaQ™ powers-up, acquires and equalizes the signal, and continues to equalize until/unless it is powered-down. If the signal is lost in **Lock Until Reset** mode, the LOCKED pin will not

go low until/unless the device is reset by toggling the INVERT pin. A reset should only be necessary if the length or type of cable was changed without cycling power.

To enable the **Lock Until Reset** mode, tie the LOCKED output pin to the FREEZE input pin as shown in Figure 9 on page 9.

To generate a reset (and trigger a re-equalization), toggle the external INVERT pin. Depending on the initial state of INVERT, this would be a high-low-high or low-high-low sequence.

### CONTINUOUS UPDATE

In the **Continuous Update** mode, 960MegaQ™ will continuously try to find the optimum equalization solution. When the equalization has settled for 100 sequential video lines with no changes, the LOCKED pin will go high. However, once lock is achieved, noise and average-picture-level changes may cause the device to unlock, causing some image perturbation while 960MegaQ™ re-equalizes.

The **Continuous Update** mode is enabled whenever the FREEZE pin is set to a logic low (grounded).

### Polarity Detection and Correction

960MegaQ™ features polarity detection and correction, automatically detecting incorrectly-wired input signals and inverting the signal inside the IC as necessary. The detected polarity is indicated by the state of the INVERT pin.

The INVERT pin has 2 modes of operation. It is typically used to indicate whether or not the incoming signal is inverted (the “+” signal on the “-” input and vice-versa). The state of the invert signal is then used to tell the signal processing logic whether or not to invert the signal in the signal path.

A logic high on INVERT indicates that the positive differential input signal is on IN- (pin 5) and the negative differential input signal is on IN+ (pin 3). A logic low indicates nominal polarity.

However, the unique design of the INVERT I/O pin (Figure 12) also allows 960MegaQ™'s internal inversion detector to be overdriven externally, forcing 960MegaQ™ to invert or not invert the signal regardless of the state of the inversion detection function. This is not necessary in normal operation, but it may improve performance in particularly noisy environments when the polarity of the signal is guaranteed to be correct.

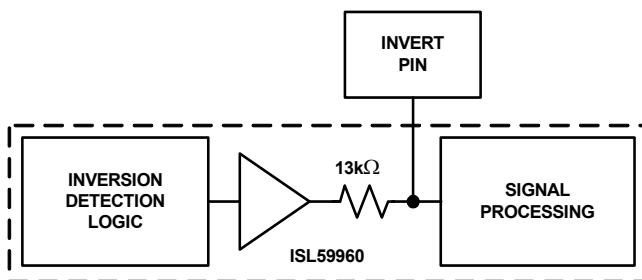


FIGURE 12. INVERT PIN STRUCTURE

### The COLOR Pin

The color pin has 2 modes of operation. It is typically used to indicate whether or not the incoming signal has a colorburst or not. The state of the color signal is then used to tell the signal processing logic whether or not it can rely on the presence of a colorburst signal. A logic high indicates a color signal; a logic low indicates monochrome.

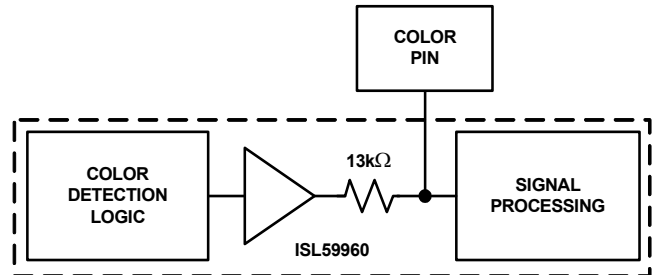


FIGURE 13. COLOR PIN STRUCTURE

However, the unique design of the COLOR I/O pin (Figure 13) also allows 960MegaQ™'s internal color detector to be overdriven externally. This is not necessary in normal operation, but it may improve performance in particularly noisy environments when the signal type is predetermined.

### Monochrome Video Signals

960MegaQ™ will equalize monochrome signals to the same distance as color signals. However, due to the high level of noise past ~3500 feet, the COLOR and LOCKED indicators may become invalid for monochrome signals. The device will still equalize properly if this occurs.

### Security Cameras

960MegaQ™ is ideal for security camera installations.

The automatic adaptive equalizer doesn't need any active silicon on the transmit side of the cable, enabling upgrading of older installations without having to touch the installed camera base, including older monochrome cameras.

960MegaQ™ automatically adjusts for wiring polarity errors as well as for optimum image quality. These features eliminate the need for the installer to make any adjustments.

With an extended equalization range of 4000ft, the ISL59960 enables cameras to be placed in even more remote locations, enabling coverage of up to three square miles from a single monitoring station.

### Additional Equalization Modes Available With the Serial Interface

In addition to the **Lock Until Reset** and **Continuous Update** modes, software control of 960MegaQ™ through the SPI interface adds a **Lock Until Signal Loss** mode and a **Manual Equalization** mode.

*Note: When controlling 960MegaQ™ through the SPI interface, the external FREEZE pin must be tied to ground (logic low). Failure to keep FREEZE at a logic low will prevent the software controls from working properly.*

All of the equalization modes are selected via the two “Locking Mode/Manual Length Enable” register bits, 0x05[1:0].

### CONTINUOUS UPDATE

Continuous Update mode is entered by setting address 0x05[1:0] = 00b. **Continuous Update** behavior is the same as described in the stand-alone mode.

### LOCK UNTIL RESET

**Lock Until Reset** mode is entered by setting address 0x05[1:0] = 10b. **Lock Until Reset** behavior is the same as described in the stand-alone mode, with the exception of how to generate a reset.

To generate a reset via software, select **Continuous Update** mode and then return to **Lock Until Reset** mode (register 0x05[1:0] = 00b then 10b). Toggling INVERT (either the hardware pin or the software bit) will *not* cause a reset/re-equalization event.

### LOCK UNTIL SIGNAL LOSS

**Lock Until Signal Loss** mode is entered by setting address 0x05[1:0] = 01b. **Lock Until Signal Loss** can only be enabled via the SPI interface.

In the **Lock Until Signal Loss** mode, 960MegaQ™ will freeze the equalization once the LOCKED pin goes high (in the same way as **Lock Until Reset**). Unlike the “Settled” state in the **Continuous Update** mode, only a signal loss lasting more than 1ms (typical) will cause 960MegaQ™ to re-equalize the signal when it returns. In this sense, the **Lock Until Signal Loss** mode can be considered as halfway between the **Continuous Update** mode and the **Lock Until Reset** mode. The **Lock Until Signal Loss** mode is useful, for example, when testing or demonstrating a system by plugging in multiple different length cables - it eliminates the need to also generate a reset. To prevent potentially undesired re-equalization, signal losses lasting less than 1ms (typical) do not trigger a re-equalization.

### MANUAL LENGTH

**Manual Length** mode is entered by setting address 0x05[1:0] = 11b. **Manual Length** mode allows the forcing of specific cable lengths, cable type, DC gains, etc. (see the “Register Listing” table on page 13). The “Cable Type” bit (0x05 [4]) allows selection between the two most common cable types for security video: Cat 5/Cat 6 or steel core RG-59 coaxial. However, since many of 960MegaQ™’s automatic functions and adjustments are disabled in **Manual Length** mode, performance is almost always worse than what is achieved in any of the automatic modes. For example, automatic polarity correction is disabled so the polarity must be manually set using the INVERT bit. There is no practical reason to ever use **Manual Length** mode in normal operation.

## Serial Interface Protocol

While 960MegaQ™ is designed to work as a stand-alone equalizer, it does have a serial interface that can be used to control it and monitor its state.

The serial interface is used to read and write the configuration registers. It uses three signals (SCK, SD, and SEN) for programming. The serial clock can operate up to 5MHz (5Mbits/s). The “Serial Timing Diagram” on page 8 shows the timing of serial I/O.

A transaction begins when the host microcontroller takes SEN (serial enable) high. The first 8 bits on the SD (serial data) pin are latched by 960MegaQ™ on the rising edge of SCK (serial clock) to form the address byte. The MSB of the address byte indicates whether the operation is a read (1) or a write (0), and the next seven bits indicate which register is to be read from or written to. Each read and write operation consists of 16 bits: 8 bits for an address byte followed by 8 bits of data. See the “Serial Timing Diagram” on page 6 for more details on using the SPI interface.

TABLE 2. ADDRESS BYTE FORMAT

|                       |    |    |    |    |    |    |       |
|-----------------------|----|----|----|----|----|----|-------|
| 0 = Write<br>1 = Read | A6 | A5 | A4 | A3 | A2 | A1 | A0    |
| (MSB)                 |    |    |    |    |    |    | (LSB) |

### WRITE OPERATION

After the address byte is clocked in, the next 8 bits should contain the data to be sent to the register identified in the address byte.

### READ OPERATION

After the rising edge of the 8th clock after the address byte is clocked in, the microcontroller should tristate the SD line so 960MegaQ™ can begin to output data on the SD pin (from the register identified in the address byte), beginning on the 9th rising edge of SCK. The data should be latched on the *falling* edge of SCK to allow enough time for the data to settle. See “Serial Timing Diagram” on page 6 for more details on how to read from the registers.

## Register Listing

| ADDRESS | REGISTER<br>(DEFAULT VALUE) | BIT(S) | FUNCTION NAME     | DESCRIPTION   |
|---------|-----------------------------|--------|-------------------|---|
| 0x00    | Device ID (0x30)            | 3:0    | Device Revision   | 0 = initial silicon, 1 = first revision, etc.   |
|         |                             | 7:4    | Device ID         | 0x3   |
| 0x01    | Signal Status (N/A)         | 0      | Signal Present    | 0: A signal is not present at the input<br>1: A signal is present at the input  |
|         |                             | 1      | DLL Locked        | 0: DLL is not locked<br>1: DLL is locked  |
|         |                             | 2      | Signal Polarity   | 0: Inverted Polarity<br>1: Nominal Polarity<br>This bit is only valid if the INVERT pin is connected as an output. If INVERT is overdriven, this value may not reflect the polarity of the input signal.  |
|         |                             | 3      | Color Detected    | 0: Signal is monochrome<br>1: Signal has a colorburst   |
|         |                             | 4      | Signal Overloaded | 0: Signal (if present) is within normal range<br>1: Signal appears to be overloaded   |
|         |                             | 5      | Settled           | 0: EQ is not settled, though DLL may be locked.<br>1: EQ has stabilized and equalization achieved.  |
| 0x02    | Manual Length (0x00)        | 5:0    | Manual Length     | Manual Length Control; 0x0 through 0x3F,<br>64 feet per bit.<br>0x0: 0 feet.<br>0x3F: 4000 feet (Cat 5 mode)<br>This register sets the EQ setting when 960MegaQ™ is in manual length mode (reg 0x05[1:0] = 11).<br>Note that the length in this register is for Cat 5 cable when "Cable Type" (reg 0x05[4]) equals 0. When "Cable Type" is set to 1 (coax mode), then the length is for steel core coax. In coax mode, the maximum length is 0x0F (~1200 feet) and setting the register higher than this value does not provide any increase in equalization. |
| 0x03    | Manual DC Gain (0x20)       | 5:0    | Manual DC Gain    | 0x00: Maximum DC Gain (+3dB)<br>0x20: Mid-Scale 0dB<br>0x3F: Minimum DC Gain (-3dB)<br>This register sets the DC Gain when the device is in manual length mode (reg 0x05[1:0] = 11).  |

## Register Listing (Continued)

| ADDRESS | REGISTER<br>(DEFAULT VALUE) | BIT(S) | FUNCTION NAME                     | DESCRIPTION  |
|---------|-----------------------------|--------|-----------------------------------|--|
| 0x04    | Pin Overrides (0x00)        | 0      | Freeze Select                     | 0: Use value of FREEZE pin.<br>1: Use value in "Freeze Value" bit  |
|         |                             | 1      | Freeze Value                      | If Freeze Select = 1, then:<br>0: Equalization is not frozen<br>1: Equalization is frozen at current setting.<br>If Freeze Select = 0, then this bit is ignored.   |
|         |                             | 2      | Eq-Disable Select                 | 0: Use value of EQ_DISABLE pin.<br>1: Use value in "Eq-Disable Value" bit  |
|         |                             | 3      | Eq-Disable Value                  | If Eq-Disable Select = 1, then:<br>0: Equalizer is enabled<br>1: Equalizer is disabled (allows data to be sent upstream over cable pair connected to inputs)<br>If Eq-Disable Select = 0, then this bit is ignored.  |
|         |                             | 4      | Color Select                      | 0: Use value of COLOR pin<br>1: Use value in "Color Value" bit   |
|         |                             | 5      | Color Value                       | If Color Select = 1, then<br>0: Monochrome Mode<br>1: Color Mode<br>If Color Select = 0, then this bit is ignored.   |
|         |                             | 6      | Invert Select                     | 0: Use value of INVERT pin.<br>1: Use value in "Invert Value" bit  |
|         |                             | 7      | Invert Value                      | If Invert Select = 1, then<br>0: Incoming signal is not inverted<br>1: Incoming signal is inverted<br>If Invert Select = 0, then this bit is ignored.  |
| 0x05    | Equalization Control (0x00) | 1:0    | Locking Mode/Manual Length Enable | 00 = <b>Continuous Monitoring</b><br>01 = <b>Lock Until Signal Loss*</b><br>10 = <b>Lock Until Reset</b><br>11 = <b>Manual Length**</b><br>*Signal must be missing for at least 1ms in order to trigger a re-equalization.<br>**In <b>Manual Length</b> mode, the polarity corrector is disabled and the polarity must be set using the INVERT bit or pin.<br>Note: The FREEZE pin must be tied to ground/a logic low for this function to work correctly. |
|         |                             | 3:2    | Noise Filter                      | 00: No Noise Filtering<br>01: Min Noise Filtering<br>10 or 11: Max Noise Filtering   |
|         |                             | 4      | Cable Type                        | 0: Cat 5/Cat 6 Mode<br>1: Steel Core Coax Mode<br>This bit is ignored in all modes except <b>Manual Length</b> (reg 0x05[1:0] = 11).<br>Set to 1 if using copper-coated steel-core coaxial cable and you are in <b>Manual Length</b> .   |

## Bypassing and Layout Considerations

**960MegaQ™ requires a dedicated ground plane in order to function properly.** For 2-layer boards, pour a quarter-inch ground plane extending around the device on both the top and bottom layers. Ensure that the ground plane on the bottom layer is a **solid** plane with no traces cutting through it. Bypass capacitors must be placed as close as possible to the device in order to ensure good performance at longer lengths of equalization. Ensure that the ground connections for the bypass capacitors connect **directly** to the same uniform ground plane described previously.

### General PowerPAD Design Considerations

The thermal pad must be connected to the ground plane for heat dissipation. Figure 14 is an example of how to use vias to remove heat from the IC.

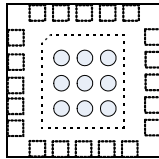


FIGURE 14. PCB VIA PATTERN

The thermal pad is electrically connected to GND through the high resistance IC substrate. We recommend you fill the thermal pad area with vias. The via array should be centered in the thermal pad and placed such that the center on center spacing is 3x the via radius. Vias should be small, but large enough to allow solder wicking during reflow. Connect all vias to ground. It is important the vias have a low thermal resistance for efficient heat transfer. Do not use “thermal relief” patterns. It is important to have a solid connection of the plated-through hole to each plane.

## Power Dissipation

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad (EQ. 1)$$

Where:

$T_{JMAX}$  = Maximum junction temperature

$T_{AMAX}$  = Maximum ambient temperature

$\theta_{JA}$  = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing use Equation 2:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \quad (EQ. 2)$$

for sinking use Equation 3:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT} - V_S) \times I_{LOAD} \quad (EQ. 3)$$

Where:

$V_S$  = Supply voltage

$I_{SMAX}$  = Maximum quiescent supply current

$V_{OUT}$  = Maximum output voltage of the application

$R_{LOAD}$  = Load resistance tied to ground

$I_{LOAD}$  = Load current

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE              | REVISION | CHANGE          |
|-------------------|----------|-----------------|
| December 18, 2012 | FN8358.0 | Initial Release |

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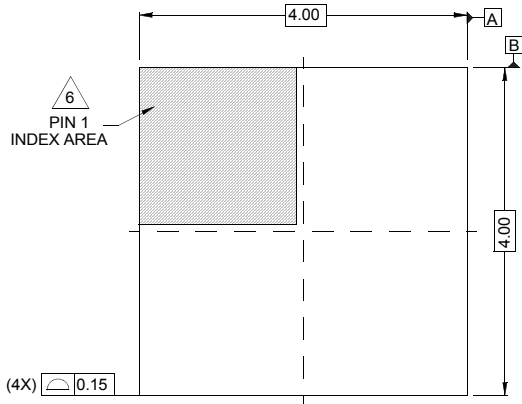
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# Package Outline Drawing

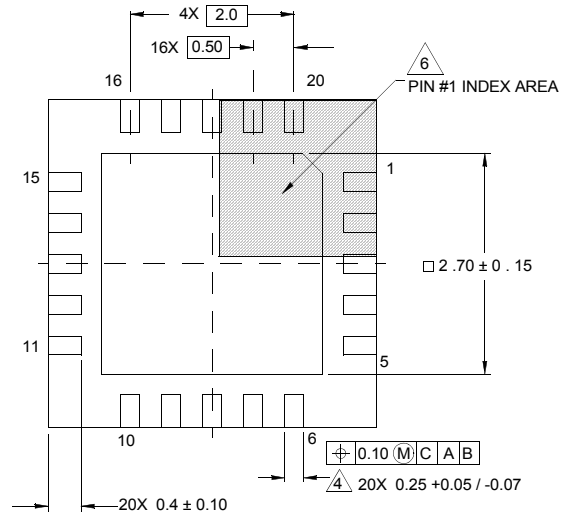
## L20.4x4C

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

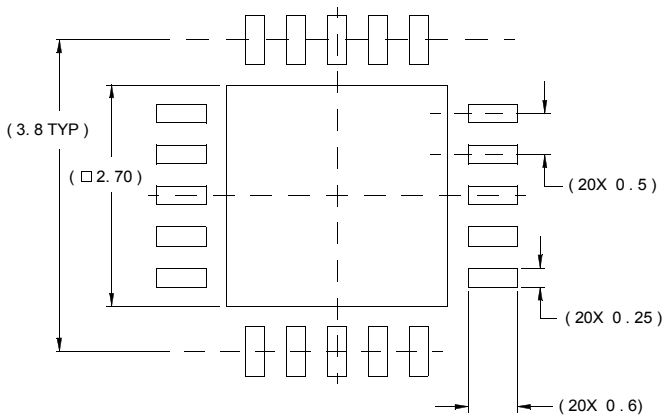
Rev 0, 11/06



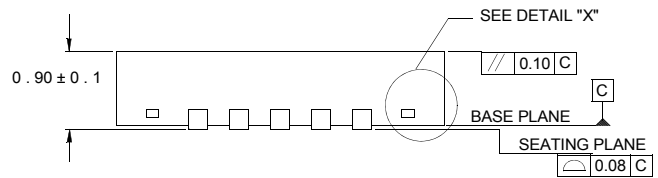
TOP VIEW



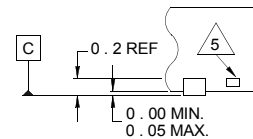
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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