



**THE DATASHEET OF  
IDT5T940-10NLGI**





# PRECISION CLOCK GENERATOR OC-192 APPLICATIONS

## IDT5T940

**PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES OCTOBER 28, 2014**

### FEATURES:

- **Input frequency:**
  - For SONET non-FEC: 19.44MHz, 38.88MHz, 77.76MHz, 155.52MHz, 311.04MHz, or 622.08MHz
  - For SONET FEC: 20.83MHz, 41.66MHz, 83.31MHz, 166.63MHz, 333.26MHz, or 666.52MHz
  - For 10GE copper: 19.53MHz, 39.06MHz, 78.125MHz, 156.25MHz, 312.5MHz, or 625MHz
  - For 10GE optical: 20.14MHz, 40.28MHz, 80.56MHz, 161.13MHz, 322.26MHz, or 644.53MHz
- **3-level inputs for feedback divide ratio and output frequency range selection**
- **1x, 2x, 4x, 8x, 16x, and 32x outputs on QOUT**
- **Regenerated input clock or QOUT/4 on QREG**
- **Lock indicator**
- **Power-down mode**
- **LVPECL or LVDS outputs**
- **Three modes of output frequency range**
  - Mode 0: QOUT range 155.5 - 166.6MHz. QREG is a regenerated version of the input clock.
  - Mode 1: QOUT range 622 - 666.5MHz. QREG output 155.5-166.6MHz.
  - Mode 2: QOUT range 622 - 666.5MHz. QREG is a regenerated version of the input clock frequency.
- **Selectable loop bandwidths**
- **Hitless switchover**
- **Differential LVPECL, LVDS, or single-ended LVTTTL input interface**
- **2.375 - 3.465V core and I/O**
- **Available in VFQFPN package**
- **use replacement part:8T49N222B-dddNLGI**

### DESCRIPTION:

The IDT5T940 generates a high precision FEC (Forward Error Correction) or non-FEC source clock for SONET/SDH systems as well as a source clock for Gigabit Ethernet systems. This device also has clock regeneration capability: it creates a "clean" version of the clock input by using the internal oscillator to square the input clock's rising and falling edges and remove jitter. In the event that the main clock input fails, the device automatically locks to a backup reference clock using a hitless switchover mechanism.

This device detects loss of valid CLKIN and leaves the VCO of the PLL at the last valid frequency while an alternate input REFIN is selected. If CLKIN and REFIN are different frequencies, the multiplication factor will be adjusted to retain the same output frequency.

The IDT5T940 can act as a translator from a differential LVPECL, LVDS, or single-ended LVTTTL input to LVPECL or LVDS outputs. The IDT5T940-10 has LVDS outputs and the IDT5T940-30 has LVPECL outputs.

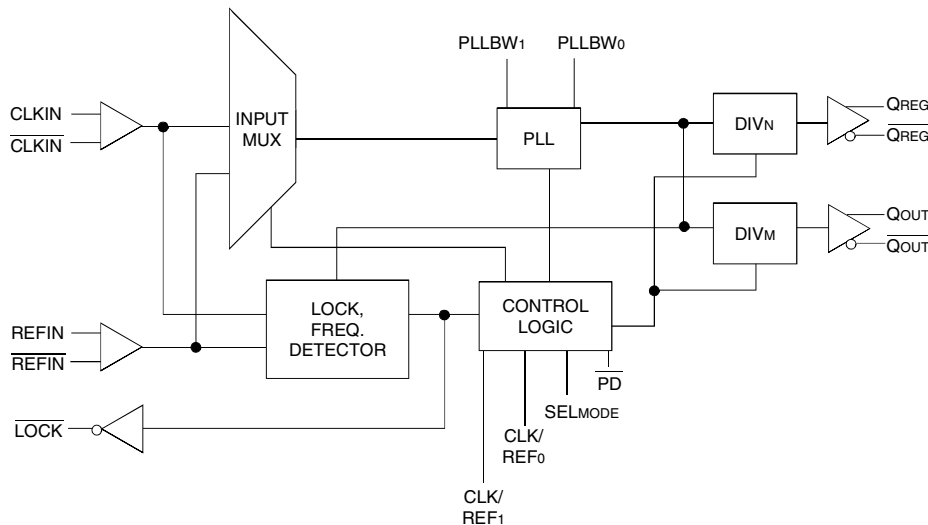
The three modes of output frequency range are controlled by the SELmode, which is a 3-level pin. When SELmode is high or low, the QOUT is a multiplied version of the input clock while QREG is a regenerated version of the input clock. When SELmode is mid, the QOUT is a multiplied version of the input clock while QREG is QOUT/4.

The IDT5T940 features a selectable loop bandwidth.

### APPLICATIONS:

- Terabit routers
- Gigabit ethernet systems
- SONET / SDH systems
- Digital cross connects
- Optical transceiver modules

### FUNCTIONAL BLOCK DIAGRAM

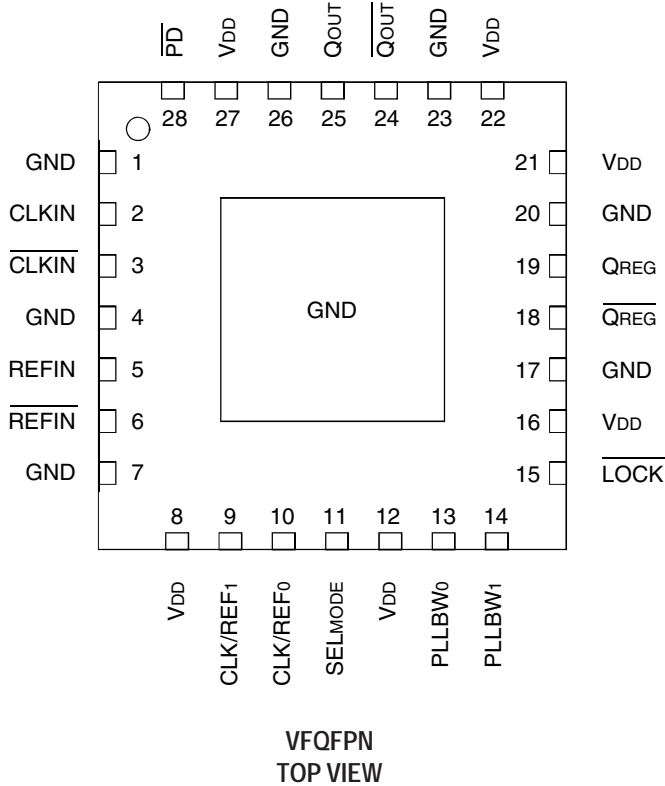


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**INDUSTRIAL TEMPERATURE RANGE**

**MAY 2013**

### PIN CONFIGURATION



### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>DD</sub>	Power Supply Voltage	-0.5 to +4.1	V
V <sub>I</sub>	Input Voltage	-0.5 to +4.1	V
V <sub>O</sub>	Output Voltage	-0.5 to V <sub>DD</sub> +0.5	V
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +165	°C

**NOTE:**

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### CAPACITANCE (T<sub>A</sub> = +25°C, f = 1MHz, V<sub>IN</sub> = 0V)

Parameter	Description	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	2.5	3	pF
C <sub>OUT</sub>	Output Capacitance	—	—	pF

**NOTE:**

- Capacitance applies to all inputs except CLK/REF<sub>[1:0]</sub> and SELmode.

### RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T <sub>A</sub>	Ambient Operating Temperature	-40	+25	+85	°C
V <sub>DD</sub>	Power Supply Voltage	2.375	—	3.465	V
V <sub>T</sub>	Termination Voltage (LVPECL)	—	V <sub>DD</sub> - 2	—	V
	Termination Voltage (LVDS)	—	1.2	—	

### PLL BANDWIDTH SELECTION

PLLBW[1:0]	Min.	Max.	Min. CLKIN/REFIN
LL	65KHz	120KHz	19.44MHz
LH	250KHz	500KHz	19.44MHz
HL	1MHz	2MHz	38.88MHz
HH	4MHz	8MHz	155.52MHz

### OUTPUT FREQUENCY RANGE

SELmode	Q <sub>OUT</sub> / $\overline{Q}$ <sub>OUT</sub>	Q <sub>REG</sub> / $\overline{Q}$ <sub>REG</sub>	Unit
L	155.5 - 166.6	regenerated CLKIN/CLKIN $\overline{}$	MHz
M	622 - 666.5	155.5 - 166.6	MHz
H	622 - 666.5	regenerated CLKIN/CLKIN $\overline{}$	MHz

### INPUT FREQUENCY RANGE

CLK/REF[1:0]	Input Frequency Range
HH	19.4MHz - 20.9MHz
HM	reserved
HL	38.8MHz - 41.7MHz
MH	77.7MHz - 83.4MHz
MM	Automatic Detection
ML	155.5MHz - 167MHz
LH	311MHz - 334MHz
LM	reserved
LL	622MHz - 667MHz

### LOCK FREQUENCY DETECTOR

The 5T940 will lock to, and track, a valid CLKIN signal;  $\overline{LOCK}$  will be low when this has occurred. If CLKIN fails, the 5T940 PLL will smoothly switch to lock to REFIN without generating any glitches on the output. The fact that the PLL is locked to REFIN rather than CLKIN is indicated by a high state on  $\overline{LOCK}$ . When a valid input is then applied to CLKIN, the 5T940 will smoothly switch back to locking on CLKIN, and  $\overline{LOCK}$  will go low.  $\overline{LOCK}$  will also switch to high should the frequency of CLKIN drift close to the limits of the VCO tuning range.

### PIN DESCRIPTION

Pin Name	I/O	Type	Description
CLKIN, $\overline{CLKIN}$	I	Adjustable <sup>(1)</sup>	Differential or single-ended clock input signal. For differential, LVPECL or LVDS supported. If left open-circuited, inputs will float to LVTTTL threshold voltage so that either input may be used as a single-ended input. A capacitor to ground should be connected on the floating input.
REFIN, $\overline{REFIN}$	I	Adjustable <sup>(1)</sup>	Differential reference clock input. The reference clock input is used as an input to the PLL when CLKIN/ $\overline{CLKIN}$ fails. Differential or single-ended clock input signal. For differential, LVPECL or LVDS supported. If left open-circuited, inputs will float to LVTTTL threshold voltage so that either input may be used as a single-ended input. A capacitor to ground should be connected on the floating input.
CLK/REF[1:0]	I	3-level <sup>(2)</sup>	3 level inputs controlling PLL feedback divider ratio. Automatic detection is used if both inputs are MID.
SELmode	I	3-level <sup>(2)</sup>	3 level input to select output frequency range for Q <sub>OUT</sub> / $\overline{Q}$ <sub>OUT</sub> and Q <sub>REG</sub> / $\overline{Q}$ <sub>REG</sub> (see Output Frequency Range table)
PLLBW[1:0]	I	LVTTTL	PLL Bandwidth Select Inputs (see PLL Bandwidth Selection table)
$\overline{PD}$	I	LVTTTL	Power Down Control. Shuts off entire chip when LOW.
Q <sub>OUT</sub> , $\overline{Q}$ <sub>OUT</sub>	O	Adjustable <sup>(3)</sup>	Differential clock output. LVPECL or LVDS outputs.
Q <sub>REG</sub> , $\overline{Q}$ <sub>REG</sub>	O	Adjustable <sup>(3)</sup>	Regenerated clock output from CLKIN/ $\overline{CLKIN}$ , LVPECL, or LVDS outputs.
$\overline{LOCK}$	O	LVTTTL	LOW when PLL is locked to CLKIN, HIGH in all other conditions
V <sub>DD</sub>		PWR	Power Supply
GND		PWR	Ground

#### NOTES:

- Inputs are capable of translating the following interface standards:  
Single-ended 3.3V LVTTTL levels  
Single-ended 2.5V LVTTTL levels  
Differential LVPECL levels  
Differential LVDS levels
- 3-level inputs are static inputs and must be tied to V<sub>DD</sub> or GND or left floating.
- Outputs can be LVPECL or LVDS.

*CLOCK INPUT/OUTPUT CONFIGURATION DESCRIPTION*

Application	REFIN (MHz)	CKIN (MHz)	SELmode	QREG (MHz)	QOUT (MHz)	
Non-FEC	19.44, 38.88, 77.76, 155.52, 311.04, 622.08	19.44	LOW	19.44	155.52	
			MID	155.52	622.08	
			HIGH	19.44	622.08	
		38.88	LOW	38.88	155.52	155.52
			MID	155.52	622.08	622.08
			HIGH	38.88	622.08	622.08
		77.76	LOW	77.76	155.52	155.52
			MID	155.52	622.08	622.08
			HIGH	77.76	622.08	622.08
		155.52	LOW	155.52	155.52	155.52
			MID	155.52	622.08	622.08
			HIGH	155.52	622.08	622.08
		311.04	LOW	311.04	155.52	155.52
			MID	155.52	622.08	622.08
			HIGH	311.04	622.08	622.08
		622.08	LOW	622.08	155.52	155.52
			MID	155.52	622.08	622.08
			HIGH	622.08	622.08	622.08
FEC	20.83, 41.66, 83.31, 166.63, 333.26, 666.52	20.83	LOW	20.83	166.63	
			MID	166.63	666.52	
			HIGH	20.83	666.52	
		41.66	LOW	41.66	166.63	166.63
			MID	166.63	666.52	666.52
			HIGH	41.66	666.52	666.52
		83.31	LOW	83.31	166.63	166.63
			MID	166.63	666.52	666.52
			HIGH	83.31	666.52	666.52
		166.63	LOW	166.63	166.63	166.63
			MID	166.63	666.52	666.52
			HIGH	166.63	666.52	666.52
		333.26	LOW	333.26	166.63	166.63
			MID	166.63	666.52	666.52
			HIGH	333.26	666.52	666.52
		666.52	LOW	666.52	166.63	166.63
			MID	166.63	666.52	666.52
			HIGH	666.52	666.52	666.52

*CLOCK INPUT/OUTPUT CONFIGURATION DESCRIPTION (CONTINUED)*

Application	REFIN (MHz)	CKIN (MHz)	SEL mode	QREG (MHz)	QOUT (MHz)
10GE copper	19.53, 39.06, 78.12, 156.25, 312.5, 625	19.53	LOW	19.53	156.25
			MID	156.25	625
			HIGH	19.53	625
		39.06	LOW	39.06	156.25
			MID	156.25	625
			HIGH	39.06	625
		78.12	LOW	78.12	156.25
			MID	156.25	625
			HIGH	78.12	625
		156.25	LOW	156.25	156.25
			MID	156.25	625
			HIGH	156.25	625
		312.5	LOW	312.50	156.25
			MID	156.25	625
			HIGH	312.5	625
		625	LOW	625	156.25
			MID	156.25	625
			HIGH	625	625
10GE optical	20.14, 40.28, 80.56, 161.13, 322.26, 644.53	20.14	LOW	20.14	161.13
			MID	161.13	644.53
			HIGH	20.14	644.53
		40.28	LOW	40.28	161.13
			MID	161.13	644.53
			HIGH	40.28	644.53
		80.56	LOW	80.56	161.13
			MID	161.13	644.53
			HIGH	80.56	644.53
		161.13	LOW	161.13	161.13
			MID	161.13	644.53
			HIGH	161.13	644.53
		322.26	LOW	322.26	161.13
			MID	161.13	644.53
			HIGH	322.26	644.53
		644.53	LOW	644.53	161.13
			MID	161.13	644.53
			HIGH	644.53	644.53

### POWER SUPPLY CHARACTERISTICS<sup>(1,2)</sup>

Symbol	Parameter	Test Conditions	Typ.	Max	Unit
I <sub>DD_PD</sub>	Power Supply Current	V <sub>DD</sub> = Max., P <sub>D</sub> = GND, All outputs unloaded	—	50	μA
ΔI <sub>DD</sub>	Power Supply Current per Input HIGH (LVTTL inputs only)	V <sub>DD</sub> = Max., V <sub>IN</sub> = 2.375V	—	100	μA
I <sub>TOT</sub>	Total Power Supply Current	V <sub>DD</sub> = Max., Q <sub>OUT</sub> = 622MHz, All outputs unloaded	—	200	mA

**NOTES:**

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. As a general requirement, these parts must be capable of operating at the maximum frequency under a nominal load at a reasonable operating temperature. That means that these parts must not burn up under extended use in a typical application.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Max	Unit
V <sub>IHH</sub>	Input HIGH Voltage Level <sup>(1)</sup>	3-Level Inputs Only	V <sub>DD</sub> - 0.4	—	V
V <sub>IMM</sub>	Input MID Voltage Level <sup>(1)</sup>	3-Level Inputs Only	V <sub>DD</sub> /2 - 0.2	V <sub>DD</sub> /2 + 0.2	V
V <sub>ILL</sub>	Input LOW Voltage Level <sup>(1)</sup>	3-Level Inputs Only	—	0.4	V
I <sub>3</sub>	3-Level Input DC Current	V <sub>IN</sub> = V <sub>DD</sub> HIGH Level	—	200	μA
		V <sub>IN</sub> = V <sub>DD</sub> /2 MID Level	-50	+50	
		V <sub>IN</sub> = GND LOW Level	-200	—	

**NOTE:**

1. These inputs are normally wired to V<sub>DD</sub>, GND, or left floating. Internal termination resistors bias unconnected inputs to V<sub>DD</sub>/2. If these inputs are switched dynamically after powerup, the function and timing of the outputs may be glitched, and the PLL may require additional t<sub>AO</sub> time before all datasheet limits are achieved.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVTTL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
I <sub>IH</sub>	Input HIGH Current	V <sub>DD</sub> = 3.465V	—	—	±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>DD</sub> = 3.465V	—	—	±1	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>DD</sub> = 2.375V, I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V
V <sub>IN</sub>	DC Input Voltage		-0.3	—	+3.465	V
V <sub>IH</sub>	DC Input HIGH		1.7	—	—	V
V <sub>IL</sub>	DC Input LOW		—	—	0.7	V

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVPECL<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Input Characteristics</b>						
I <sub>IN</sub>	Input Current (CLKIN, REFIN)	V <sub>DD</sub> = 3.465V	-20	—	+20	μA
V <sub>CMR</sub>	Common Mode Input Voltage		1	—	V <sub>DD</sub> - 0.3	V
V <sub>DIF</sub>	Differential Voltage Required to Toggle Input		100	—	—	mV
<b>Output Characteristics</b>						
V <sub>OH</sub>	Output Voltage HIGH (terminated through 50Ω tied to V <sub>DD</sub> - 2V) <sup>(2)</sup>		V <sub>DD</sub> - 1.15	—	V <sub>DD</sub> - 0.9	V
V <sub>OL</sub>	Output Voltage LOW (terminated through 50Ω tied to V <sub>DD</sub> - 2V) <sup>(2)</sup>		V <sub>DD</sub> - 1.95	—	V <sub>DD</sub> - 1.61	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		0.55	—	0.93	V

**NOTES:**

1. V<sub>DD</sub> = 2.375 - 3.645V.
2. Not to exceed V<sub>DD</sub> - 0.05V.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVDS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Input Characteristics</b>						
I <sub>IN</sub>	Input Current (CLKIN, REFIN)	V <sub>DD</sub> = 3.465V	-20	—	+20	μA
V <sub>CM</sub>	Common Mode Input Voltage Range <sup>(1)</sup>		0.9	—	V <sub>DD</sub> - 0.05	V
V <sub>DIF</sub>	Differential Voltage Required to Toggle Input		100	—	—	mV
<b>Output Characteristics</b>						
V <sub>OT(+)</sub>	Differential Output Voltage for the TRUE Binary State		247	—	454	mV
V <sub>OT(-)</sub>	Differential Output Voltage for the FALSE Binary State		-247	—	-454	mV
ΔV <sub>OT</sub>	Change in V <sub>OT</sub> Between Complementary Output States		—	—	50	mV
V <sub>OS</sub>	Output Common Mode Voltage (Offset Voltage)		1.125	1.2	1.375	V
ΔV <sub>OS</sub>	Change in V <sub>OS</sub> Between Complementary Output States		—	—	50	mV
I <sub>OS</sub>	Outputs Short Circuit Current	V <sub>OUT(+)</sub> and V <sub>OUT(-)</sub> = 0V	—	9	24	mA
I <sub>OSD</sub>	Differential Outputs Short Circuit Current	V <sub>OUT(+)</sub> = V <sub>OUT(-)</sub>	—	6	12	mA

**NOTE:**

1. Not to exceed V<sub>DD</sub> - 0.05V.

### INPUT TIMING REQUIREMENTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
REF <sub>H</sub>	Input Reference Clock Duty Cycle	40	50	60	%
F <sub>REF</sub>	Input Reference Clock Range	19.44	—	666.52	MHz
REF <sub>TOL</sub>	Input Reference Clock Frequency Tolerance	-100	—	100	ppm
F <sub>CLKIN</sub>	Clock in Frequency Range	19.44	—	666.52	MHz
CLKIN <sub>H</sub>	Clock in Duty Cycle	40	50	60	%
t <sub>AO</sub>	Acquisition Time from Return of Valid CLKIN	—	60	150	us
LOCK <sub>TOL</sub>	Frequency Tolerance for LOCK	-600	±450	600	ppm
t <sub>INT(TOL)</sub>	Tolerance to Input Jitter	GR-253 Sect. 5.6.2.2			

### AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (OC-192)

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Q <sub>OUT</sub>	Multiplied Clock Output Frequency	SELmode = LOW	155.52	—	166.63	MHz
		SELmode = MID	155.52	—	666.52	
		SELmode = HIGH	622.08	—	666.52	
Q <sub>REG</sub>	Regenerated Clock Output Frequency	19.44	—	666.52	MHz	
CLKIN	Input Clock Frequency	19.44	—	667	MHz	
t <sub>r</sub>	Output Rise Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t <sub>f</sub>	Output Fall Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t <sub>SK</sub>	Skew between Q <sub>OUT</sub> and Q <sub>REG</sub>	—	10	20	ps	
PLL <sub>BW</sub>	PLL Bandwidth Setting	65	80	120	KHz	
ƒ <sub>p</sub>	Jitter Transfer Peaking	—	—	0.1	dB	
t <sub>j</sub>	Jitter Generation <sup>(1)</sup> (with 50KHz to 80MHz band pass filter)	Output Frequency = 622MHz - 666.5MHz	—	0.3	0.65	ps (RMS)
		Output Frequency = 155.5MHz - 166.6MHz	—	1	2	
t <sub>DUTY</sub>	Output Duty Cycle	45	—	55	%	

**NOTE:**

1. All input frequencies and PLL<sub>BW</sub>[1:0] permitted by PLL Bandwidth Selection table.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (OC-48)

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Q <sub>OUT</sub>	Multiplied Clock Output Frequency	SELmode = LOW	155.52	—	166.63	MHz
		SELmode = MID	155.52	—	666.52	
		SELmode = HIGH	622.08	—	666.52	
Q <sub>REG</sub>	Regenerated Clock Output Frequency	19.44	—	666.52	MHz	
CLK <sub>IN</sub>	Input Clock Frequency	19.44	—	667	MHz	
t <sub>r</sub>	Output Rise Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t <sub>f</sub>	Output Fall Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t <sub>sk</sub>	Skew between Q <sub>OUT</sub> and Q <sub>REG</sub>	—	10	20	ps	
PLL <sub>BW</sub>	PLL Bandwidth Setting	65	80	120	KHz	
		250	305	500		
⌈	Jitter Transfer Peaking	—	0.05	0.1	dB	
t <sub>j</sub>	Jitter Generation (with 12KHz to 20MHz filter) <sup>(1)</sup>	Output frequency = 622MHz - 666.5MHz	—	0.1	0.3	ps (RMS)
		Output frequency = 155.5MHz - 166.6MHz	—	0.4	1.5	
		Output frequency = 77.7MHz - 83.4MHz	—	0.5	1.7	
t <sub>DUTY</sub>	Output Duty Cycle	45	—	55	%	

NOTE:

1. All input frequencies and PLL<sub>BW</sub>[1:0] permitted by PLL Bandwidth Selection table.

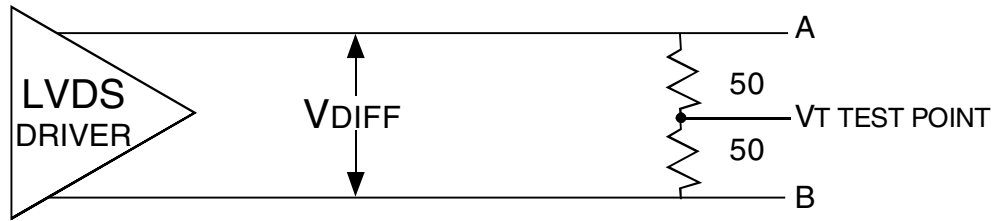
AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (OC-12)

Symbol	Parameter	Min.	Typ.	Max.	Unit	
Q <sub>OUT</sub>	Multiplied Clock Output Frequency	SELmode = LOW	155.52	—	166.63	MHz
		SELmode = MID	155.52	—	666.52	
		SELmode = HIGH	622.08	—	666.52	
Q <sub>REG</sub>	Regenerated Clock Output Frequency	19.44	—	666.52	MHz	
CLK <sub>IN</sub>	Input Clock Frequency	19.44	—	667	MHz	
t <sub>r</sub>	Output Rise Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t <sub>f</sub>	Output Fall Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t <sub>sk</sub>	Skew between Q <sub>OUT</sub> and Q <sub>REG</sub>	—	10	20	ps	
PLL <sub>BW</sub>	PLL Bandwidth Setting	65	80	120	KHz	
		250	305	500		
		1000	1250	2000		
⌈	Jitter Transfer Peaking	—	0.05	0.1	dB	
t <sub>j</sub>	Jitter Generation (with 3KHz to 5MHz filter) <sup>(1)</sup>	Output frequency = 155.5MHz - 166.6MHz	—	0.3	1.1	ps (RMS)
		Output frequency = 77.7MHz - 83.4MHz	—	0.4	1.3	
		Output frequency = 19.4MHz - 20.9MHz	—	0.5	1.6	
t <sub>DUTY</sub>	Output Duty Cycle	45	—	55	%	

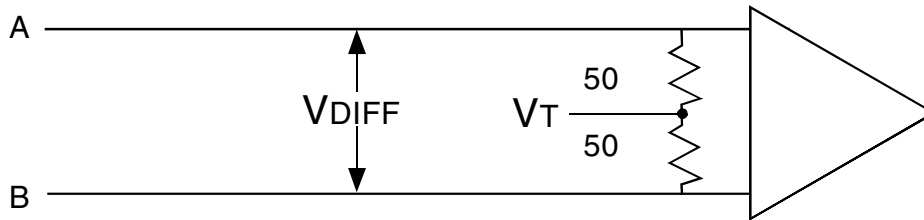
NOTE:

1. All input frequencies and PLL<sub>BW</sub>[1:0] permitted by PLL Bandwidth Selection table.

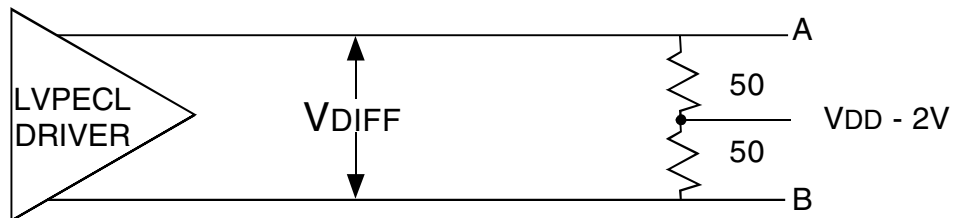
TEST CONDITIONS



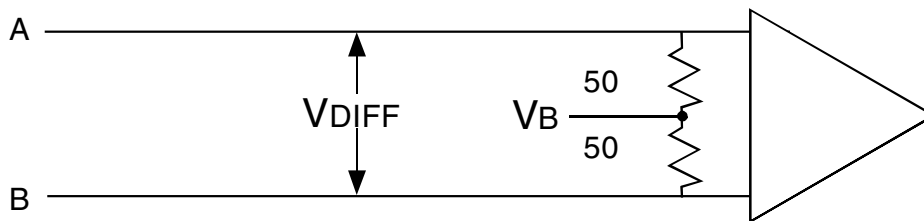
Test Circuit for LVDS Output Characteristics



Test Circuit for LVDS Input Characteristics



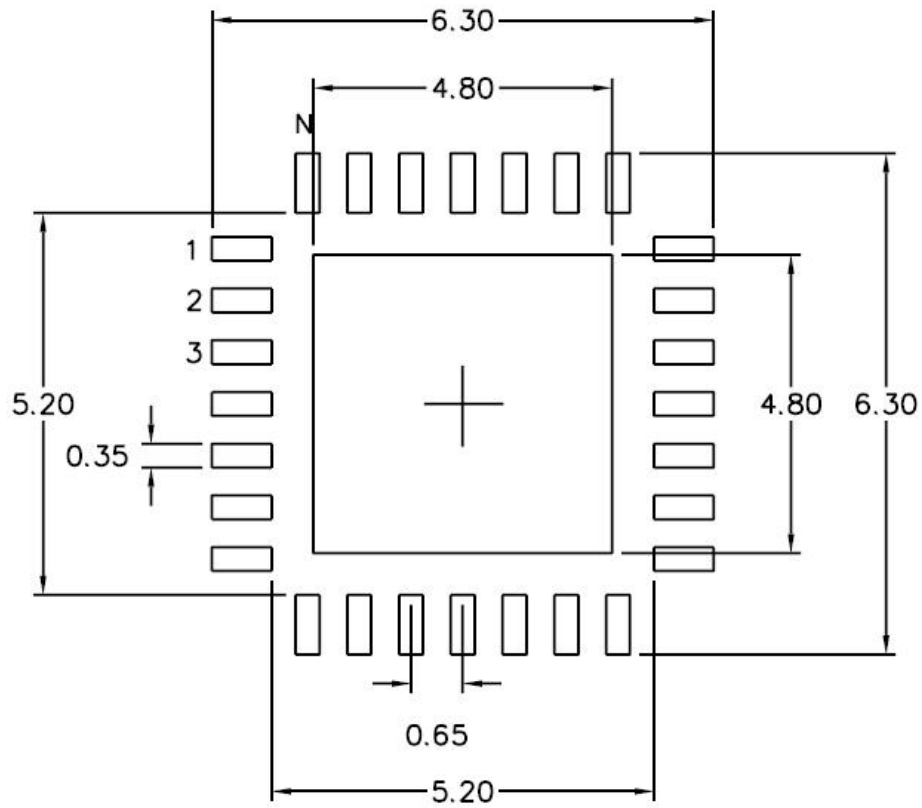
Test Circuit for LVPECL Output Characteristics



$$V_B = V_{DD} - 2V$$

Test Circuit for LVPECL Input Characteristics

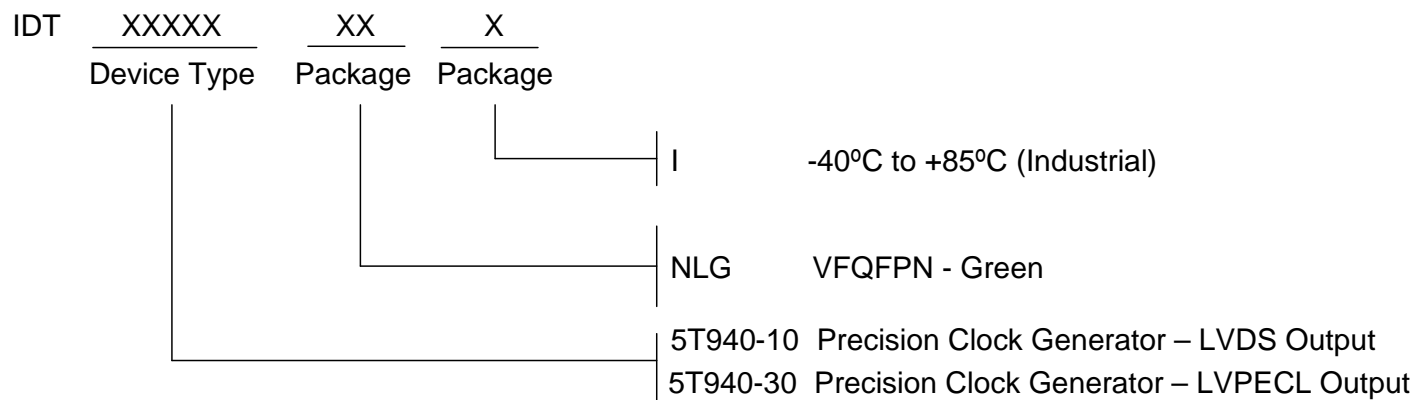
RECOMMENDED LANDING PATTERN



*NL 28 pin*

NOTE: All dimensions are in millimeters.

*ORDERING INFORMATION*



*REVISION HISTORY*

<b>Rev</b>	<b>Table</b>	<b>Page</b>	<b>Discription of Change</b>	<b>Date</b>
A		1	NRND - Not Recommended for New Designs	5/16/13
A		1	Product Discontinuation Notice - Last Time Buy Expires October 28, 2014, PDN# CQ-13-02	11/27/13

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