



THE DATASHEET OF
853S111AYILF



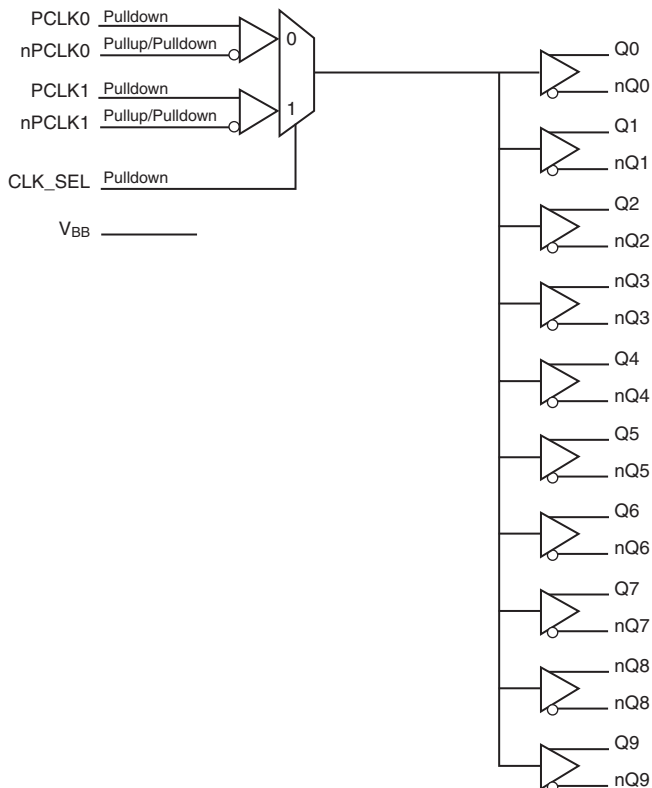
General Description

The 853S111AI is a low skew, high performance 1-to-10 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer. The 853S111AI is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the 853S111AI ideal for those clock distribution applications demanding well defined performance and repeatability.

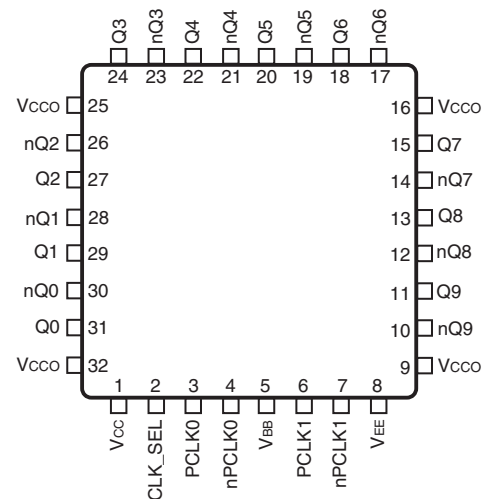
Features

- Ten differential 2.5V, 3.3V LVPECL/ECL outputs
- Two selectable differential input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, SSTL, CML
- Maximum output frequency: 2.5GHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Output skew: 55ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 780ps (maximum)
- Additive phase jitter, RMS: 0.07ps (typical)
- LVPECL mode operating voltage supply range: $V_{CC} = 2.375V$ to $3.465V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -3.465V$ to $-2.375V$
- $-40^{\circ}C$ to $85^{\circ}C$ ambient operating temperature
- Available lead-free (RoHS 6) package

Block Diagram



Pin Assignment



853S111AI

32-Lead LQFP

7mm x 7mm x 1.4mm package body

Y Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V _{CC}	Power		Positive supply pin.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. LVPECL interface levels. Also accepts standard LVCMOS/LVTTL input levels.
3	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V _{CC} /2 default when left floating.
5	V _{BB}	Output		Bias voltage to be connected for single-ended LVPECL input.
6	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V _{CC} /2 default when left floating.
8	V _{EE}	Power		Negative supply pin.
9, 16, 25, 32	V _{CC0}	Power		Output supply pins.
10, 11	nQ9, Q9	Output		Differential output pair. LVPECL/ECL interface levels.
12, 13	nQ8, Q8	Output		Differential output pair. LVPECL/ECL interface levels.
14, 15	nQ7, Q7	Output		Differential output pair. LVPECL/ECL interface levels.
17, 18	nQ6, Q6	Output		Differential output pair. LVPECL/ECL interface levels.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL/ECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL/ECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL/ECL interface levels.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL/ECL interface levels.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL/ECL interface levels.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R _{PULLDOWN}	Input Pulldown Resistor			75		kΩ
R _{VCC/2}	Pullup/Pulldown Resistors			50		kΩ

Function Tables

Table 3A. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
PCLK0 or PCLK1	nPCLK0 or nPCLK1	Q0:Q9	nQ0:nQ9		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

Note 1: Please refer to the Applications Information, "Wiring the Differential Input to Accept Single Ended Levels".

Table 3B. Control Input Function Table

Inputs	
CLK_SEL	Selected Source
0	PCLK0, nPCLK0
1	PCLK1, nPCLK1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, $V_{EE} = 0V$)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, $V_{CC} = 0V$)
Inputs, V_I (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, V_I (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, I_O Continuous Current Surge Current	50mA 100mA
V_{BB} Sink//Source, I_{BB}	$\pm 0.5mA$
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	80.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 2.375V$ to $3.465V$; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				74	mA

Table 4B. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V$; $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	2.27	2.36	2.45	2.16	2.33	2.45	2.06	2.32	2.45	V
V_{OL}	Output Low Voltage; NOTE 1	1.44	1.58	1.71	1.41	1.55	1.71	1.33	1.54	1.71	V
V_{IH}	Input High Voltage (Single-ended)	2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage (Single-ended)	1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2	1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1		200			200			200	μA
I_{IL}	Input Low Current	PCLK0, PCLK1		-10			-10			-10	μA
		nPCLK0, nPCLK1		-200			-200			-200	μA

NOTE: Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

NOTE 2: Single-ended input operation is limited. $V_{CC} \geq 3V$ in LVPECL mode.

NOTE 3: Common mode voltage is defined as V_{IH} .

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 2.5V$; $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	1.47	1.56	1.65	1.36	1.53	1.65	1.26	1.52	1.65	V
V_{OL}	Output Low Voltage; NOTE 1	0.64	0.78	0.91	0.61	0.75	0.91	0.53	0.74	0.91	V
V_{IH}	Input High Voltage (Single-ended)	1.275		1.56	1.275		1.56	1.275		1.56	V
V_{IL}	Input Low Voltage (Single-ended)	0.63		0.965	0.63		0.965	0.63		0.965	V
V_{PP}	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1		200			200			200	μA
I_{IL}	Input Low Current	PCLK0, PCLK1		-10			-10			-10	μA
		nPCLK0, nPCLK1		-200			-200			-200	μA

NOTE: Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

Table 4D. ECL DC Characteristics, $V_{CC} = 0V$; $V_{EE} = -3.465V$ to $-2.375V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	-1.030	-0.94	-0.85	-1.140	-0.97	-0.85	-1.24	-0.98	-0.85	V
V_{OL}	Output Low Voltage; NOTE 1	-1.86	-1.72	-1.59	-1.89	-1.75	-1.59	-1.97	-1.76	-1.59	V
V_{IH}	Input High Voltage (Single-ended)	-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage (Single-ended)	-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2	-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
V_{PP}	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3	$V_{EE}+1.2$		0	$V_{EE}+1.2$		0	$V_{EE}+1.2$		0	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1		200			200			200	μA
I_{IL}	Input Low Current	PCLK0, PCLK1		-10			-10			-10	μA
		nPCLK0, nPCLK1		-200			-200			-200	μA

NOTE: Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CC0} - 2V$.

NOTE 2: Single-ended input operation is limited. $V_{CC} \geq 3V$ in LVPECL mode.

NOTE 3: Common mode voltage is defined as V_{IH} .

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = V_{CC0} = -3.465V$ to $-2.375V$ or $V_{CC} = V_{CC0} = 2.375V$ to $3.465V$; $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	-40°C			25°C			85°C			Units		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
f_{OUT}	Output Frequency			2.5			2.5			2.5	GHz		
t_{PD}	Propagation Delay; NOTE 1	450	575	700	490	625	745	550	650	800	ps		
$t_{sk(o)}$	Output Skew; NOTE 2, 4		30	55		30	55		30	55	ps		
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4		100	250		100	250		100	250	ps		
f_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, 12kHz - 20MHz		0.07			0.07			0.07	ps		
t_R / t_F	Output Rise/Fall Time	20% to 80%		85	200	315	85	200	285	85	200	315	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters are measured at $f_{OUT} \leq 1GHz$, unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage, and with equal load conditions. Measured at the output differential cross points.

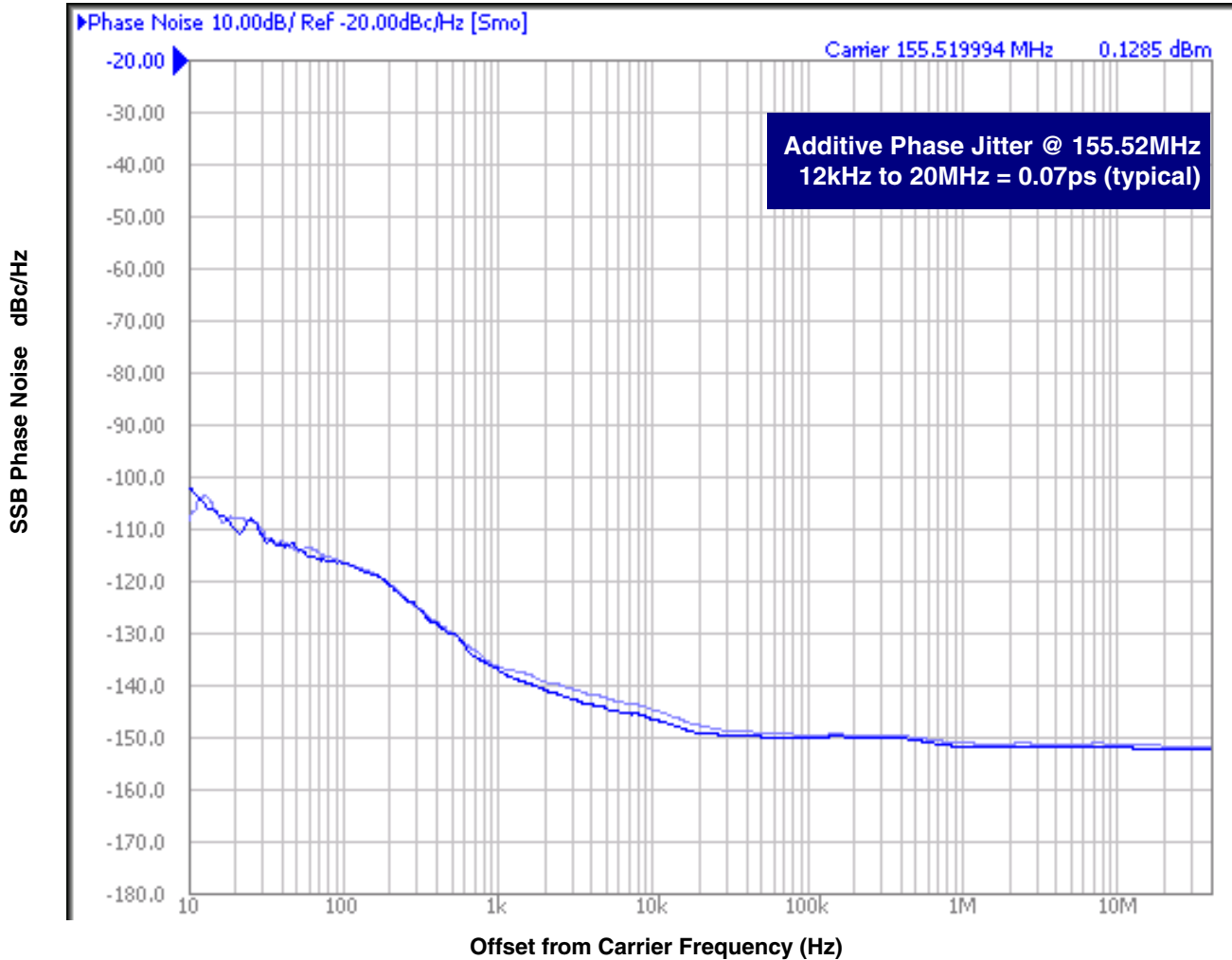
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

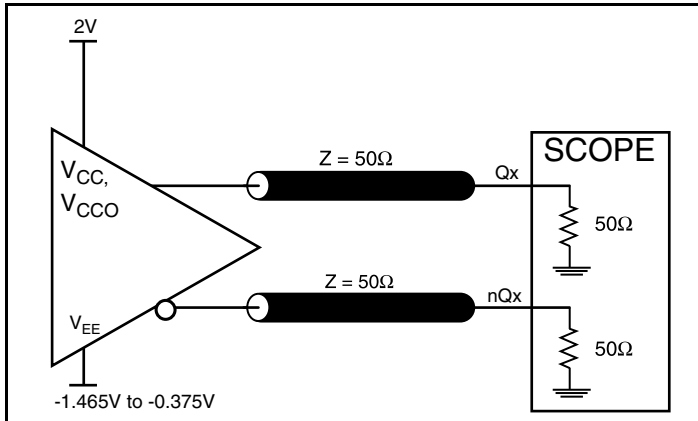
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



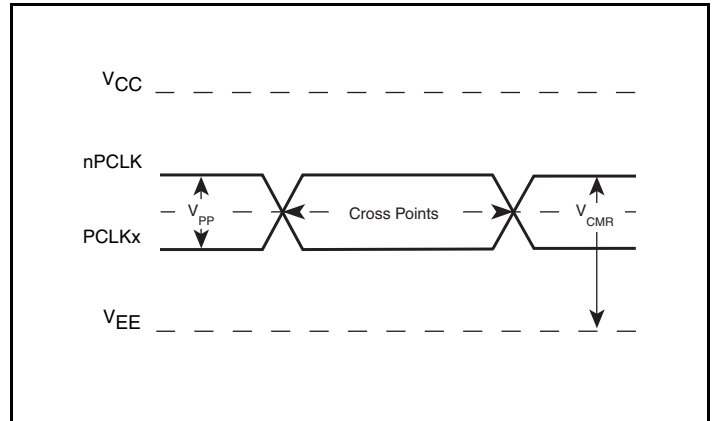
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "Rhode & Schwartz SMA 100A Signal Generator 9kHz – 6GHz as external input to a Hewlett Packard 8133A 3GHz Pulse Generator".

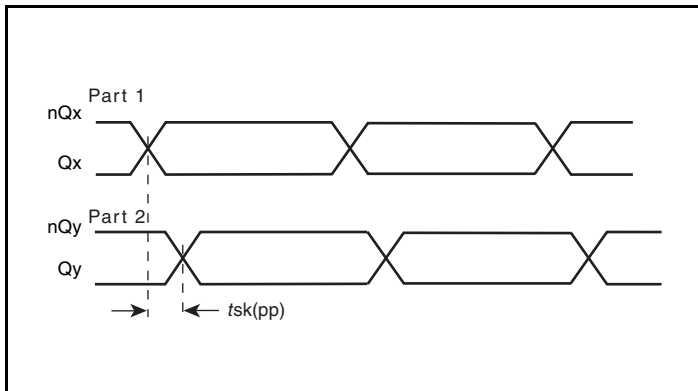
Parameter Measurement Information



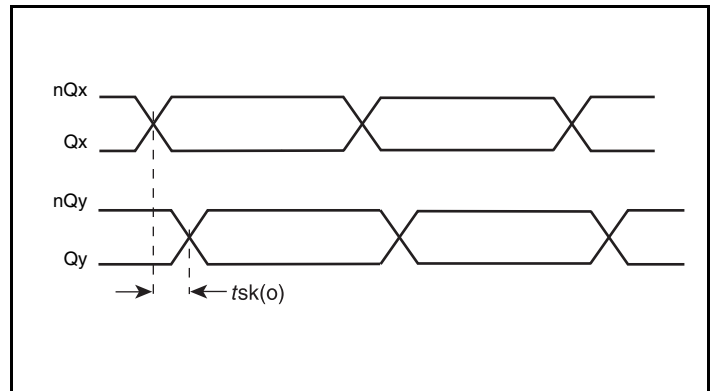
LVPECL Output Load AC Test Circuit



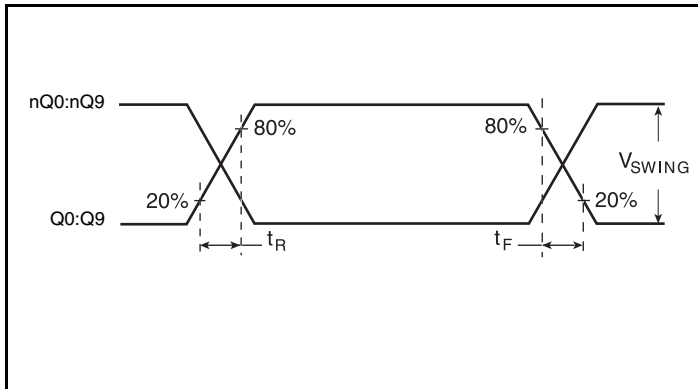
Differential Input Level



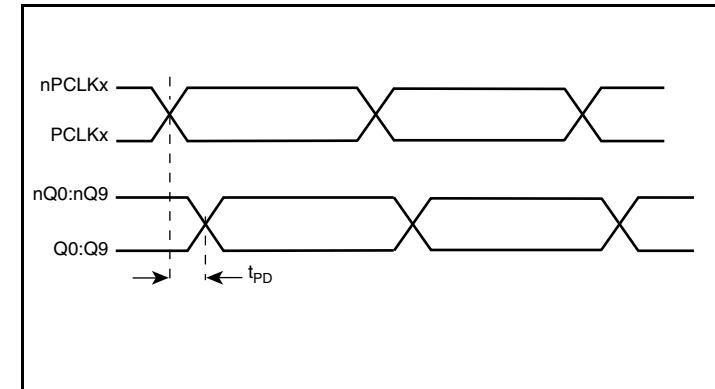
Part-to-Part Skew



Output Skew



Output Rise/Fall Time



Propagation Delay

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than $V_{CC} + 0.3V$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

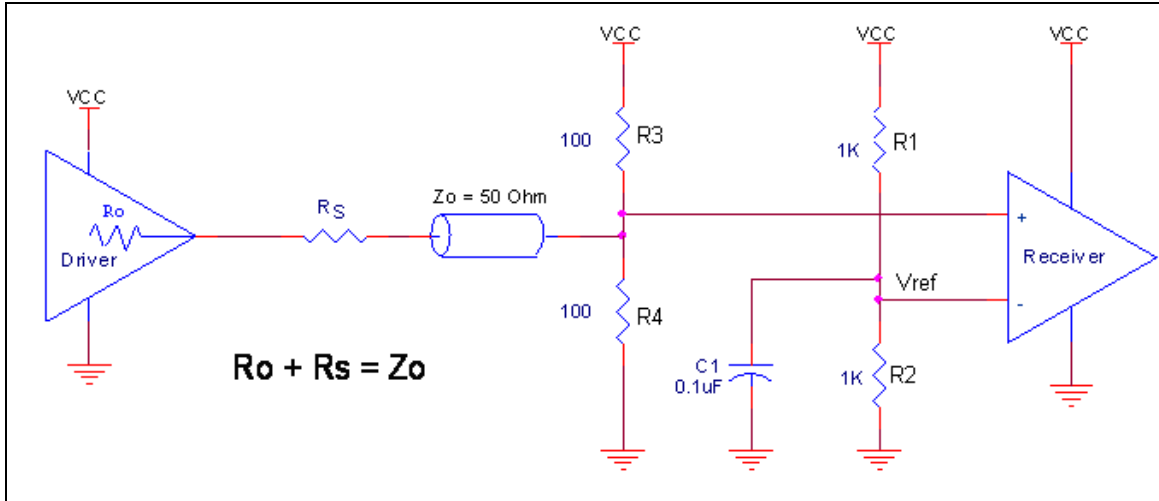


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, SSTL, CML and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2F show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

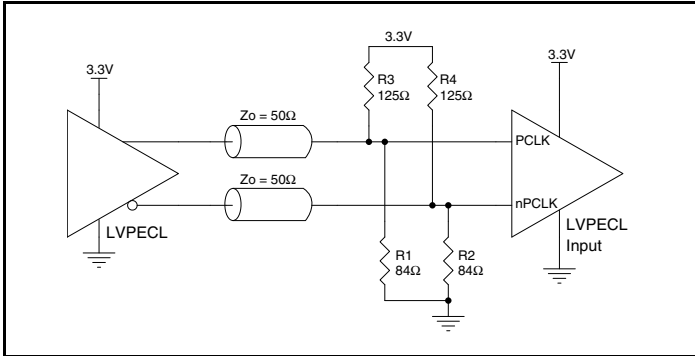


Figure 2A. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

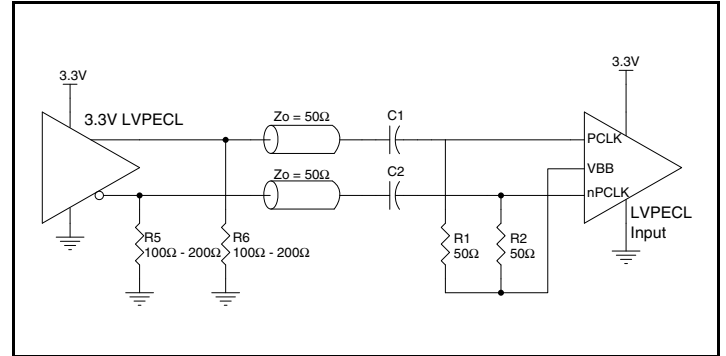


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

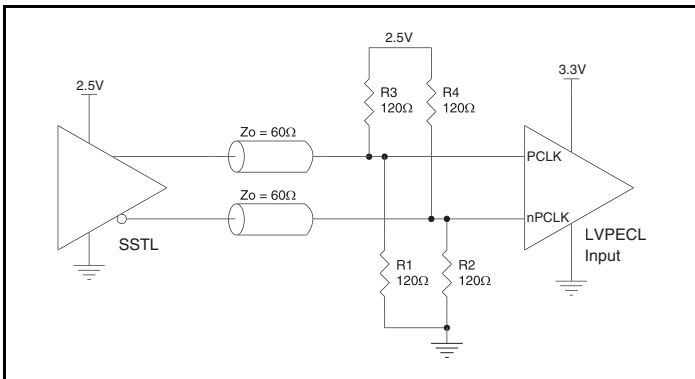


Figure 2C. PCLK/nPCLK Input Driven by an SSTL Driver

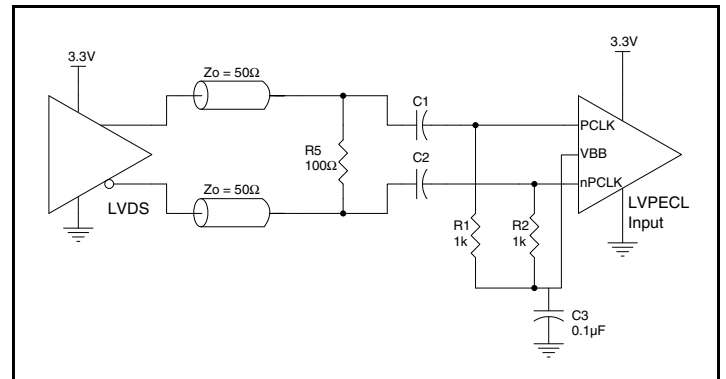


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

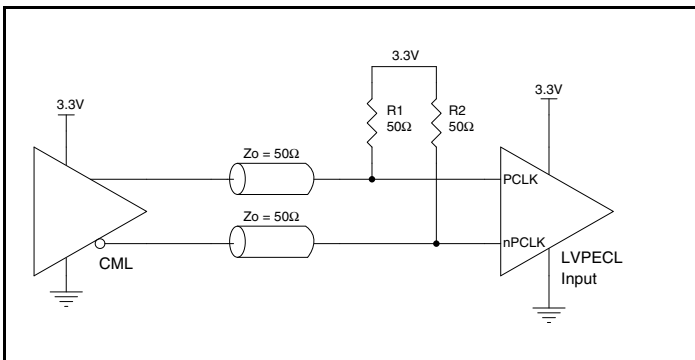


Figure 2E. PCLK/nPCLK Input Driven by a CML Driver

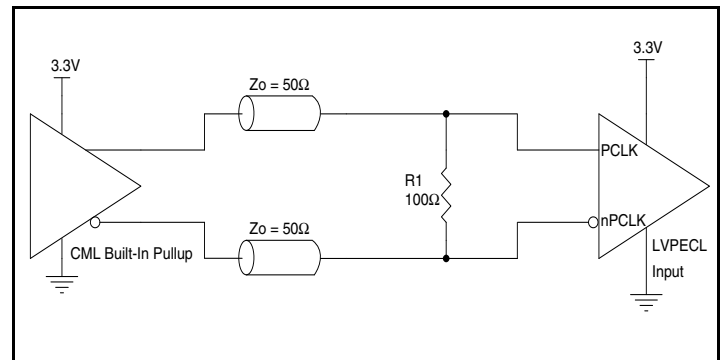


Figure 2F. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

Recommendations for Unused Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground. For applications

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

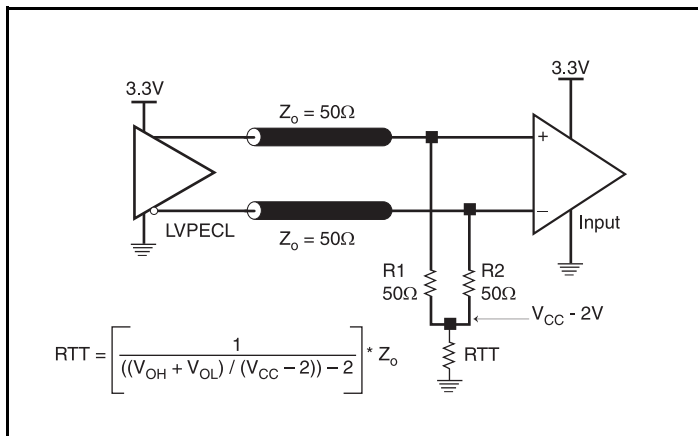


Figure 3A. 3.3V LVPECL Output Termination

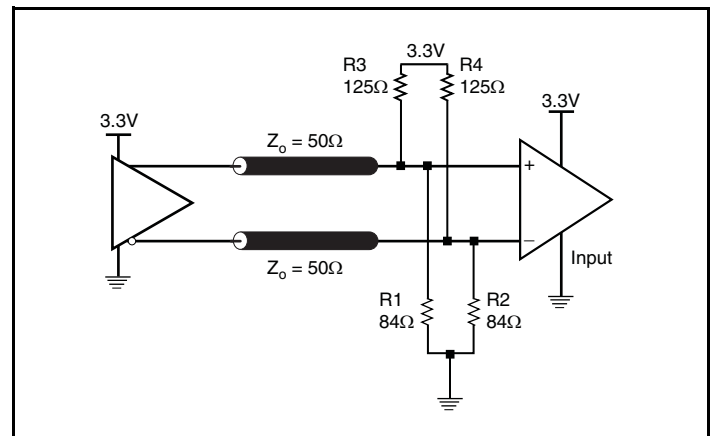


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to ground

level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.

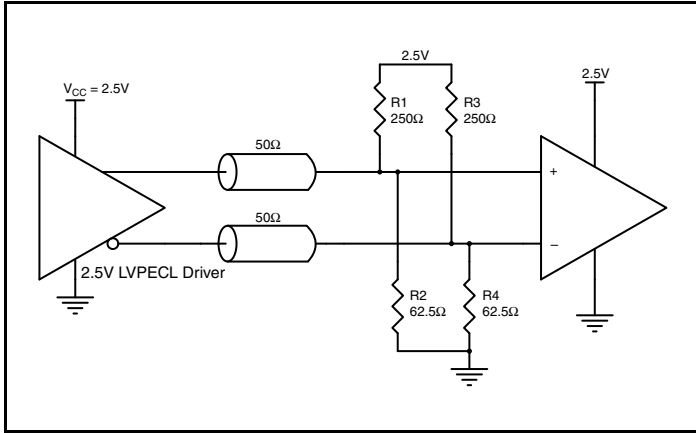


Figure 4A. 2.5V LVPECL Driver Termination Example

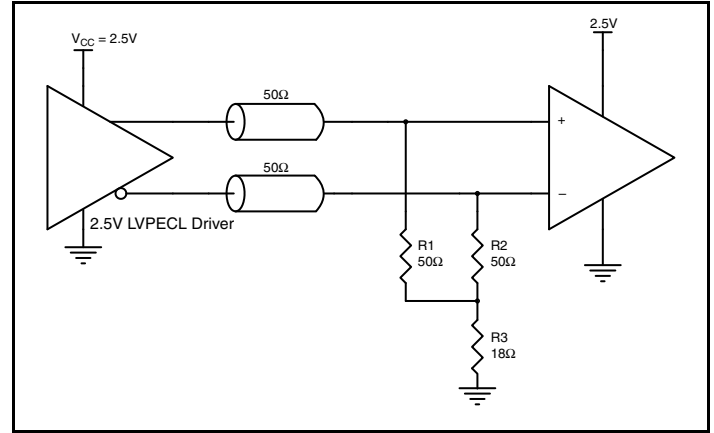


Figure 4B. 2.5V LVPECL Driver Termination Example

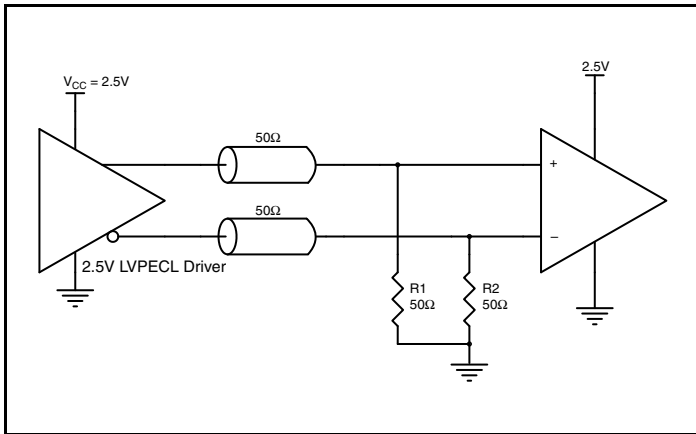


Figure 4C. 2.5V LVPECL Driver Termination Example

Schematic Example

This application note provides a general design guide using 853S111AI LVPECL buffer. Figure 5 shows a schematic example of the 853S111AI LVPECL clock buffer. In this example, the input is

driven by an LVPECL driver. CLK_SEL is set at logic high to select PCLK0/nPCLK0 input.

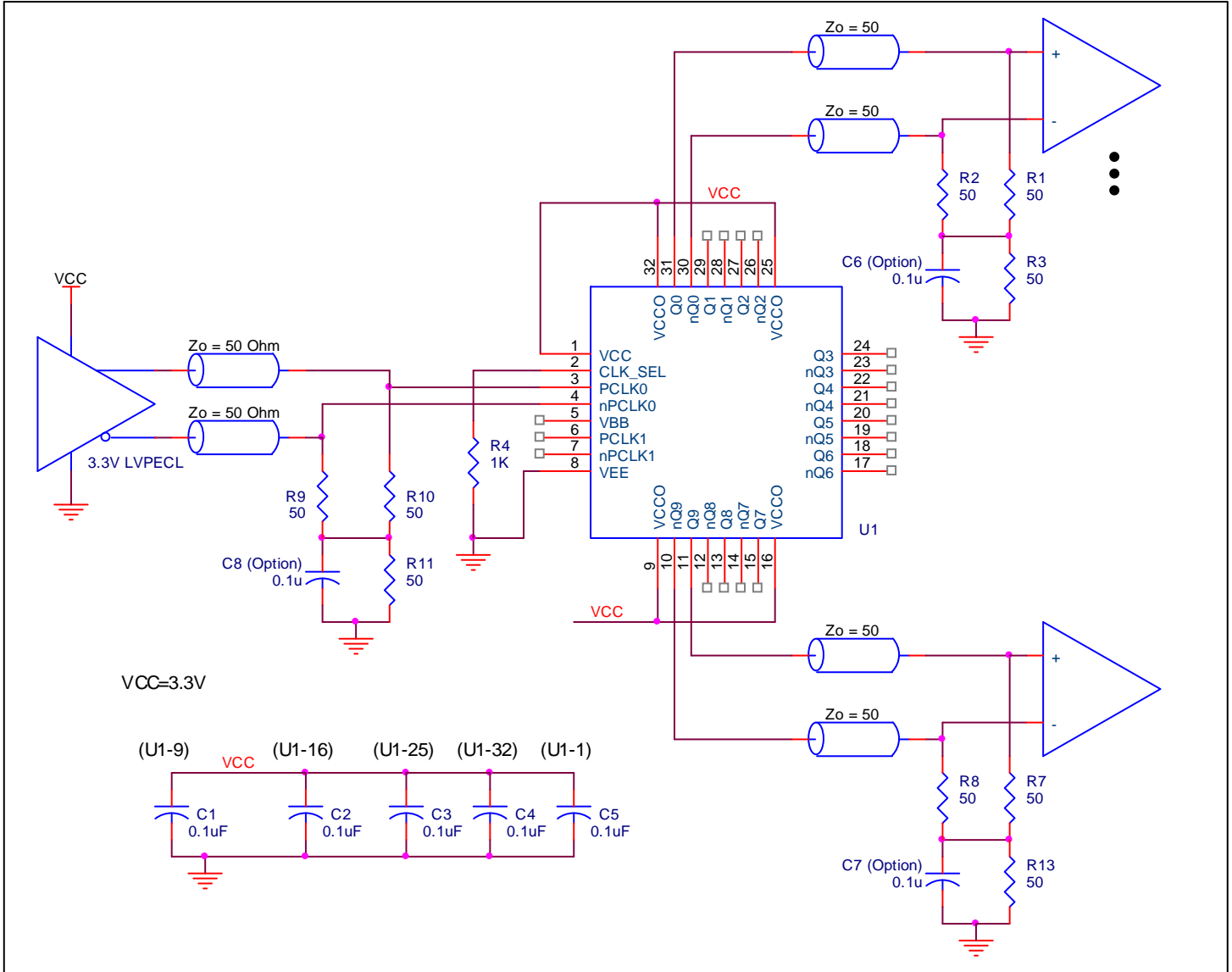


Figure 5. 853S111AI Example LVPECL Clock Output Buffer Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the 853S111AI. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 853S111AI is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 74mA = 256.41mW$
- Power (outputs)_{MAX} = **32.59mW/Loaded Output pair**
If all outputs are loaded, the total power is $10 * 32.59mW = 325.90mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $256.41mW + 325.90mW = 582.31mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 2.5 meter per second and a multi-layer board, the appropriate value is 67.7°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.582W * 67.7^\circ C/W = 124.4^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	80.9°C/W	71.4°C/W	67.7°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 6*.

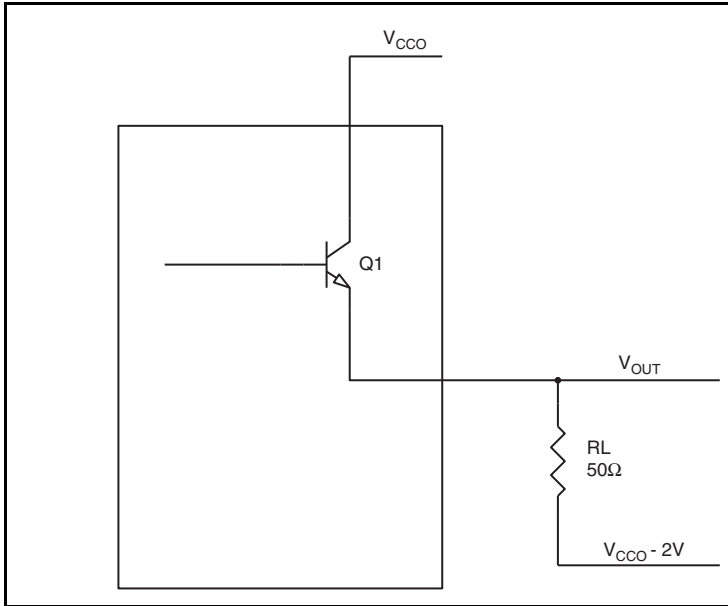


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, V_{OUT} = V_{OH_MAX} = **V_{CCO_MAX} - 0.85V**
(V_{CCO_MAX} - V_{OH_MAX}) = **0.85V**
- For logic low, V_{OUT} = V_{OL_MAX} = **V_{CCO_MAX} - 1.59V**
(V_{CCO_MAX} - V_{OL_MAX}) = **1.59V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.85V)/50\Omega] * 0.85V = \mathbf{19.55mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.59V)/50\Omega] * 1.59V = \mathbf{13.04mW}$$

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.59mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	80.9°C/W	71.4°C/W	67.7°C/W

Transistor Count

The transistor count for 853S111AI is: 365

This device is pin and functional compatible with and is the suggested replacement for the ICS853111A.

Package Outline and Package Dimensions

Package Outline - G Suffix for 32 Lead LQFP

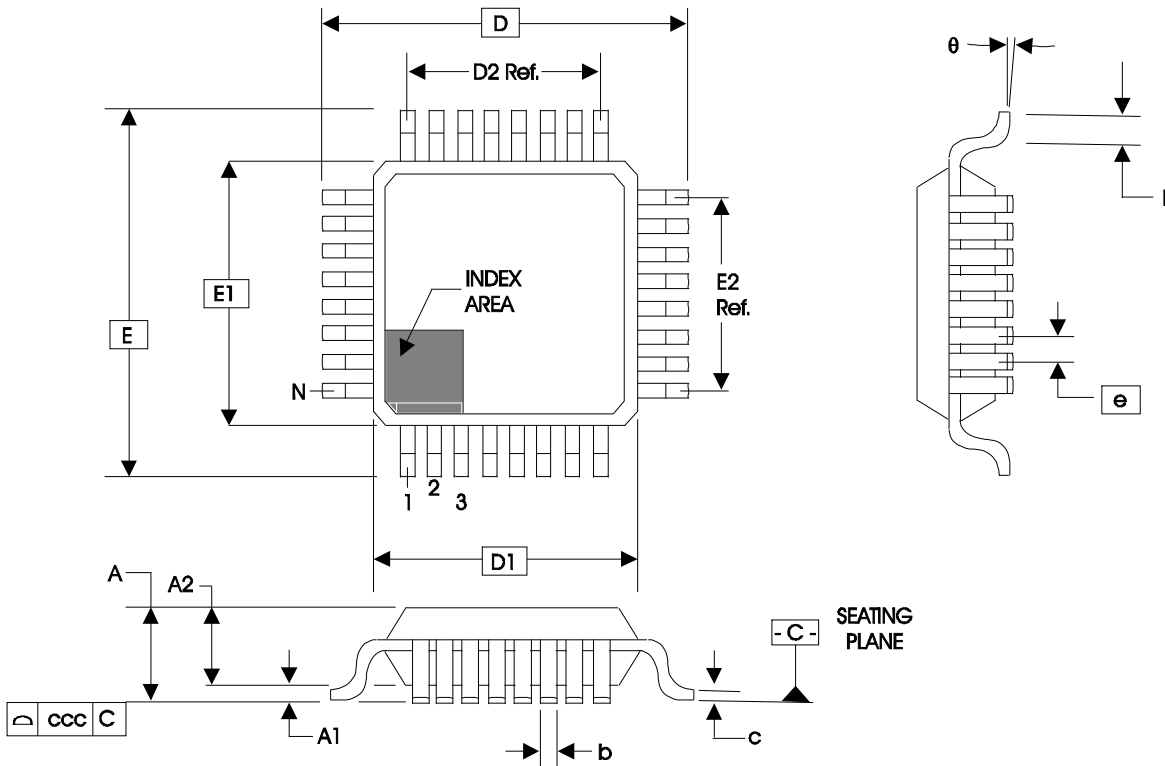


Table 8. Package Dimensions for 32 Lead LQFP

JEDEC Variation: BBA			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E	9.00 Basic		
D1 & E1	7.00 Basic		
D2 & E2	5.60 Ref.		
e	0.80 Basic		
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S111AYILF	ICS53S111AIL	32 Lead LQFP	Tray	-40°C to 85°C
853S111AYILFT	ICS53S111AIL	32 Lead LQFP	Tape & Reel, pin 1 orientation: EIA-481-C	-40°C to 85°C
853S111AYILF/W	ICS53S111AIL	32 Lead LQFP	Tape & Reel, pin 1 orientation EIA-481-D	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Table 10. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10 T9	18 18	Added Pin 1 Orientation in Tape and Reel Table. Ordering Information - Added W part number.	6/30/15

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View 853S111AYILF on WIN SOURCE](#)
-  [Renesas Electronics America](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management