



**THE DATASHEET OF
FNA25060**



Motion SPM[®] 2 Series, 600 V

FNA25060

General Description

The FNA25060 is a Motion SPM 2 module providing a fully-featured, high-performance inverter output stage for AC induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features: under-voltage lockouts, over-current shutdown, temperature sensing, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to high-voltage, high-current drive signals to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

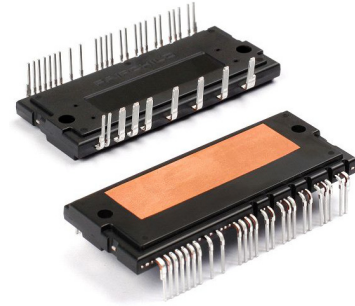
- UL Certified No. E209204 (UL1557)
- 600 V – 50 A 3-Phase IGBT Inverter, Including Control ICs for Gate Drive and Protections
- Low-Loss, Short-Circuit-Rated IGBTs
- Very Low Thermal Resistance Using Al₂O₃ DBC Substrate
- Built-In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply Supported
- Built-In NTC Thermistor for Temperature Monitoring and Management
- Adjustable Over-Current Protection via Integrated Sense-IGBTs
- Isolation Rating of 2500 Vrms / 1 min.
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

Applications

- Motion Control – Industrial Motor (AC 200 V Class)

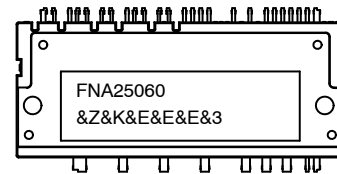
Related Resources

- [AN-9121 – Users Guide for 600V SPM 2 Series](#)
- [AN-9076 – Mounting Guide for New SPM 2 Package](#)
- [AN-9079 – Thermal Performance of Motion SPM 2 Series by Mounting Torque](#)



SPMCA-A34
CASE MODFQ

MARKING DIAGRAM



- FNA25060 = Specific Device Code
- &Z = Assembly Plant Code
- &K = Lot Code
- &E = Space Designator
- &3 = 3-Digit Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FNA25060

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Packing Type	Quantity
FNA25060	FNA25060	SPMCA-A34	Rail	6

Integrated Power Functions

- 600 V – 50 A IGBT inverter for three-phase DC / AC power conversion (refer to Figure 2)

Integrated Drive, Protection, and System Control Functions

- For inverter high-side IGBTs:
 - gate-drive circuit, high-voltage isolated high-speed level-shifting control circuit,
 - Under-Voltage Lock-Out Protection (UVLO),
 - Available bootstrap circuit example is given in Figures 4 and 14
- For inverter low-side IGBTs:
 - gate-drive circuit, Short-Circuit Protection (SCP)
 - control circuit,
 - Under-Voltage Lock-Out Protection (UVLO)
- Fault signaling:
 - corresponding to UV (low-side supply) and SC faults
- Input interface:
 - active-HIGH interface, works with 3.3 / 5 V logic,
 - Schmitt-trigger input

Pin Configuration

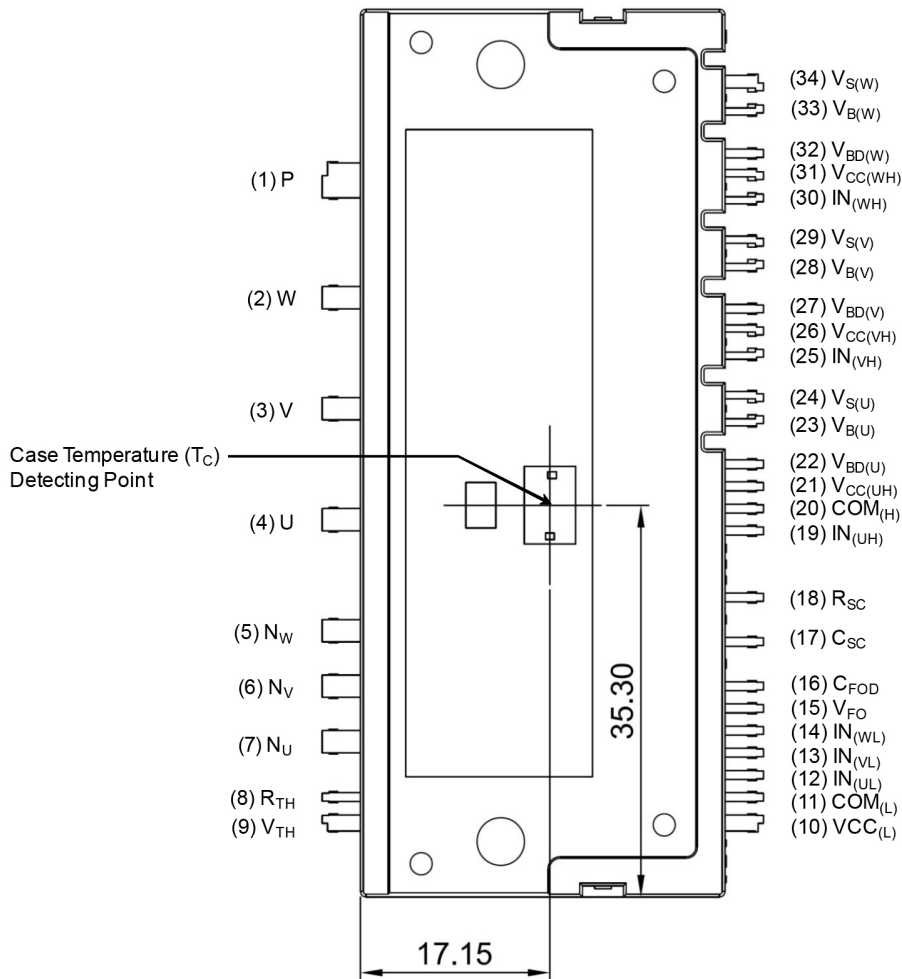


Figure 1. Top View

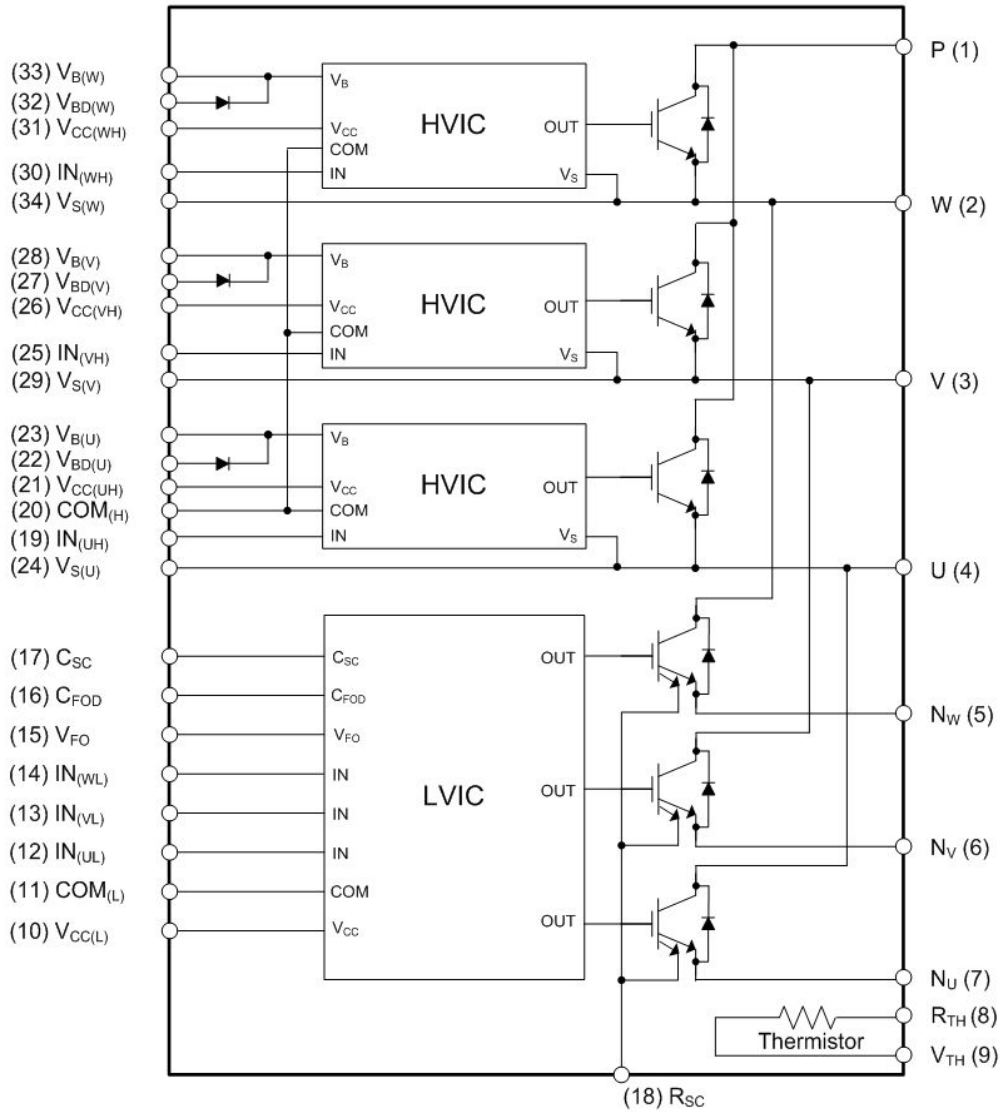
FNA25060

PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Description
1	P	Positive DC-Link Input
2	W	Output for W Phase
3	V	Output for V Phase
4	U	Output for U Phase
5	N _W	Negative DC-Link Input for W Phase
6	N _V	Negative DC-Link Input for V Phase
7	N _U	Negative DC-Link Input for U Phase
8	R _{TH}	Series Resistor for Thermistor (Temperature Detection)
9	V _{TH}	Thermistor Bias Voltage
10	V _{CC(L)}	Low-Side Bias Voltage for IC and IGBTs Driving
11	COM _(L)	Low-Side Common Supply Ground
12	IN _(UL)	Signal Input for Low-Side U Phase
13	IN _(VL)	Signal Input for Low-Side V Phase
14	IN _(WL)	Signal Input for Low-Side W Phase
15	V _{FO}	Fault Output
16	C _{FOD}	Capacitor for Fault Output Duration Selection
17	C _{SC}	Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input
18	R _{SC}	Resistor for Short-Circuit Current Detection
19	IN _(UH)	Signal Input for High-Side U Phase
20	COM _(H)	High-Side Common Supply Ground
21	V _{CC(UH)}	High-Side Bias Voltage for U Phase IC
22	V _{BD(U)}	Anode of Bootstrap Diode for U Phase High-Side Bootstrap Circuit
23	V _{B(U)}	High-Side Bias Voltage for U Phase IGBT Driving
24	V _{S(U)}	High-Side Bias Voltage Ground for U Phase IGBT Driving
25	IN _(VH)	Signal Input for High-Side V Phase
26	V _{CC(VH)}	High-Side Bias Voltage for V Phase IC
27	V _{BD(V)}	Anode of Bootstrap Diode for V Phase High-Side Bootstrap Circuit
28	V _{B(V)}	High-Side Bias Voltage for V Phase IGBT Driving
29	V _{S(V)}	High-Side Bias Voltage Ground for V Phase IGBT Driving
30	IN _(WH)	Signal Input for High-Side W Phase
31	V _{CC(WH)}	High-Side Bias Voltage for W Phase IC
32	V _{BD(W)}	Anode of Bootstrap Diode for W Phase High-Side Bootstrap Circuit
33	V _{B(W)}	High-Side Bias Voltage for W Phase IGBT Driving
34	V _{S(W)}	High-Side Bias Voltage Ground for W Phase IGBT Driving

FNA25060

Internal Equivalent Circuit and Input/Output Pins



NOTES:

1. Inverter high-side is composed of three normal-IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low-side is composed of three sense-IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

Figure 2. Internal Block Diagram

FNA25060

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P – N_U , N_V , N_W	450	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P – N_U , N_V , N_W	500	V
V_{CES}	Collector – Emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	$T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$ (Note 4)	50	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$, Under 1 ms Pulse Width (Note 4)	100	A
P_C	Collector Dissipation	$T_C = 25^\circ\text{C}$ per One Chip (Note 4)	192	W
T_J	Operating Junction Temperature		-40 ~ 150	$^\circ\text{C}$

CONTROL PART

V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ – COM	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM	-0.3 ~ $V_{CC}+0.3$	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} – COM	-0.3 ~ $V_{CC}+0.3$	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} – COM	-0.3 ~ $V_{CC}+0.3$	V

BOOTSTRAP DIODE PART

V_{RRM}	Maximum Repetitive Reverse Voltage		600	V
I_F	Forward Current	$T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$ (Note 4)	1.0	A
I_{FP}	Forward Current (Peak)	$T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$, Under 1 ms Pulse Width (Note 4)	2.0	A
T_J	Operating Junction Temperature		-40 ~ 150	$^\circ\text{C}$

TOTAL SYSTEM

$V_{PN(\text{PROT})}$	Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	$V_{CC} = V_{BS} = 13.5 \sim 16.5 \text{ V}$, $T_J = 150^\circ\text{C}$, $V_{CES} < 600 \text{ V}$, Non-Replicative, $< 2 \mu\text{s}$	400	V
T_C	Module Case Operation Temperature	See Figure 2	-40 ~ 125	$^\circ\text{C}$
T_{STG}	Storage Temperature		-40 ~ 125	$^\circ\text{C}$
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 Minute, Connection Pins to Heat Sink Plate	2500	V_{rms}

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 5)	Inverter IGBT Part (per 1 / 6 Module)	-	-	0.65	$^\circ\text{C}/\text{W}$
$R_{th(j-c)F}$		Inverter FWD Part (per 1 / 6 Module)	-	-	1.12	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. These values had been made an acquisition by the calculation considered to design factor.

5. For the measurement point of case temperature (T_C), please refer to Figure 1.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
INVERTER PART							
$V_{CE(SAT)}$	Collector - Emitter Saturation Voltage	$V_{CC} = V_{BS} = 15\text{ V}$ $V_{IN} = 5\text{ V}$		1.50	2.10	V	
V_F	FWDi Forward Voltage	$V_{IN} = 0\text{ V}$		1.80	2.40	V	
HS	t_{ON}	Switching Times $V_{PN} = 300\text{ V}$, $V_{CC} = 15\text{ V}$, $I_C = 50\text{ A}$ $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$, Inductive Load See Figure 4 (Note 6)	0.80	1.30	1.90	μs	
			$t_{C(ON)}$	-	0.30	0.70	μs
			t_{OFF}	-	1.20	1.80	μs
			$t_{C(OFF)}$	-	0.15	0.55	μs
			t_{rr}	-	0.25	-	μs
LS	t_{ON}	$V_{PN} = 300\text{ V}$, $V_{CC} = 15\text{ V}$, $I_C = 50\text{ A}$ $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$, Inductive Load See Figure 4 (Note 6)	0.50	1.00	1.60	μs	
			$t_{C(ON)}$	-	0.30	0.70	μs
			t_{OFF}	-	1.20	1.80	μs
			$t_{C(OFF)}$	-	0.25	0.65	μs
			t_{rr}	-	0.20	-	μs
I_{CES}	Collector - Emitter Leakage Current	$V_{CE} = V_{CES}$	-	-	5	mA	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of IGBT under the given gate-driving condition internally. For the detailed information, please see Figure 3.

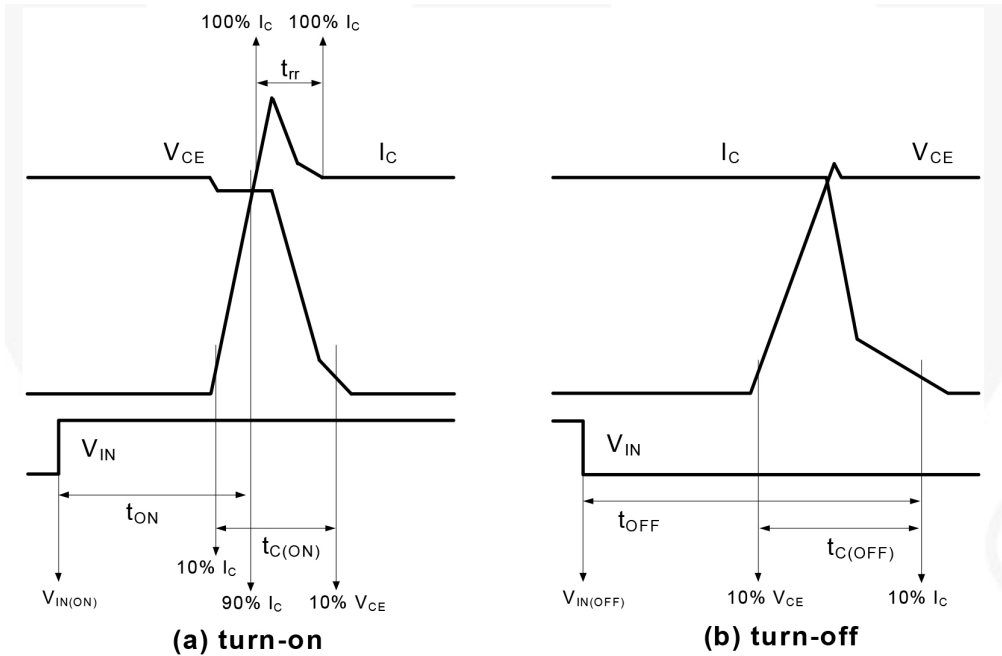


Figure 3. Switching Time Definition

FNA25060

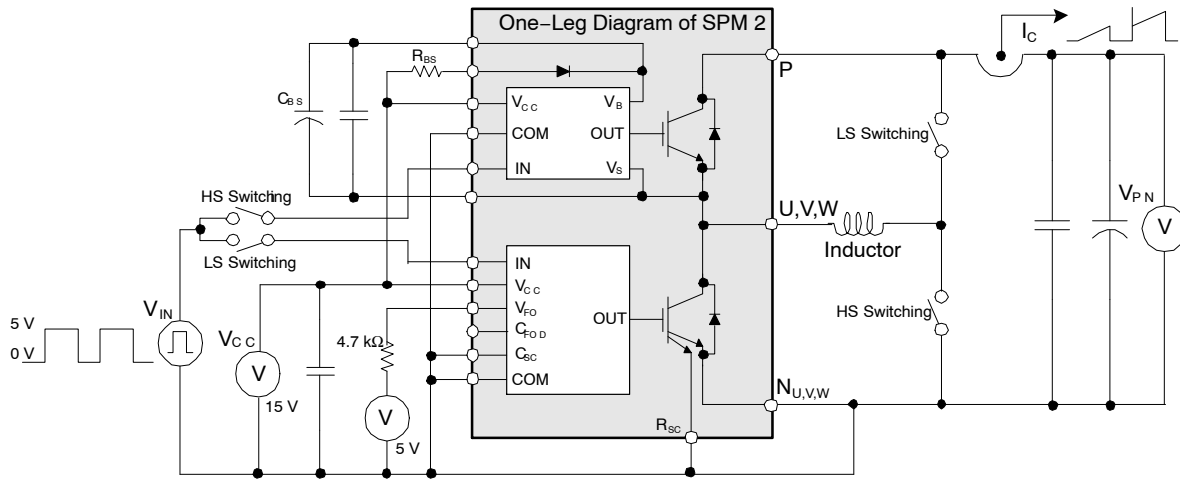


Figure 4. Example Circuit for Switching Test

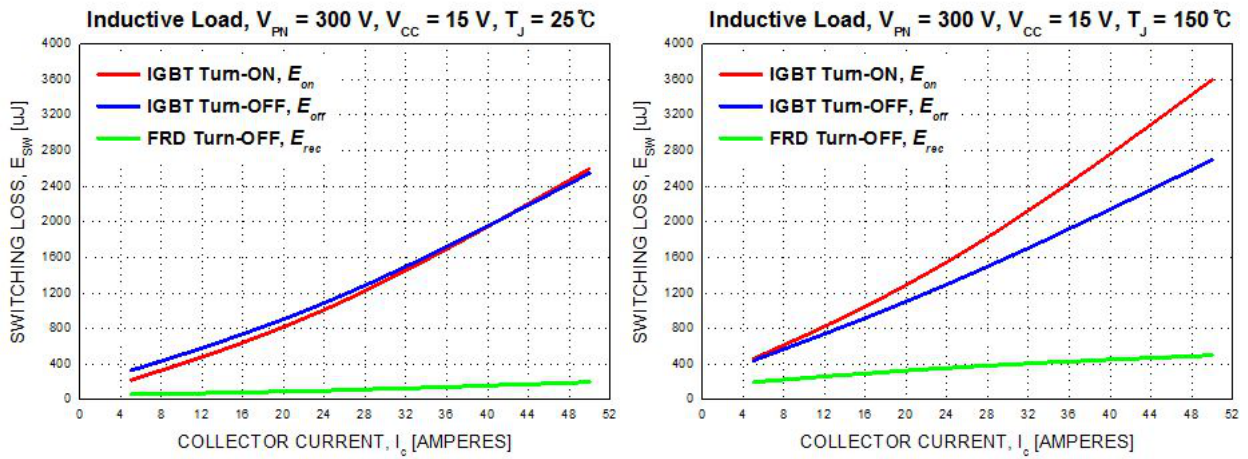


Figure 5. Switching Loss Characteristics (Typical)

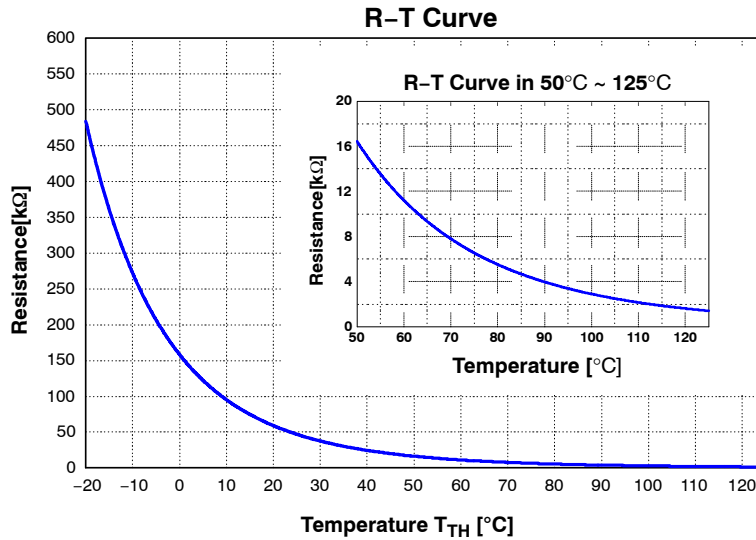


Figure 6. R-T Curve of Built-in Thermistor

FNA25060

BOOTSTRAP DIODE PART

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_F	Forward Voltage	$I_F = 1.0 \text{ A}$, $T_J = 25^\circ\text{C}$	–	2.2	–	V
trr	Reverse-Recovery Time	$I_F = 1.0 \text{ A}$, $dI_F / dt = 50 \text{ A} / \mu\text{s}$, $T_J = 25^\circ\text{C}$	–	80	–	ns

CONTROL PART

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
I_{QCCH}	Quiescent V_{CC} Supply Current	$V_{CC(UH, VH, WH)} = 15 \text{ V}$, $I_{N(UH, VH, WH)} = 0 \text{ V}$	$V_{CC(UH)} - COM_{(H)}$, $V_{CC(VH)} - COM_{(H)}$, $V_{CC(WH)} - COM_{(H)}$	–	–	0.15	mA
I_{QCCL}		$V_{CC(L)} = 15 \text{ V}$, $I_{N(UL, VL, WL)} = 0 \text{ V}$	$V_{CC(L)} - COM_{(L)}$	–	–	5.00	mA
I_{PCCH}	Operating V_{CC} Supply Current	$V_{CC(UH, VH, WH)} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for High-Side	$V_{CC(UH)} - COM_{(H)}$, $V_{CC(VH)} - COM_{(H)}$, $V_{CC(WH)} - COM_{(H)}$	–	–	0.30	mA
I_{PCCL}		$V_{CC(L)} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for Low-Side	$V_{CC(L)} - COM_{(L)}$	–	–	9.00	mA
I_{QBS}	Quiescent V_{BS} Supply Current	$V_{BS} = 15 \text{ V}$, $I_{N(UH, VH, WH)} = 0 \text{ V}$	$V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	–	–	0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	$V_{CC} = V_{BS} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for High-Side	$V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	–	–	6.50	mA
V_{FOH}	Fault Output Voltage	$V_{CC} = 15 \text{ V}$, $V_{SC} = 0 \text{ V}$, V_{FO} Circuit: 4.7 k Ω to 5 V Pull-up		4.5	–	–	V
V_{FOL}		$V_{CC} = 15 \text{ V}$, $V_{SC} = 1 \text{ V}$, V_{FO} Circuit: 4.7 k Ω to 5 V Pull-up		–	–	0.5	V
I_{SEN}	Sensing Current of Each Sense IGBT	$V_{CC} = 15 \text{ V}$, $V_{IN} = 5 \text{ V}$, $R_{SC} = 0 \Omega$, No Connection of Shunt Resistor at $N_{U, V, W}$ Terminal	$I_C = 50 \text{ A}$	–	20	–	mA
$V_{SC(ref)}$	Short Circuit Trip Level	$V_{CC} = 15 \text{ V}$ (Note 7)	$CSC - COM_{(L)}$	0.43	0.50	0.57	V
I_{SC}	Short Circuit Current Level for Trip	$R_{SC} = 18 \Omega (\pm 1\%)$, No Connection of Shunt Resistor at $N_{U, V, W}$ Terminal (Note 7)		–	100	–	A
UV_{CCD}	Supply Circuit Under-Voltage Protection	Detection Level		10.3	–	12.8	V
UV_{CCR}		Reset Level		10.8	–	13.3	V
UV_{BSD}		Detection Level		9.5	–	12.0	V
UV_{BSR}		Reset Level		10.0	–	12.5	V
t_{FOD}	Fault-Out Pulse Width	$C_{FOD} = \text{Open}$	(Note 8)	50	–	–	μs
		$C_{FOD} = 2.2 \text{ nF}$		1.7	–	–	ms
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $I_{N(UH, VH, WH)} - COM_{(H)}$, $I_{N(UL, VL, WL)} - COM_{(L)}$		–	–	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8	–	–	V
R_{TH}	Resistance of Thermistor	at $T_{TH} = 25^\circ\text{C}$	See Figure 6	–	47	–	k Ω
		at $T_{TH} = 100^\circ\text{C}$	(Note 9)	–	2.9	–	k Ω

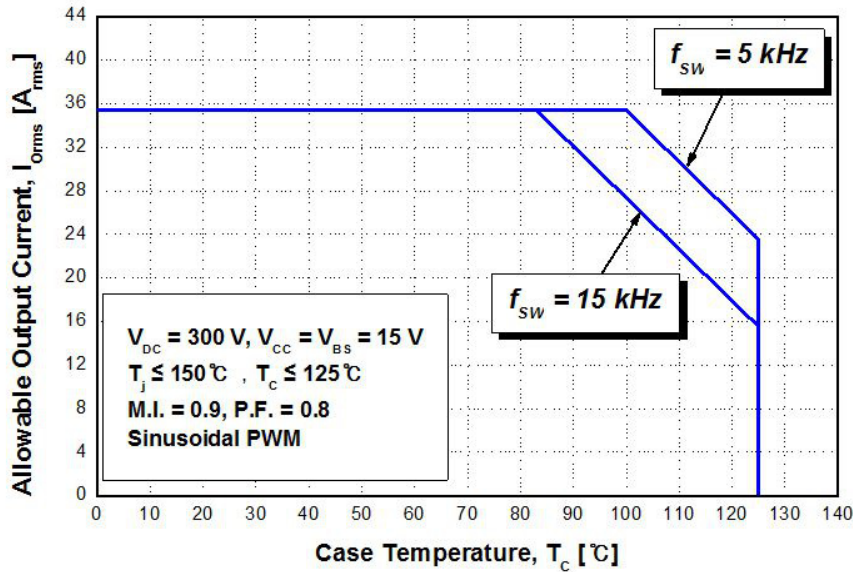
7. Short-circuit current protection functions only at the low-sides because the sense current is divided from main current at low-side IGBTs. Inserting the shunt resistor for monitoring the phase current at N_U , N_V , N_W terminal, the trip level of the short-circuit current is changed.
8. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation:
 $t_{FOD} = 0.8 \times 10^6 \times C_{FOD} [\text{s}]$.
9. T_{TH} is the temperature of thermistor itself. To know case temperature (T_C), conduct experiments considering the application.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V _{PN}	Supply Voltage	Applied between P – N _U , N _V , N _W	–	300	400	V
V _{CC}	Control Supply Voltage	Applied between V _{CC(UH, VH, WH)} – COM _(H) , V _{CC(L)} – COM _(L)	14.5	15.0	16.5	V
V _{BS}	High-Side Bias Voltage	Applied between V _{B(U)} – V _{S(U)} , V _{B(V)} – V _{S(V)} , V _{B(W)} – V _{S(W)}	13.5	15.0	18.5	V
dV _{CC} / dt, dV _{BS} / dt	Control Supply Variation		–1	–	1	V / μs
t _{dead}	Blanking Time for Preventing Arm – Short	For Each Input Signal	2.0	–	–	μs
f _{PWM}	PWM Input Signal	–40°C ≤ T _C ≤ 125°C, –40°C ≤ T _J ≤ 150°C	–	–	20	kHz
V _{SEN}	Voltage for Current Sensing	Applied between N _U , N _V , N _W – COM _(H, L) (Including Surge Voltage)	–5		5	V
PW _{IN(ON)}	Minimum Input Pulse Width	V _{CC} = V _{BS} = 15 V, I _C ≤ 100 A, Wiring Inductance between N _U , V, W and DC Link N < 10nH (Note 10)	2.5	–	–	μs
PW _{IN(OFF)}			2.5	–	–	
T _J	Junction Temperature		–40	–	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

10. This product might not make right output response if input pulse width is less than the recommended value.



11. This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.

Figure 7. Allowable Maximum Output Current

FNA25060

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions	Min.	Typ.	Max.	Unit	
Device Flatness	See Figure 9	0	-	+200	μm	
Mounting Torque	Mounting Screw: M4 See Figure 10	Recommended 1.0 N/m	0.9	1.0	1.5	N/m
		Recommended 10.1 kg/cm	9.1	10.1	15.1	kg/cm
Terminal Pulling Strength	Load 19.6 N	10	-	-	s	
Terminal Bending Strength	Load 9.8 N, 90 degrees Bend	2	-	-	times	
Weight		-	50	-	g	

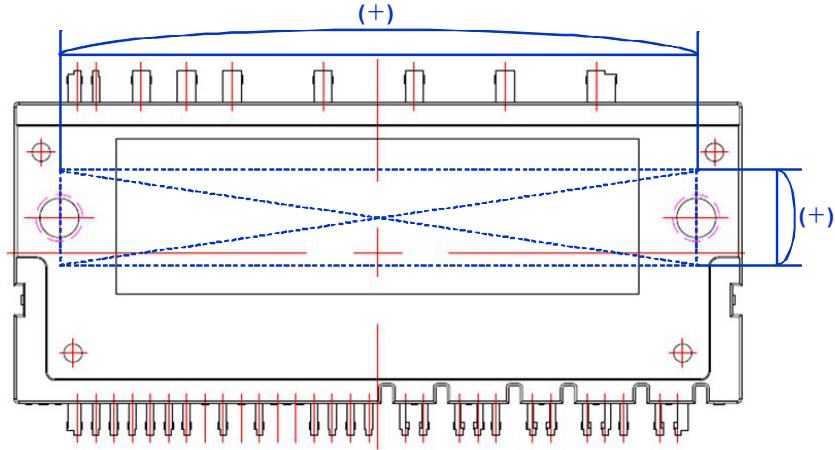


Figure 8. Flatness Measurement Position

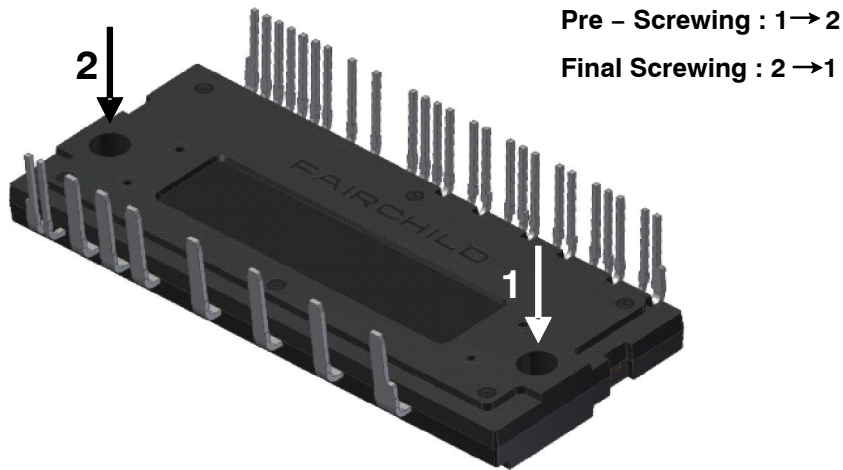
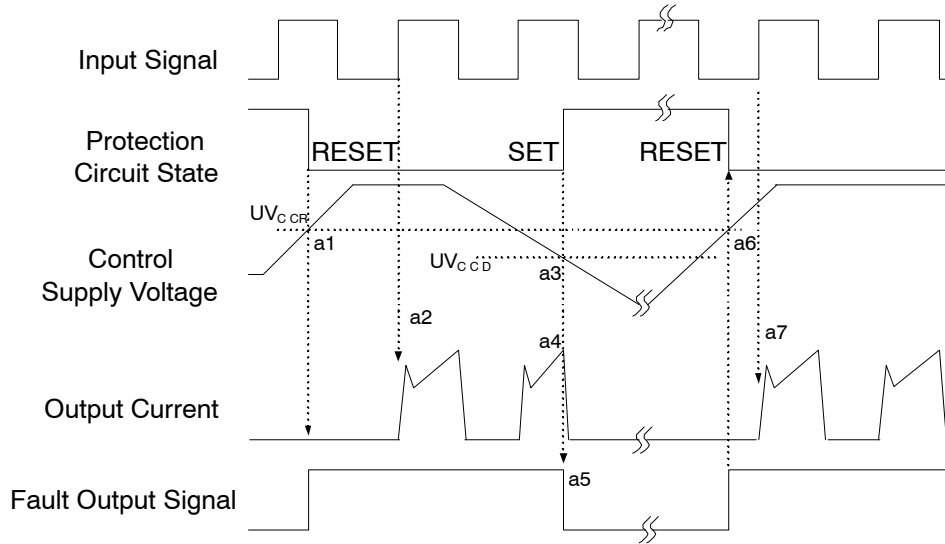


Figure 9. Mounting Screws Torque Order

NOTES:

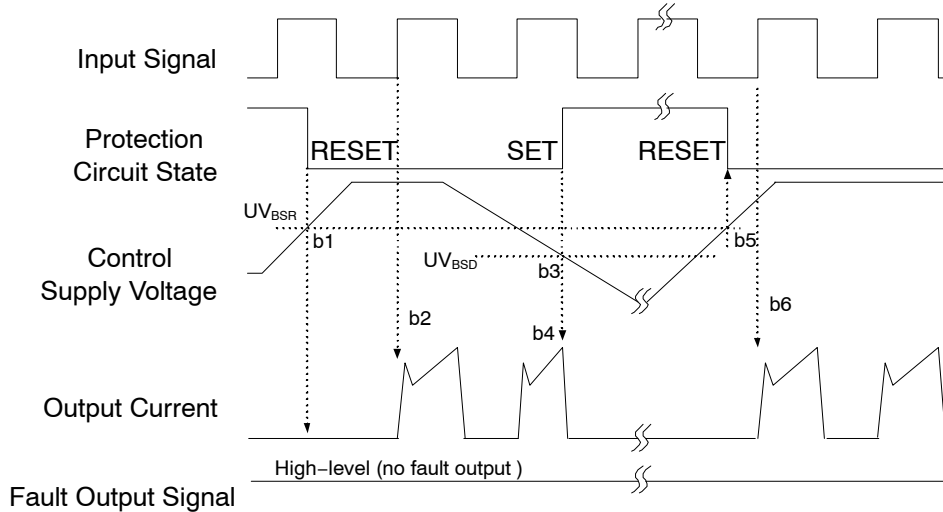
- 12. Do not over torque when mounting screws. Too much mounting torque may cause DBC cracks, as well as bolts and Al heat-sink destruction.
- 13. Avoid one-sided tightening stress. Figure 9 shows the recommended torque order for the mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre-screwing torque is set to 20 ~ 30% of maximum torque rating.

Time Charts of SPMs Protective Function



- a1 : Control supply voltage rises: after the voltage rises UV_{CCR} , the circuits start to operate when the next input is applied.
- a2 : Normal operation: IGBT ON and carrying current.
- a3 : Under-voltage detection (UV_{CCD}).
- a4 : IGBT OFF in spite of control input condition.
- a5 : Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD} .
- a6 : Under-voltage reset (UV_{CCR}).
- a7 : Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

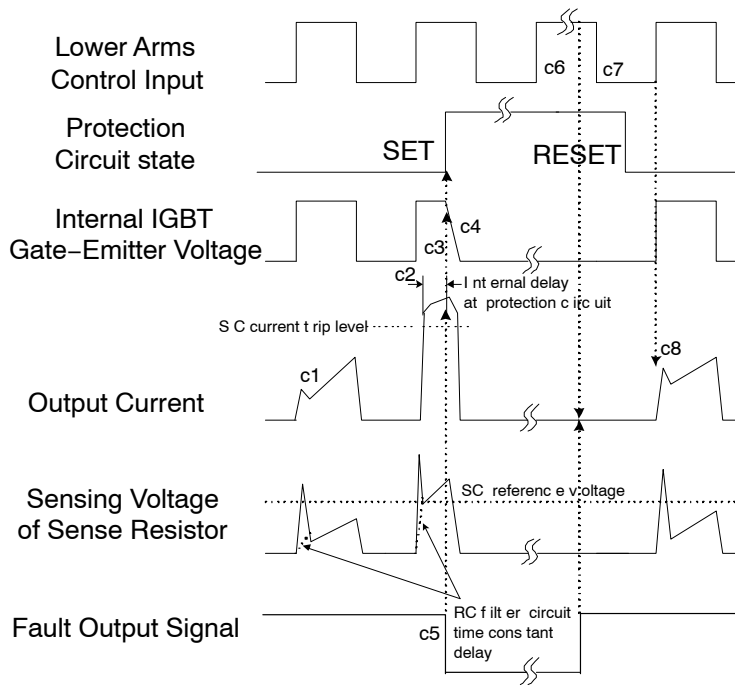
Figure 10. Under-Voltage Protection (Low-Side)



- b1 : Control supply voltage rises: after the voltage reaches UV_{BSR} , the circuits start to operate when the next input is applied.
- b2 : Normal operation: IGBT ON and carrying current.
- b3 : Under-voltage detection (UV_{BSD}).
- b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5 : Under-voltage reset (UV_{BSR}).
- b6 : Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

Figure 11. Under-Voltage Protection (High-Side)

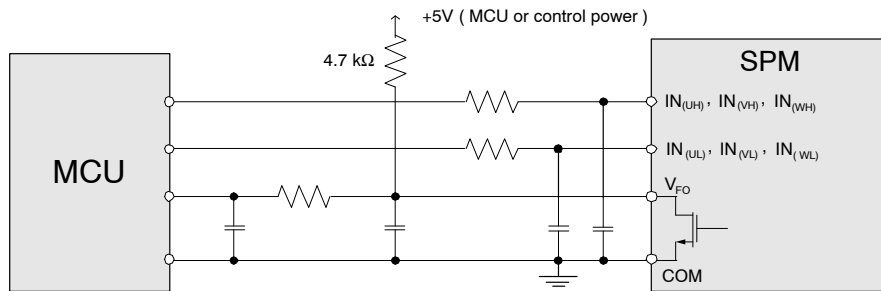
FNA25060



- c1 : Normal operation: IGBT ON and carrying current.
- c2 : Short-circuit current detection (SC trigger).
- c3 : All low-side IGBTs gate are hard interrupted.
- c4 : All low-side IGBTs turn OFF.
- c5 : Fault output operation starts with a fixed pulse width according to the condition of the external capacitor CFOD.
- c6 : Input HIGH: IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
- c7 : Fault output operation finishes, but IGBT doesn't turn on until triggering the next signal from LOW to HIGH.
- c8 : Normal operation: IGBT ON and carrying current.

Figure 12. Short-Circuit Current Protection (Low-Side Operation only)

Input/Output Interface Circuit



14. RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 2 product integrates 5 kW (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Figure 13. Recommended MCU I/O Interface Circuit

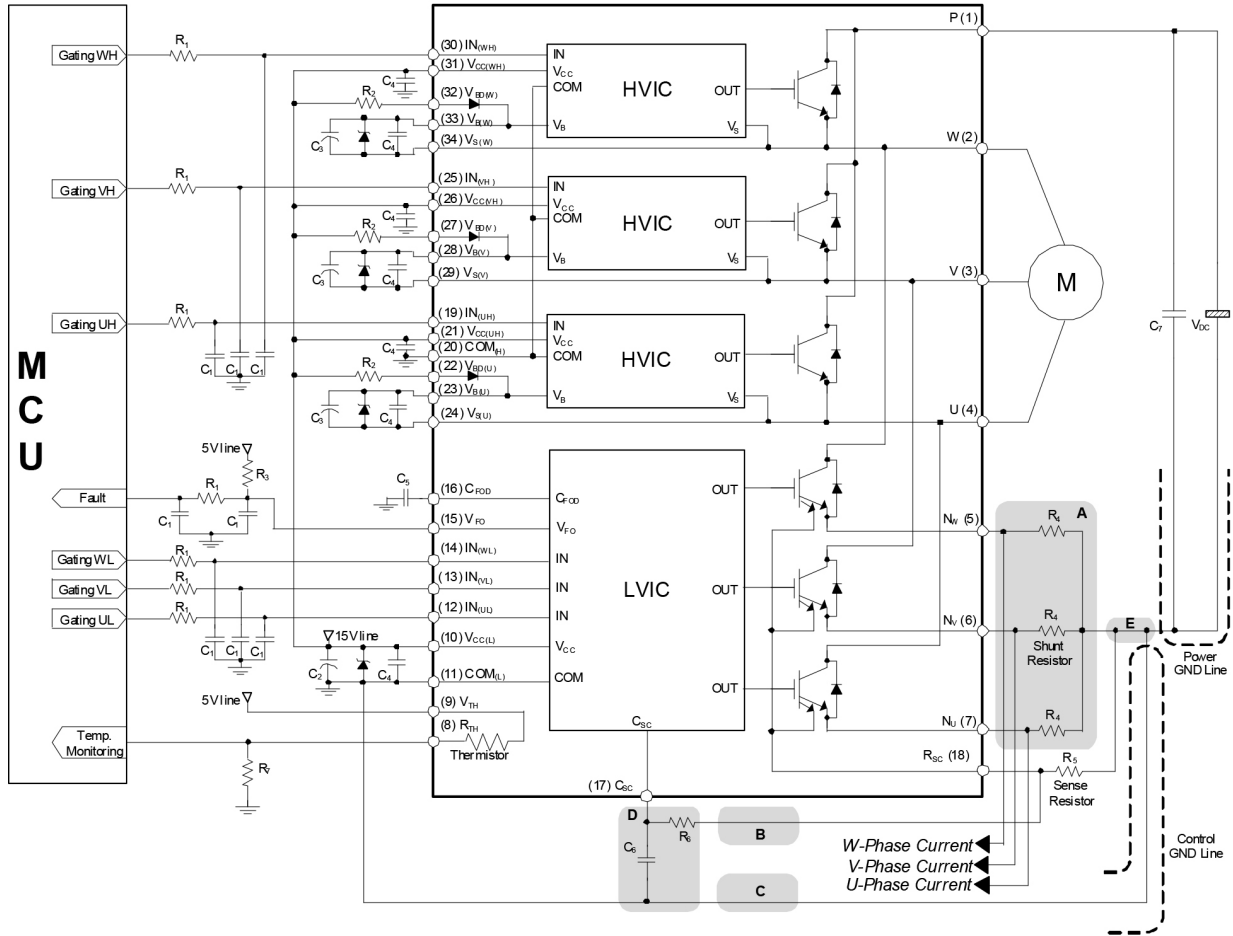


Figure 14. Typical Application Circuit

15. To avoid malfunction, the wiring of each input should be as short as possible (less than 2 – 3 cm).
16. V_{FO} output is an open–drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 2 mA. Please refer to Figure 13.
17. Fault out pulse width can be adjust by capacitor C_5 connected to the C_{FOD} terminal.
18. Input signal is active–HIGH type. There is a 5 k Ω resistor inside the IC to pull–down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. R_1C_1 time constant should be selected in the range 50 ~ 150 ns (recommended $R_1 = 100 \Omega$, $C_1 = 1$ nF).
19. Each wiring pattern inductance of point A should be minimized (recommend less than 10 nH). Use the shunt resistor R_4 of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R_4 as close as possible.
20. To insert the shunt resistor to measure each phase current at N_U , N_V , N_W terminal, it makes to change the trip level I_{SC} about the short–circuit current.
21. To prevent errors of the protection function, the wiring of points B, C, and D should be as short as possible. The wiring of B between C_{SC} filter and R_{SC} terminal should be divided at the point that is close to the terminal of sense resistor R_5 .
22. For stable protection function, use the sense resistor R_5 with resistance variation within 1% and low inductance value.
23. In the short–circuit protection circuit, select the R_6C_6 time constant in the range 1.0 ~ 1.5 μ s. R_6 should be selected with a minimum of 10 times larger resistance than sense resistor R_5 . Do enough evaluation on the real system because short–circuit protection time may vary wiring pattern layout and value of the R_6C_6 time constant.
24. Each capacitor should be mounted as close to the pins of the Motion SPM 2 product as possible.
25. To prevent surge destruction, the wiring between the smoothing capacitor C_7 and the P & GND pins should be as short as possible. The use of a high–frequency non– inductive capacitor of around 0.1 ~ 0.22 μ F between the P & GND pins is recommended.
26. Relays are used in most systems of electrical equipments in industrial application. In these cases, there should be sufficient distance between the MCU and the relays.
27. The Zener diode or transient voltage suppressor should be adapted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended Zener diode is 22 V / 1 W, which has the lower Zener impedance characteristic than about 15 Ω). C_2 of around seven times larger than bootstrap capacitor C_3 is recommended.
28. Please choose the electrolytic capacitor with good temperature characteristic in C_3 . Choose 0.1 ~ 0.2 μ F R–category ceramic capacitors with good temperature and frequency characteristics in C_4 .

SPM is a registered trademark of Semiconductor Components Industries, LLC dba “onsemi” or its affiliates and/or subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE

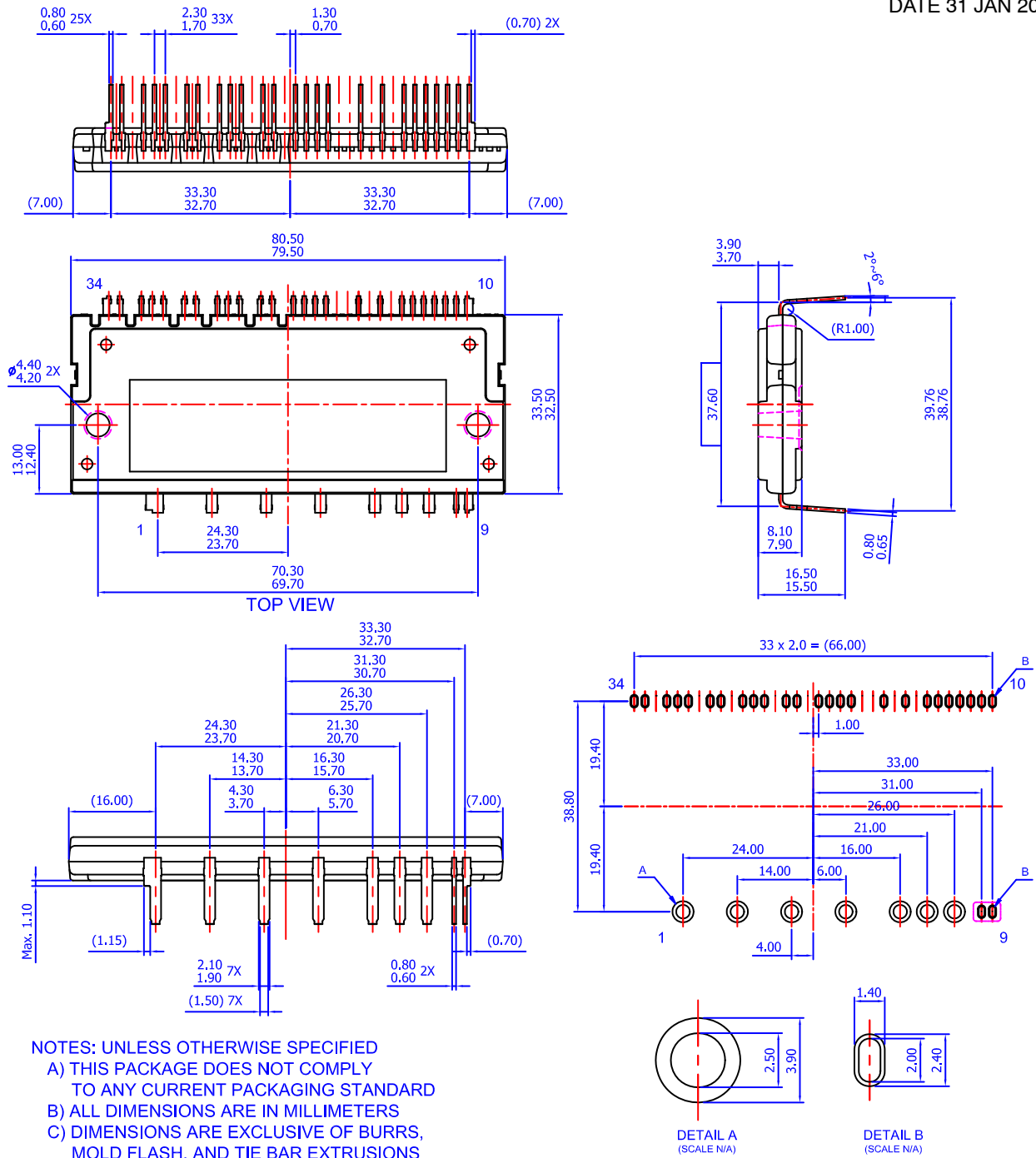
PACKAGE DIMENSIONS

ON Semiconductor®



SPMCA-A34 / 34LD, PDD STD, DBC DIP TYPE CASE MODFQ ISSUE O

DATE 31 JAN 2017



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
 - B) ALL DIMENSIONS ARE IN MILLIMETERS
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D) PACKAGE SURFACE VOID SHALL NOT EXCEED 2.3 x 2.3 x 1.0mm
 - E) () IS REFERENCE

LAND PATTERN RECOMMENDATIONS

DOCUMENT NUMBER:	98AON13565G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SPMCA-A34 / 34LD, PDD STD, DBC DIP TYPE	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View FNA25060](#) on WIN SOURCE

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management