



**THE DATASHEET OF  
FH12A-33S-0.5SH(55)**



# LM6171 High-Speed, Low-Power, Low-Distortion Voltage Feedback Amplifier

## 1 Features

- Typical unless otherwise noted
- Easy-to-use voltage feedback topology
- Very high slew rate: 3600 V/ $\mu$ s
- Wide unity-gain-bandwidth product: 76 MHz
- $-3$ -dB frequency at  $A_V = +2$ : 75 MHz
- Low supply current: 2.5 mA
- High CMRR: 110 dB
- High open-loop gain: 90 dB
- Specified for  $\pm 15$ -V and  $\pm 5$ -V operation

## 2 Applications

- Multimedia broadcast systems
- Line driver, switch
- Video amplifier
- NTSC, PAL<sup>®</sup> and SECAM systems
- ADC/DAC buffer
- HDTV amplifier
- Pulse amplifier and peak detector
- Instrumentation amplifier
- Active filter

## 3 Description

The LM6171 is a high-speed, unity-gain-stable voltage-feedback amplifier. The LM6171 offers a high slew rate of 3600 V/ $\mu$ s and a unity-gain bandwidth of 100 MHz while consuming only 2.5 mA of supply current. The LM6171 has very impressive ac and dc performance that is a great benefit for high-speed signal processing and video applications.

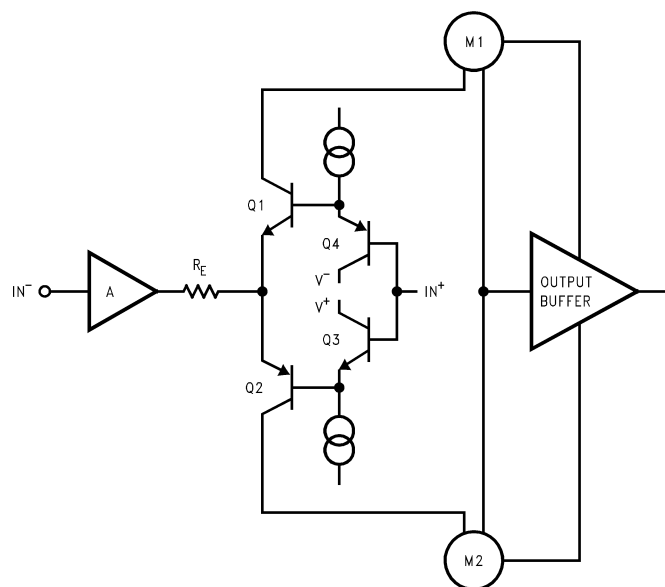
The  $\pm 15$ -V power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio (SNR). The LM6171 has a high output current drive, low spurious-free dynamic range (SFDR) and total harmonic distortion (THD), and is an excellent choice for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) systems. The LM6171 is specified for  $\pm 5$ -V operation for portable applications.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
LM6171	D (SOIC, 8)	4.9 mm $\times$ 6 mm
	P (PDIP, 8)	9.81 mm $\times$ 9.43 mm

(1) For more information, see [Section 10](#).

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



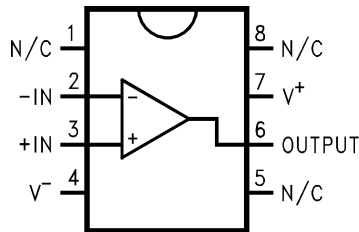
**Simplified Schematic**



## Table of Contents

<b>1 Features</b> .....	1	6.3 Feature Description.....	26
<b>2 Applications</b> .....	1	6.4 Device Functional Modes.....	26
<b>3 Description</b> .....	1	<b>7 Application and Implementation</b> .....	27
<b>4 Pin Configuration and Functions</b> .....	2	7.1 Application Information.....	27
<b>5 Specifications</b> .....	3	7.2 Typical Applications.....	30
5.1 Absolute Maximum Ratings.....	3	7.3 Power Supply Recommendations.....	31
5.2 ESD Ratings.....	3	7.4 Layout.....	31
5.3 Recommended Operating Conditions.....	3	<b>8 Device and Documentation Support</b> .....	32
5.4 Thermal Information.....	3	8.1 Receiving Notification of Documentation Updates....	32
5.5 Electrical Characteristics: $\pm 15$ V.....	4	8.2 Support Resources.....	32
5.6 Electrical Characteristics: $\pm 5$ V.....	6	8.3 Trademarks.....	32
5.7 Typical Characteristics: LM6171A Only.....	8	8.4 Electrostatic Discharge Caution.....	32
5.8 Typical Characteristics.....	17	8.5 Glossary.....	32
<b>6 Detailed Description</b> .....	26	<b>9 Revision History</b> .....	33
6.1 Overview.....	26	<b>10 Mechanical, Packaging, and Orderable Information</b> .....	33
6.2 Functional Block Diagram.....	26		

## 4 Pin Configuration and Functions



**Figure 4-1. D Package, 8-Pin SOIC  
P Package, 8-Pin PDIP  
(Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
-IN	2	I	Negative input pin
+IN	3	I	Positive input pin
N/C	1, 5, 8	—	This pin is not internally connected; leave floating or connect to any other pin on the device.
OUTPUT	6	O	Output pin.
V-	4	I/O	Negative supply voltage pin.
V+	7	I/O	Positive supply voltage pin.

(1) Signal types: I = input, O = output, I/O = input or output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage (V <sup>+</sup> – V <sup>-</sup> )		36	V
V <sub>I</sub>	Differential input voltage		±10	V
V <sub>CM</sub>	Common-mode voltage	(V <sup>-</sup> ) – 0.3	(V <sup>+</sup> ) + 0.3	V
I <sub>IN</sub>	Input current		±10	mA
I <sub>SC</sub>	Output current short to ground <sup>(3)</sup>		Continuous	A
T <sub>stg</sub>	Storage temperature	–65	150	°C
T <sub>J</sub>	Junction temperature <sup>(4)</sup>		150	°C
T <sub>SOLDER</sub>	Infrared or convection reflow (20 seconds)		235	°C
	Wave soldering lead temp (10 seconds)		260	

- (1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (2) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (3) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (4) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> – T<sub>A</sub>)/R<sub>θJA</sub>. All numbers apply for packages soldered directly into a PC board.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP155 states that 2500-V HBM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V <sub>S</sub>	Supply voltage	5.5		34	V
T <sub>A</sub>	Ambient temperature	–40		85	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM6171			UNIT
		D (SOIC) A Version	D (SOIC) B Version	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	122.5	172	108	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	64.7	62.4	52.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	65.9	55.7	51.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	17.6	16.5	6.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	65.1	55.1	51.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics: $\pm 15$ V

at  $T_J = 25^\circ\text{C}$ ,  $V^+ = 15$  V,  $V^- = -15$  V,  $V_{CM} = 0$  V, and  $R_L = 1$  k $\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(1)</sup>	MAX <sup>(2)</sup>	UNIT
$V_{OS}$	Input offset voltage	LM6171A	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.5	3	mV	
				5			
		LM6171B	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.5	6		
				8			
$TCV_{OS}$	Input offset voltage average drift			6		$\mu\text{V}/^\circ\text{C}$	
$I_B$	Input bias current			1	3	$\mu\text{A}$	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			4		
$I_{OS}$	Input offset current			0.03	2	$\mu\text{A}$	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			3		
$R_{IN}$	Input resistance	Common-mode		40		M $\Omega$	
		Differential-mode		4.9			
$R_O$	Open-loop output resistance			14		$\Omega$	
CMRR	Common-mode rejection ratio	LM6171A, $V_{CM} = \pm 10$ V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	80	110	dB	
				75			
		LM6171B, $V_{CM} = \pm 10$ V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	75	110		
				70			
PSRR	Power supply rejection ratio	LM6171A, $V_S = \pm 5$ V to $\pm 15$ V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	85	95	dB	
				80			
		LM6171B, $V_S = \pm 5$ V to $\pm 15$ V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	80	95		
				75			
$V_{CM}$	Input common-mode voltage	CMRR > 60 dB		$\pm 13.5$		V	
$A_V$	Large signal voltage gain <sup>(3)</sup>	$R_L = 1$ k $\Omega$ , $V_{OUT} = \pm 5$ V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	80	90	dB	
				70			
		$R_L = 100$ $\Omega$ , $V_{OUT} = \pm 5$ V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	70	83		
				60			
$V_O$	Output swing	$R_L = 1$ k $\Omega$ , sourcing	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	12.5	13.3	V	
				12			
		$R_L = 1$ k $\Omega$ , sinking	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-12.5	-13.3		
				-12			
		$R_L = 100$ $\Omega$ , sourcing	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	9	11.6		
				8.5			
		$R_L = 100$ $\Omega$ , sinking	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-9	-10.5		
				-8.5			
	Continuous output current (open loop) <sup>(4)</sup>	Sourcing, $R_L = 100$ $\Omega$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	90	116	mA	
				85			
		Sinking, $R_L = 100$ $\Omega$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	90	105		
				85			
	Continuous output current (in linear region)	Sourcing, $R_L = 100$ $\Omega$		100	mA		
		Sinking, $R_L = 100$ $\Omega$		80			
$I_{SC}$	Output short circuit current	Sourcing		135	mA		
		Sinking		135			
$I_S$	Supply current			2.5	4	mA	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			4.5		

## 5.5 Electrical Characteristics: $\pm 15$ V (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V^+ = 15$  V,  $V^- = -15$  V,  $V_{CM} = 0$  V, and  $R_L = 1$  k $\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(1)</sup>	MAX <sup>(2)</sup>	UNIT
SR	Slew rate <sup>(5)</sup>	$A_V = +2$ , $V_{IN} = 13$ V <sub>PP</sub>		3600			V/ $\mu$ s
		$A_V = +2$ , $V_{IN} = 10$ V <sub>PP</sub>		3000			
	Unity-gain bandwidth	LM6171A		76			MHz
		LM6171B		100			MHz
	-3-dB frequency	LM6171A	$A_V = +1$	200			MHz
			$A_V = +2$	75			
		LM6171B	$A_V = +1$	160			
			$A_V = +2$	62			
$\phi_m$	Phase margin	LM6171A		58			Deg
		LM6171B		40			
$t_s$	Settling time (0.1%)	$A_V = -1$ , $V_{OUT} = \pm 5$ V, $R_L = 500$ $\Omega$	LM6171A	21			ns
			LM6171B	48			
$t_p$	Propagation delay	$A_V = -2$ , $V_{IN} = \pm 5$ V, $R_L = 500$ $\Omega$	LM6171A	4.1			ns
			LM6171B	6			
$A_D$	Differential gain <sup>(6)</sup>			0.03			%
$\phi_D$	Differential phase <sup>(6)</sup>			0.5			$^\circ$
$e_n$	Input-referred voltage noise	$f = 10$ kHz		12			nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-referred current noise	$f = 10$ kHz		1			pA/ $\sqrt{\text{Hz}}$

- (1) Typical values represent the most likely parametric norm
- (2) All limits are specified by testing or statistical analysis.
- (3) Large-signal voltage gain is the total output swing divided by the input signal required to produce that swing. For  $V_S = \pm 15$  V,  $V_{OUT} = \pm 5$  V. For  $V_S = +5$  V,  $V_{OUT} = \pm 1$  V.
- (4) The open-loop output current is the output swing with the 100- $\Omega$  load resistor divided by that resistor.
- (5) Slew rate is the average of the rising and falling slew rates.
- (6) Differential gain and phase are measured with  $A_V = +2$ ,  $V_{IN} = 1$  V<sub>PP</sub> at 3.58 MHz and both input and output 75  $\Omega$  terminated.

## 5.6 Electrical Characteristics: $\pm 5$ V

at  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5$  V,  $V^- = -5$  V,  $V_{CM} = 0$  V, and  $R_L = 1$  k $\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(1)</sup>	MAX <sup>(2)</sup>	UNIT
$V_{OS}$	Input offset voltage	LM6171A	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.2	3	mV	
				5			
		LM6171B	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.2	6		
				8			
$TCV_{OS}$	Input offset voltage average drift			4		$\mu\text{V}/^\circ\text{C}$	
$I_B$	Input bias current		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1	2.5	$\mu\text{A}$	
				3.5			
$I_{OS}$	Input offset current		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	0.03	1.5	$\mu\text{A}$	
				2.2			
$R_{IN}$	Input resistance			40		M $\Omega$	
				Differential-mode	4.9		
$R_O$	Open loop output resistance			14		$\Omega$	
CMRR	Common-mode rejection ratio	LM6171A, $V_{CM} = \pm 2.5$ V	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	80	105	dB	
				75			
		LM6171B, $V_{CM} = \pm 2.5$ V	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	75	105		
				70			
PSRR	Power supply rejection ratio	LM6171A, $V_S = \pm 5$ V to $\pm 15$ V	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	85	95	dB	
				80			
		LM6171B, $V_S = \pm 5$ V to $\pm 15$ V	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	80	95		
				75			
$V_{CM}$	Input common-mode voltage	CMRR > 60 dB		LM6171A	$\pm 3.2$	V	
				LM6171B	$\pm 3.7$		
$A_V$	Large signal voltage gain <sup>(3)</sup>	$R_L = 1$ k $\Omega$ , $V_{OUT} = \pm 1$ V	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	75	84	dB	
				65			
		$R_L = 100$ $\Omega$ , $V_{OUT} = \pm 1$ V	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	70	80		
				60			
$V_O$	Output swing	$R_L = 1$ k $\Omega$ , sourcing	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.2	3.5	V	
				3			
		$R_L = 1$ k $\Omega$ , sinking	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-3.2	-3.4		
				-3			
		$R_L = 100$ $\Omega$ , sourcing	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.8	3.2		
				2.5			
		$R_L = 100$ $\Omega$ , sinking	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-2.8	-3.0		
				-2.5			
	Continuous output current (open loop) <sup>(4)</sup>	Sourcing, $R_L = 100$ $\Omega$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	28	32	mA	
				25			
		Sinking, $R_L = 100$ $\Omega$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	28	30		
				25			
$I_{SC}$	Output short circuit current			Sourcing	130	$\mu\text{A}$	
				Sinking	100		
$I_S$	Supply current		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.3	3	$\mu\text{A}$	
				3.5			
SR	Slew rate <sup>(5)</sup>			$A_V = +2$ , $V_{IN} = 3.5$ V <sub>PP</sub>	750	V/ $\mu\text{s}$	
				$A_V = +2$ , $V_{IN} = 2$ V <sub>PP</sub>	450		

## 5.6 Electrical Characteristics: $\pm 5$ V (continued)

at  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5$  V,  $V^- = -5$  V,  $V_{CM} = 0$  V, and  $R_L = 1$  k $\Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(1)</sup>	MAX <sup>(2)</sup>	UNIT
	Unity-gain bandwidth	LM6171A		70			MHz
		LM6171B		70			
	-3-dB frequency	LM6171A	$A_V = +1$	190			MHz
			$A_V = +2$	75			
		LM6171B	$A_V = +1$	130			
			$A_V = +2$	45			
$\phi_m$	Phase margin			57			Deg
$t_s$	Settling time (0.1%)	$A_V = -1$ , $V_{OUT} = \pm 1$ V, $R_L = 500$ $\Omega$	LM6171A	25			ns
			LM6171B	60			
$t_p$	Propagation delay	$A_V = -2$ , $V_{IN} = \pm 1$ V, $R_L = 500$ $\Omega$	LM6171A	4.5			ns
			LM6171B	8			
$A_D$	Differential gain <sup>(6)</sup>			0.04			%
$\phi_D$	Differential phase <sup>(6)</sup>			0.7			°
$e_n$	Input-referred voltage noise	$f = 10$ kHz		11			nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-referred current noise	$f = 10$ kHz		1			pA/ $\sqrt{\text{Hz}}$

- (1) Typical values represent the most likely parametric norm
- (2) All limits are specified by testing or statistical analysis.
- (3) Large-signal voltage gain is the total output swing divided by the input signal required to produce that swing. For  $V_S = \pm 15$  V,  $V_{OUT} = \pm 5$  V. For  $V_S = +5$  V,  $V_{OUT} = \pm 1$  V
- (4) The open-loop output current is the output swing with the 100- $\Omega$  load resistor divided by that resistor.
- (5) Slew rate is the average of the rising and falling slew rates.
- (6) Differential gain and phase are measured with  $A_V = +2$ ,  $V_{IN} = 1$  V<sub>PP</sub> at 3.58 MHz and both input and output 75  $\Omega$  terminated.

### 5.7 Typical Characteristics: LM6171A Only

at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)

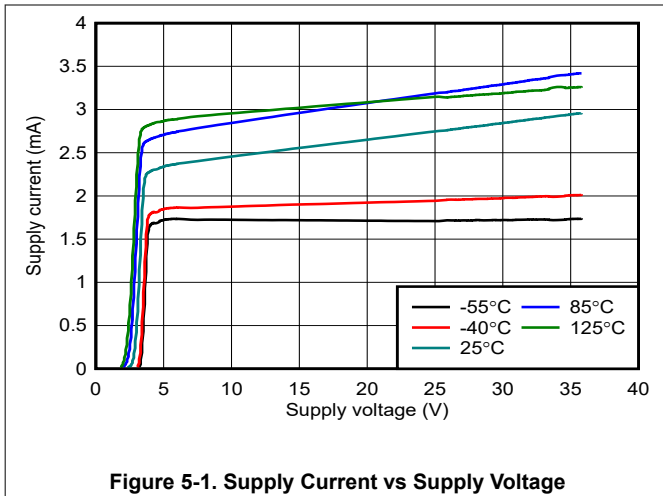


Figure 5-1. Supply Current vs Supply Voltage

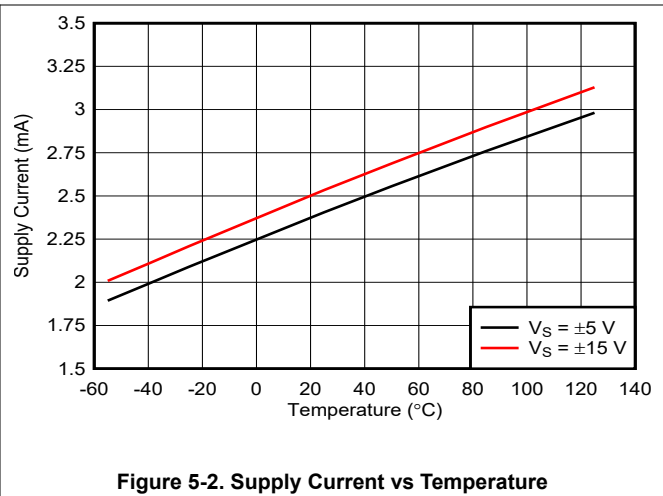


Figure 5-2. Supply Current vs Temperature

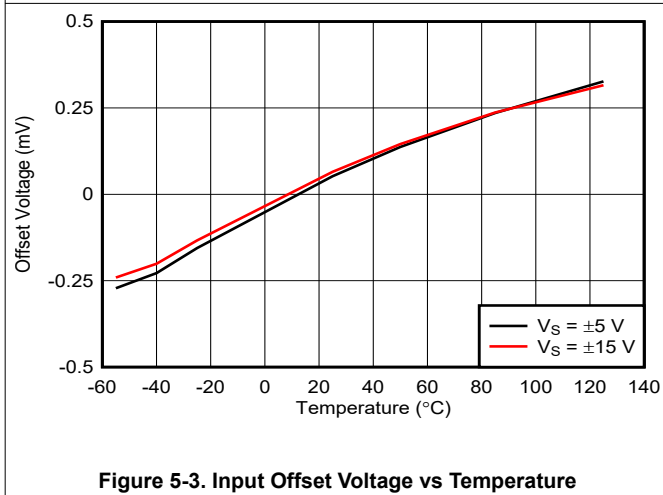


Figure 5-3. Input Offset Voltage vs Temperature

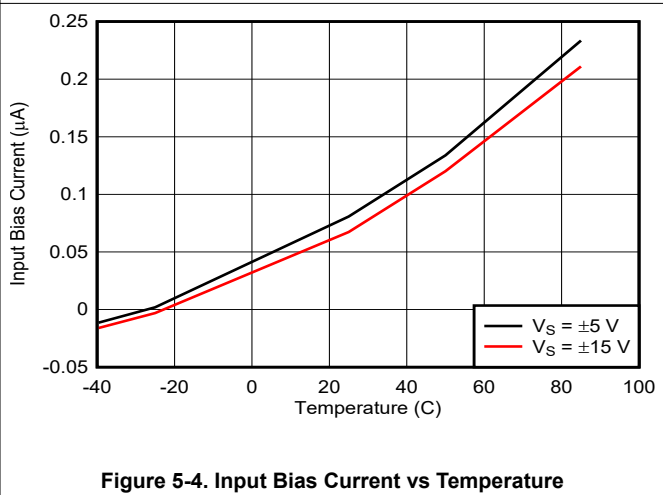


Figure 5-4. Input Bias Current vs Temperature

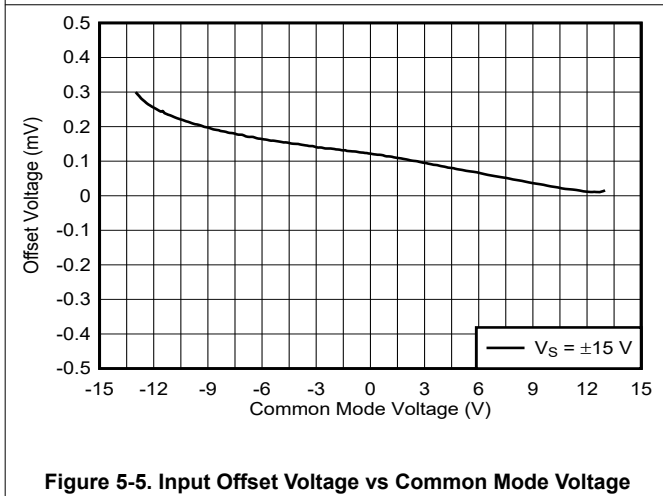


Figure 5-5. Input Offset Voltage vs Common Mode Voltage

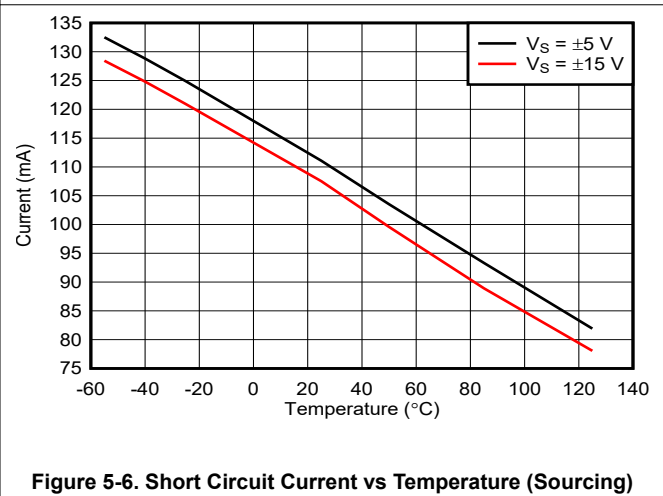
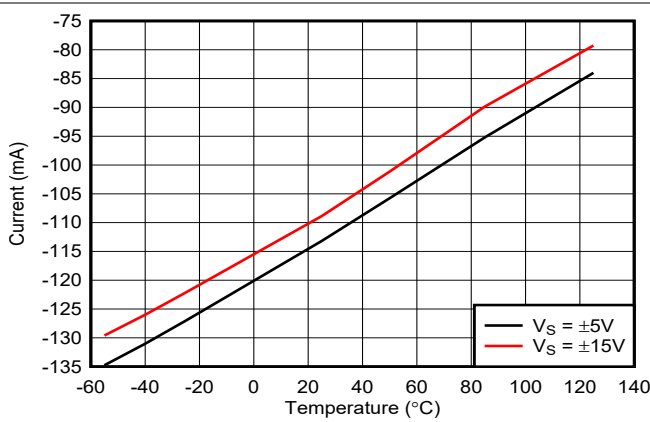


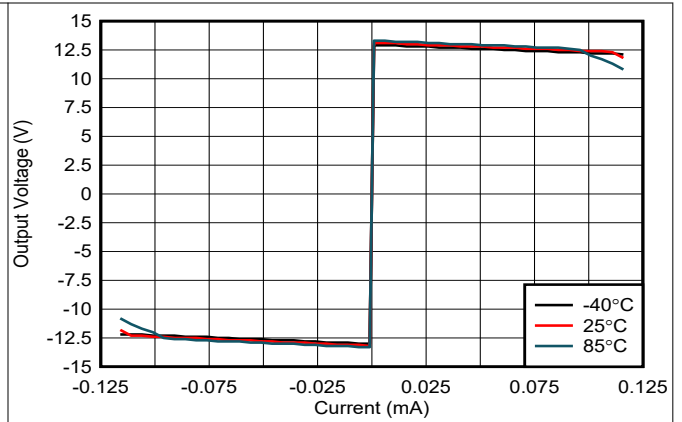
Figure 5-6. Short Circuit Current vs Temperature (Sourcing)

### 5.7 Typical Characteristics: LM6171A Only (continued)

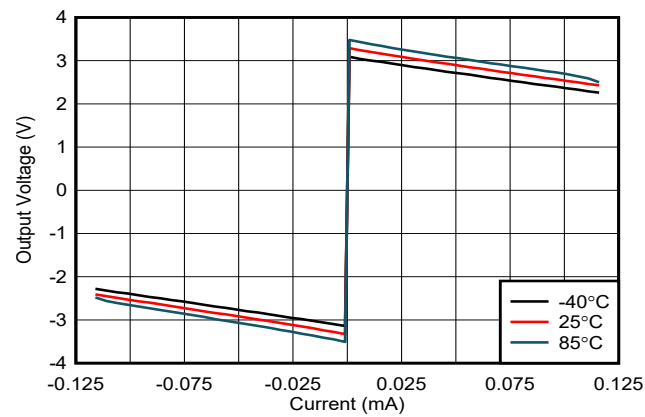
at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)



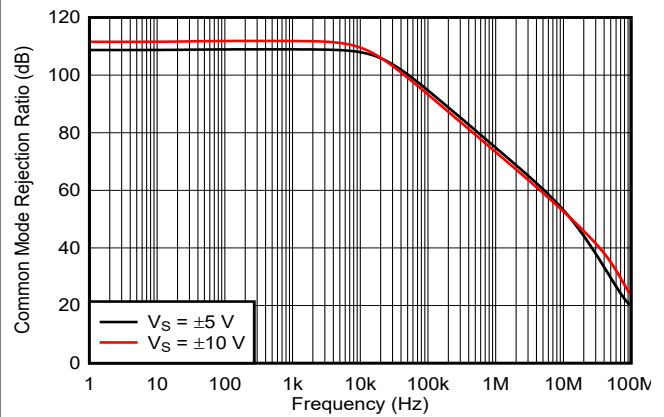
**Figure 5-7. Short Circuit Current vs Temperature (Sinking)**



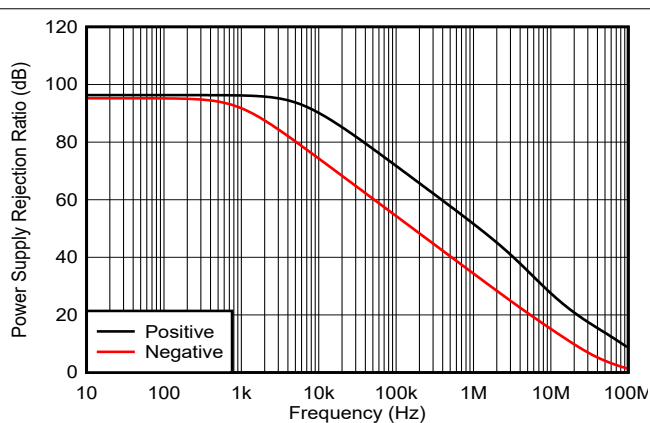
**Figure 5-8. Output Voltage vs Output Current**



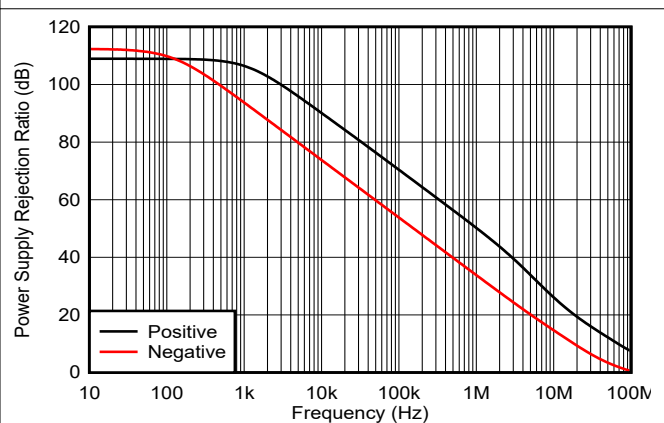
**Figure 5-9. Output Voltage vs Output Current**



**Figure 5-10. CMRR vs Frequency**



**Figure 5-11. PSRR vs Frequency**



**Figure 5-12. PSRR vs Frequency**

### 5.7 Typical Characteristics: LM6171A Only (continued)

at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)

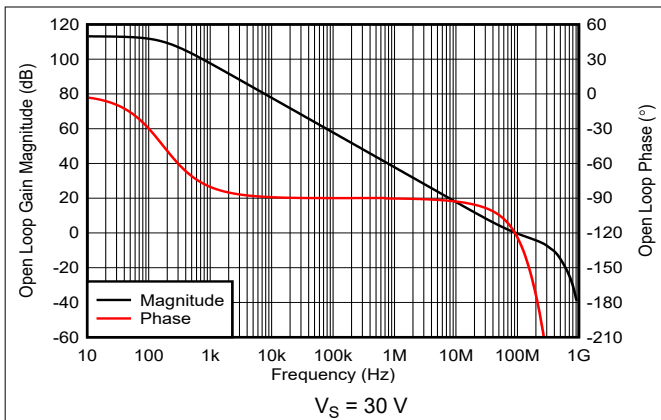


Figure 5-13. Open-Loop Frequency Response

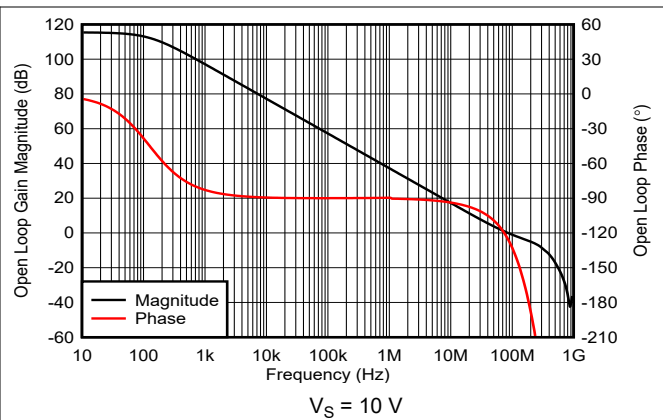


Figure 5-14. Open-Loop Frequency Response

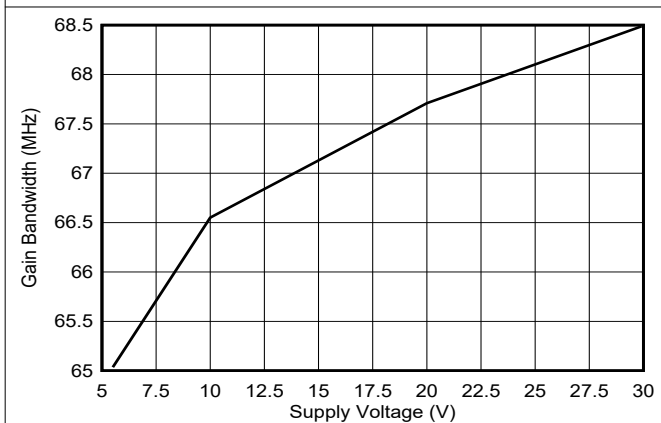


Figure 5-15. Gain Bandwidth Product vs Supply Voltage

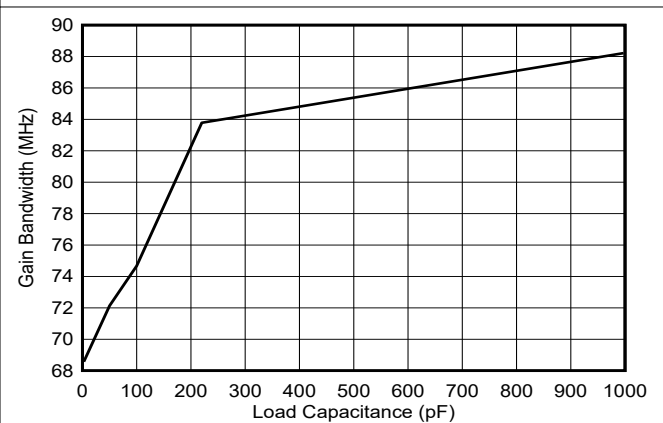


Figure 5-16. Gain Bandwidth Product vs Load Capacitance

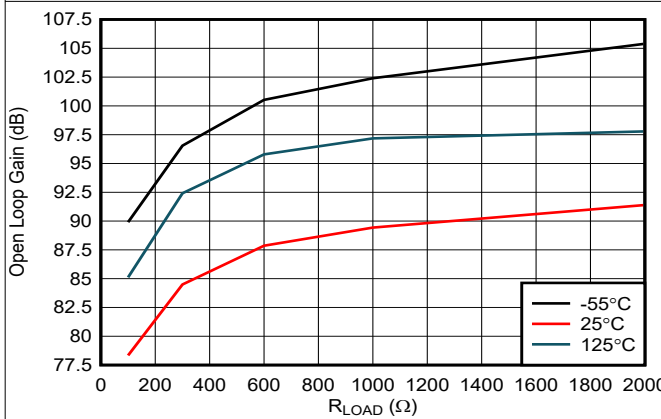


Figure 5-17. Large-Signal Voltage Gain vs Load

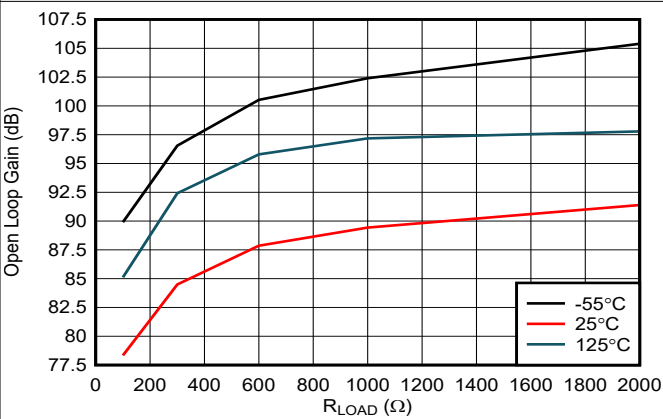
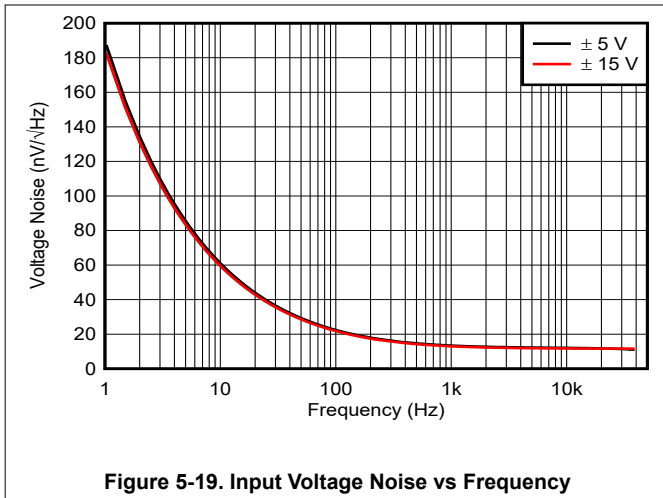


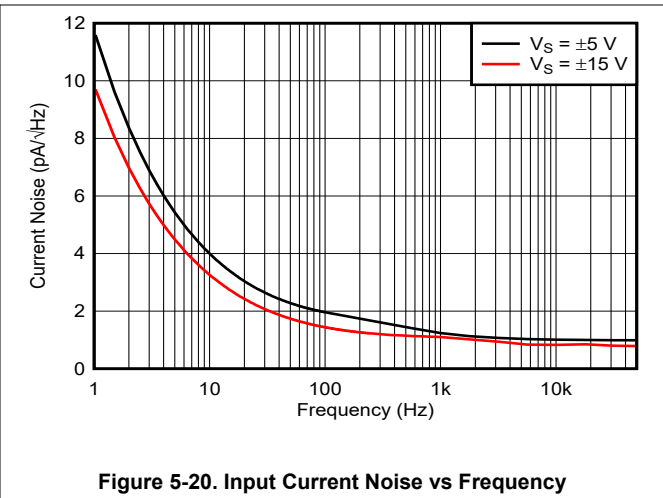
Figure 5-18. Large-Signal Voltage Gain vs Load

### 5.7 Typical Characteristics: LM6171A Only (continued)

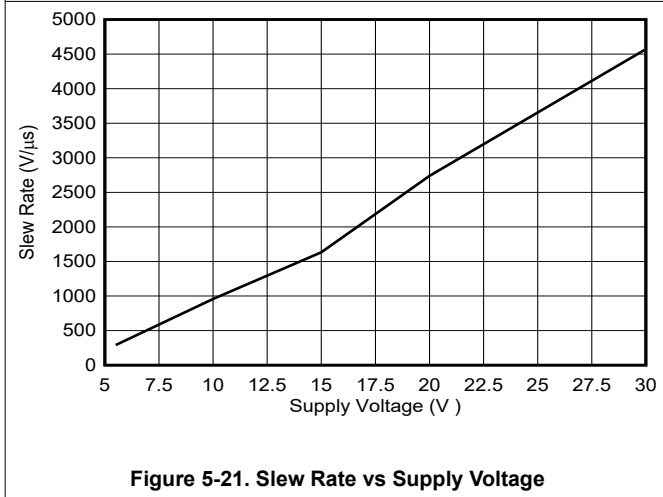
at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)



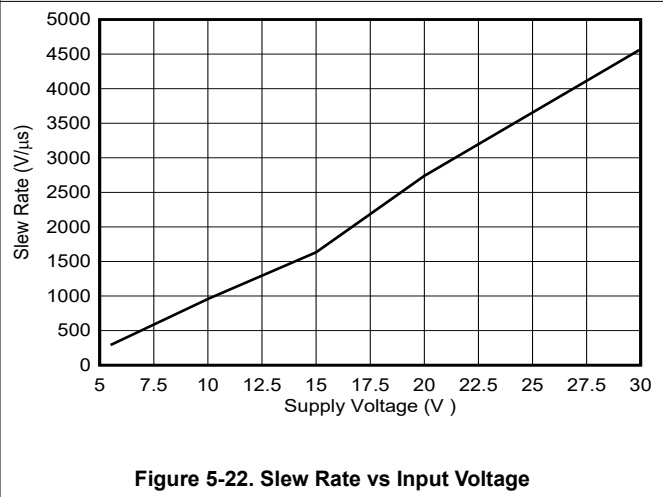
**Figure 5-19. Input Voltage Noise vs Frequency**



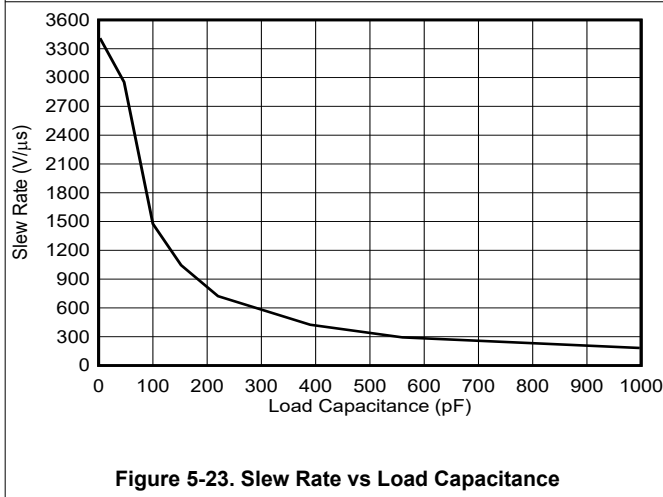
**Figure 5-20. Input Current Noise vs Frequency**



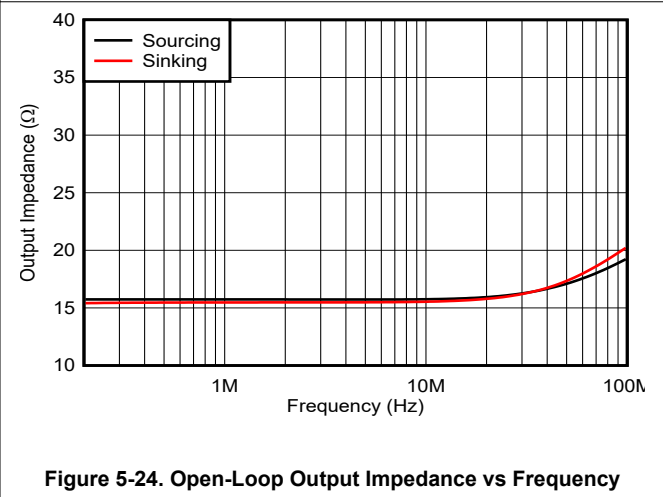
**Figure 5-21. Slew Rate vs Supply Voltage**



**Figure 5-22. Slew Rate vs Input Voltage**



**Figure 5-23. Slew Rate vs Load Capacitance**



**Figure 5-24. Open-Loop Output Impedance vs Frequency**

### 5.7 Typical Characteristics: LM6171A Only (continued)

at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)

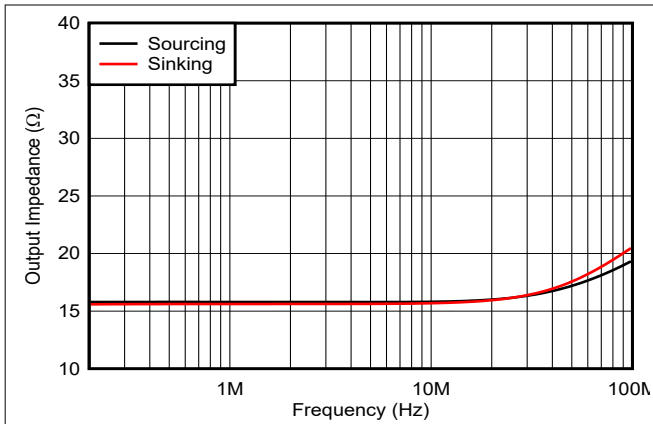
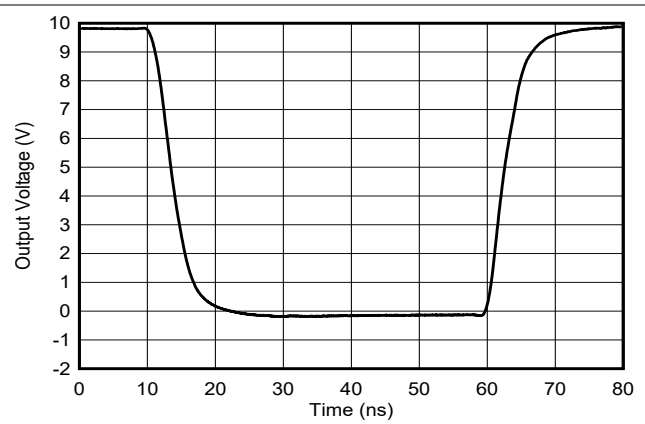
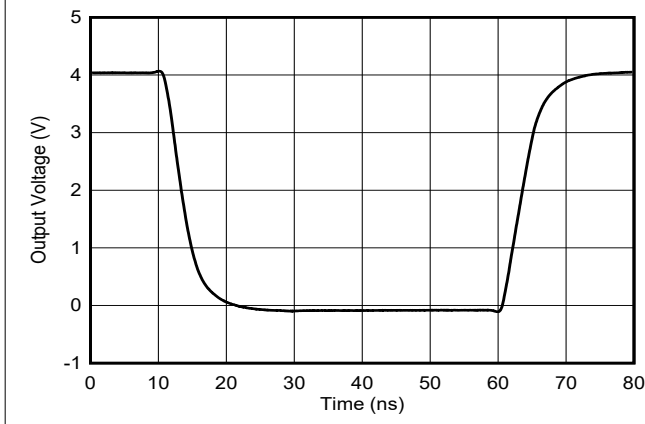


Figure 5-25. Open-Loop Output Impedance vs Frequency



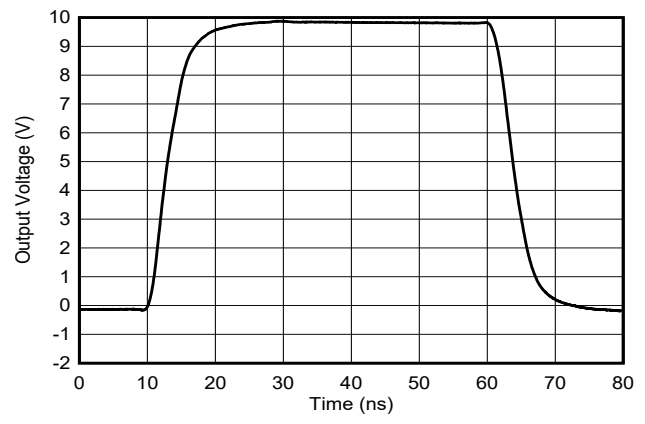
$A_V = -1, V_S = \pm 15\text{ V}$

Figure 5-26. Large-Signal Pulse Response



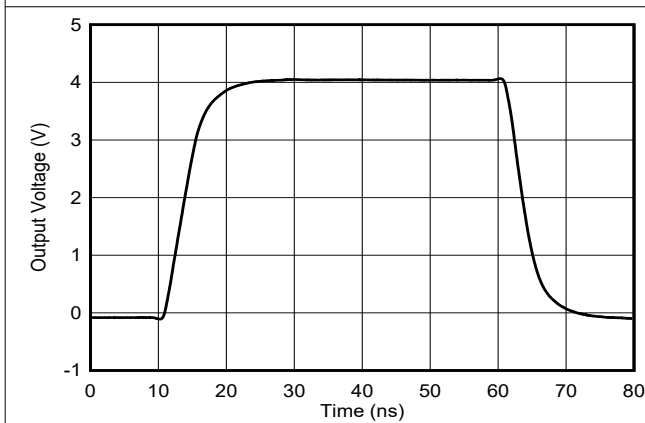
$A_V = -1, V_S = \pm 5\text{ V}$

Figure 5-27. Large-Signal Pulse Response



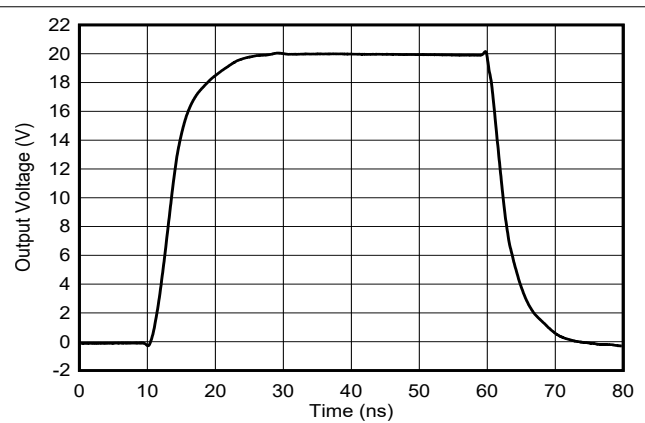
$A_V = 1, V_S = \pm 15\text{ V}$

Figure 5-28. Large-Signal Pulse Response



$A_V = 1, V_S = \pm 5\text{ V}$

Figure 5-29. Large-Signal Pulse Response

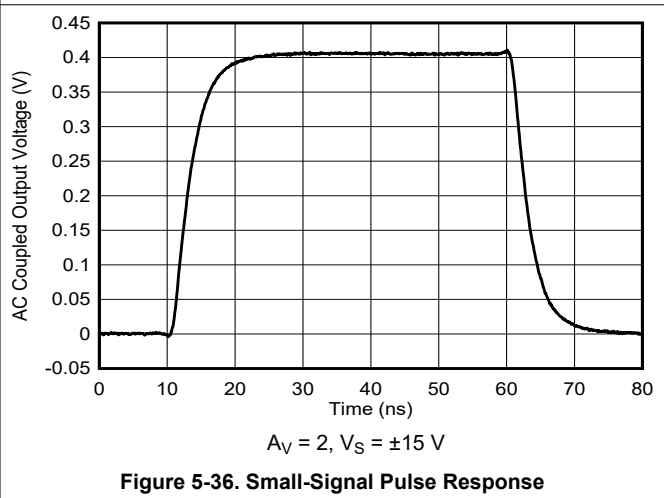
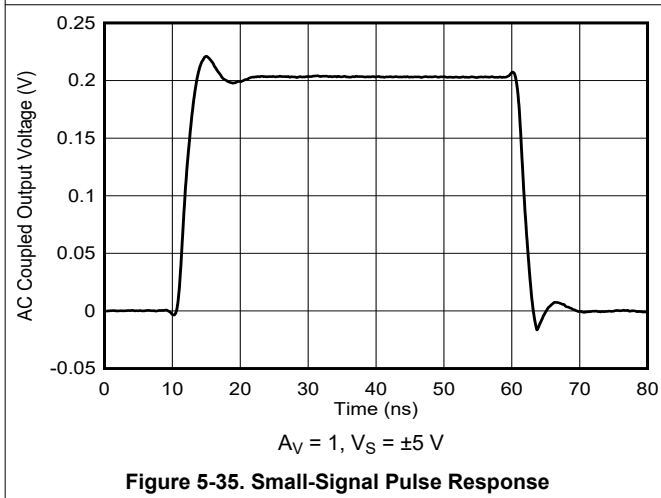
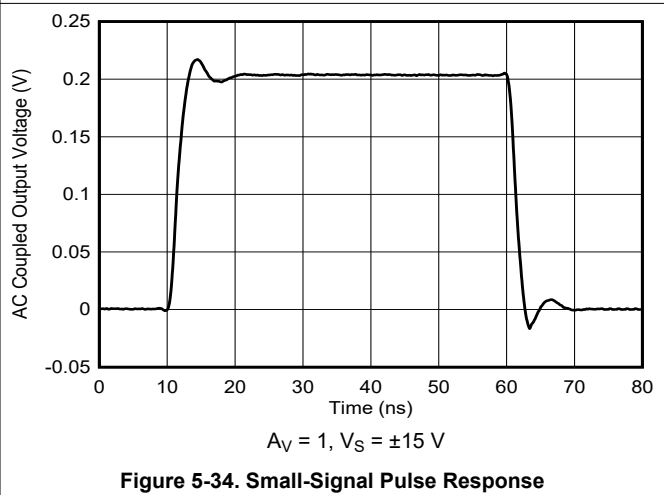
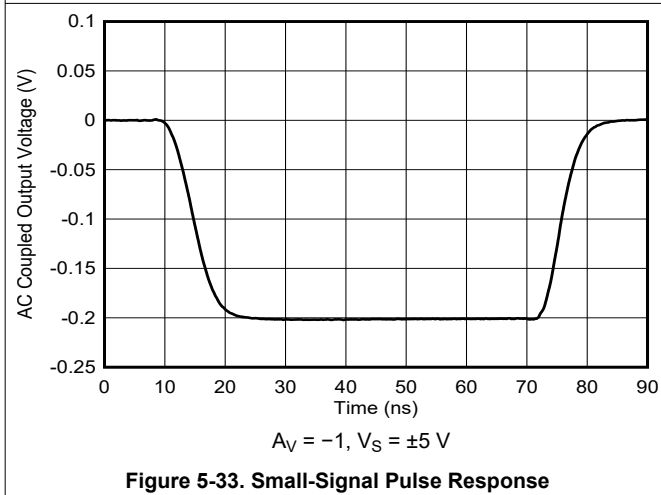
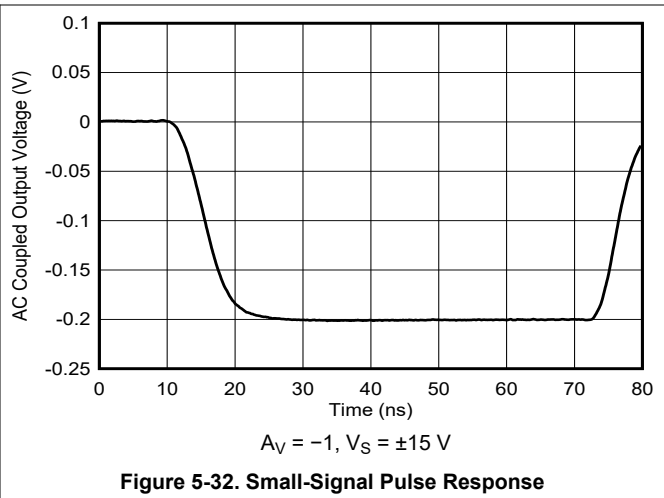
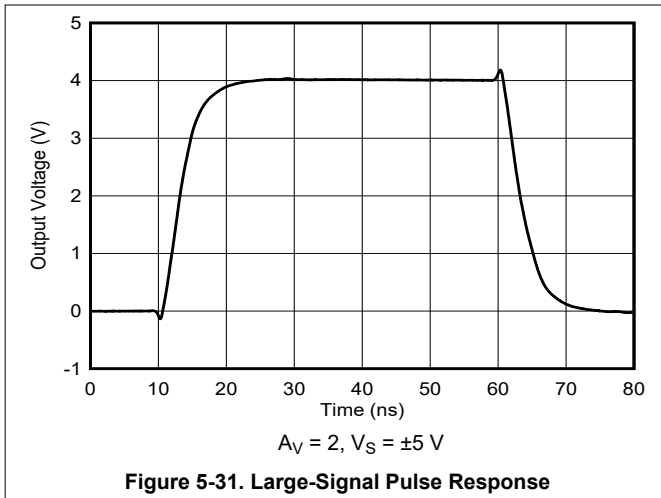


$A_V = 2, V_S = \pm 15\text{ V}$

Figure 5-30. Large-Signal Pulse Response

### 5.7 Typical Characteristics: LM6171A Only (continued)

at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)



### 5.7 Typical Characteristics: LM6171A Only (continued)

at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)

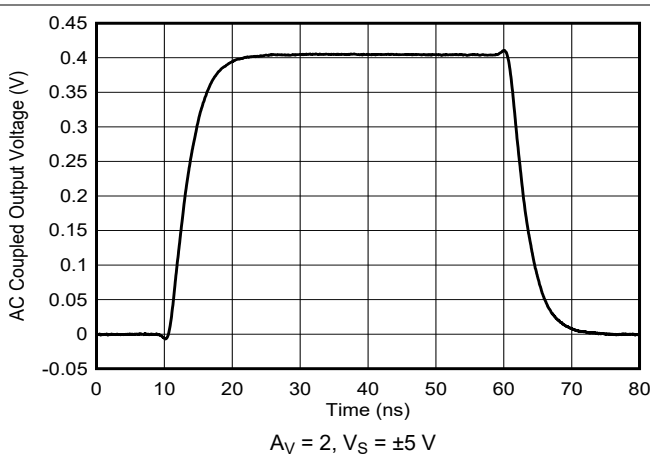


Figure 5-37. Small-Signal Pulse Response

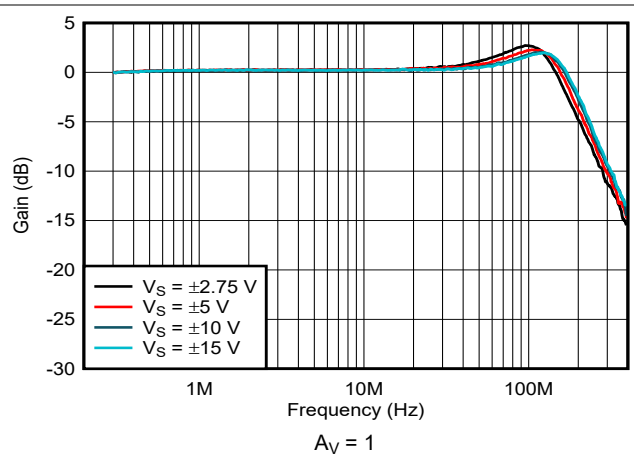


Figure 5-38. Closed-Loop Frequency Response vs Supply Voltage

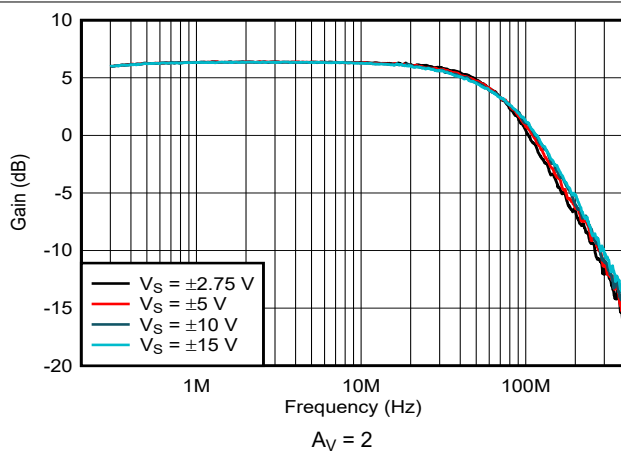


Figure 5-39. Closed-Loop Frequency Response vs Supply Voltage

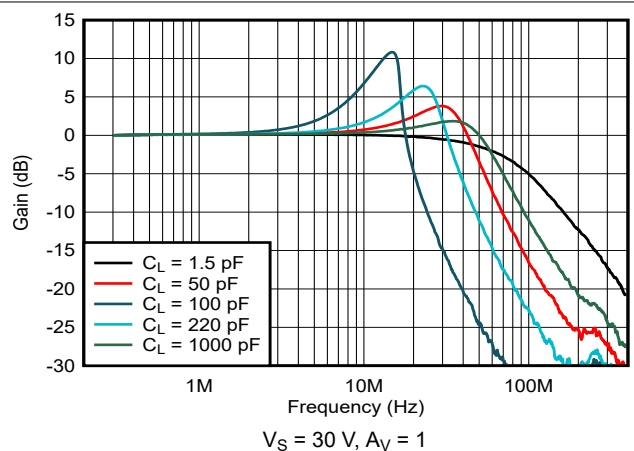


Figure 5-40. Closed-Loop Frequency Response vs Capacitive Load

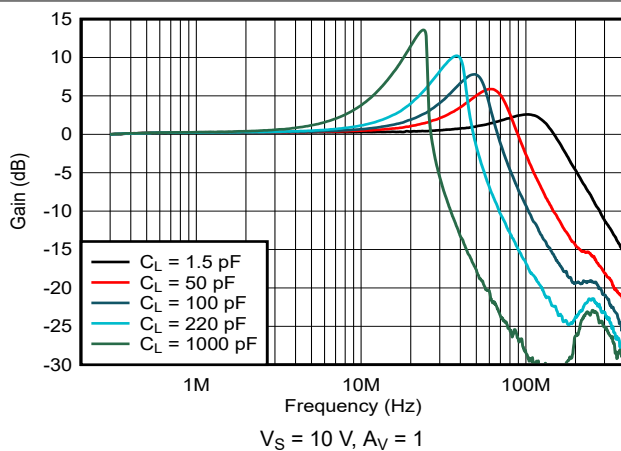


Figure 5-41. Closed Loop Frequency Response vs Capacitive Load

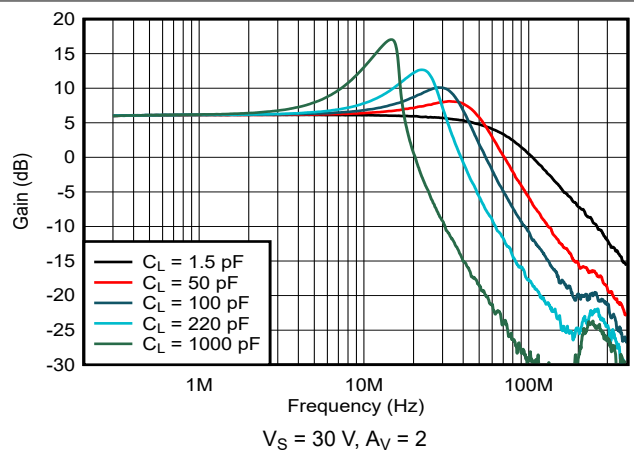
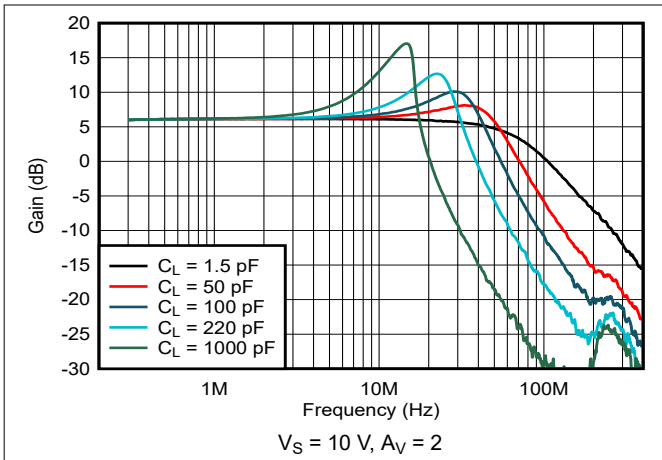


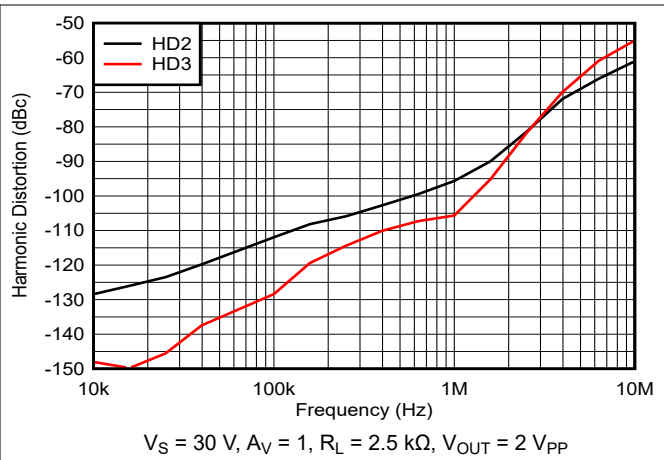
Figure 5-42. Closed-Loop Frequency Response vs Capacitive Load

### 5.7 Typical Characteristics: LM6171A Only (continued)

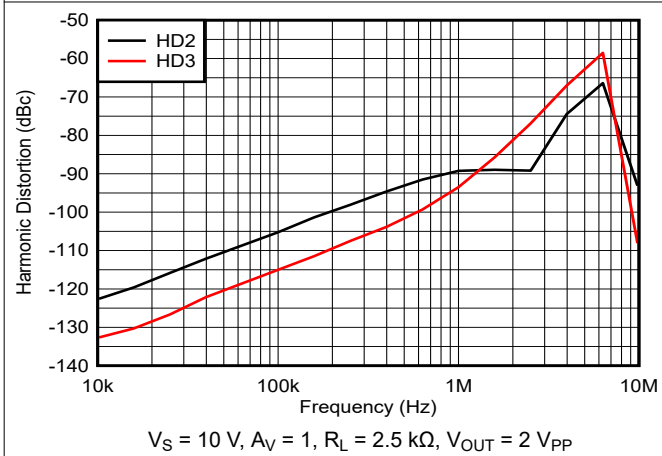
at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)



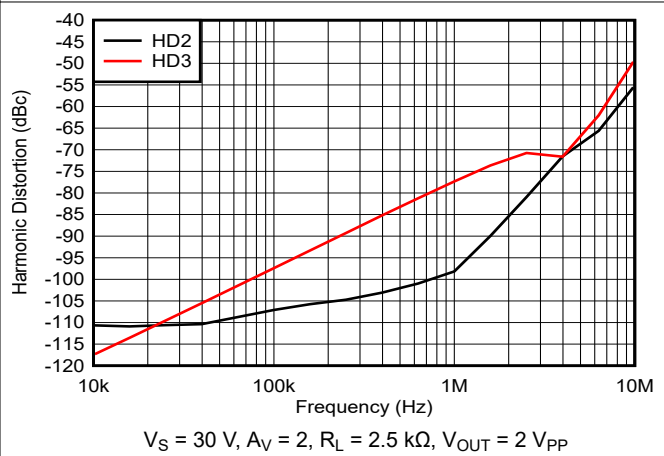
**Figure 5-43. Closed-Loop Frequency Response vs Capacitive Load**



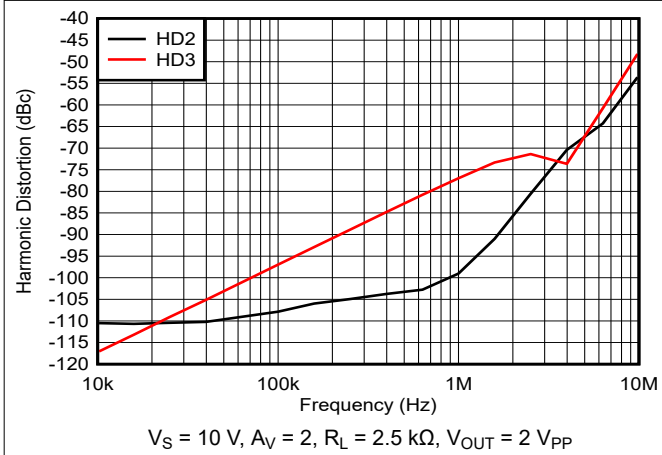
**Figure 5-44. Harmonic Distortion vs Frequency**



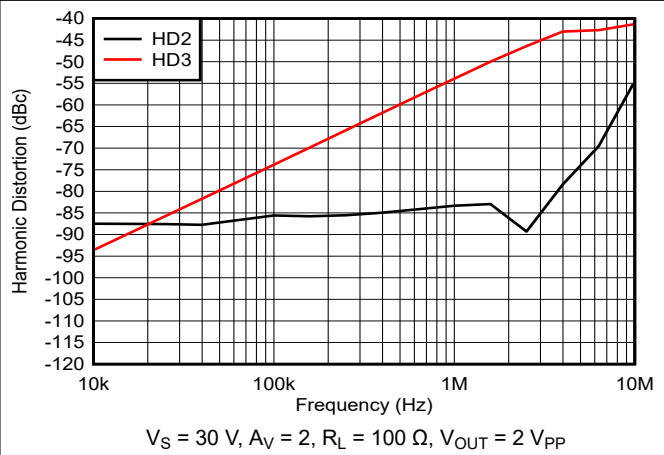
**Figure 5-45. Total Harmonic Distortion vs Frequency**



**Figure 5-46. Total Harmonic Distortion vs Frequency**



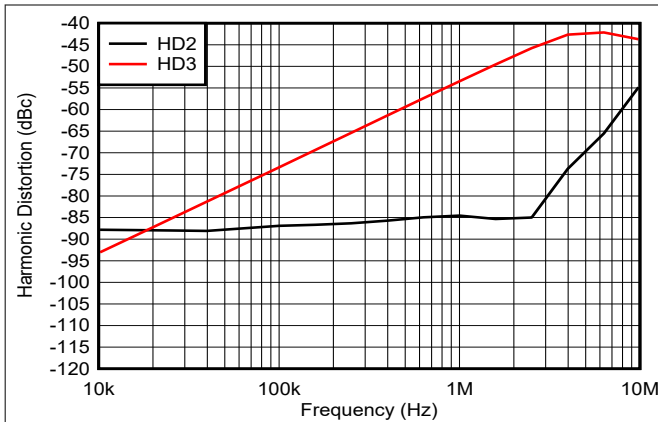
**Figure 5-47. Total Harmonic Distortion vs Frequency**



**Figure 5-48. Harmonic Distortion vs Frequency**

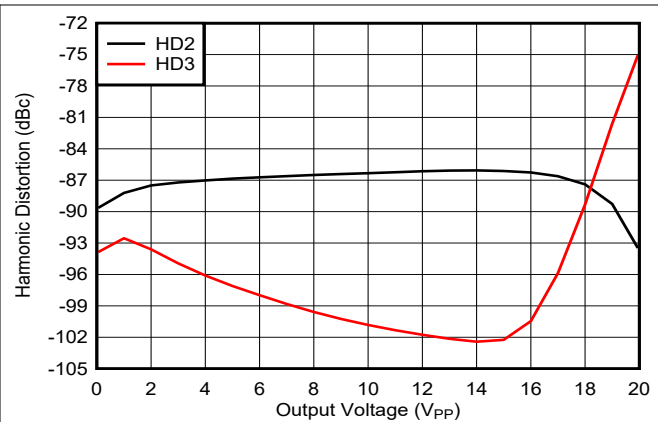
### 5.7 Typical Characteristics: LM6171A Only (continued)

at  $T_A = 25^\circ\text{C}$ , and for LM6171A only (unless otherwise noted)



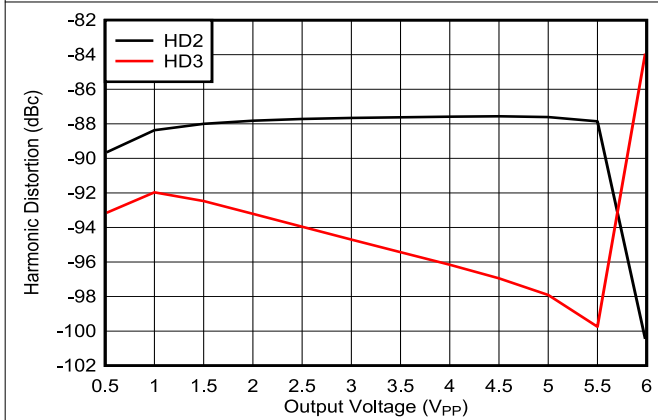
$V_S = 10\text{ V}$ ,  $A_V = 2$ ,  $R_L = 100\ \Omega$ ,  $V_{OUT} = 2\ V_{PP}$

**Figure 5-49. Harmonic Distortion vs Frequency**



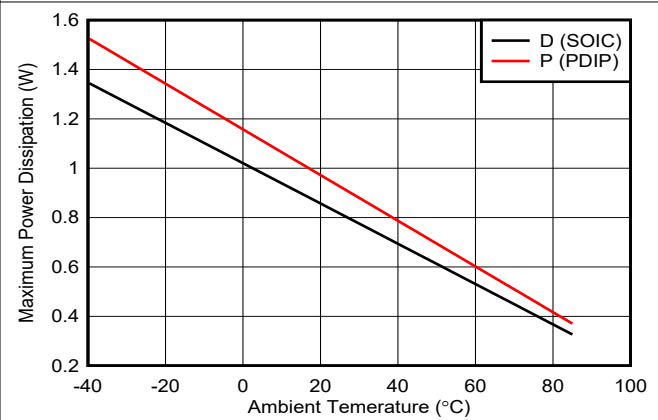
$V_S = 30\text{ V}$ ,  $A_V = 2$ ,  $R_L = 100\ \Omega$ ,  $V_{OUT} = 2\ V_{PP}$ ,  $f = 10\text{ kHz}$

**Figure 5-50. Harmonic Distortion vs Output Voltage Peak to Peak**



$V_S = 10\text{ V}$ ,  $A_V = 2$ ,  $R_L = 100\ \Omega$ ,  $V_{OUT} = 2\ V_{PP}$ ,  $f = 10\text{ kHz}$

**Figure 5-51. Harmonic Distortion vs Output Voltage Peak to Peak**



**Figure 5-52. Total Power Dissipation vs Ambient Temperature**

### 5.8 Typical Characteristics

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

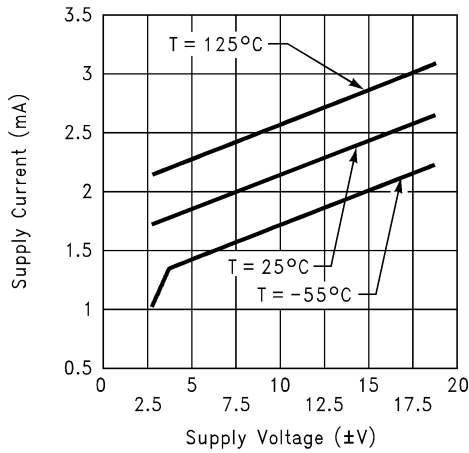


Figure 5-53. Supply Current vs Supply Voltage

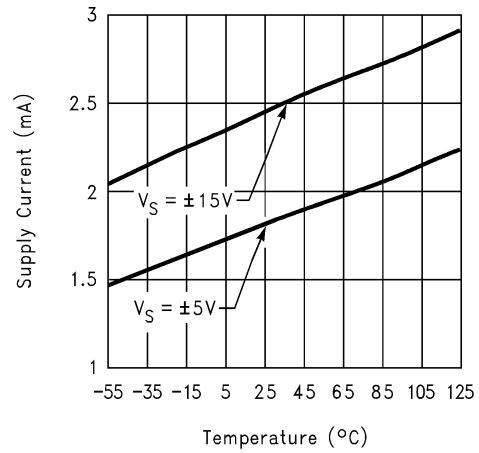


Figure 5-54. Supply Current vs Temperature

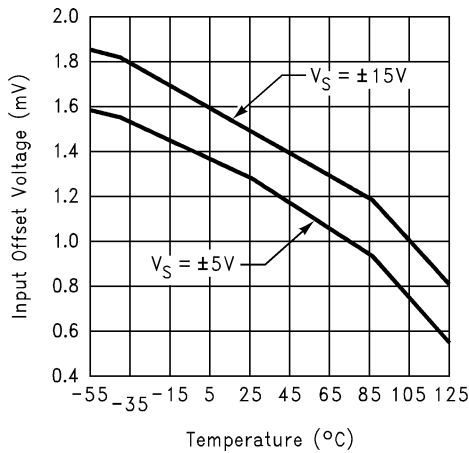


Figure 5-55. Input Offset Voltage vs Temperature

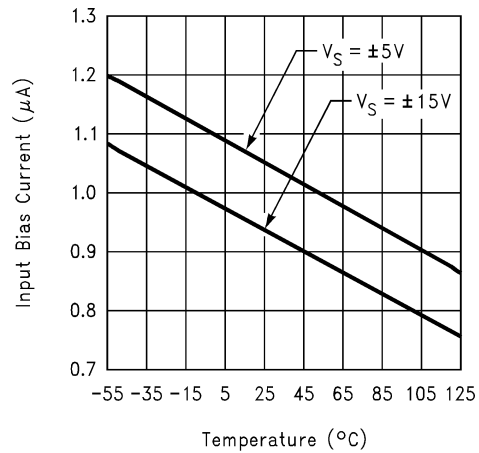


Figure 5-56. Input Bias Current vs Temperature

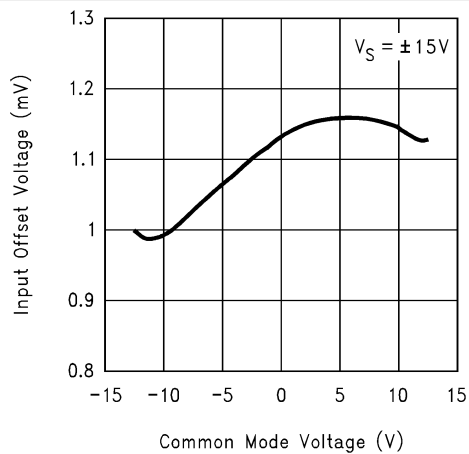


Figure 5-57. Input Offset Voltage vs Common Mode Voltage

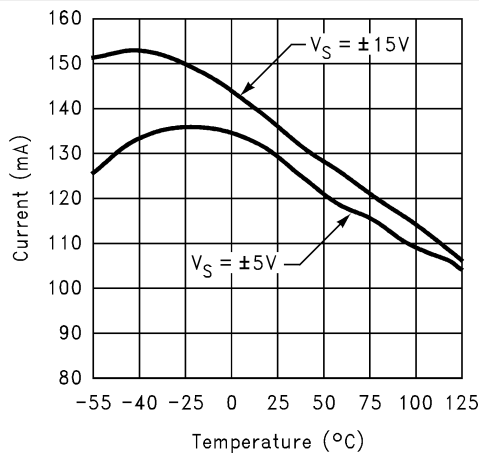


Figure 5-58. Short Circuit Current vs Temperature (Sourcing)

### 5.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

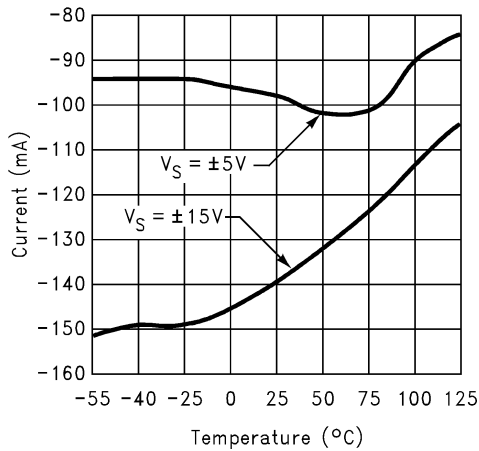


Figure 5-59. Short Circuit Current vs Temperature (Sinking)

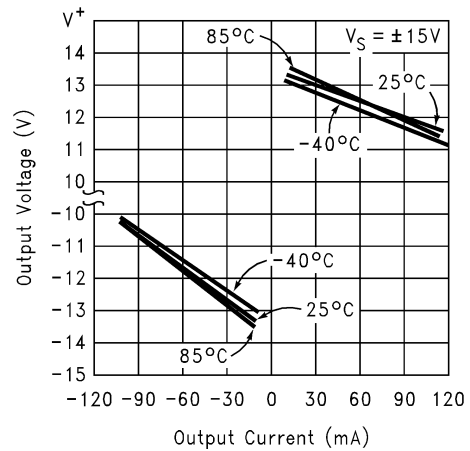


Figure 5-60. Output Voltage vs Output Current

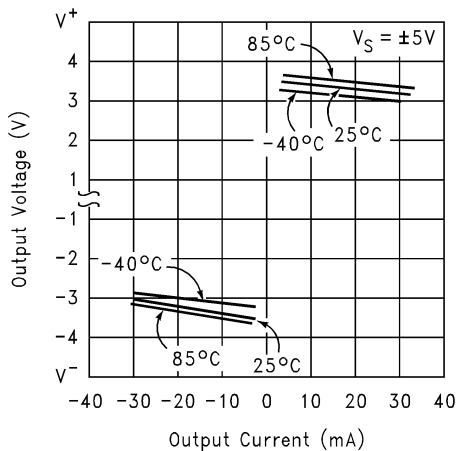


Figure 5-61. Output Voltage vs Output Current

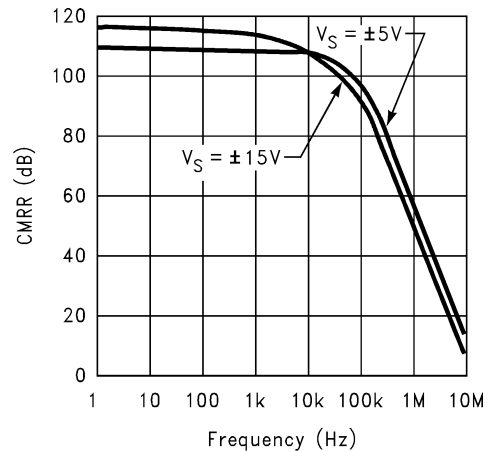


Figure 5-62. CMRR vs Frequency

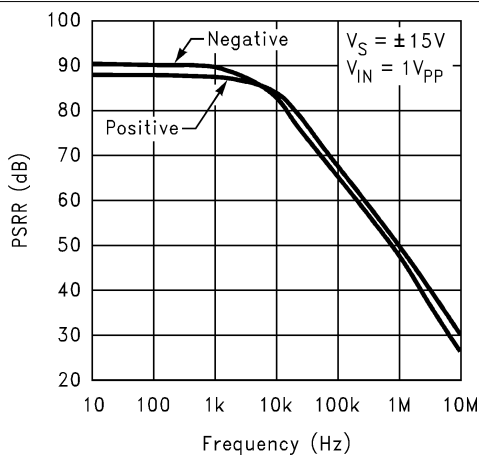


Figure 5-63. PSRR vs Frequency

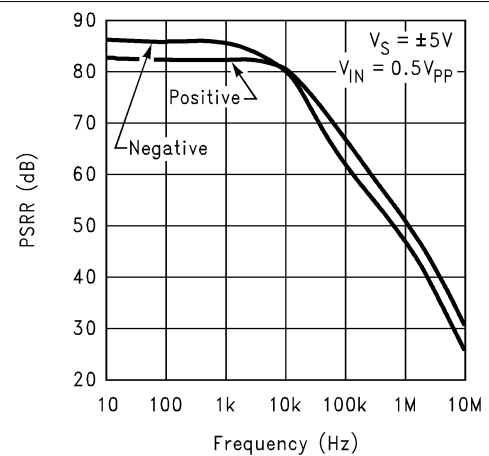
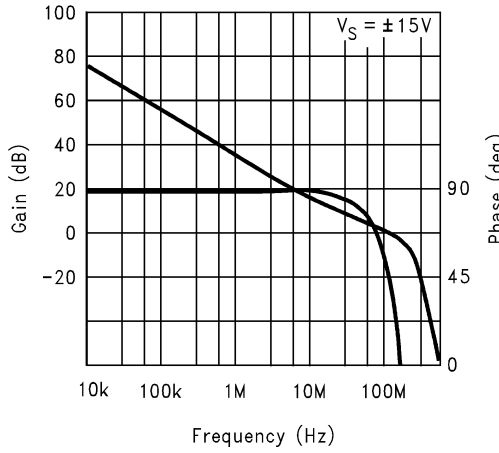


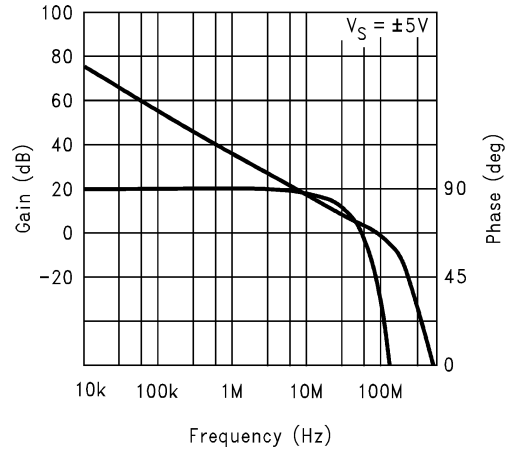
Figure 5-64. PSRR vs Frequency

### 5.8 Typical Characteristics (continued)

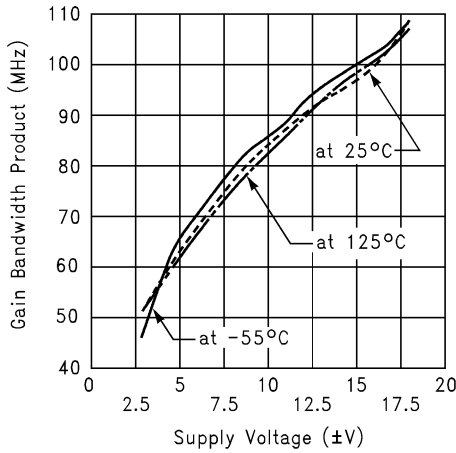
at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



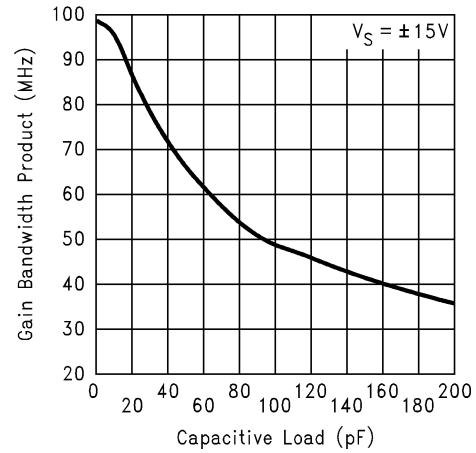
**Figure 5-65. Open-Loop Frequency Response**



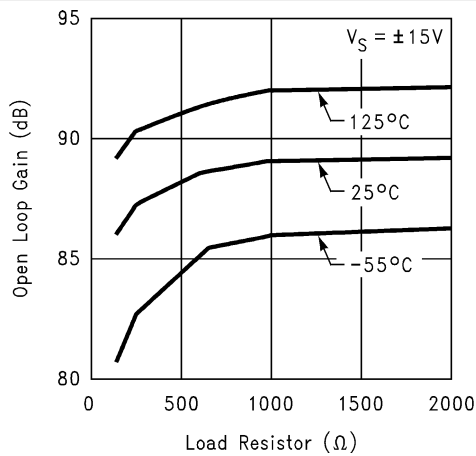
**Figure 5-66. Open-Loop Frequency Response**



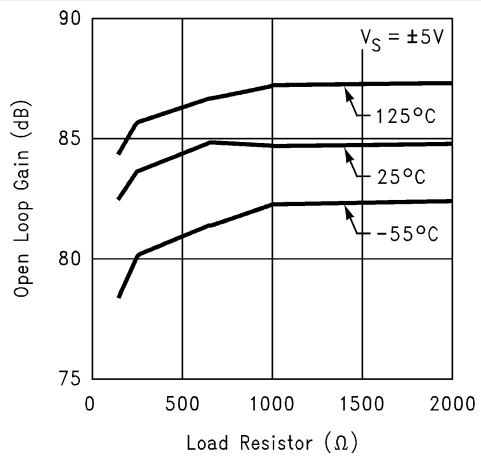
**Figure 5-67. Gain Bandwidth Product vs Supply Voltage**



**Figure 5-68. Gain Bandwidth Product vs Load Capacitance**



**Figure 5-69. Large-Signal Voltage Gain vs Load**



**Figure 5-70. Large-Signal Voltage Gain vs Load**

### 5.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

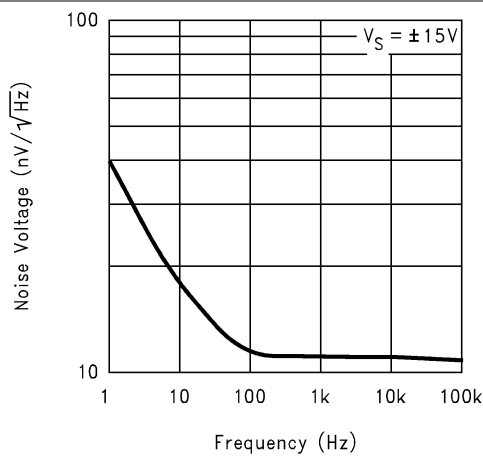


Figure 5-71. Input Voltage Noise vs Frequency

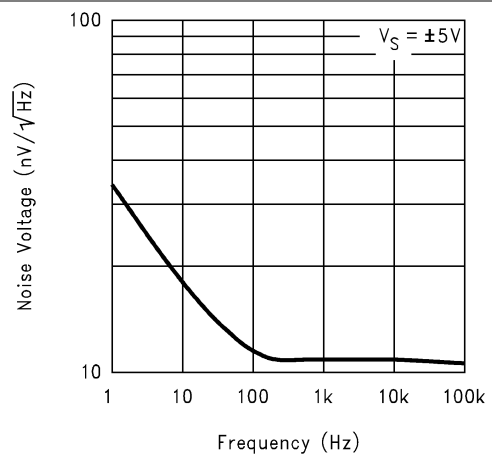


Figure 5-72. Input Voltage Noise vs Frequency

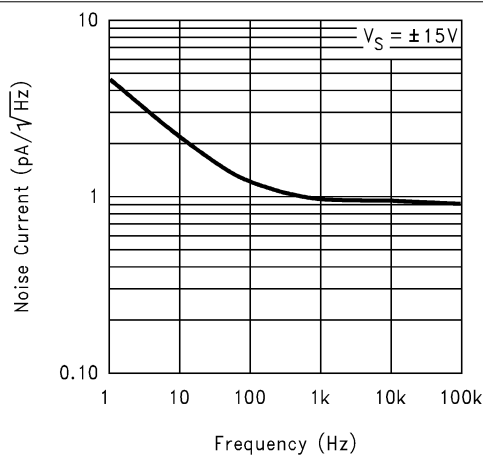


Figure 5-73. Input Current Noise vs Frequency

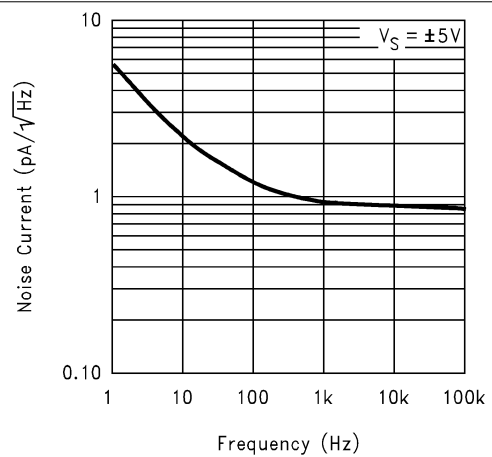


Figure 5-74. Input Current Noise vs Frequency

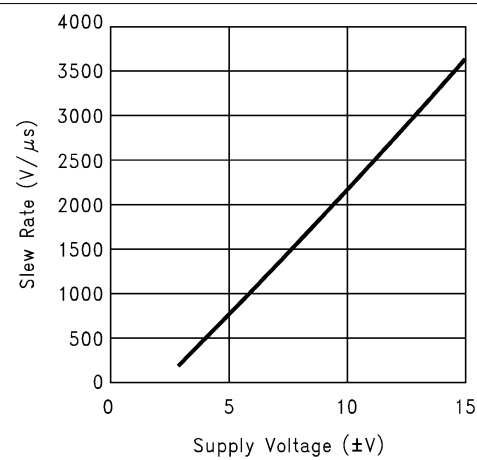


Figure 5-75. Slew Rate vs Supply Voltage

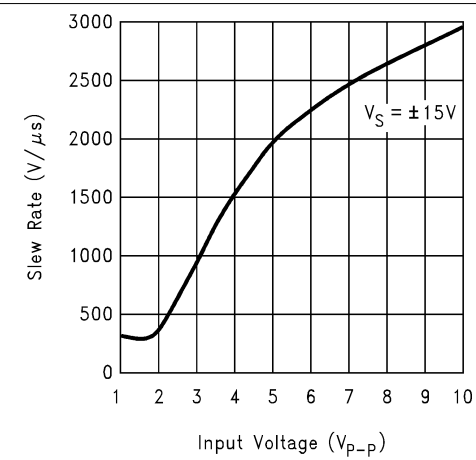
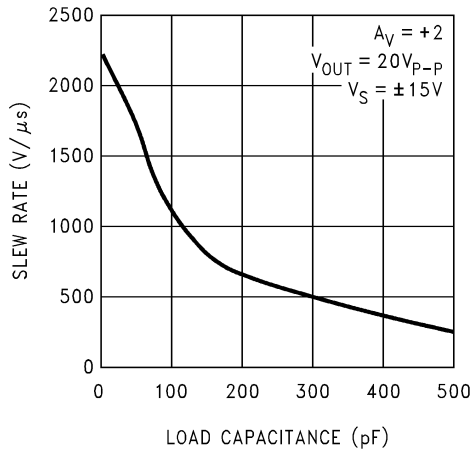


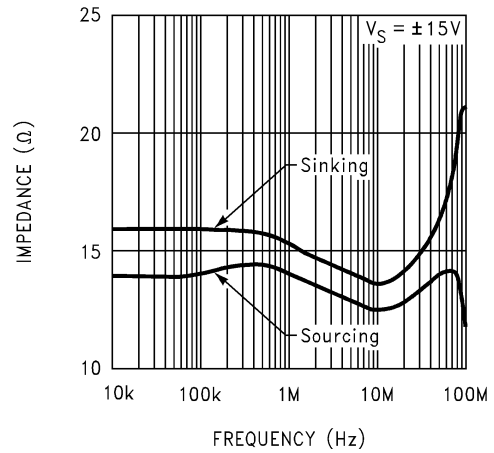
Figure 5-76. Slew Rate vs Input Voltage

### 5.8 Typical Characteristics (continued)

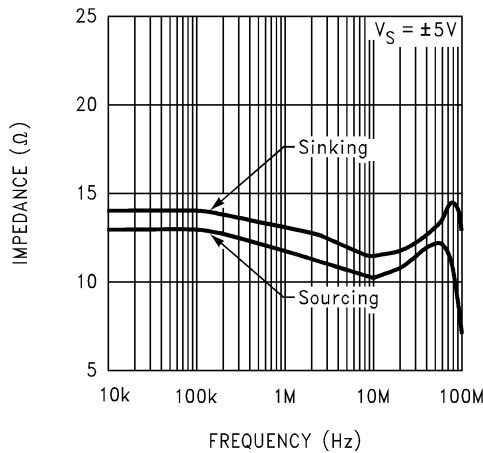
at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



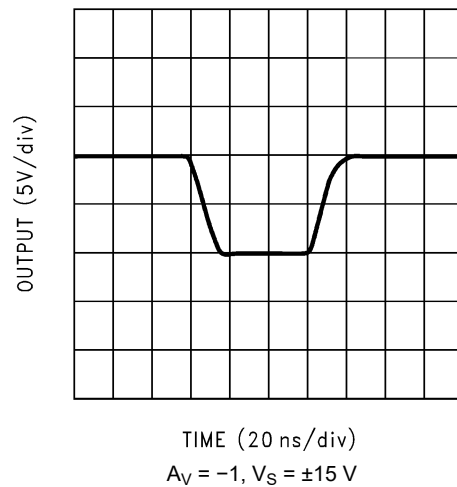
**Figure 5-77. Slew Rate vs Load Capacitance**



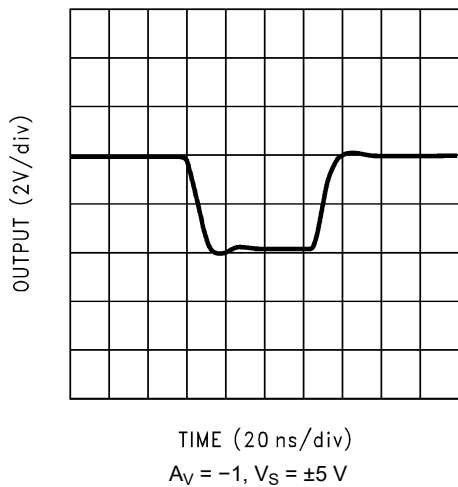
**Figure 5-78. Open-Loop Output Impedance vs Frequency**



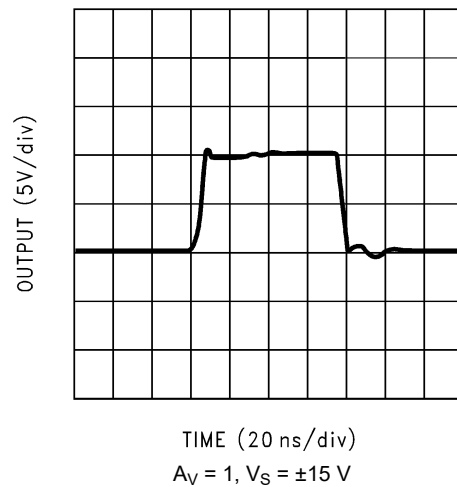
**Figure 5-79. Open-Loop Output Impedance vs Frequency**



**Figure 5-80. Large-Signal Pulse Response**



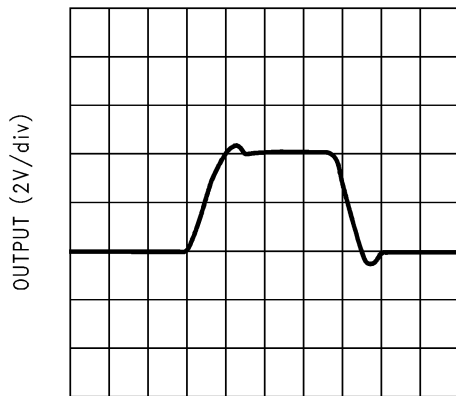
**Figure 5-81. Large-Signal Pulse Response**



**Figure 5-82. Large-Signal Pulse Response**

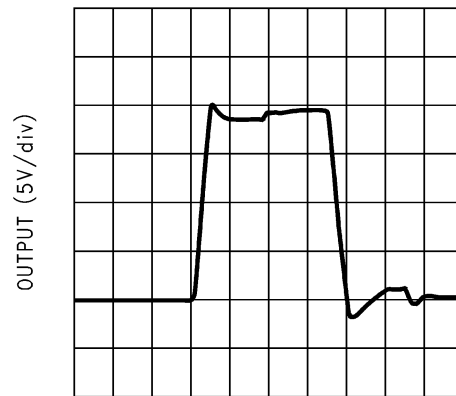
## 5.8 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



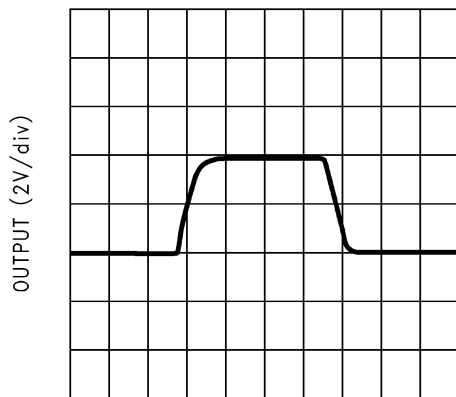
TIME (2 ns/div)  
 $A_V = 1, V_S = \pm 5\text{ V}$

**Figure 5-83. Large-Signal Pulse Response**



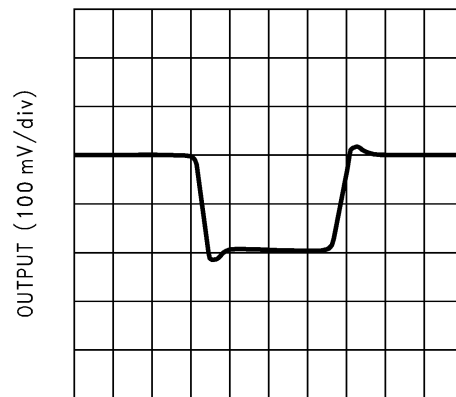
TIME (20 ns/div)  
 $A_V = 2, V_S = \pm 15\text{ V}$

**Figure 5-84. Large-Signal Pulse Response**



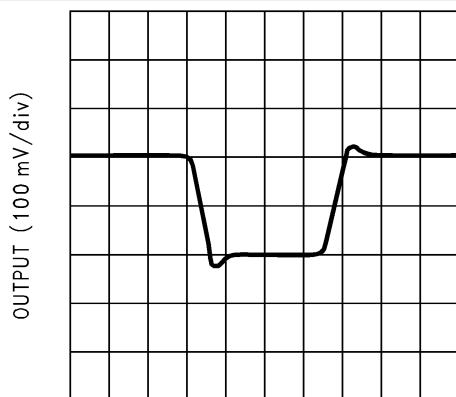
TIME (20 ns/div)  
 $A_V = 2, V_S = \pm 5\text{ V}$

**Figure 5-85. Large-Signal Pulse Response**



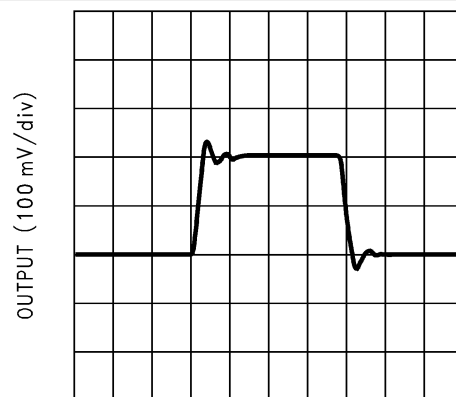
TIME (20 ns/div)  
 $A_V = -1, V_S = \pm 15\text{ V}$

**Figure 5-86. Small-Signal Pulse Response**



TIME (20 ns/div)  
 $A_V = -1, V_S = \pm 5\text{ V}$

**Figure 5-87. Small-Signal Pulse Response**

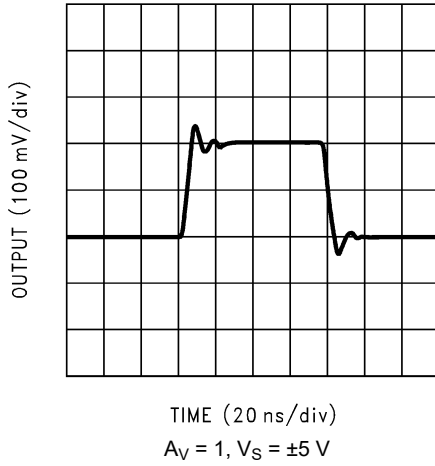


TIME (20 ns/div)  
 $A_V = 1, V_S = \pm 15\text{ V}$

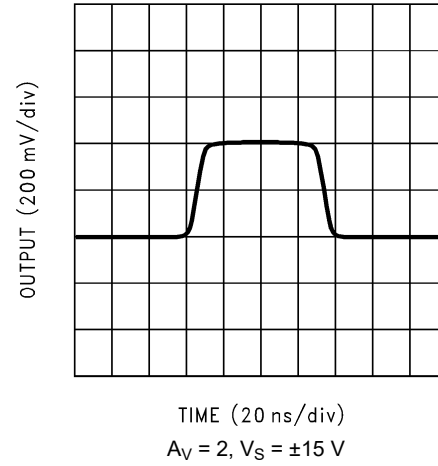
**Figure 5-88. Small-Signal Pulse Response**

### 5.8 Typical Characteristics (continued)

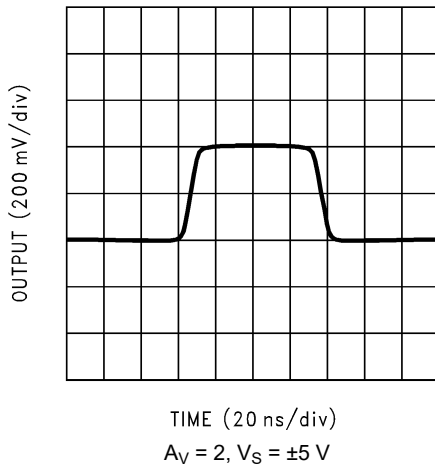
at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



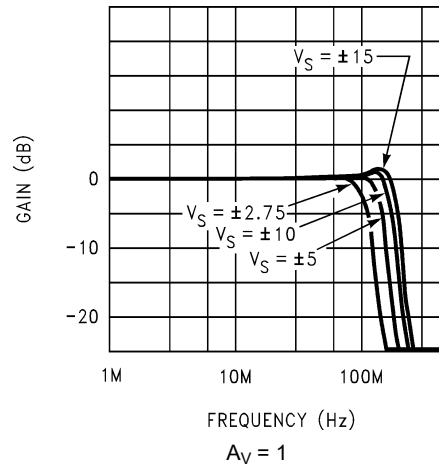
**Figure 5-89. Small-Signal Pulse Response**



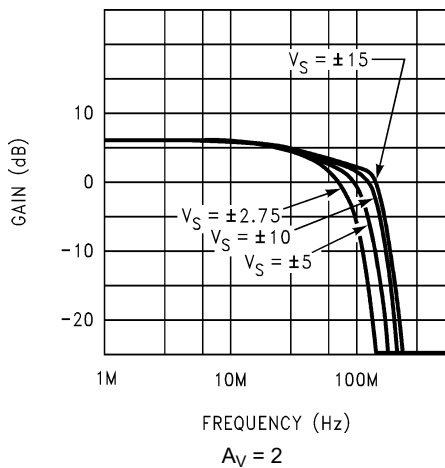
**Figure 5-90. Small-Signal Pulse Response**



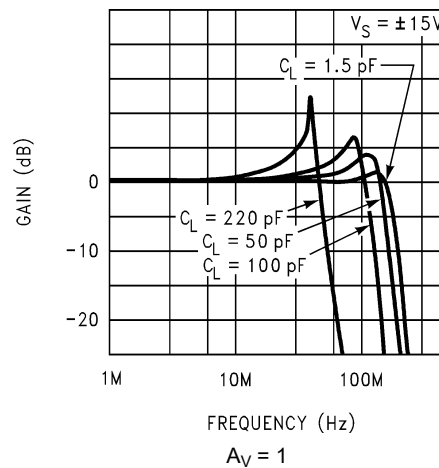
**Figure 5-91. Small-Signal Pulse Response**



**Figure 5-92. Closed-Loop Frequency Response vs Supply Voltage**



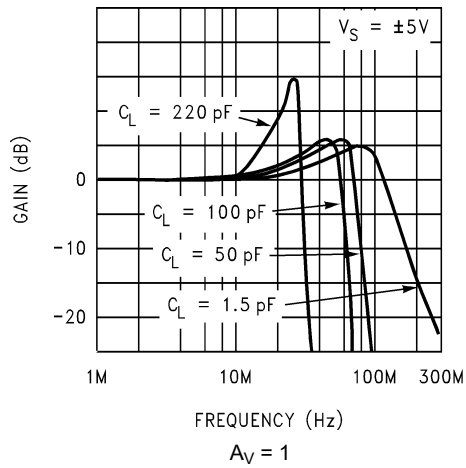
**Figure 5-93. Closed-Loop Frequency Response vs Supply Voltage**



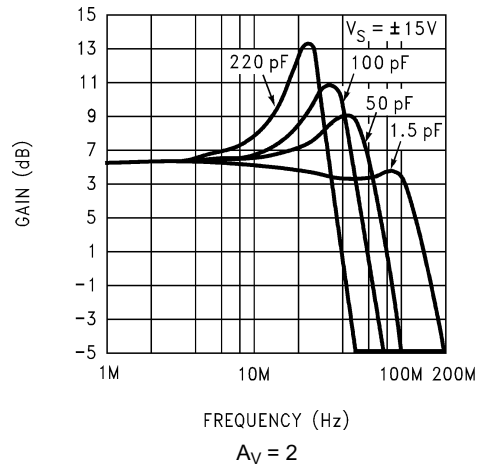
**Figure 5-94. Closed-Loop Frequency Response vs Capacitive Load**

### 5.8 Typical Characteristics (continued)

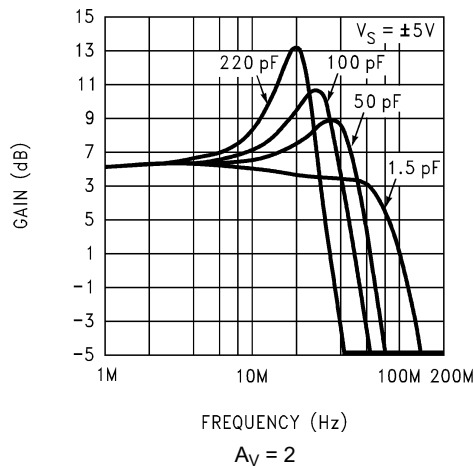
at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



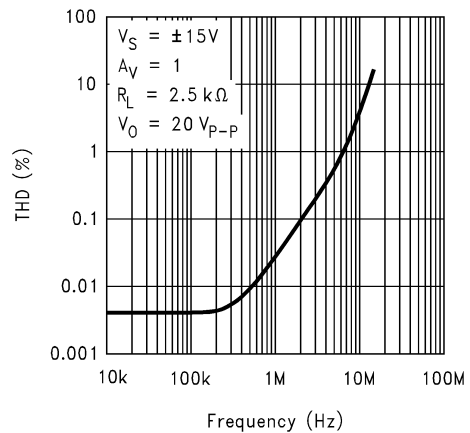
**Figure 5-95. Closed Loop Frequency Response vs Capacitive Load**



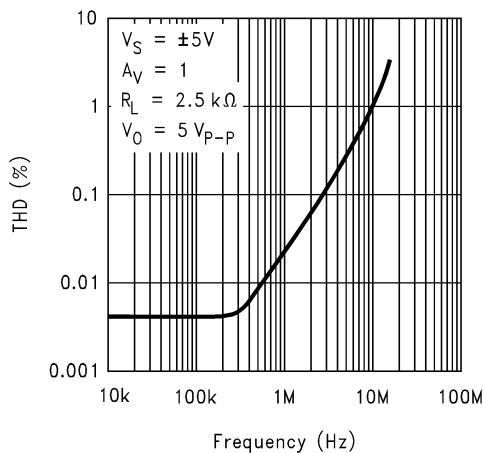
**Figure 5-96. Closed-Loop Frequency Response vs Capacitive Load**



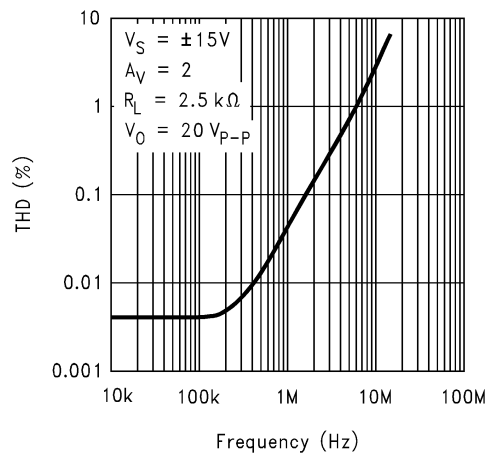
**Figure 5-97. Closed-Loop Frequency Response vs Capacitive Load**



**Figure 5-98. Total Harmonic Distortion vs Frequency**



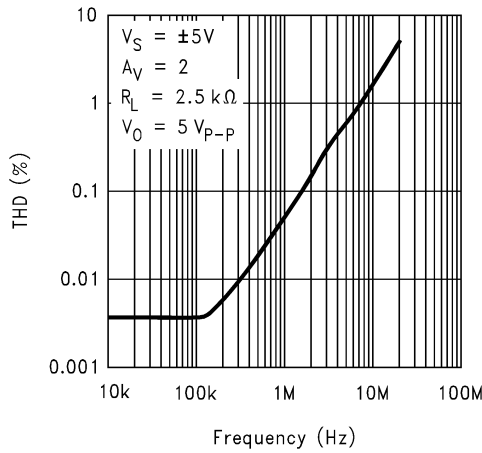
**Figure 5-99. Total Harmonic Distortion vs Frequency**



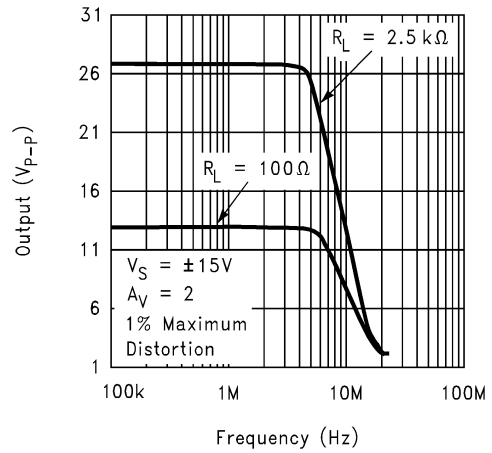
**Figure 5-100. Total Harmonic Distortion vs Frequency**

### 5.8 Typical Characteristics (continued)

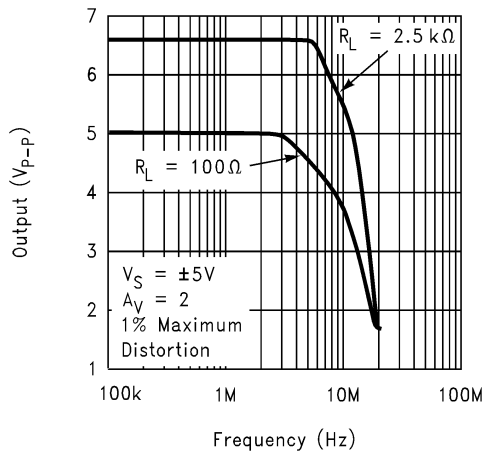
at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



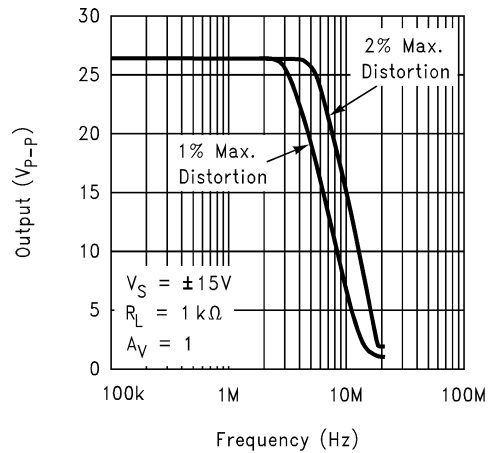
**Figure 5-101. Total Harmonic Distortion vs Frequency**



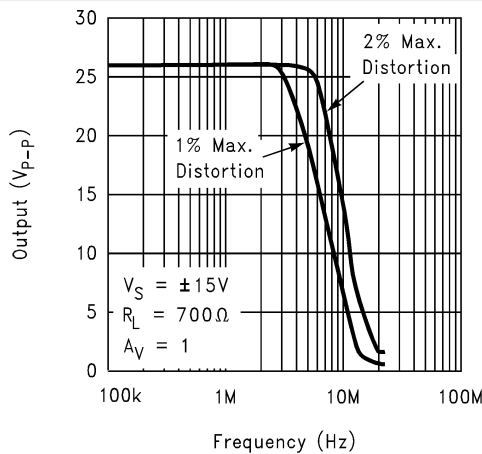
**Figure 5-102. Undistorted Output Swing vs Frequency**



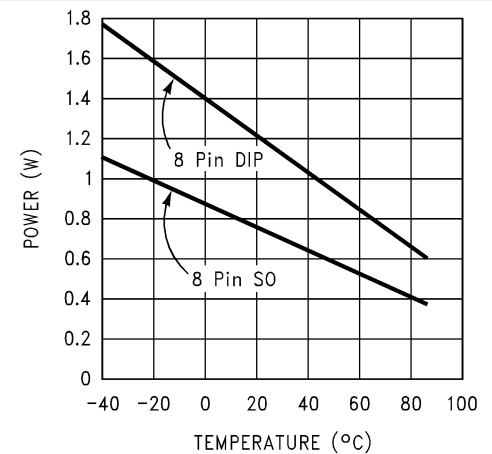
**Figure 5-103. Undistorted Output Swing vs Frequency**



**Figure 5-104. Undistorted Output Swing vs Frequency**



**Figure 5-105. Undistorted Output Swing vs Frequency**



**Figure 5-106. Total Power Dissipation vs Ambient Temperature**

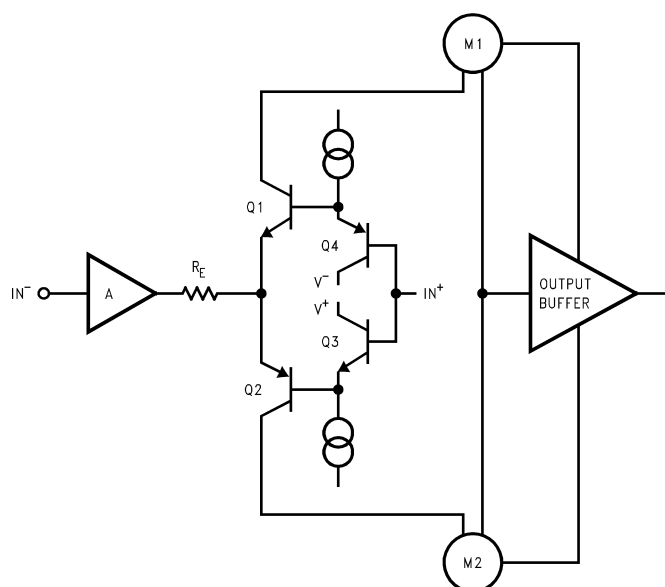
## 6 Detailed Description

### 6.1 Overview

The LM6171 is a high-speed, unity-gain-stable voltage-feedback amplifier. The device consumes only 2.5 mA of supply current while providing a gain-bandwidth product of 100 MHz and a slew rate of 3600 V/ $\mu$ s. The LM6171 has additional features, such as low differential gain and phase, and high output current. The LM6171 is a great choice in high-speed circuits.

The LM6171 is a true voltage-feedback amplifier. Unlike current-feedback amplifiers (CFAs) with a low inverting input impedance and a high noninverting input impedance, both inputs of voltage-feedback amplifiers (VFAs) have high-impedance nodes. The low-impedance inverting input in CFAs couples with a feedback capacitor and causes oscillation. As a result, CFAs cannot be used in traditional op-amp circuits, such as photodiode amplifiers, I-to-V converters, and integrators.

### 6.2 Functional Block Diagram



### 6.3 Feature Description

#### 6.3.1 Circuit Operation

The class AB input stage in the LM6171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the [Section 6.2](#), Q1 through Q4 form the equivalent of the current feedback input buffer,  $R_E$  forms the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

#### 6.3.2 Slew Rate

The slew rate of the LM6171 is determined by the current available to charge and discharge an internal high impedance node capacitor. The current is the differential input voltage divided by the total degeneration resistor  $R_E$ . Therefore, the slew rate is proportional to the input voltage level, and higher slew rates are achievable in lower-gain configurations.

When a very fast, large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor, such as 1 k $\Omega$ , to the input of the LM6171, the bandwidth is reduced to help reduce overshoot.

### 6.4 Device Functional Modes

The LM6171 has a single functional mode and can be used with both single-supply or split power-supply configurations. The power-supply voltage must be greater than 9 V ( $\pm 4.5$  V) and less than 33 V ( $\pm 16.5$  V).

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

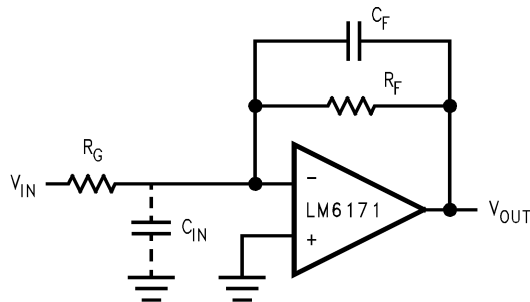
### 7.1 Application Information

#### 7.1.1 Compensation for Input Capacitance

The combination of an amplifier input capacitance and gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, use a feedback capacitor with the following value to cancel that pole:

$$C_F > \frac{R_G \times C_{IN}}{R_F} \quad (1)$$

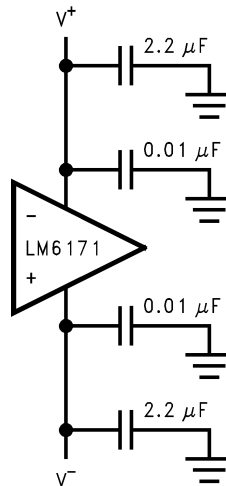
For the LM6171, a feedback capacitor of 2 pF is recommended. [Figure 7-1](#) illustrates the compensation circuit.



**Figure 7-1. Compensating for Input Capacitance**

### 7.1.2 Power Supply Bypassing

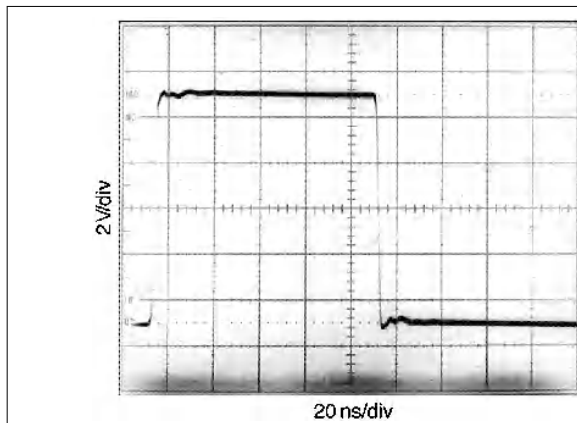
Bypassing the power supply is necessary to maintain low power-supply impedance across frequency. Individually bypass both positive and negative power supplies by placing 0.01- $\mu\text{F}$  ceramic capacitors directly to power-supply pins and 2.2- $\mu\text{F}$  tantalum capacitors close to the power-supply pins.



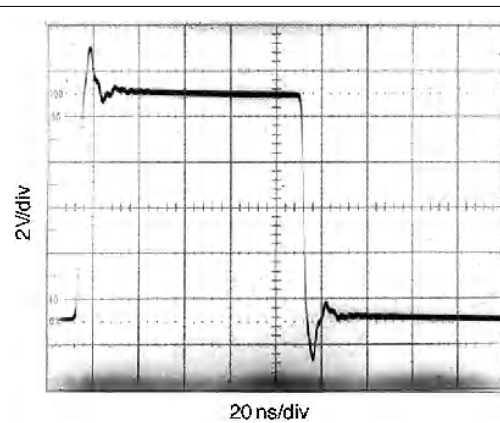
**Figure 7-2. Power Supply Bypassing**

### 7.1.3 Termination

In high-frequency applications, reflections occur if signals are not properly terminated. [Figure 7-3](#) shows a properly terminated signal and [Figure 7-4](#) shows an improperly terminated signal.



**Figure 7-3. Properly Terminated Signal**

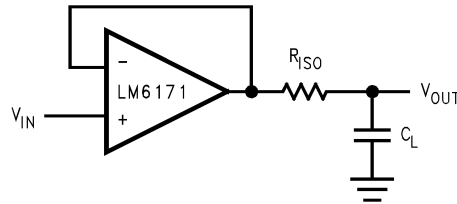


**Figure 7-4. Improperly Terminated Signal**

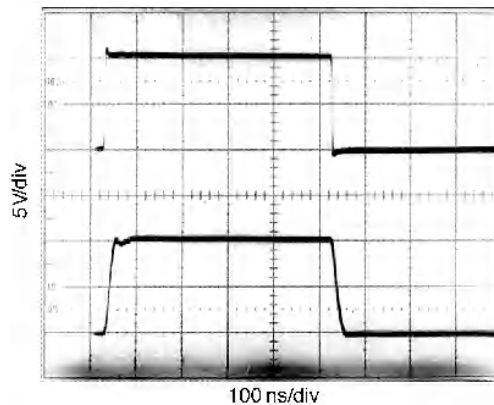
To minimize reflection, use coaxial cable with matching characteristic impedance to the signal source. Terminate the other end of the cable with the same value terminator or resistor. For commonly used cables, RG59 has a 75- $\Omega$  characteristic impedance, and RG58 has a 50- $\Omega$  characteristic impedance.

### 7.1.4 Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, place an isolation resistor as shown in [Figure 7-5](#). The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For the LM6171, a 50-Ω isolation resistor is recommended for initial evaluation. [Figure 7-6](#) shows the LM6171 driving a 200-pF load with the 50-Ω isolation resistor.



**Figure 7-5. Isolation Resistor Used to Drive Capacitive Load**



**Figure 7-6. The LM6171 Driving a 200-pF Load With a 50-Ω Isolation Resistor**

### 7.1.5 Using Probes

Active (FET) probes are an excellent choice for taking high-frequency measurements because of a wide bandwidth, high input impedance, and low input capacitance. However, the probe ground leads provide a long ground loop that produces errors in measurement. Instead, ground the probes directly by removing the ground leads and probe jackets and using scope probe jacks.

### 7.1.6 Components Selection and Feedback Resistor

In high-speed applications, keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface-mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high-speed amplifiers. For the LM6171, a feedback resistor of 510 Ω gives optimized performance.

## 7.2 Typical Applications

### 7.2.1 Fast Instrumentation Amplifier

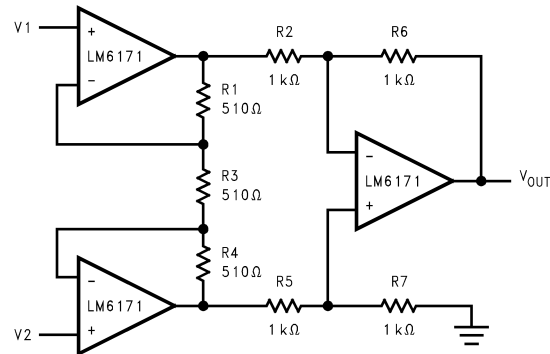


Figure 7-7. Fast Instrumentation Amplifier

$$V_{IN} = V2 - V1$$

if  $R6 = R2$ ,  $R7 = R5$  and  $R1 = R4$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R6}{R2} \left( 1 + 2 \frac{R1}{R3} \right) = 3$$

### 7.2.2 Multivibrator

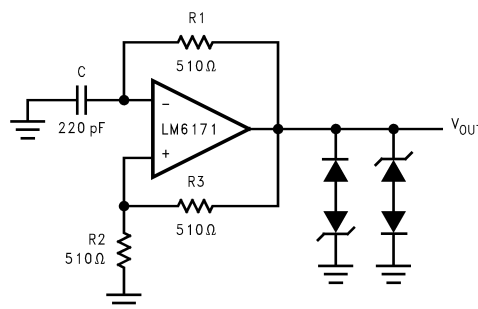


Figure 7-8. Multivibrator

$$f = \frac{1}{2 \left( R1C \ln \left[ 1 + 2 \frac{R2}{R3} \right] \right)}$$

$$f = 4 \text{ MHz}$$

### 7.2.3 Pulse Width Modulator

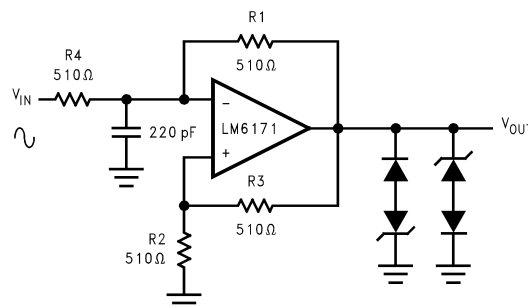


Figure 7-9. Pulse Width Modulator

## 7.3 Power Supply Recommendations

### 7.3.1 Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (2)$$

where

- $P_D$  is the power dissipation in a device
- $T_{J(max)}$  is the maximum junction temperature
- $T_A$  is the ambient temperature
- $\theta_{JA}$  is the thermal resistance of a particular package

For example, for the LM6171 in a SOIC-8 package, the maximum power dissipation at 25°C ambient temperature is 730 mW.

Thermal resistance,  $\theta_{JA}$ , depends on parameters such as die size, package size, and package material. The smaller the die size and package, the higher  $\theta_{JA}$  becomes. The 8-pin PDIP package has a lower thermal resistance (108°C/W) than the 8-pin SOIC-8 (172°C/W). Therefore, for higher dissipation capability, use an 8-pin PDIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L \quad (3)$$

where

- $P_Q$  = the quiescent power dissipated in a device with no load connected at the output.
  - $P_Q$  = supply current × total supply voltage with no load
- $P_L$  = the power dissipated in the device with a load connected at the output;  $P_L$  is not the power dissipated by the load.
  - $P_L$  = output current × (voltage difference between supply voltage and output voltage of the same supply)

For example, the total power dissipated by the LM6171 with  $V_S = \pm 15$  V, and the output voltage of 10 V into a 1-kΩ load resistor (one end tied to ground) is:

$$\begin{aligned} P_D &= P_Q + P_L \\ &= (2.5 \text{ mA}) \times (30 \text{ V}) + (10 \text{ mA}) \times (15 \text{ V} - 10 \text{ V}) \\ &= 75 \text{ mW} + 50 \text{ mW} \\ &= 125 \text{ mW} \end{aligned}$$

## 7.4 Layout

### 7.4.1 Layout Guidelines

#### 7.4.1.1 Printed Circuit Boards and High-Speed Op Amps

There are many things to consider when designing a printed circuit board (PCB) for high-speed op amps. Without proper caution, excessive ringing, oscillation, and other degraded ac performance in high-speed circuits can be frustrating. As a rule, keep the signal traces short and wide to provide low inductance and low-impedance paths. Ground any unused board space to reduce stray signal pickup. Also ground any critical components at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. If possible, solder the amplifier directly into the PCB without using any socket.

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.3 Trademarks

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PAL® is a registered trademark of and used under license from Advanced Micro Devices, Inc..

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### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (March 2013) to Revision D (November 2023)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added the <i>Pin Configuration and Functions, Specifications, ESD Ratings, Thermal Information, Detailed Description, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information</i> sections.....	1
• Changed wide unity-gain bandwidth product from 100 MHz to 76 MHz in <i>Features</i> .....	1
• Changed –3-dB frequency from 62 MHz to 75 MHz in <i>Features</i> .....	1
• Deleted text stating that LM6171 is developed in TI's vertically integrated process.....	1
• Changed <i>Operating Ratings</i> to <i>Recommended Operating Conditions</i> and moved Thermal Resistance content to new <i>Thermal Information</i> section .....	3
• Deleted ESD information and footnote from <i>Absolute Maximum Ratings</i> and moved to <i>ESD Ratings</i> .....	3
• Deleted footnote from <i>Recommended Operating Conditions</i> .....	3
• Changed DC and AC specifications tables to <i>Electrical Characteristics: ±15 V</i> .....	4
• Changed LM6171A unity-gain bandwidth from 100 MHz to 76 MHz in <i>Electrical Characteristics: ±15 V</i> .....	4
• Changed LM6171A –3-dB freq for $A_V = +1$ from 160 MHz to 200 MHz in <i>Electrical Characteristics: ±15 V</i> ....	4
• Changed LM6171A –3-dB freq for $A_V = +2$ from 62 MHz to 75 MHz in <i>Electrical Characteristics: ±15 V</i> .....	4
• Changed LM6171A phase margin from 40° to 58° in <i>Electrical Characteristics: ±15 V</i> .....	4
• Changed LM6171A settling time from 48 ns to 21 ns in <i>Electrical Characteristics: ±15 V</i> .....	4
• Changed LM6171A propagation delay from 6 ns to 4.1 ns in <i>Electrical Characteristics: ±15 V</i> .....	4
• Changed 5 V DC and AC specifications tables to <i>Electrical Characteristics: ±5 V</i> .....	6
• Changed LM6171A input common-mode voltage from ±3.7 V to ±3.2 V in <i>Electrical Characteristics: ±5 V</i> .....	6
• Changed LM6171A –3-dB frequency for $A_V = +1$ from 130 MHz to 190 MHz in <i>Electrical Characteristics: ±5 V</i> .....	6
• Changed LM6171A –3-dB frequency for $A_V = +2$ from 45 MHz to 75 MHz in <i>Electrical Characteristics: ±5 V</i> .	6
• Changed LM6171A settling time from 60 ns to 25 ns in <i>Electrical Characteristics: ±5 V</i> .....	6
• Changed LM6171A propagation delay from 8 ns to 4.5 ns in <i>Electrical Characteristics: ±5 V</i> .....	6
• Added new <i>Typical Characteristics</i> section for LM6171A.....	8
<hr/>	
<b>Changes from Revision B (March 2013) to Revision C (March 2013)</b>	<b>Page</b>
• Changed National Semiconductor data-sheet layout to Texas Instruments format.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6171AIM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM61 71AIM	
LM6171AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(L61AIM, LM61) 71AIM	Samples
LM6171BIM/NOPB	LIFEBUY	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM61 71BIM	
LM6171BIMX/NOPB	LIFEBUY	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM61 71BIM	
LM6171BIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LM6171 BIN	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

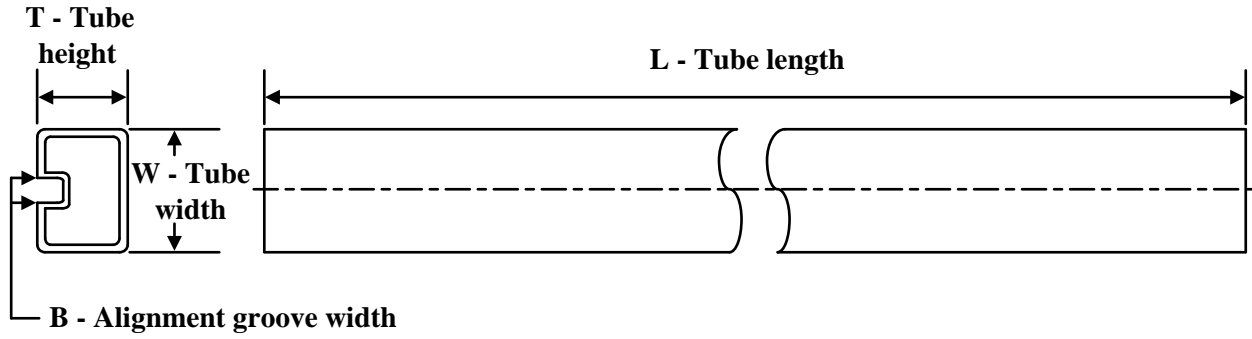

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6171AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM6171BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6171AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM6171BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM6171AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM6171BIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM6171BIN/NOPB	P	PDIP	8	40	502	14	11938	4.32



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

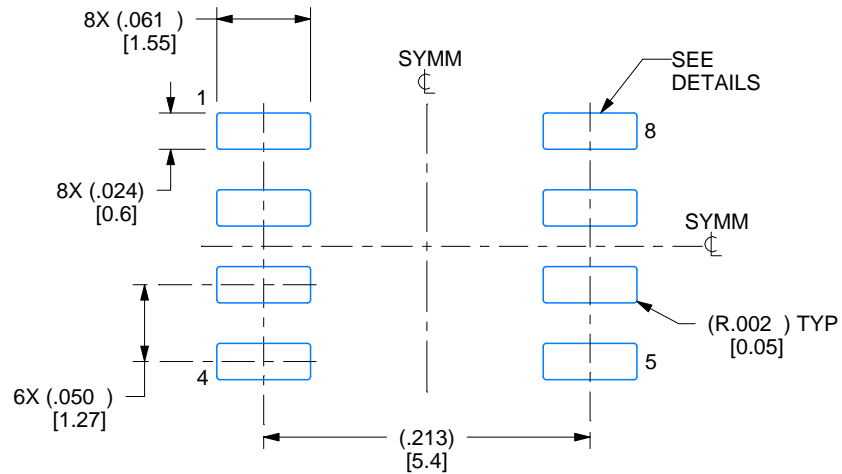
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

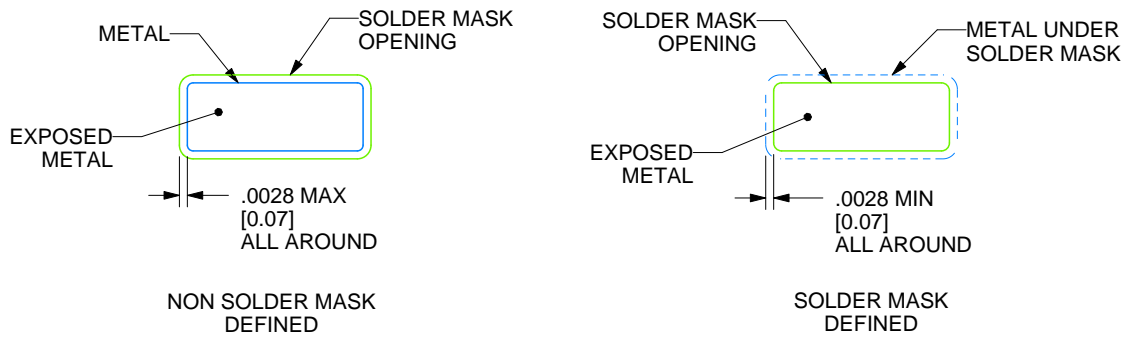
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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