



**THE DATASHEET OF
ESD5205P6T6G**



ESD5205

ESD Protection Diodes

Low Capacitance ESD Protection Diode for High Speed Data Line

The ESD5205 surge protection is designed to protect high speed data lines from ESD. Low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

Features

- Protection for the Following IEC Standards:
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- This is a Pb-Free Device

Typical Applications

- μ SD Connector

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|------------|----------------------|------------------|
| Peak Power Dissipation, 8 x 20 μs | P_{PK} | 18 | W |
| Operating Junction Temperature Range | T_J | -55 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Lead Solder Temperature – Maximum (10 Seconds) | T_L | 260 | $^\circ\text{C}$ |
| IEC 61000-4-2 Contact (ESD) IEC 61000-4-2 Air (ESD) | ESD ESD | ± 15 ± 15 | kV kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.



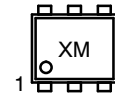
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MARKING DIAGRAM

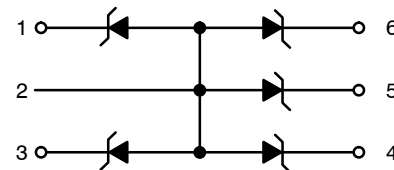


SOT-963
CASE 527AD



X = Specific Device Code
M = Month Code

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

| Device | Package | Shipping |
|--------------|----------------------|-----------------------|
| ESD5205P6T6G | SOT-963 (Pb-Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ESD5205

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|-----------|--|---------------------|------------------------------|---------|---------------|
| Reverse Working Voltage | V_{RWM} | I/O Pin to GND | | | 5.0 | V |
| Breakdown Voltage | V_{BR} | $I_T = 1\text{ mA}$, I/O Pin to GND | 5.5 | | | V |
| Reverse Leakage Current | I_R | $V_{RWM} = 5\text{ V}$, I/O Pin to GND | | | 1.0 | μA |
| Clamping Voltage (Note 1) | V_C | $I_{PP} = 1\text{ A}$, I/O Pin to GND (8 x 20 μs pulse) $I_{PP} = 2\text{ A}$, I/O Pin to GND (8 x 20 μs pulse) | | | 9 10 | V |
| Clamping Voltage (Note 2) | V_C | IEC61000-4-2, $\pm 8\text{ KV}$ Contact | See Figures 1 and 2 | | | V |
| Clamping Voltage TLP (Note 3) | V_C | $I_{PP} = 8\text{ A}$ $I_{PP} = 16\text{ A}$ $I_{PP} = -8\text{ A}$ $I_{PP} = -16\text{ A}$ | | 11.4 15.6 -4.5 -8.1 | | |
| Junction Capacitance | C_J | $V_R = 0\text{ V}$, $f = 1\text{ MHz}$ between I/O Pins and GND | | | 9.0 | pF |

- Surge current waveform per Figure 5.
- For test procedure see Figures 3 and 4 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 4\text{ ns}$, averaging window; $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$.

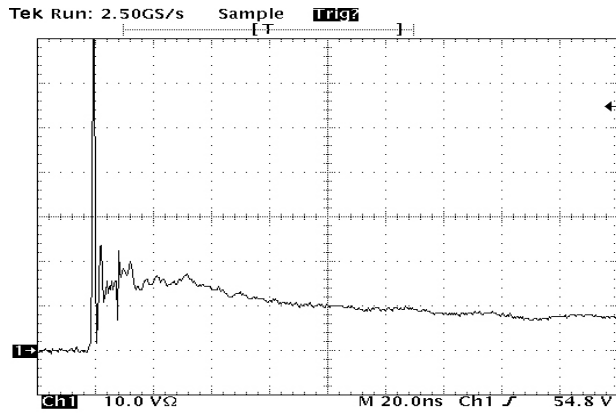


Figure 1. IEC61000-4-2 +8 KV Contact Clamping Voltage

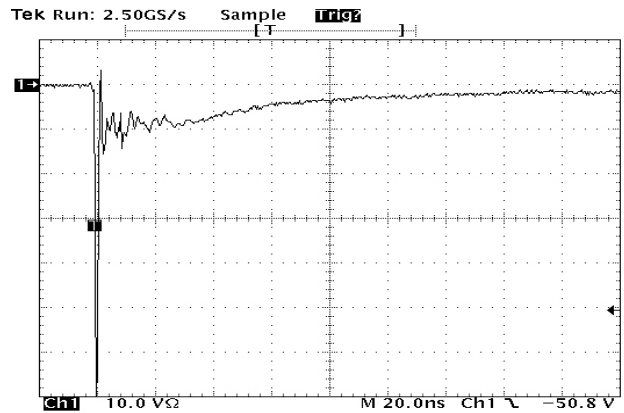


Figure 2. IEC61000-4-2 -8 KV Contact Clamping Voltage

ESD5205

IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |



Figure 3. IEC61000-4-2 Spec

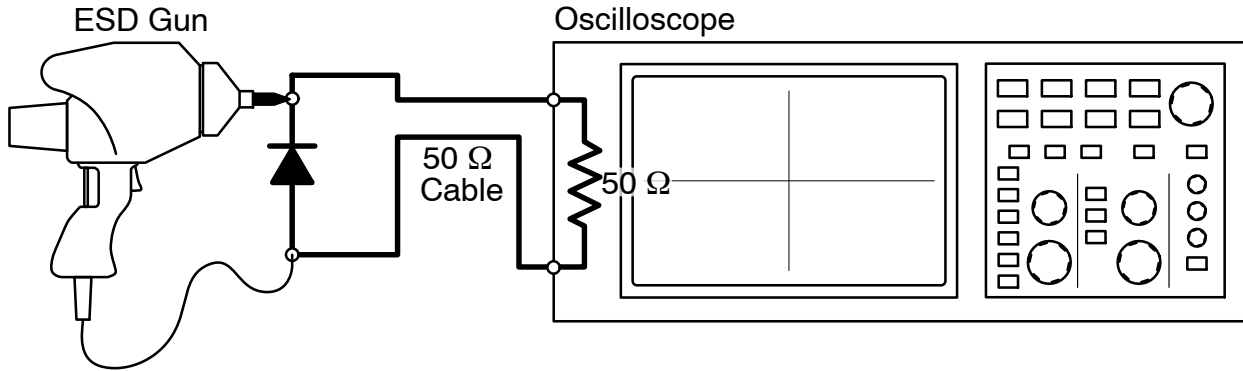


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

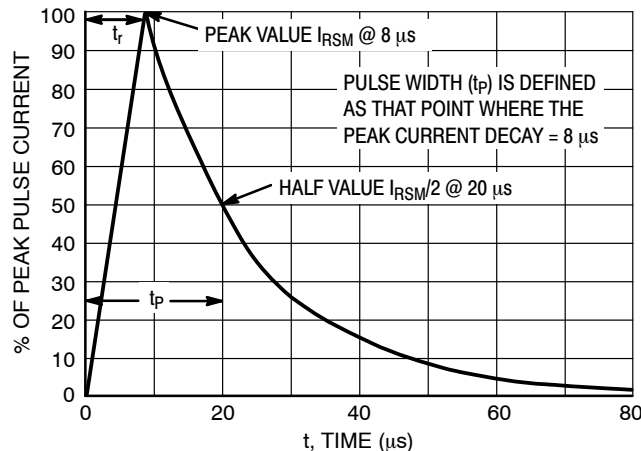
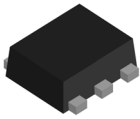


Figure 5. 8 X 20 μs Pulse Waveform

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

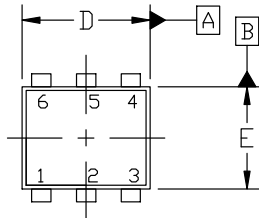


SOT-963 1.00x1.00x0.37, 0.35P
CASE 527AD
ISSUE F

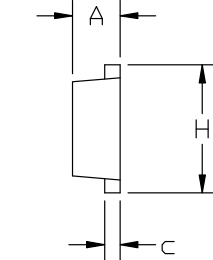
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NOTES:

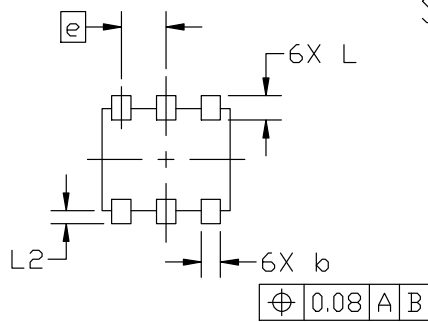
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



TOP VIEW

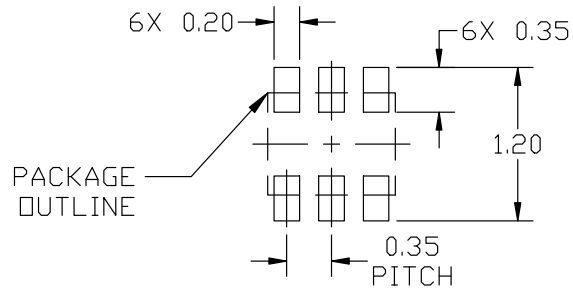


SIDE VIEW



BOTTOM VIEW

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| c | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H | 0.95 | 1.00 | 1.05 |
| L | 0.19 REF | | |
| L2 | 0.05 | 0.10 | 0.15 |

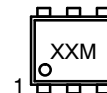


RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

- | | | |
|--|---|--|
| <p>STYLE 1: PIN 1. EMITTER 1 2. BASE 1 3. COLLECTOR 2 4. EMITTER 2 5. BASE 2 6. COLLECTOR 1</p> | <p>STYLE 2: PIN 1. EMITTER 1 2. EMITTER2 3. BASE 2 4. COLLECTOR 2 5. BASE 1 6. COLLECTOR 1</p> | <p>STYLE 3: PIN 1. CATHODE 1 2. CATHODE 1 3. ANODE/ANODE 2 4. CATHODE 2 5. CATHODE 2 6. ANODE/ANODE 1</p> |
| <p>STYLE 4: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR</p> | <p>STYLE 5: PIN 1. CATHODE 2. CATHODE 3. ANODE 4. ANODE 5. CATHODE 6. CATHODE</p> | <p>STYLE 6: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE</p> |
| <p>STYLE 7: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. ANODE 6. CATHODE</p> | <p>STYLE 8: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN</p> | <p>STYLE 9: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1</p> |
| <p>STYLE 10: PIN 1. CATHODE 1 2. N/C 3. CATHODE 2 4. ANODE 2 5. N/C 6. ANODE 1</p> | | |

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
 M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|--------------------------------------|--|
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