



# THE DATASHEET OF TEA2208T/1J





# TEA2208T

Active bridge rectifier controller

Rev. 1.4 — 14 April 2021

Product data sheet

## 1 General description

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The TEA2208T is the first product of a new generation of active bridge rectifier controllers replacing the traditional diode bridge.

Using the TEA2208T with low-ohmic high-voltage external MOSFETs significantly improves the efficiency of the power converter as the typical rectifier diode-forward conduction losses are eliminated. Efficiency can improve up to about 1.4 % at 90 V (AC) mains voltage.

The TEA2208T is designed in a silicon-on insulator (SOI) process.

## 2 Features and benefits

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### 2.1 Efficiency features

- Forward conduction losses of the diode rectifier bridge are eliminated
- Very low IC power consumption (2 mW).

### 2.2 Application features

- Integrated high-voltage level shifters
- Directly drives all four rectifier MOSFETs
- Very low external part count
- Integrated X-capacitor discharge (2 mA)
- Self-supplying
- Full-wave drive improving total harmonic distortion (THD)
- S014 package

### 2.3 Control features

- Undervoltage lockout (UVLO) for high-side and low-side drivers
- Drain-source overvoltage protection for all external power MOSFETs
- Gate pull-down currents at start-up for all external power MOSFETs



### 3 Applications

The TEA2208T is intended for power supplies with a boost-type power-factor controller as a first stage. The second stage can be a resonant controller, a flyback controller, or any other controller topology. It can be used in all power supplies requiring high efficiency:

- Adapters
- Power supplies for desktop PC and all-in-one PC
- Power supplies for television
- Power supplies for servers

### 4 Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
TEA2208T/1	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

### 5 Marking

Table 2. Marking

Type number	Marking code
TEA2208T/1	TEA2208T

### 6 Block diagram

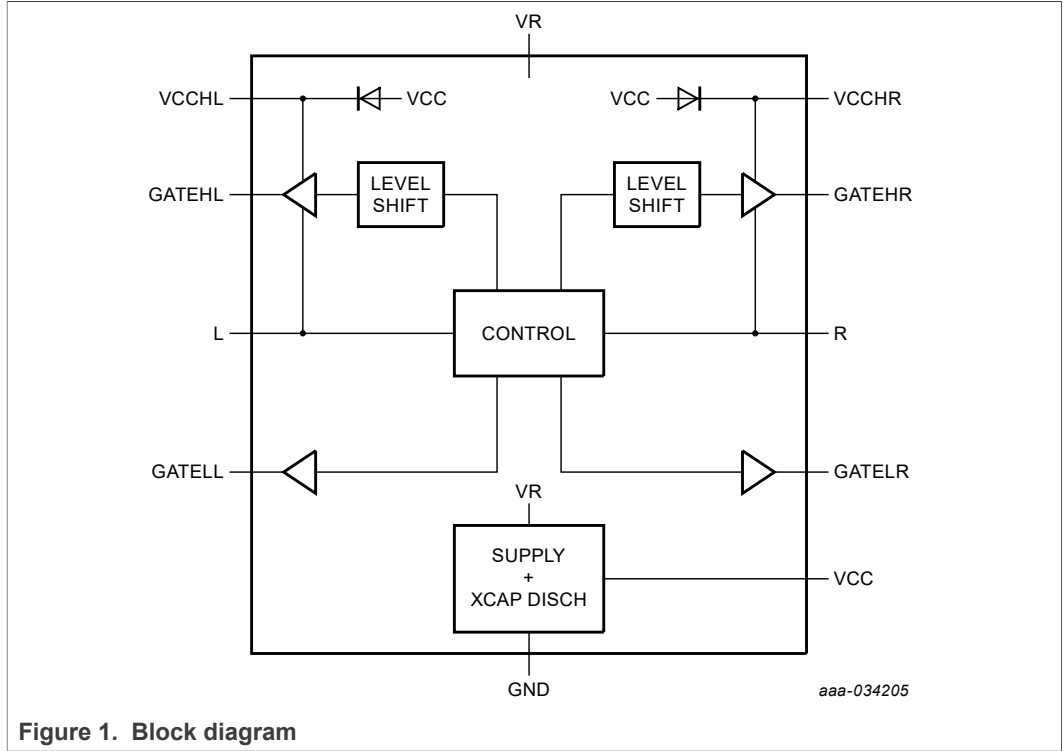


Figure 1. Block diagram

### 7 Pinning information

#### 7.1 Pinning

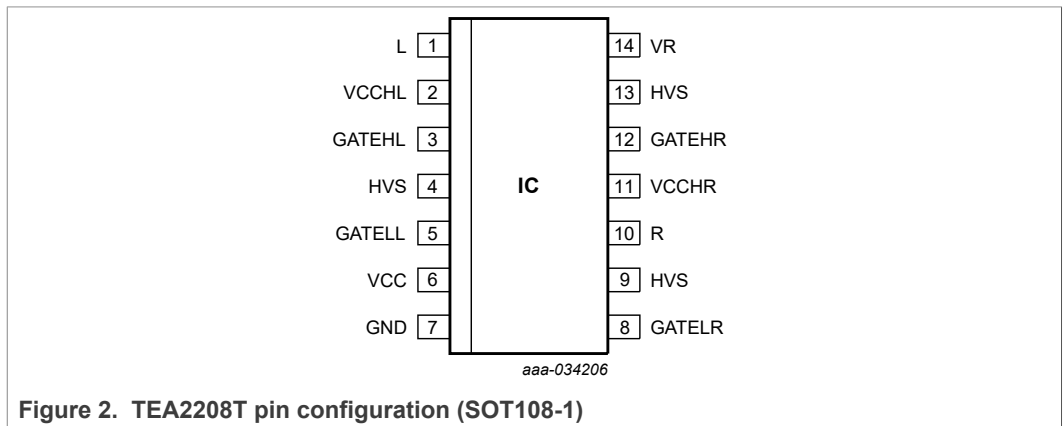


Figure 2. TEA2208T pin configuration (SOT108-1)

## 7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
L	1	left input, source of upper-left MOSFET
VCCHL	2	left high-side floating supply
GATEHL	3	gate driver left high side
HVS	4	high-voltage spacer; not to be connected
GATELL	5	gate driver left low side
VCC	6	supply voltage
GND	7	ground
GATELR	8	gate driver right low side
HVS	9	high-voltage spacer; not to be connected
R	10	right input, source of upper-right MOSFET
VCCHR	11	right high-side floating supply
GATEHR	12	gate driver right high side
HVS	13	high-voltage spacer; not to be connected
VR	14	rectified mains voltage

## 8 Functional description

### 8.1 Introduction

The TEA2208T is a controller IC for an active bridge rectifier. It can directly drive the four MOSFETs in an active bridge. Figure 3 shows a typical configuration. Since the output is a rectified sine wave, a boost-type power-factor circuit must follow the application.

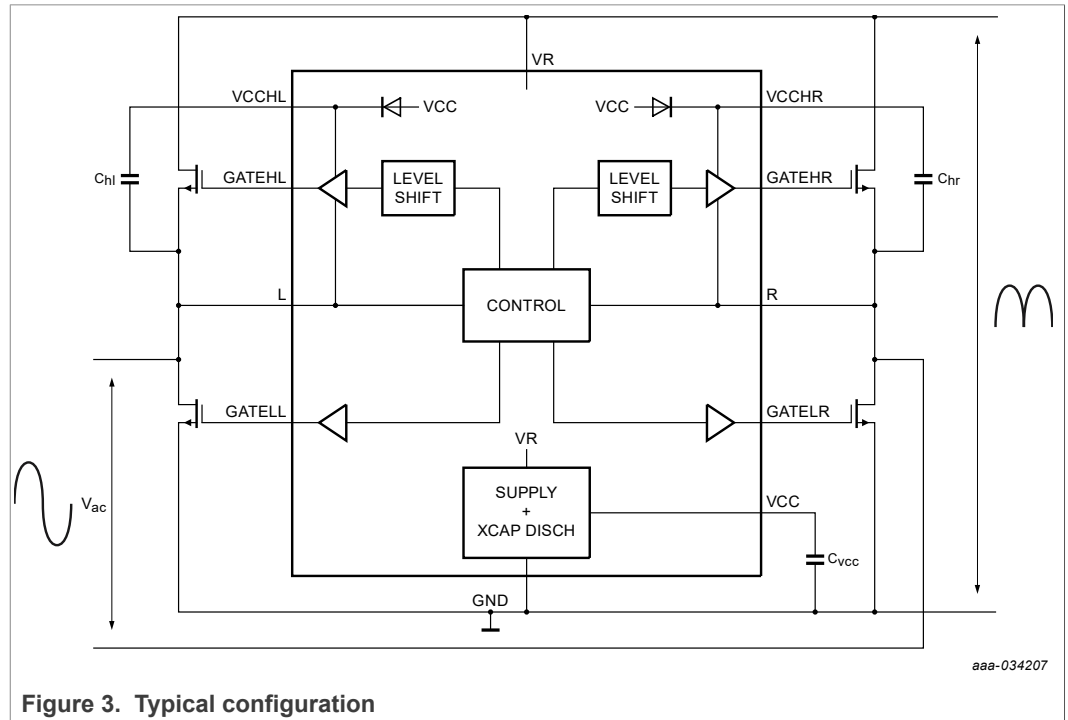


Figure 3. Typical configuration

### 8.2 Operation

The control circuit of the TEA2208T senses the polarity of the mains voltage between pins L and R. Depending on the polarity, diagonal pairs of power MOSFETs are switched on or off. Depending on the slope polarity, the comparator in the control circuit, which compares the L and R voltages, has thresholds of 250 mV and -250 mV.

The gate drivers are high-current rail-to-rail MOS output drivers. An on-chip supply circuit which draws current from the rectified sine-wave pin VR generates the gate driver voltage. After a zero-crossing of the mains voltage, the supply capacitor  $C_{VCC}$  is charged to the regulation level  $V_{reg}$ . Then the discharge state is entered. The resulting power dissipation from the mains voltage is about 1 mW, excluding gate charge losses of the external power MOSFETs. These gate charge losses typically add a 1 mW dissipation.

At start-up, the body diodes of the power MOSFETs act as a traditional diode bridge. They cause a peak rectified voltage at pin VR. From this high voltage, the supply capacitor is first charged to the  $V_{start}$  voltage and then enters the start-up state. After a next zero-crossing of the mains voltage, the supply capacitor is charged to  $V_{reg}$  in the charging state. When the voltage at the supply capacitor exceeds  $V_{disable}$ , the gate driver outputs are enabled. The high-side drivers start up later than the low-side drivers. The floating supplies must first be charged and the drain-source voltage of the high-side power MOSFETs must be less than the drain-source protection voltage. When all drivers

are active, the MOSFETs take over the role of the diodes. The result is a much lower power loss than a passive diode rectifier bridge.

In the discharge state, when the mains voltage is disconnected, the internal bias current discharges the supply capacitor. When the voltage at pin VCC drops to below  $V_{disable}$  the X-capacitor discharge state is entered, which draws a 2 mA current from pin VR to discharge the X-capacitor. The waiting time,  $t_d$  until the X-capacitor discharge starts is:

$$T_{delay} = C_{VCC} * (V_{reg} - V_{disable}) / 20 \text{ uA} = 200k * C_{VCC} \tag{1}$$

Using a typical value of 2.2  $\mu\text{F}$  for  $C_{VCC}$  yields about 0.45 s. While the VR pin discharges the X-capacitor, the mains can be reconnected. In that case, the charge mode is entered again.

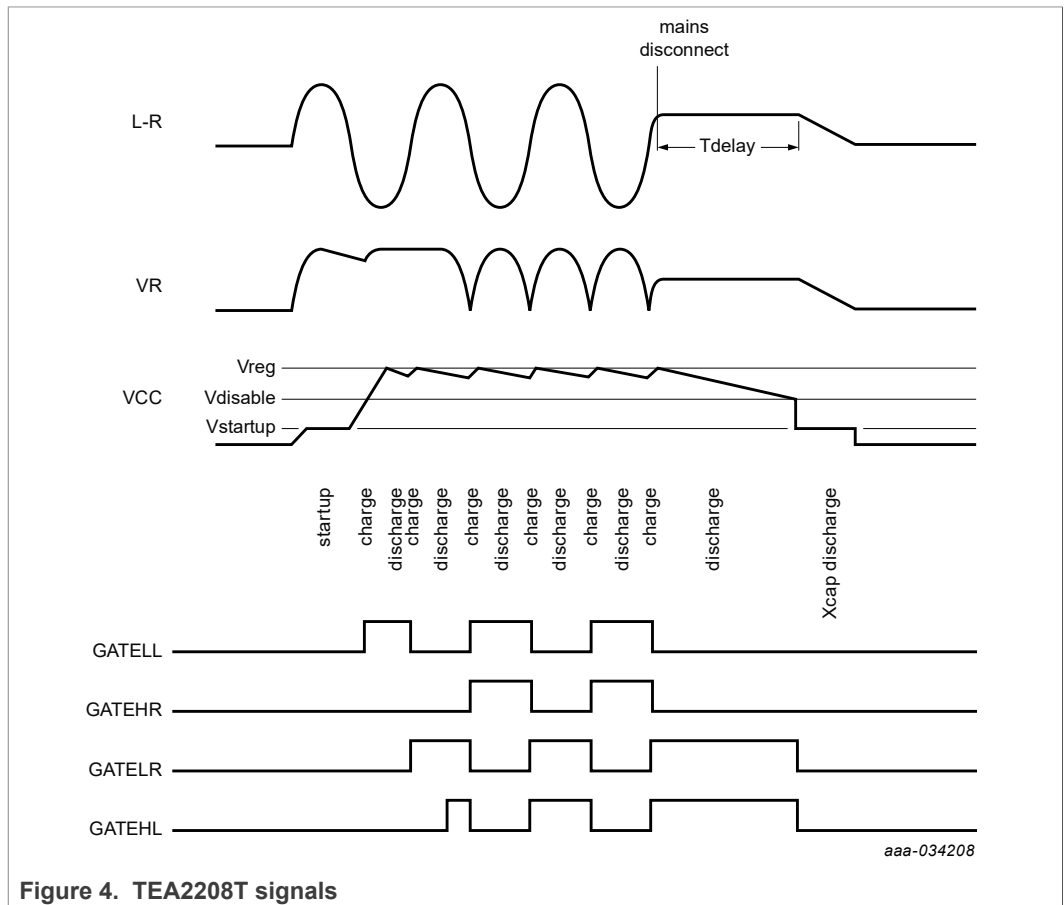


Figure 4. TEA2208T signals

Table 4. TEA2208T states

State	Description	I <sub>VR</sub>	I <sub>VCC</sub>
start-up	supply capacitor kept stable at 4.8 V	2 mA	0
charge	supply capacitor is charged from pin VR with 2 mA	+2 mA	-2 mA
discharge	Internal bias currents and gate charge losses discharge the supply capacitor	1 $\mu$ A	20 $\mu$ A
X-capacitor discharge	supply capacitor and X-capacitor at pin VR are discharged by 2 mA	2 mA	-2 mA

### 8.3 Protections

#### 8.3.1 Gate pull-down

All gate driver outputs have a pull-down circuit. It ensures that, if a driver supply voltage is lower than the undervoltage lockout level, the discharge of the gate driver output discharges to less than 2 V.

#### 8.3.2 Power MOSFET drain-source protection

If the drain-source voltage of the external power MOSFET exceeds  $V_{CC} - 2$  V (low-side),  $V_{CCHL} - 3.5$  V (high-side left), or  $V_{CCHR} - 3.5$  V (high-side right), all gate driver outputs are disabled. Disabling the gate driver outputs avoids high dissipation and high current peaks in the power MOSFETs during start-up.

#### 8.3.3 Minimum mains voltage

Only when the voltage at either node L or R exceeds 22 V, the charge state is entered.

## 9 Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 7). Positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated. Current ratings are valid provided the other ratings are not violated.*

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Voltages</b>					
V <sub>VR</sub>	voltage on pin VR	operating	-0.4	440	V
		mains transient: maximum 10 minutes over lifetime	-0.4	700	V
V <sub>VCCHL</sub>	voltage on pin VCCHL	operating	-0.4	440	V
		mains transient: maximum 10 minutes over lifetime	-0.4	700	V
V <sub>VCCHR</sub>	voltage on pin VCCHR	operating	-0.4	440	V
		mains transient: maximum 10 minutes over lifetime	-0.4	700	V
V <sub>L</sub>	voltage on pin L	operating	-5	+440	V
		mains transient: maximum 10 minutes over lifetime	-5	+700	V
V <sub>R</sub>	voltage on pin R	operating	-5	+440	V
		mains transient: maximum 10 minutes over lifetime	-5	+700	V
ΔV <sub>(VR-L)</sub>	voltage difference between pins VR and L	operating	-10	+440	V
		mains transient: maximum 10 minutes over lifetime	-10	+700	V
ΔV <sub>(VR-R)</sub>	voltage difference between pins VR and R	operating	-10	+440	V
		mains transient: maximum 10 minutes over lifetime	-10	+700	V
V <sub>GATEHR</sub>	voltage on pin GATEHR	operating	-5	+440	V
		mains transient: maximum 10 minutes over lifetime	-5	+700	V
V <sub>GATEHL</sub>	voltage on pin GATEHL	operating	-5	+440	V
		mains transient: maximum 10 minutes over lifetime	-5	+700	V

**Table 5. Limiting values...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 7). Positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated. Current ratings are valid provided the other ratings are not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
SR <sub>max</sub>	maximum slew rate	pins VR, L, R, VCCHL, VCCHR, GATEHL, GATEHR	-	50	V/ns
V <sub>VCC</sub>	voltage on pin VCC		-0.4	14	V
V <sub>GATELR</sub>	voltage on pin GATELR		-0.4	14	V
V <sub>GATELL</sub>	voltage on pin GATELL		-0.4	14	V
V <sub>DD(float)</sub>	Float supply voltage	pins GATEHL-L, GATEHR-R, VCCHR-R, VCCHL-L	-0.4	14	V
<b>General</b>					
T <sub>j</sub>	junction temperature		-40	+125	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C
<b>Electrostatic discharge (ESD)</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	human body model (HBM)			
		pins: VR, L,R,VCCHL, VCCHR, GATEHL, and GATEHR	-1000	+1000	V
		other pins	-2000	+2000	V
		charge device model (CDM)	-500	+500	V

## 10 Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-c)</sub>	thermal resistance from junction to case	in free air <sup>[1]</sup>	43	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air; 1-layer PCB <sup>[1]</sup>	143	K/W
		in free air; 4-layer PCB; JEDEC test board <sup>[1]</sup>	105	K/W

[1] Given thermal resistance values are based on simulation results.

## 11 Characteristics

Table 7. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>VR pin</b>						
$I_{on}$	on-state current	Charging state; X-capacitor discharge state; start-up state	1.5	2	2.75	mA
$I_{off}$	off-state current	discharge state	0.5	0.8	1.2	$\mu\text{A}$
$V_{start}$	start voltage	high-voltage start-up	9	-	-	V
<b>VCC pin</b>						
$I_{dch}$	discharge current	X-capacitor discharge	3	4	5.5	mA
$I_{bias}$	bias current	discharge state	15	20	30	$\mu\text{A}$
$I_{ch}$	charge current	charge state	1.5	2	2.75	mA
$V_{UVLO}$	undervoltage lockout voltage		3.6	4.2	4.9	V
$V_{startup}$	start-up voltage	start-up state	4.3	4.8	5.3	V
$V_{dis}$	disable voltage	high level	9.2	9.7	10.2	V
		hysteresis	1.1	1.5	1.8	V
$V_{regd}$	regulated output voltage		11.4	12	12.8	V
<b>Floating supply pins (VCCHL, VCCHR)</b>						
$I_{I(VCCHL)}$	input current on pin VCCHL	$V_L = 0\text{ V}$	1.4	1.8	2.5	$\mu\text{A}$
		$V_L = 200\text{ V}$	4	7	12	$\mu\text{A}$
$I_{I(VCCHR)}$	input current on pin VCCHR	$V_R = 0\text{ V}$	1.4	1.8	2.5	$\mu\text{A}$
		$V_R = 200\text{ V}$	4	7	12	$\mu\text{A}$
$V_{DD(float)UVLO}$	float supply undervoltage lockout voltage		3.6	4.2	5.0	V
$V_{d(bs)}$	bootstrap diode voltage	current on diode = 1 mA	0.8	1	1.3	V
<b>Gate driver output pins (GATELL, GATELR, GATEHL, GATEHR)</b>						
$I_{source}$	source current	$V_{VCC} = 12\text{ V};$ $V_{GATELL} = V_{GATEHL} = 6\text{ V};$ $V_{GATELR} = V_{GATEHR} = 6\text{ V}$	[1] 125	200	400	mA
$I_{sink}$	sink current	$V_{VCC} = 12\text{ V};$ $V_{GATELL} = V_{GATEHL} = 6\text{ V};$ $V_{GATELR} = V_{GATEHR} = 6\text{ V}$	[1] 150	200	500	mA
$I_{pd}$	pull-down current	off-state current; $V_{VCC} = 2\text{ V};$ $V_{GATELL} = V_{GATEHL} = 2\text{ V};$ $V_{GATELR} = V_{GATEHR} = 2\text{ V}$	100	200	250	$\mu\text{A}$
$R_{on}$	on-state resistance		11	15	20	$\Omega$
$R_{off}$	off-state resistance		7	10	14	$\Omega$

Table 7. Characteristics...continued

$T_{amb} = 25\text{ °C}$ ; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>prot(G)</sub>	gate driver protection voltage	VR-VCCHR; VR-VCCHL	-5	-3.5	-2	V
		L-VCC; R-VCC	-3	-2.3	-1	V
<b>Control circuit (pin L and R)</b>						
V <sub>th</sub>	threshold voltage	peak detector threshold voltage	15	22	32	V
I <sub>det</sub>	detection current	peak detector current	0.4	0.5	0.6	μA
V <sub>offset</sub>	offset voltage	zero-crossing comparator offset voltage	150	250	350	mV
t <sub>d</sub>	delay time	zero-crossing comparator delay time				
		dV/dt = 0.1 V/μs <sup>[2]</sup>	1200	1500	2500	ns
		dV/dt = 10 V/μs <sup>[2]</sup>	550	700	1200	ns

[1] Covered by correlating measurement.

[2] Covered by design and validation.

## 12 Application information

A switched-mode power supply (SMPS) with the TEA2208T typically consists of a mains filter in front of the TEA2208T followed by a boost-type power factor controller. A resonant controller, flyback controller, or any other topology can follow this boost-type PFC.

Special attention must be given to the connection of the VR, L, and R pins of the TEA2208T. Mains transients or surges must be limited to voltages below 700 V. Placing an additional metal-oxide varistor (MOV) after the mains filter may be required. Adding diodes from pins L and R to the boost capacitor of the boost-type PFC may also be necessary. As mains transient currents can be high, the PCB tracks must have a suitable width. Inductance (track length) must be minimized.

Typical values for the three external capacitors are 1  $\mu\text{F}$  to 2.2  $\mu\text{F}$  (supply capacitor) and 100 nF to 220 nF (bootstrap capacitors). Supply capacitors with higher values increase the delay time ( $t_d$ ) for the X-capacitor discharge. They may also increase the dissipation because the supply capacitor  $C_{VCC}$  may not be charged every half-mains cycle. Bootstrap capacitors with lower value may cause a voltage drop that is too high because of the gate charge losses.

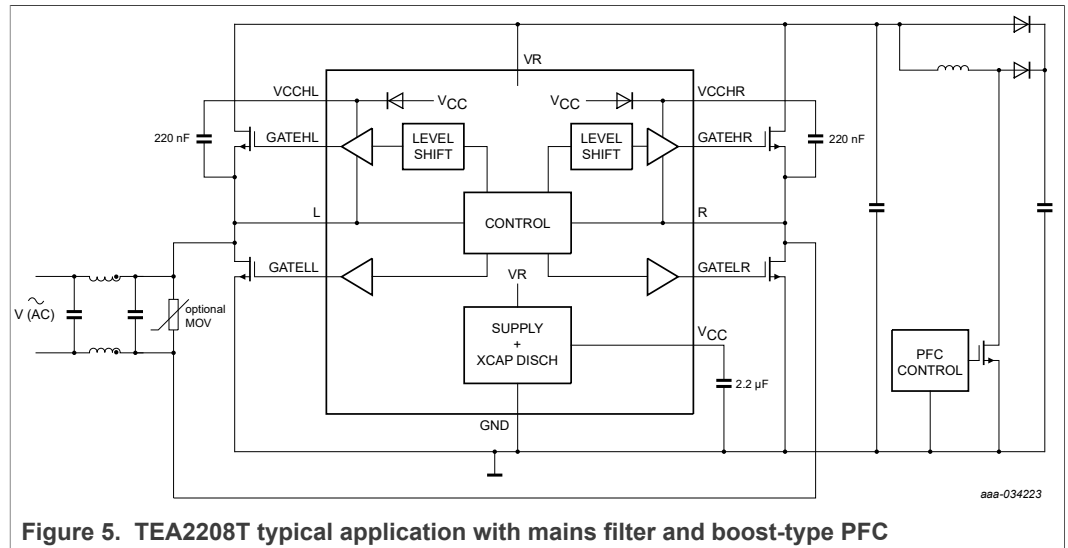


Figure 5. TEA2208T typical application with mains filter and boost-type PFC

13 Package outline

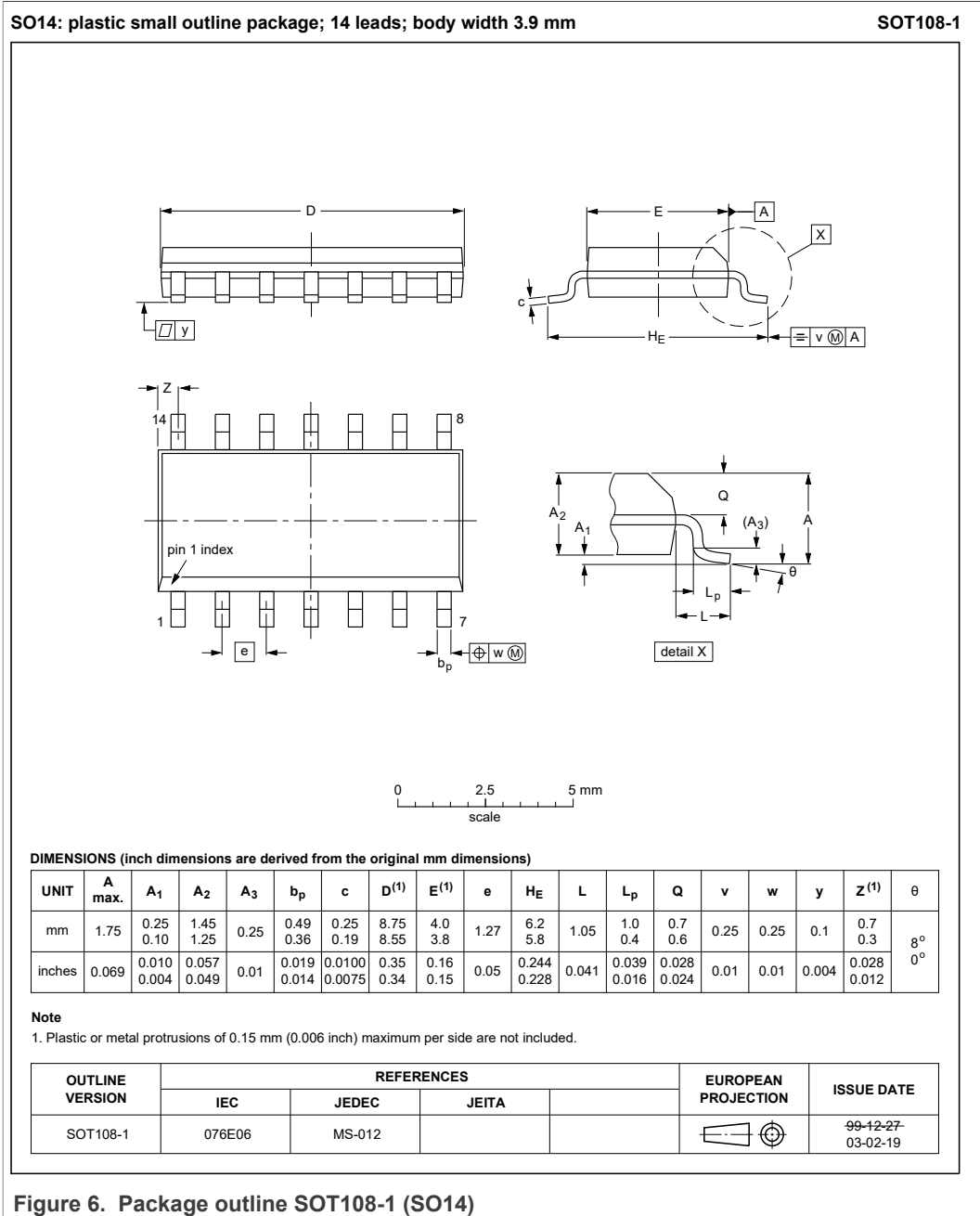


Figure 6. Package outline SOT108-1 (SO14)

## 14 Abbreviations

Table 8. Abbreviations

Acronym	Description
CDM	change device model
ESD	electrostatic discharge
HBM	human body model
MOSFET	metal–oxide–semiconductor field-effect transistor
MOV	metal-oxide varistor
PFC	power-factor controller
SMPS	switched-mode power supply
SOI	silicon-on insulator
THD	total harmonic distortion
UVLO	undervoltage lockout

## 15 Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA2208T v.1.4	20210414	Product data sheet	-	TEA2208T v.1.3
Modifications:	• <a href="#">Section 11</a> "Characteristics" has been updated.			
TEA2208T v.1.3	20201216	Product data sheet	-	TEA2208T v.1.2
TEA2208T v.1.2	20201029	Product data sheet	-	TEA2208T v.1.1
TEA2208T v.1.1	20200325	Product data sheet	-	TEA2208T v.1
TEA2208T v.1	20191019	Product data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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