THE DATASHEET OF

DS90UR907QSQ/NOPB

DS90UR907Q-Q1 5 to 65-MHz, 24-Bit Color FPD-Link to FPD-Link II Converter

1 Features

- 5-MHz to 65-MHz Support (140-Mbps to 1.82-Gbps Serial Link)
- 5-Channel (4 data + 1 clock) FPD-Link Receiver Inputs
- AC-Coupled STP Interconnect up to 10 Meters in Length
- Integrated Output Termination
- At Speed Link BIST Mode
- Optional I^2C Compatible Serial Control Bus
- RGB888 + VS, HS, DE support
- Power-Down Mode Minimizes Power Dissipation
- Randomizer/Scrambler – DC-Balanced Data Stream
- Low EMI FPD-Link Input
- Selectable Output VOD and Adjustable De-Emphasis
- 1.8-V or 3.3-V Compatible Control Bus Interface
- Automotive Grade Product: AEC-Q100 Grade 2 Qualified
- >8-kV HBM and ISO 10605 ESD Rating
- Backward Compatible Mode for Operation With Older Generation Devices

2 Applications

- Automotive Display for Navigation
- Automotive Display for Entertainment

3 Description

The DS90UR907Q-Q1 converts FPD-Link to FPD-Link II. It translates four LVDS data/control streams and one LVDS clock pair (FPD-Link) into a high-speed serialized interface (FPD-Link II) over a single pair. This serial bus scheme greatly eases system design by eliminating skew problems between clock and data, reduces the number of connector pins, reduces the interconnect size, weight, and cost, and overall eases PCB layout. In addition, internal DC balanced encoding is used to support AC-coupled interconnects.

The DS90UR907Q-Q1 converts, balances and level shifts four LVDS data/control streams, and embeds one LVDS clock pair (FPD-Link) to a serial stream (FPD-Link II). Up to 24 bits of RGB in the FPD-Link are serialized along with the three video control signals.

Serial transmission is optimized by a user selectable de-emphasis and differential output level select features. EMI is minimized by the use of low voltage differential signaling and spread spectrum clocking compatibility.

With fewer wires to the physical interface of the host, FPD-Link input with LVDS technology is ideal for high speed, low power and low EMI data transfer.

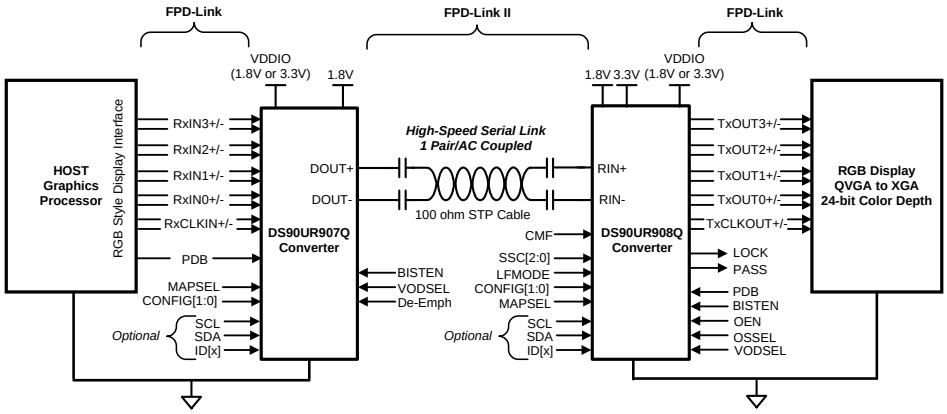
The device is offered in a 36-pin WQFN package and is specified over the automotive AEC-Q100 Grade 2 temperature range of –40˚C to 105˚C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UR907Q-Q1	WQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Applications Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2013) to Revision G — **Page**

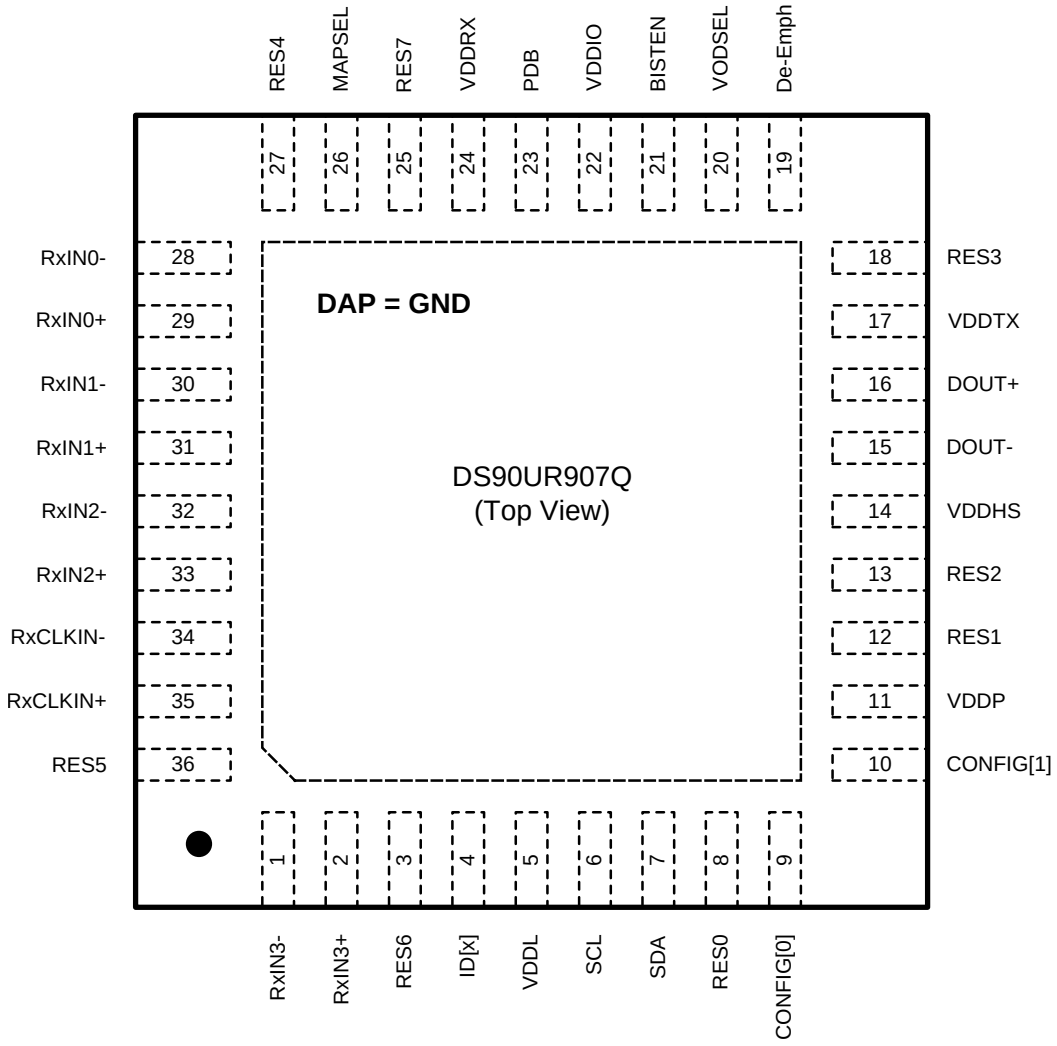
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted table note from *Pin Functions* ... 3
- Deleted 36L WQFN Package row from *Absolute Maximum Ratings* ... 5

Changes from Revision E (April 2013) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format ... 27

5 Pin Configuration and Functions

NJK Package
36-Pin WQFN
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
FPD-LINK INPUT INTERFACE			
RxIN[3:0]+	2, 33, 31, 29	I, LVDS	True LVDS Data Input This pair requires an external 100 Ω termination for standard LVDS levels.
RxIN[3:0]-	1, 34, 32, 30, 28	I, LVDS	Inverting LVDS Data Input This pair requires an external 100 Ω termination for standard LVDS levels.
RxCLKIN+	35	I, LVDS	True LVDS Clock Input This pair requires an external 100 Ω termination for standard LVDS levels.
RxCLKIN-	34	I, LVDS	Inverting LVDS Clock Input This pair requires an external 100 Ω termination for standard LVDS levels.

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
CONTROL AND CONFIGURATION			
PDB	23	I, LVCMOS w/ pulldown	Power-down Mode Input PDB = 1, Device is enabled (normal operation). Refer to *Power-Up Requirements and PDB Pin* in the Applications Information Section. PDB = 0, Device is powered down When the Device is in the power-down state, the driver outputs (DOUT+/-) are both logic high, the PLL is shutdown, IDD is minimized. Control Registers are **RESET**.
VODSEL	20	I, LVCMOS w/ pulldown	Differential Driver Output Voltage Select — Pin or Register Control VODSEL = 1, LVDS VOD is ±450 mV, 900 mVp-p (typical) — Long Cable / De-E Applications VODSEL = 0, LVDS VOD is ±300 mV, 600 mVp-p (typical)
De-Emph	19	I, Analog w/ pullup	De-Emphasis Control — Pin or Register Control De-Emph = open (float) - disabled To enable De-emphasis, tie a resistor from this pin to GND or control through register. See Table 3
MAPSEL	26	I, LVCMOS w/ pulldown	FPD-Link Map Select — Pin or Register Control MAPSEL = 1, MSB on RxIN3+/-. Figure 17 MAPSEL = 0, LSB on RxIN3+/-. Figure 16
CONFIG[1:0]	10, 9	I, LVCMOS w/ pulldown	Operating Modes Determine the device operating mode and interfacing device. Table 1 CONFIG[1:0] = 00: Interfacing to DS90UR906 or DS90UR908, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS90UR906 or DS90UR908, Control Signal Filter ENABLED CONFIG [1:0] = 10: Interfacing to DS90UR124, DS99R124 CONFIG [1:0] = 11: Interfacing to DS90C124
ID[x]	4	I, Analog	Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10-kΩ pullup to 1.8-V rail. See Table 5.
SCL	6	I, LVCMOS	Serial Control Bus Clock Input - Optional SCL requires an external pullup resistor to V_{DDIO}.
SDA	7	I/O, LVCMOS Open Drain	Serial Control Bus Data Input / Output - Optional SDA requires an external pullup resistor V_{DDIO}.
BISTEN	21	I, LVCMOS w/ pulldown	BIST Mode — Optional BISTEN = 1, BIST is enabled BISTEN = 0, BIST is disabled
RES[7:0]	25, 3, 36, 27, 18, 13, 12, 8	I, LVCMOS w/ pulldown	***Reserved*** - tie LOW
FPD-LINK II SERIAL INTERFACE			
DOUT+	16	O, LVDS	True Output. The output must be AC Coupled with a 100 nF capacitor.
DOUT-	15	O, LVDS	Inverting Output. The output must be AC Coupled with a 100 nF capacitor.
POWER AND GROUND			
VDDL	5	Power	Logic Power, 1.8 V ±5%
VDDP	11	Power	PLL Power, 1.8 V ±5%
VDDHS	14	Power	TX High Speed Logic Power, 1.8 V ±5%
VDDTX	17	Power	Output Driver Power, 1.8 V ±5%
VDDRX	24	Power	RX Power, 1.8 V ±5%
V_{DDIO}	22	Power	LVCMOS I/O Power and FPD-Link I/O Power **1.8 V ±5% OR 3.3 V ±10%**
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. **Connect to the ground plane** (GND) with at least 9 vias.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltage – V_{DDn} (1.8 V)	–0.3	2.5	V
Supply voltage – V_{DDIO}	−0.3	4	V
LVCMOS I/O voltage	−0.3	V_{DDIO} + 0.3	V
LVDS input voltage	−0.3	V_{DDIO} + 0.3	V
Driver output voltage	−0.3	V_{DDn} + 0.3	V
Junction temperature		150	°C
Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings—JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±8000	V
		Charged-device model (CDM), per AEC Q100-011	±1250	
		Machine model	±250	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC and ISO

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	R_D = 330 Ω, C_S = 150 pF	IEC, powered-up only contact discharge (R_{IN+}, R_{IN-})	≥±6000	V
			IEC, powered-up only air-gap discharge (R_{IN+}, R_{IN-})	≥±30000	
		R_D = 330 Ω, C_S = 150 and 330 pF	ISO10605 contact discharge (R_{IN+}, R_{IN-})	≥±8000	V
			ISO10605 air-gap discharge (R_{IN+}, R_{IN-})	≥±15000	
		R_D = 2 kΩ, C_S = 150 and 330 pF	ISO10605 contact discharge (R_{IN+}, R_{IN-})	≥±8000	V
			ISO10605 air-gap discharge (R_{IN+}, R_{IN-})	≥±15000	

6.4 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	3	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	25	105	°C
RxCLKIN Frequency	5		65	MHz
Supply Noise(1)			100	mV_{P-P}

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8 V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 750 kHz. The Des on the other hand shows no error when the noise frequency is less than 400 kHz.

6.5 Thermal Information

THERMAL METRIC[1]		DS90UR907Q-Q1 NJK (WQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.[1][2][3]

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
LVCMOS INPUT DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3 to 3.6 V		PDB, VODSEL, MAPSEL, CONFIG[1:0], BISTEN	2.2		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89 V			0.65* V_{DDIO}		V_{DDIO}	
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3 to 3.6 V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89 V			GND		0.35* V_{DDIO}	
I_{IN}	Input Current	V_{IN} = 0 V or V_{DDIO}	V_{DDIO} = 3 to 3.6 V		–15	±1	15	µA
			V_{DDIO} = 1.7 to 1.89 V		–15	±1	15	
FPD-LINK LVDS RECEIVER DC SPECIFICATIONS								
V_{TH}	Differential Threshold High Voltage	V_{CM} = 1.2 V, Figure 1		RxIN[3:0]+/-, RxCLKIN+/-,			100	mV
V_{TL}	Differential Threshold Low Voltage				–100			
$\|V_{ID}\|$	Differential Input Voltage Swing				200		600	mV
V_{CM}	Common Mode Voltage	V_{DDIO} = 3.3 V			0	1.2	2.4	V
		V_{DDIO} = 1.8 V			0	1.2	1.55	
I_{IN}	Input Current				−15	±1	15	µA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, Ta = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK II LVDS DRIVER DC SPECIFICATIONS								
V_{OD}	Differential Output Voltage	R_L = 100 Ω, De-Emph = disabled, Figure 3	VODSEL = 0	DOUT+, DOUT-	±225	±300	±375	mV
			VODSEL = 1		±350	±450	±550	
V_{ODp-p}	Differential Output Voltage (DOUT+) – (DOUT-)		VODSEL = 0			600		mVp-p
			VODSEL = 1			900		mVp-p
ΔV_{OD}	Output Voltage Unbalance	R_L = 100 Ω, De-Emph = disabled, VODSEL = L				1	50	mV
V_{OS}	Offset Voltage – Single-ended At TP A and B, Figure 2	R_L = 100 Ω, De-Emph = disabled	VODSEL = 0			1.65		V
			VODSEL = 1			1.575		V
ΔV_{OS}	Offset Voltage Unbalance Single-ended At TP A and B, Figure 2	R_L = 100 Ω, De-Emph = disabled				1		mV
I_{OS}	Output Short-Circuit Current	DOUT± = 0 V, De-Emph = disabled	VODSEL = 0			–35		mA
R_T	Internal Termination Resistor				80		120	Ω
SUPPLY CURRENT								
I_{DDT1}	Supply Current (includes load current) R_L = 100 Ω, f = 65 MHz	Checker Board Pattern, De-Emph = 3 kΩ, VODSEL = H, Figure 10	V_{DD}= 1.89 V	All V_{DD} pins		80	90	mA
I_{DDIOT1}			V_{DDIO}= 1.89 V	V_{DDIO}		3	5	mA
			V_{DDIO} = 3.6 V			10	13	mA
I_{DDT2}		Checker Board Pattern, De-Emph = 6 kΩ, VODSEL = L, Figure 10	V_{DD}= 1.89 V	All V_{DD} pins		75	85	mA
I_{DDIOT2}			V_{DDIO}= 1.89 V	V_{DDIO}		3	5	mA
			V_{DDIO} = 3.6 V			10	13	mA
I_{DDZ}	Supply Current Power Down	PDB = 0 V , (All other LVCMOS Inputs = 0 V)	V_{DD}= 1.89 V	All V_{DD} pins		60	1000	µA
I_{DDIOZ}			V_{DDIO}= 1.89 V	V_{DDIO}		0.5	10	µA
			V_{DDIO} = 3.6 V			1	30	µA

6.7 Recommended Timing for the Serial Control Bus

Over 3.3-V supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	
t_{LOW}	SCL Low Period	Standard Mode	4.7			us
		Fast Mode	1.3			
t_{HIGH}	SCL High Period	Standard Mode	4			us
		Fast Mode	0.6			
$t_{HD;STA}$	Hold time for a start or a repeated start condition, Figure 12	Standard Mode	4			us
		Fast Mode	0.6			
$t_{SU:STA}$	Set Up time for a start or a repeated start condition, Figure 12	Standard Mode	4.7			us
		Fast Mode	0.6			
$t_{HD;DAT}$	Data Hold Time, Figure 12	Standard Mode	0		3.45	us
		Fast Mode	0		0.9	
$t_{SU;DAT}$	Data Set Up Time, Figure 12	Standard Mode	250			ns
		Fast Mode	100			

Recommended Timing for the Serial Control Bus (continued)

Over 3.3-V supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	Units
$t_{SU;STO}$	Set Up Time for STOP Condition, Figure 12	Standard Mode	4			us
		Fast Mode	0.6			
t_{BUF}	Bus Free Time Between STOP and START, Figure 12	Standard Mode	4.7			us
		Fast Mode	1.3			
t_r	SCL and SDA Rise Time, Figure 12	Standard Mode			1000	ns
		Fast Mode			300	
t_f	SCL and SDA Fall Time, Figure 12	Standard Mode			300	ns
		Fast mode			300	

6.8 Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FPD-LINK LVDS INPUT						
t_{RSP0}	Receiver Strobe Position-bit 0	RxCLKIN = 65 MHz, RxIN[3:0] Figure 5	0.66	1.1	1.54	ns
t_{RSP1}	Receiver Strobe Position-bit 1		2.86	3.3	3.74	ns
t_{RSP2}	Receiver Strobe Position-bit 2		5.05	5.5	5.93	ns
t_{RSP3}	Receiver Strobe Position-bit 3		7.25	7.7	8.13	ns
t_{RSP4}	Receiver Strobe Position-bit 4		9.45	9.90	10.33	ns
t_{RSP5}	Receiver Strobe Position-bit 5		11.65	12.1	12.53	ns
t_{RSP6}	Receiver Strobe Position-bit 6		13.85	14.30	14.73	ns
FPD-LINK II LVDS OUTPUT						
t_{HLT}	Output Low-to-High Transition Time, Figure 4	R_L = 100 Ω, De-Emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100 Ω, De-Emphasis = disabled, VODSEL = 1		200		
t_{HLT}	Output High-to-Low Transition Time, Figure 4	R_L = 100 Ω, De-Emphasis = disabled, VODSEL = 0		200		ps
		R_L = 100 Ω, De-Emphasis = disabled, VODSEL = 1		200		
t_{XZD}	Ouput Active to OFF Delay, Figure 7			5	15	ns
t_{PLD}	PLL Lock Time, Figure 6	R_L = 100 Ω(1)		1.5	10	ms
t_{SD}	Delay - Latency, Figure 8	R_L = 100 Ω		140*T	145*T	ns
t_{DJIT}	Output Total Jitter, Figure 9	R_L = 100 Ω, De-Emphasis = disabled, RANDOM pattern, RxCLKIN = 43 and 65 MHz(2)		0.26		UI
λ_{STXBW}	Jitter Transfer Function –3-dB Bandwidth(3) (4)	RxCLKIN = 43 MHz		2.2		MHz
		RxCLKIN = 65 MHz		3		
δ_{STX}	Jitter Transfer Function Peaking(3)(4)	RxCLKIN = 43 MHz		1		dB
		RxCLKIN = 65 MHz		1		

(1) t_{PLD} is the time required by the device to obtain lock when exiting power-down state with an active RxCLKIN.
(2) UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / 28*RxCLKIN). The UI scales with RxCLKIN frequency.
(3) Specification is ensured by characterization and is not tested in production.
(4) Specification is ensured by design and is not tested in production.

6.9 DC and AC Serial Control Bus Characteristics

Over 3.3-V supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Level	SDA and SCL	0.7* V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3* V_{DDIO}	V
V_{HY}	Input Hysteresis			>50		mV

DC and AC Serial Control Bus Characteristics (continued)

Over 3.3-V supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}		SDA, IOL = 1.25 mA	0		0.36	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	–10		10	µA
t_R	SDA RiseTime – READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF, Figure 12		430		ns
t_F	SDA Fall Time – READ			20		ns
$t_{SU;DAT}$	Set Up Time — READ	See Figure 12		560		ns
$t_{HD;DAT}$	Hold Up Time — READ	See Figure 12		615		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

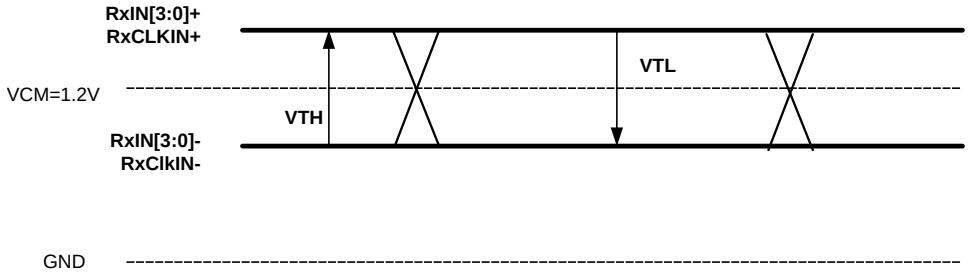


Figure 1. FPD-Link DC VTH/VTL Definition

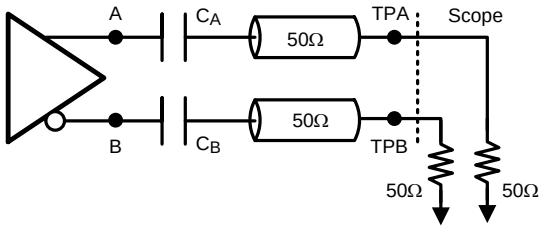


Figure 2. Output Test Circuit

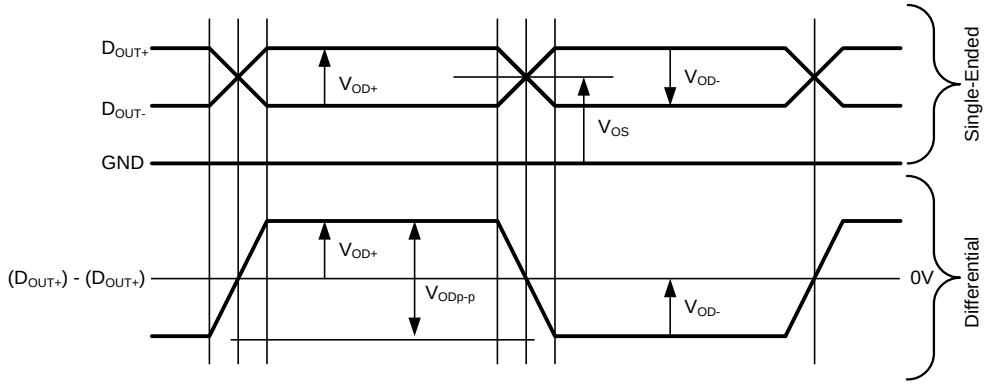


Figure 3. Output Waveforms

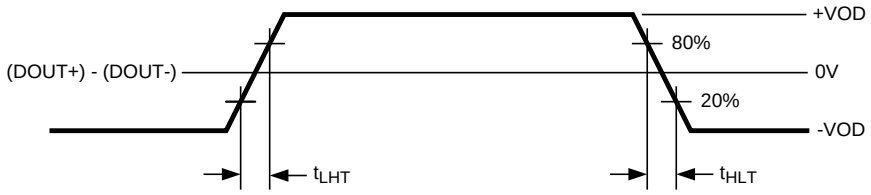


Figure 4. Output Transition Times

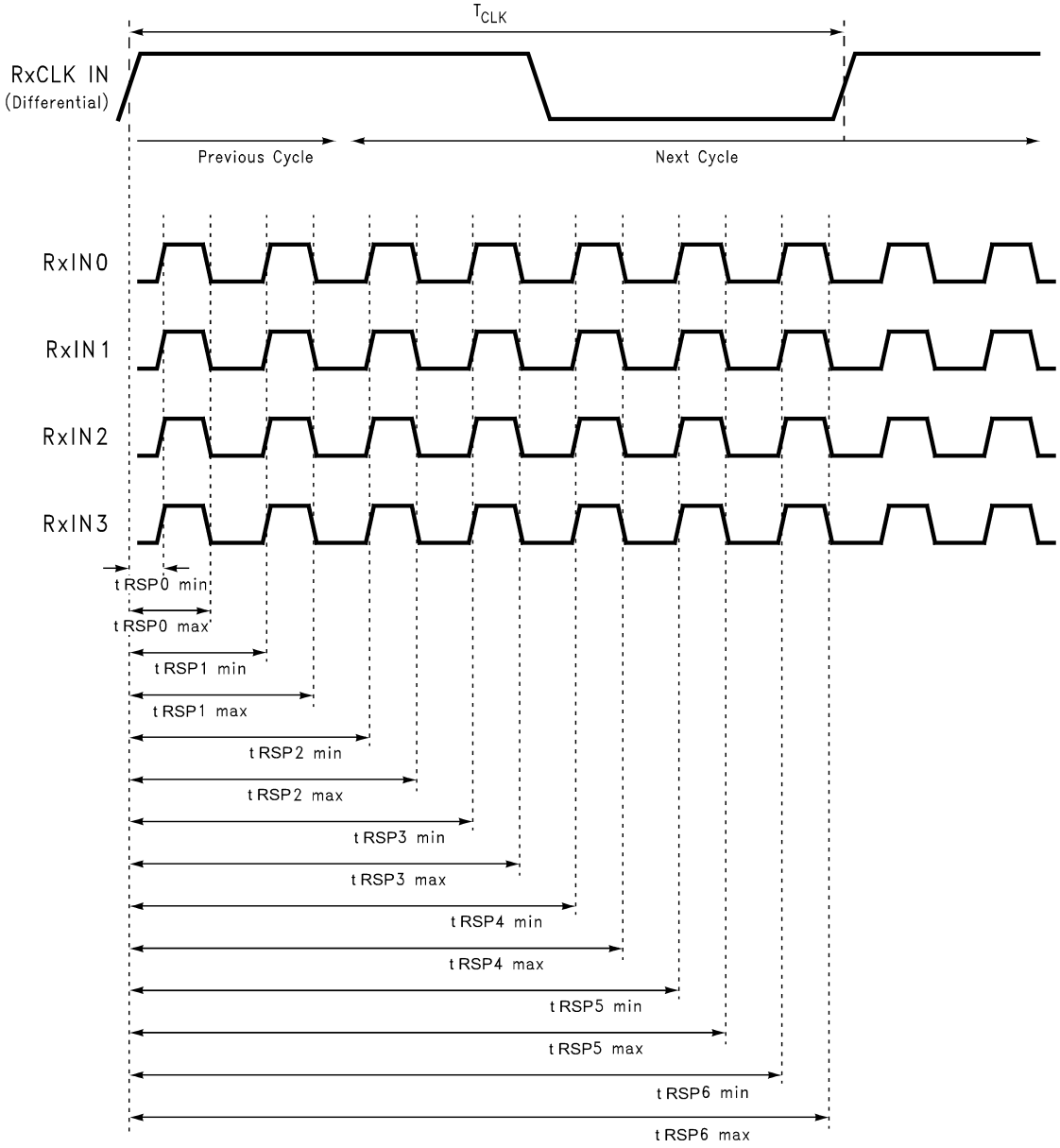


Figure 5. RSP (Receiver Strobe Position)

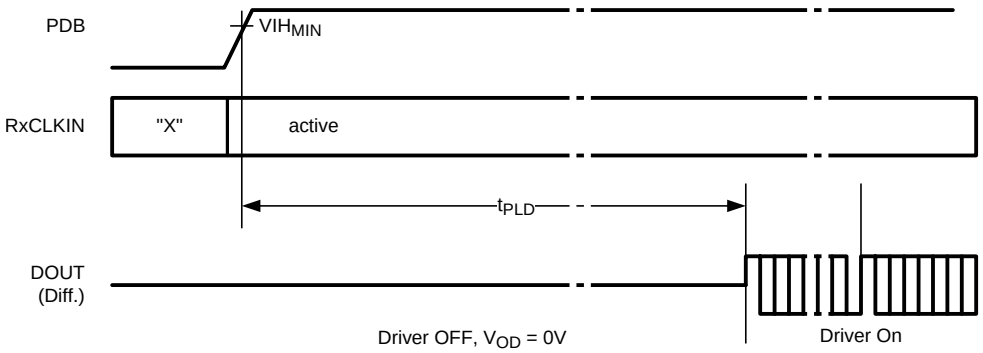


Figure 6. Lock Time

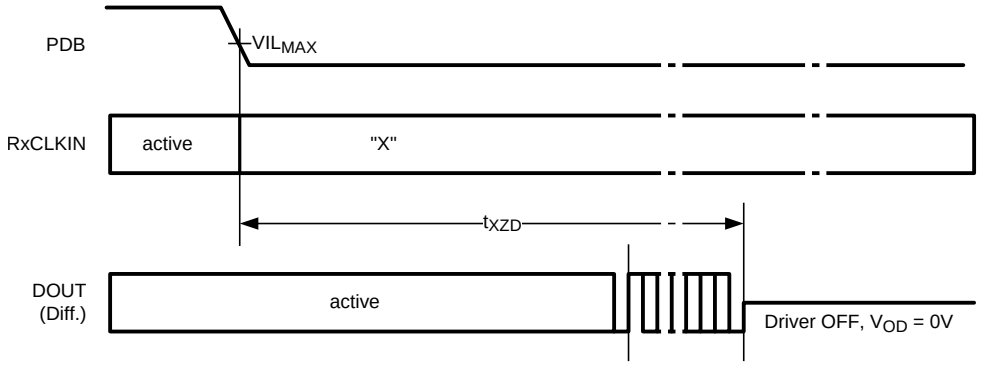


Figure 7. Disable Time

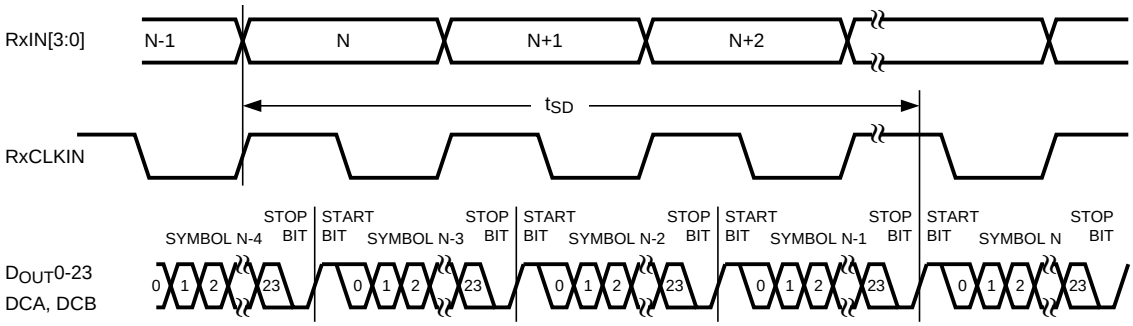


Figure 8. Latency Delay

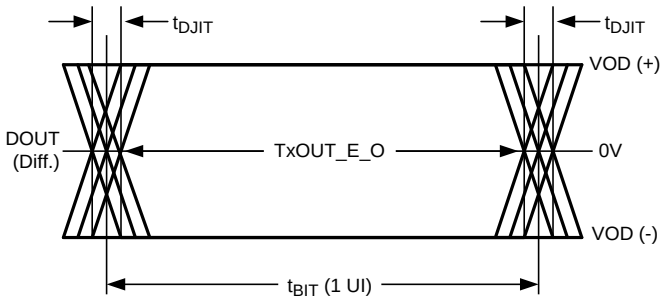


Figure 9. Output Jitter

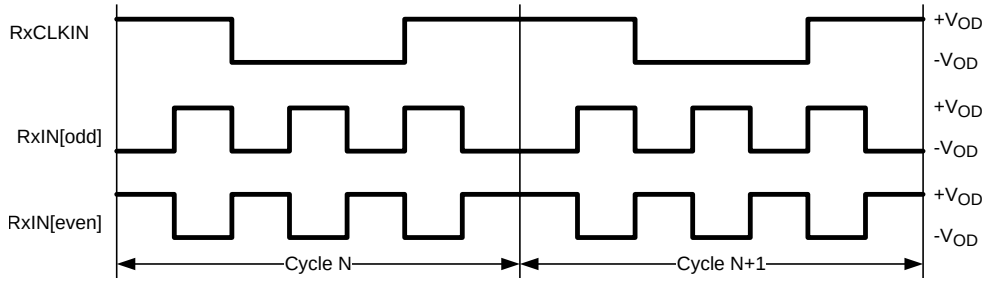


Figure 10. Checkerboard Data Pattern

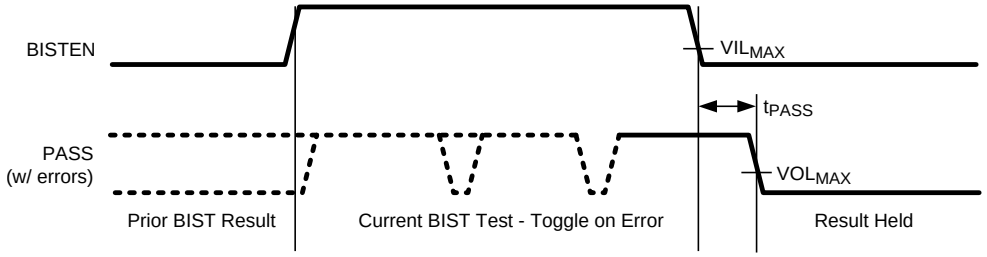


Figure 11. BIST Pass Waveform

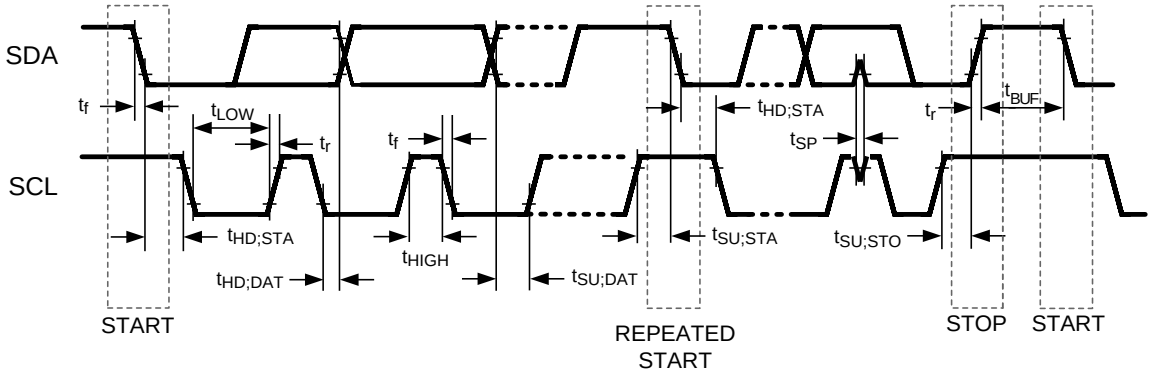


Figure 12. Serial Control Bus Timing Diagram

6.10 Typical Characteristics

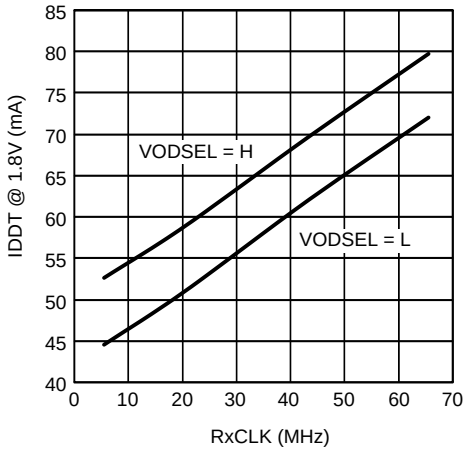


Figure 13. Typical IDDT (1.8-V Supply) Current as a Function of RxCLK

7 Detailed Description

7.1 Overview

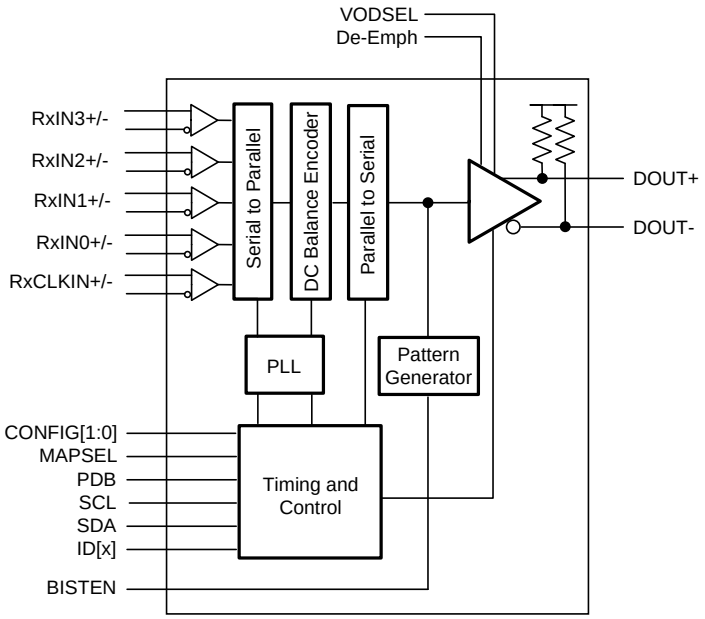
The DS90UR907Q converter transmits an FPD-Link interface (4 LVDS data channels + 1 LVDS clock) with total of 27–bits of data (24–high speed bits and 3 low speed video control signals) over a single serial FPD-Link II pair. The serial stream also contains an embedded clock and the DC-balance information which enhances signal quality and supports AC coupling. The device is intended for use with DS90UR908Q or DS90UR906Q, but is backward compatible with previous generations of FPD-Link II as well.

The DS90UR907Q can operate in 24-bit color mode (with VS,HS,DE encoded in the serial stream) or in 18-bit color mode.

The DS90UR907Q can be configured through external pins or through the optional serial control bus. It features enhanced signal quality on the link by supporting: selectable VOD level, selectable deemphasis signal conditioning and also the FPD-Link II data coding that provides randomization, scrambling, and DC Balancing of the video data. It also includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data and also the system spread spectrum PCLK support. The DS90UR907Q features power saving with a power-down mode, and auto stop clock feature.

See also *Built In Self Test (BIST)* and *Optional Serial Bus Control* for more information.

7.2 Functional Block Diagram



FPD-Link to FPD-Link II Convertor

7.3 Feature Description

7.3.1 Data Transfer

The DS90UR907Q transmits a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. b[23:0] contain the scrambled RGB data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream and can also contain encoded control (VS,HS,DE). Both DCA and DCB coding schemes are generated by the DS90UR907Q and decoded by the paring deserializer automatically reference to FPD-Link II Serial Stream. Figure 14 illustrates the serial stream per PCLK cycle.

Feature Description (continued)

NOTE

The figure only illustrates the bits but does not actually represent the bit location as the bits are scrambled and balanced continuously.

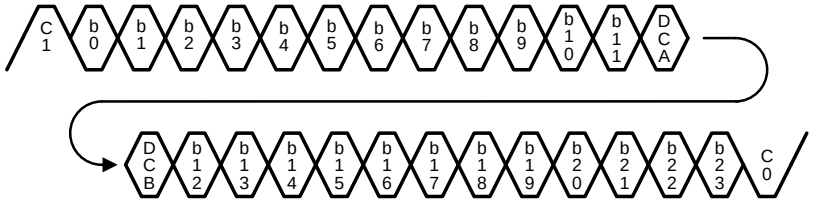


Figure 14. FPD-Link II Serial Stream

7.3.2 Operating Modes And Backward Compatibility - Config[1:0]

The DS90UR907Q is backward compatible with previous generations of FPD-Link II deserializers. Configuration modes are provided for backwards compatibility with the DS90C124 FPD-Link II Generation 1, and also the DS90UR124 FPD-Link II Generation 2 deserializers by setting the respective mode with the CONFIG[1:0] pins as shown in Table 1. The selection also determine whether the Video Control Signal filter feature is enabled or disabled in Normal mode.

Table 1. DS90UR907Q Configuration Modes

CONFIG1	CONFIG0	MODE	DES DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS90UR908Q, DS90UR906Q
L	H	Normal Mode, Control Signal Filter enabled	DS90UR908Q, DS90UR906Q
H	L	Backwards Compatible GEN2	DS90UR124, DS99R124
H	H	Backwards Compatible GEN1	DS90C124

7.3.3 Video Control Signal Filter

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled:
  - DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled:
  - DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low-frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high-frequency noise on the control signals. See Figure 15.

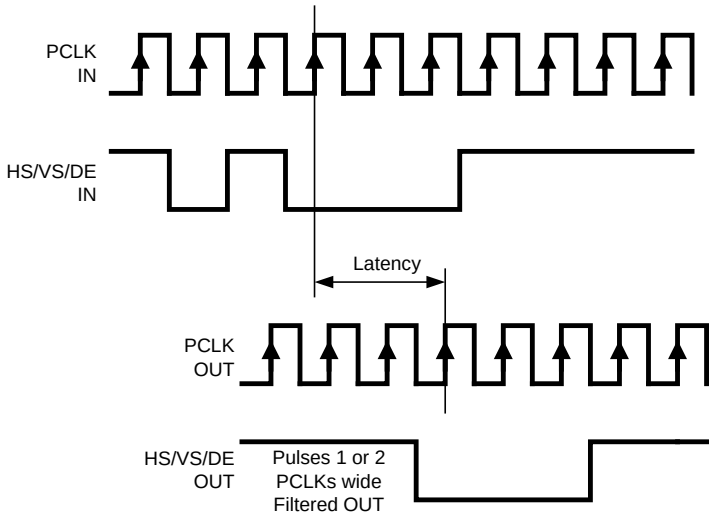


Figure 15. Video Control Signal Filter Waveform

7.3.4 Color Bit Mapping Select

The DS90UR907Q can be configured to accept 24-bit color (8-bit RGB) with 2 different mapping schemes: LSBs on RxIN[3] shown in Figure 16 or MSBs on RxIN[3] shown in Figure 17. The mapping scheme is controlled by MAPSEL pin or by Register.

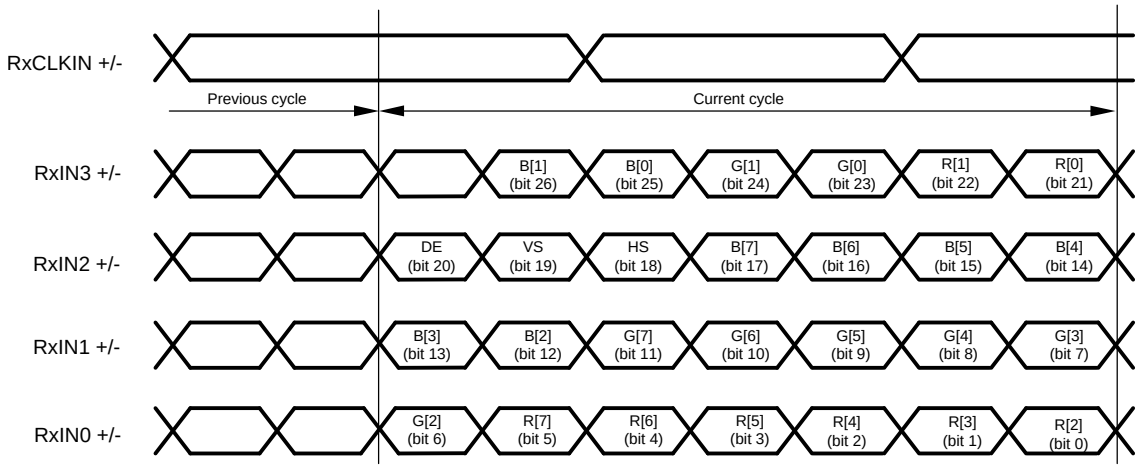


Figure 16. 8–Bit FPD-Link Mapping: LSB's on Rxin3

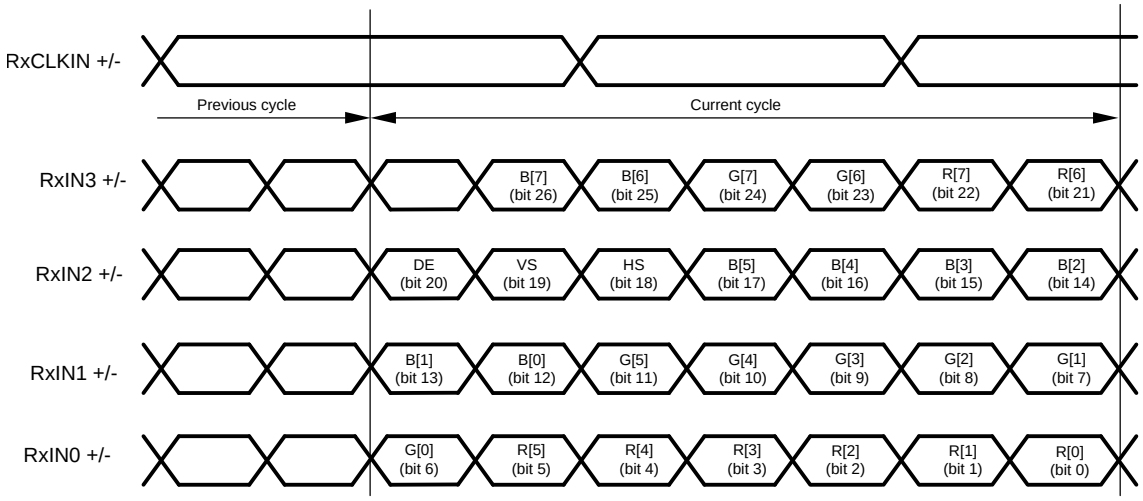


Figure 17. 8–Bit FPD-Link Mapping: MSB's on Rxin3

7.3.5 EMI Reduction Features

7.3.5.1 Spread Spectrum Compatibility

The RxCLKIN of the FPD-Link input is capable of tracking spread spectrum clocking (SSC) from a host source. The RxCLKIN will accept spread spectrum, tracking up to 35-kHz modulation and ±0.5, ±1 or ±2% deviations (center spread). The maximum conditions for the RxCLKIN input are: a modulation frequency of 35 kHz and amplitude deviations of ±2% (4% total).

7.3.6 Signal Quality Enhancers

7.3.6.1 VOD Select (VODSEL)

The DS90UR907Q differential output voltage may be increased by setting the VODSEL pin High. When VODSEL is Low, the DC VOD is at the standard (default) level. When VODSEL is High, the DC VOD is increased in level. The increased VOD is useful in extremely high noise environments and also on extra long cable length applications. When using de-emphasis, TI recommends setting VODSEL = H to avoid excessive signal attenuation especially with the larger de-emphasis settings. This feature may be controlled by the external pin or by register.

Table 2. Differential Output Voltage

INPUT	EFFECT	
VODSEL	VOD (mV)	VOD (mVp-p)
H	±450	900
L	±300	600

7.3.6.2 De-Emphasis (De-Emph)

The De-Emph pin controls the amount of de-emphasis beginning one full bit time after a logic transition that the device drives. It is the signal conditioning function for use in compensating against cable transmission loss. This pin should be left open for standard switching currents (no de-emphasis) or if controlled by register. De-emphasis is selected by connecting a resistor on this pin to ground, with R value from 0.5 kΩ to 1 MΩ, or by register setting. When using De-Emphasis, TI recommends setting VODSEL = H.

Table 3. De-Emphasis Resistor Value

RESISTOR VALUE (kΩ)	DE-EMPHASIS SETTING
Open	Disabled
0.6	–12 dB
1	–9 dB
2	–6 dB
5	–3 dB

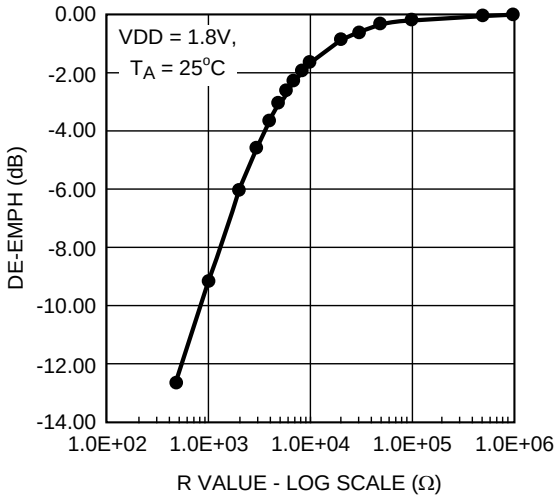


Figure 18. De-Emph vs R Value

7.3.7 Power Saving Features

7.3.7.1 Power-Down Feature (PDB)

The DS90UR907Q has a PDB input pin to ENABLE or POWER DOWN the device. This pin is controlled by the host and is used to save power, disabling the link when the display is not needed. In the POWER DOWN mode, the high-speed driver outputs present a 0V VOD state. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

7.3.7.2 Stop Clock Feature

The DS90UR907Q enters a low power SLEEP state when the RxCLKIN is stopped. A STOP condition is detected when the input clock frequency is less than 3 MHz. The clock should be held at a static Low or high state. When the RxCLKIN starts again, the device will then lock to the valid input RxCLKIN and then transmits the RGB data to the deserializer. Note – in STOP CLOCK SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

7.3.7.3 1.8-V or 3.3-V V_{DDIO} Operation

The DS90UR907Q parallel control bus operate with 1.8-V or 3.3-V levels (V_{DDIO}) for host compatibility. The 1.8-V levels will offer a system power savings.

7.4 Device Functional Modes

7.4.1 Operating Modes and Backward Compatibility (Config[1:0])

The DS90UR907Q is backward compatible with previous generations of FPD-Link II deserializers. Configuration modes are provided for backwards compatibility with the DS90C124 FPD-LinkII Generation 1, and also the DS90UR124 FPD-Link II Generation 2 deserializers by setting the respective mode with the CONFIG[1:0] pins as shown in Table 4. The selection also determines whether the Video Control Signal filter feature is enabled or disabled in Normal mode.

Table 4. DS90UR907Q

CONFIG 1	CONFIG 0	MODE	DES DEVICE
L	L	Normal Mode, Control Signal Filter disabled	DS90UR908Q, DS90UR906Q
L	H	Normal Mode, Control Signal Filter enabled	DS90UR908Q, DS90UR906Q
H	L	Backwards compatible GEN2	DS90UR124, DS99R124
H	H	Backwards compatible GEN1	DS90C124

7.5 Programming

7.5.1 Optional Serial Bus Control

See the following section on the *Optional Serial Bus Control* Interface.

7.5.2 Built In Self Test (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only a input clock is required along with control to the DS90UR907Q and deserializer BISTEN input pins. The DS90UR907Q outputs a test pattern (PRBS7) and drives the link at speed. The deserializer detects the PRBS7 pattern and monitors it for errors. A PASS output pin toggles to flag any payloads that are received with 1 to 24 errors. Upon completion of the test, the result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin.

Inter-operability is supported between this FPD-Link II device and all FPD-Link II generations (Gen 1/2/3) — see respective data sheets for details on entering BIST mode and control.

Sample BIST Sequence

See Figure 19 for the BIST mode flow diagram.

Step 1: Place the DS90UR907Q in BIST Mode by setting Ser BISTEN = H. The BIST Mode is enabled through the BISTEN pin. An RxCLKIN is required for all the Ser options. When the deserializer detects the BIST mode pattern and command (DCA and DCB code) the RGB and control signal outputs are shut off.

Step 2: Place the pairing deserializer in BIST mode by setting the BISTEN = H. The Des is now in the BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data and the final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the DS90UR907Q BISTEN input is set Low. The Link returns to normal operation.

Programming (continued)

Figure 20 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission and so forth), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or deserializer Equalization).

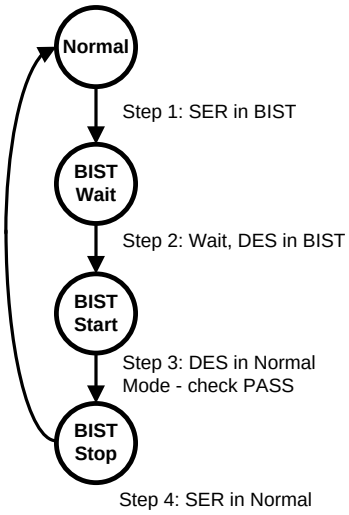


Figure 19. BIST Mode Flow Diagram

Programming (continued)

BER Calculations

It is possible to calculate the approximate Bit Error Rate (BER). The following is required:

- Pixel Clock Frequency (MHz)
- BIST Duration (seconds)
- BIST test Result (PASS)

The BER is less than or equal to one over the product of 24 times the RxCLKIN rate times the test duration. If we assume a 65-MHz RxCLKIN, a 10 minute (600 second) test, and a PASS, the BERT is ≤ 1.07 × 10E-12

The BIST mode runs a check on the data payload bits. The LOCK pin also provides a link status. It the recovery of the C0 and C1 bits does not reconstruct the expected clock signal, the LOCK pin will switch Low. The combination of the LOCK and At-Speed BIST PASS pin provides a powerful tool for system evaluation and performance monitoring.

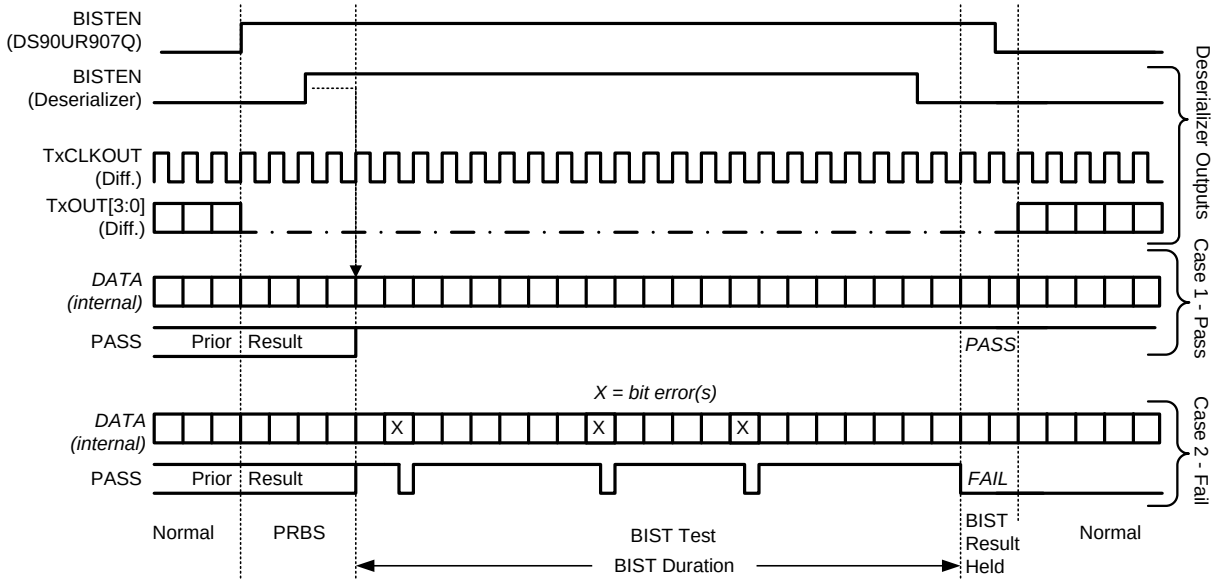


Figure 20. BIST Waveforms

7.5.3 Optional Serial Bus Control

The DS90UR907Q may be configured by the use of a serial control bus that is I^2C protocol compatible. By default, the I^2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable/allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus because multiple addresses are supported. See Figure 21.

The serial bus is comprised of three pins. The SCL is a Serial Bus Clock Input. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to V_{DDIO}. For most applications a 4.7-k pullup resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

Programming (continued)

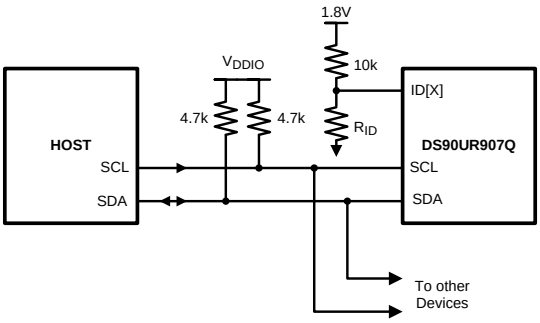


Figure 21. Serial Control Bus Connection

The third pin is the ID[x] pin. This pin sets one of four possible device addresses. Two different connections are possible. The pin may be pulled to V_{DD} (**1.8 V, NOT V_{DDIO}**)) with a 10-kΩ resistor. Or a 10-kΩ pullup resistor (to V_{DD}**1.8 V, NOT V_{DDIO}**)) and a pulldown resistor of the recommended value to set other three possible addresses may be used. See Table 5.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See Figure 22.

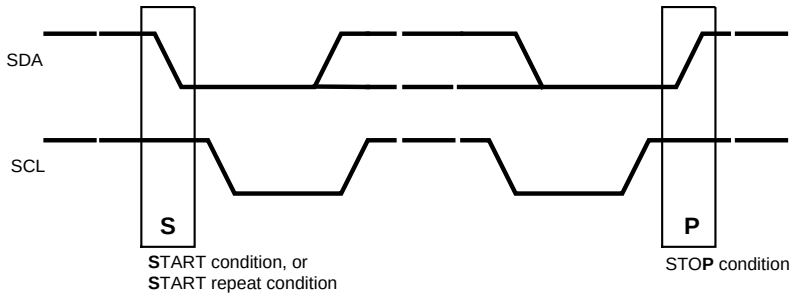


Figure 22. Start and Stop Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 23 and a WRITE is shown in Figure 24.

If the Serial Bus is not required, the three pins may be left open (NC).

Table 5. ID[x] Resistor Value – DS90UR907Q

Resistor RID kΩ	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 110 1001 (h'69)	8b' 1101 0010 (h'D2)
2.7	7b' 110 1010 (h'6A)	8b' 1101 0100 (h'D4)
8.2	7b' 110 1011 (h'6B)	8b' 1101 0110 (h'D6)
Open	7b' 110 1110 (h'6E)	8b' 1101 1100 (h'DC)

Programming (continued)

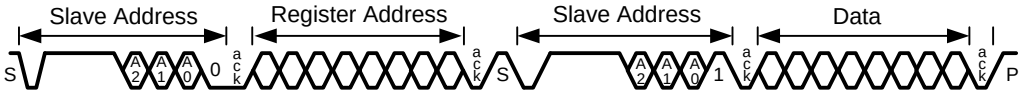


Figure 23. Serial Control Bus — Read

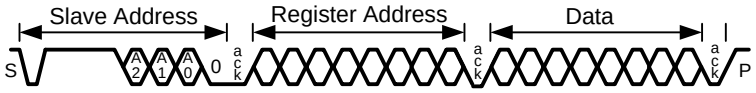


Figure 24. Serial Control Bus — Write

Table 6. Serial Bus Control Registers

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	R/W	DEFAULT (bin)	FUNCTION	DESCRIPTION
0	0	Ser Config 1	7	R/W	0	***Reserved***	***Reserved***
			6	R/W	0	MAPSEL	0: LSB on RxIN3 1: MSB on RxIN3
			5	R/W	0	VODSEL	0: Low 1: High
			4	R/W	0	***Reserved***	***Reserved***
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter DISABLED 01: Normal Mode, Control Signal Filter ENABLED 10: Backwards Compatible (DS90UR124, DS99R124) 11: Backwards Compatible (DS90C124)
			1	R/W	0	SLEEP	Note – not the same function as PowerDown (PDB) 0: normal mode 1: Sleep Mode – **Register settings retained.**
			0	R/W	0	REG	0: Configurations set from control pins 1: Configuration set from registers (except I2C_ID)
1	1	Device ID	7	R/W	0	REG ID	0: Address from ID[x] Pin 1: Address from Register
			6:0	R/W	1101000	ID[x]	Serial Bus Device ID, Five IDs are: 7b '1101 000 (h'68) 7b '1101 001 (h'69) 7b '1101 010 (h'6A) 7b '1101 011 (h'6B) 7b '1101 110 (h'6E) All other addresses are ***Reserved***.
2	2	De-Emphasis Control	7:5	R/W	000	De-Emph Setting	000: set by external Resistor 001: –1 dB 010: –2 dB 011: –3.3 dB 100: –5 dB 101: –6.7 dB 110: –9 dB 111: –12 dB
			4	R/W	0	De-Emph EN	0: De-Emphasis Enabled 1: De-Emphasis Disabled
			3:0	R/W	000	***Reserved***	***Reserved***

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90UR907Q and DS90UR908Q chipset is intended for interface between a host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888) and up to 1024 × 768 display formats. In a RGB888 application, 24 color bits (R[7:0], G[7:0], B[7:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link with PCLK rates from 5 to 65 MHz. The chipset may also be used in 18-bit color applications. In this application three to six general purpose signals may also be sent from host to display.

8.1.1 Power-Up Requirements and PDB Pin

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower then 1.5 ms then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO}, TI recommends using a 10-kΩ pullup and a 22-uF capacitor to GND to delay the PDB input signal.

8.1.2 Transmission Media

The DS90UR907Q and the companion deserializer chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The DS90UR907Q provide internal terminations providing a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or unshielded cables may be used depending upon the noise environment and application requirements.

8.1.3 Alternate Color / Data Mapping

Color Mapped data pin names are provided to specify a recommended mapping for 24-bit and 18-bit Applications. When connecting to earlier generations of FPD-Link II deserializer devices, a color mapping review is recommended to ensure the correct connectivity is obtained. Table 7 provides examples for interfacing between DS90UR907Q and different deserializers.

Table 7. Alternate Color / Data Mapping

FPD-Link	Bit Number	RGB (LSB Example)		DS90UR906Q	DS90UR124	DS99R124Q	DS90C124
RxIN3	Bit 26	B1		B1	N/A		
	Bit 25	B0		B0			
	Bit 24	G1		G1			
	Bit 23	G0		G0			
	Bit 22	R1		R1			
	Bit 21	R0		R0			

Application Information (continued)

Table 7. Alternate Color / Data Mapping (continued)

FPD-Link	Bit Number	RGB (LSB Example)		DS90UR906Q	DS90UR124	DS99R124Q	DS90C124
RxIN2	Bit 20	DE		DE	ROUT20	TxOUT2	ROUT20
	Bit 19	VS		VS	ROUT19		ROUT19
	Bit 18	HS		HS	ROUT18		ROUT18
	Bit 17	B7		B7	ROUT17		ROUT17
	Bit 16	B6		B6	ROUT16		ROUT16
	Bit 15	B5		B5	ROUT15		ROUT15
	Bit 14	B4		B4	ROUT14		ROUT14
RxIN1	Bit 13	B3		B3	ROUT13	TxOUT1	ROUT13
	Bit 12	B2		B2	ROUT12		ROUT12
	Bit 11	G7		G7	ROUT11		ROUT11
	Bit 10	G6		G6	ROUT10		ROUT10
	Bit 9	G5		G5	ROUT9		ROUT9
	Bit 8	G4		G4	ROUT8		ROUT8
	Bit 7	G3		G3	ROUT7		ROUT7
RxIN0	Bit 6	G2		G2	ROUT6	TxOUT0	ROUT6
	Bit 5	R7		R7	ROUT5		ROUT5
	Bit 4	R6		R6	ROUT4		ROUT4
	Bit 3	R5		R5	ROUT3		ROUT3
	Bit 2	R4		R4	ROUT2		ROUT2
	Bit 1	R3		R3	ROUT1		ROUT1
	Bit 0	R2		R2	ROUT0		ROUT0
N/A *** These bits are not supported by DS90UR907Q**				N/A	ROUT23*	OS2*	ROUT23*
					ROUT22*	OS1*	ROUT22*
					ROUT21*	OS0*	ROUT21*
DS90UR907Q Settings	**MAPSEL = 0**			**CONFIG [1:0] = 00**	**CONFIG [1:0] = 10**		**CONFIG [1:0] = 11**

8.2 Typical Application

Figure 25 shows a typical application of the DS90UR907Q for a 65-MHz 24-bit Color Display Application. The LVDS inputs of the FPD-Link interface require external 100-Ω terminations. The LVDS outputs of FPD-Link II require 100-nF AC coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1-µF capacitors and a 4.7-µF capacitor should be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. The application assumes the companion deserializer (DS90UR908Q); therefore, the configuration pins are also both tied Low. In this example the cable is long; therefore, the VODSEL pin is tied High and a De-Emphasis value is selected by the resistor R1. The interface to the host is with 1.8-V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8-V rail. The Optional Serial Bus Control is not used in this example, thus the SCL, SDA and ID[x] pins are left open. A delay capacitor and resistor is placed on the PDB signal to delay the enabling of the device until power is stable. Bypass capacitors are placed near the power supply pins. Ferrite beads are placed on the power lines for effective noise suppression.

Typical Application (continued)

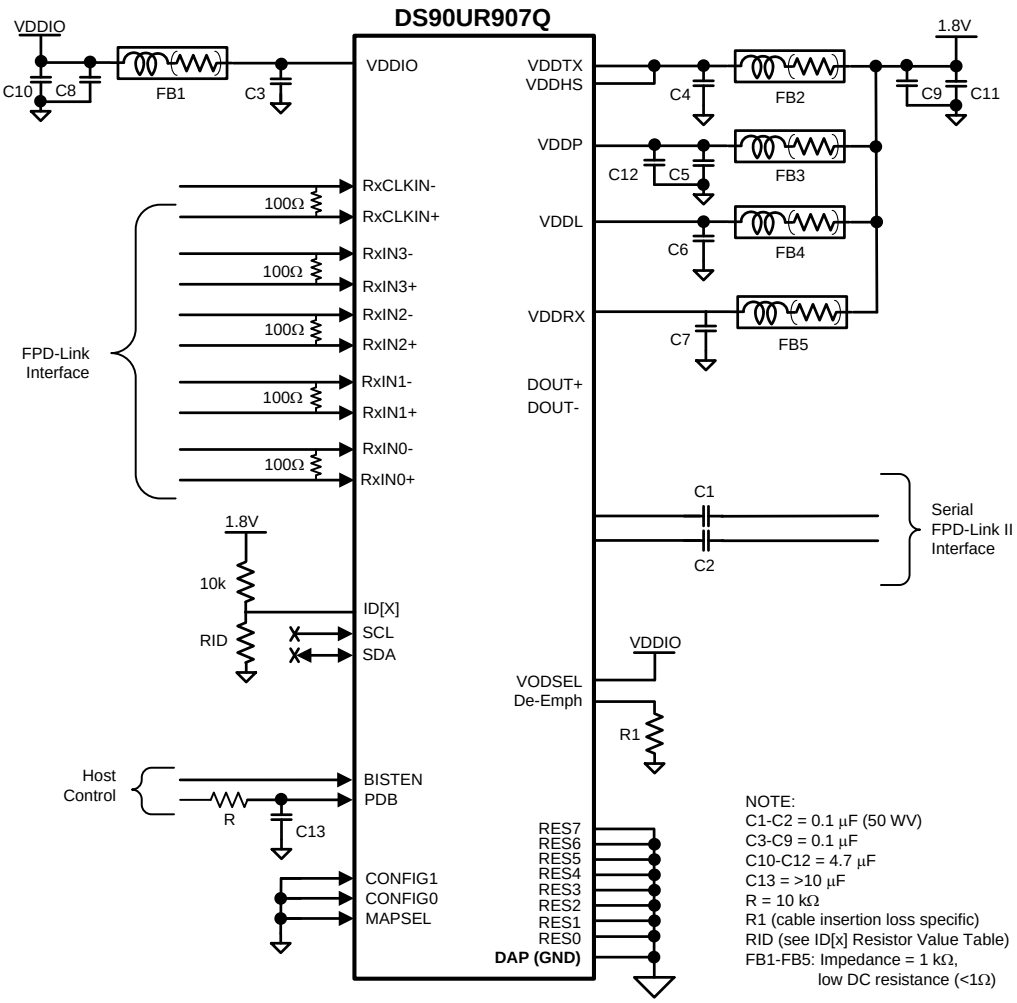


Figure 25. Typical Connection Diagram

8.2.1 Design Requirements

Table 8 shows the input parameters for the typical design application.

Table 8. Design Parameters

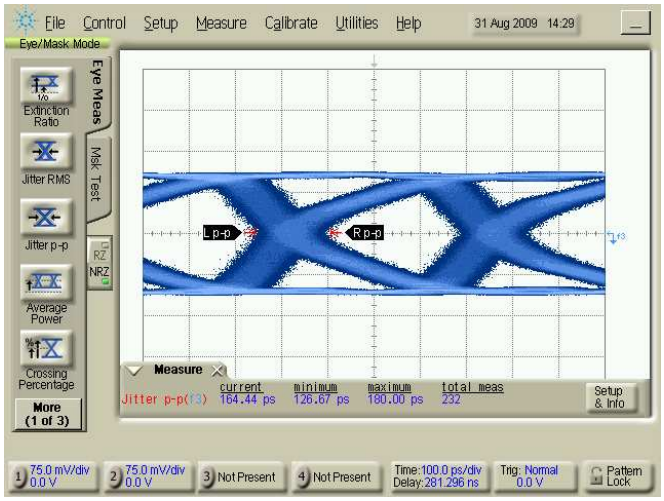
DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V or 3.3 V
VDDL, VDDP, VDDHS, VDDTX, VDDRX	1.8 V
AC Coupling Capacitor for DOUT±	100 nF

8.2.2 Detailed Design Procedure

The DOUT± outputs require 100-nF AC coupling capacitors to the line. FPD-Link data input pair required an external 100-Ω termination for standard LVDS levels. The power supply filter capacitors are placed near the power supply pins. A smaller capacitance capacitor should be located closer to the power supply pins. Adding a ferrite bead is optional. Recommend to use 1-kΩ impedance and low DC resistance such as less than 1 Ω. The VODSEL pin is tied to VDDIO for the long cable application. The De-Emph pin may connect a resistor to ground.

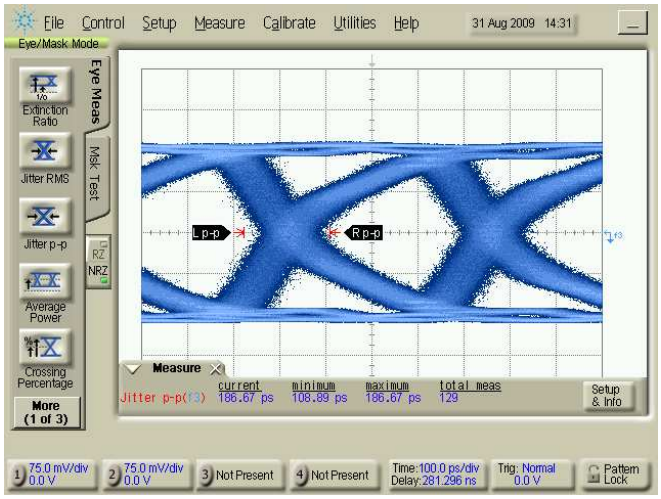
Refer to the Table 3. The PDB and BISTEN pins are assumed controlling by a microprocessor. The PDB must be low state until all power supply voltages reach the final voltage. The CONFIG[1:0] pins are set depending on operating modes and interfacing device. See the Table 1. MAPSEL pin is set the mapping scheme. Refer to the Figure 16 and Figure 17. The SCL, SDA, and ID[x] pins are left open when these Serial Bus Control pins are unused. The RES[7:0] pins and DAP should be tied to ground.

8.2.3 Application Curves



Serializer CML Output Stream with Input PCLK = 65 MHz, VODSEL = L

Figure 26. Serializer CML Output Stream With Input PCLK = 65 MHz, VODSEL = L



Serializer CML Output Stream with Input PCLK = 65 MHz, VODSEL = H

Figure 27. Serializer CML Output Stream With Input PÄCLK = 65 MHz, VODSEL = H

9 Power Supply Recommendations

The VDD (V_{DDn} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. If slower than 1.5 ms, then a capacitor on the PDB pin is needed to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to VDDIO, TI recommends using a 10-kΩ pullup and a >10-µF capacitor to GND to delay the PDB input signal.

All inputs must not be driven until all supply voltages have reached their steady-state value.

10 Layout

10.1 Layout Guidelines

10.1.1 PCB Layout and Power System Considerations

Design the circuit board layout and stack-up for the LVDS devices to provide low-noise power feed to the device. Good layout practice will also separate high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. The capacitors may use values in the range of 0.01 uF to 0.1 uF.

TI recommends surface mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. TI recommends a large bulk capacitor at the point of power entry. This is typically in the 50-uF to 100-uF range and will smooth low-frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with the via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

TI recommends a small body size X7R chip capacitor, such as the 0603, for external bypass. The X7R chip capacitor's small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, use multiple capacitors to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The table typically provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Place LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

10.1.2 LVDS Interconnect Guidelines

See SNLA008 and SNLA035 for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500-megabits per second line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI website at: www.ti.com/lvds

10.2 Layout Example

Figure 28 and Figure 29 show the PCB layout example derived from the layout design of the DS90UR907Q-Q1 Evaluation Board. The graphic and layout description are used to determine both proper routing and proper solder techniques for designing the board.

Layout Example (continued)

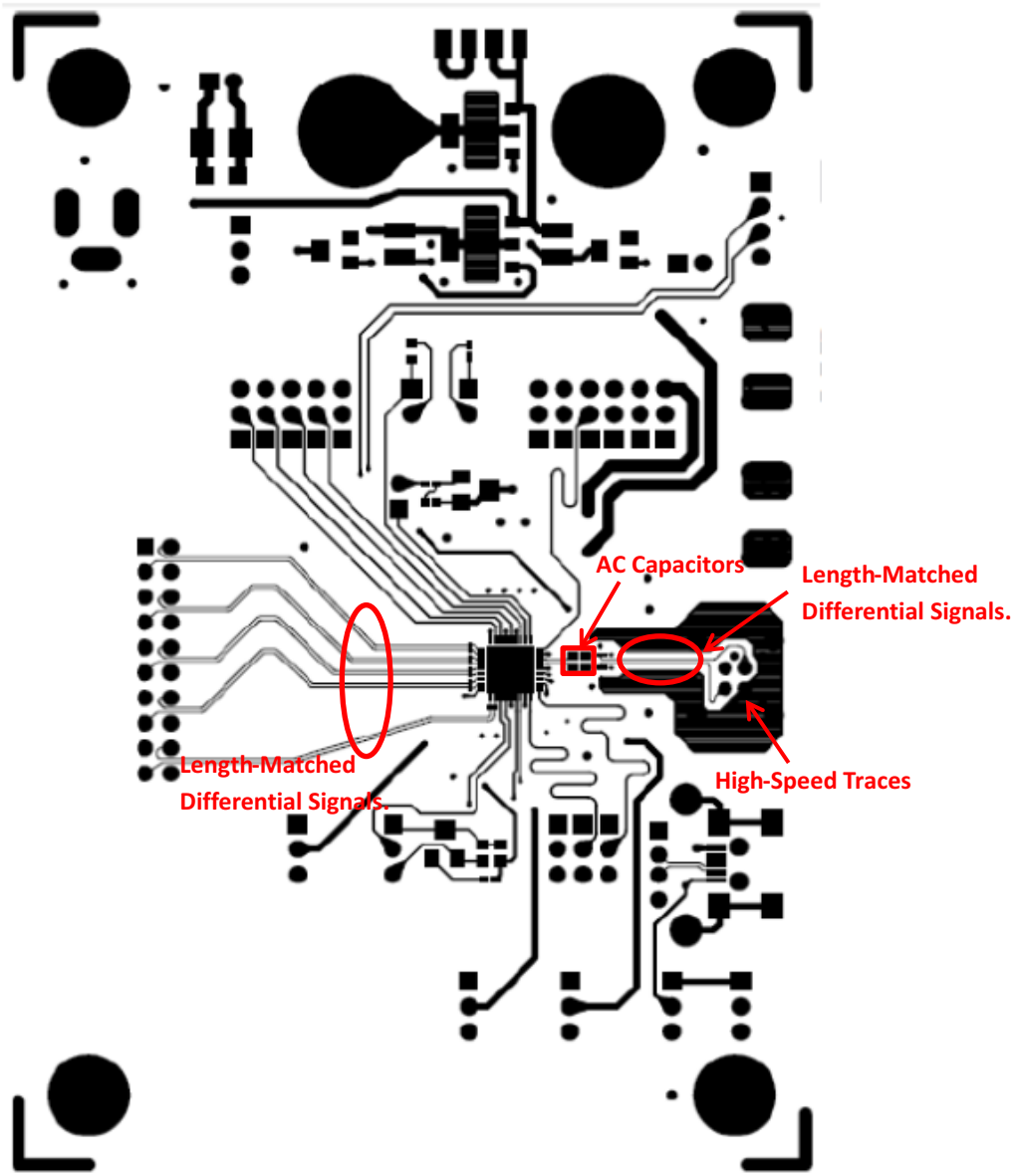


Figure 28. Top Layer

Layout Example (continued)

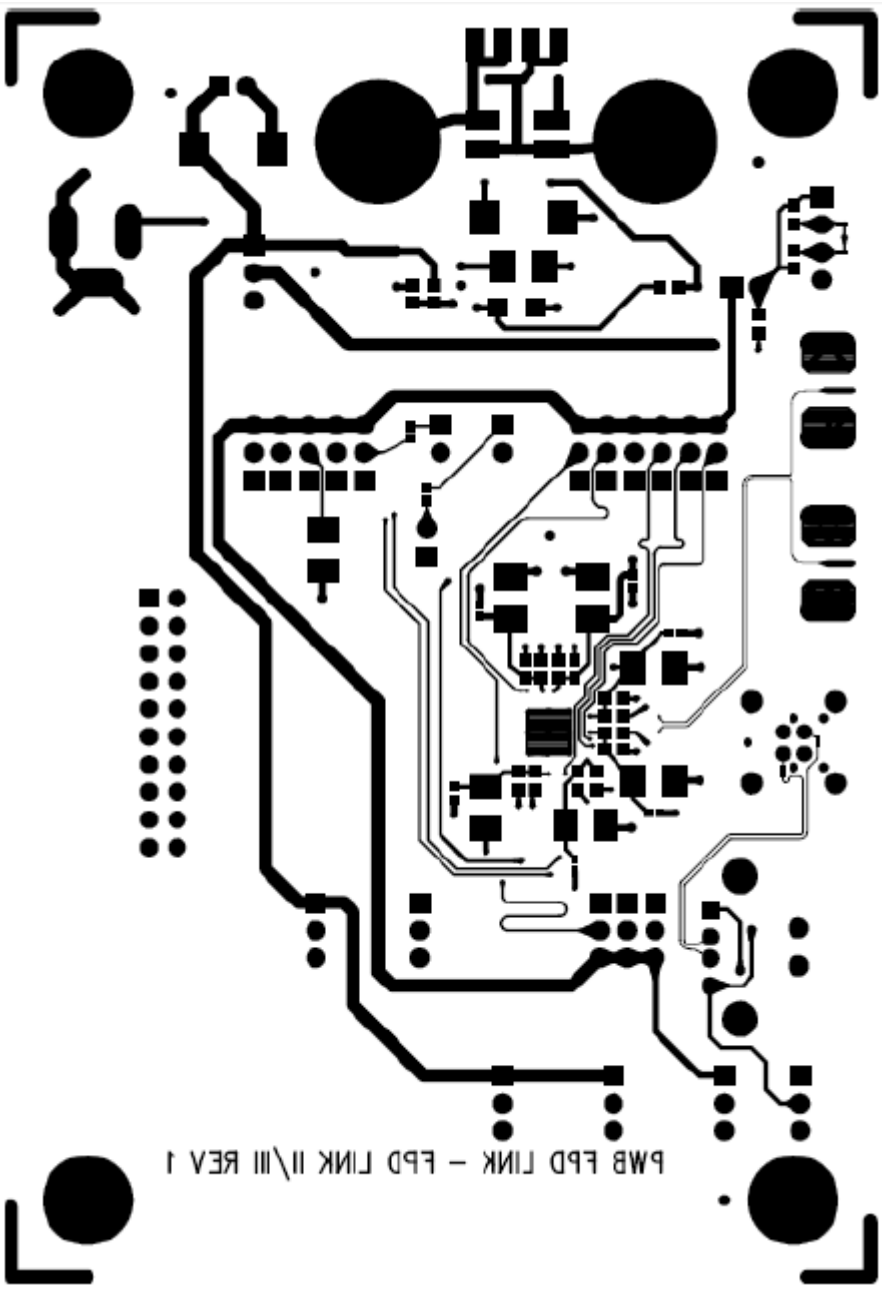


Figure 29. Bottom Layer

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Application Note 1108 Channel-Link PCB and Interconnect Design-In Guidelines*, SNLA008
- *Application Note AN-1187, Leadless Leadframe Package (LLP)*, SNOA401
- *Application Note 905 Transmission Line RAPIDESIGNER Operation and Applications Guide*, SNLA035
- *LVDS Owner's Manual Design Guide, 4th Edition*, SNLA187

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

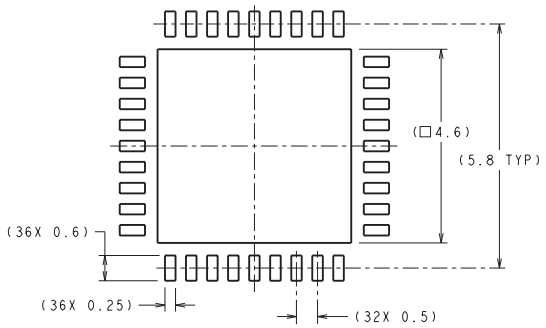
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

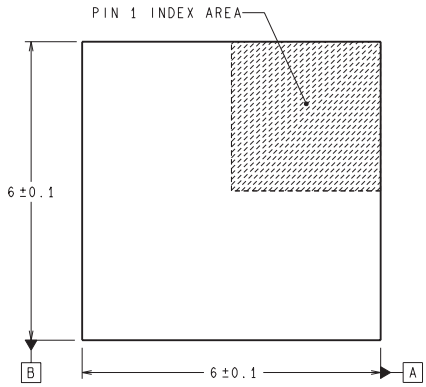
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

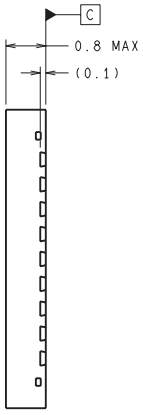
NJK0036A

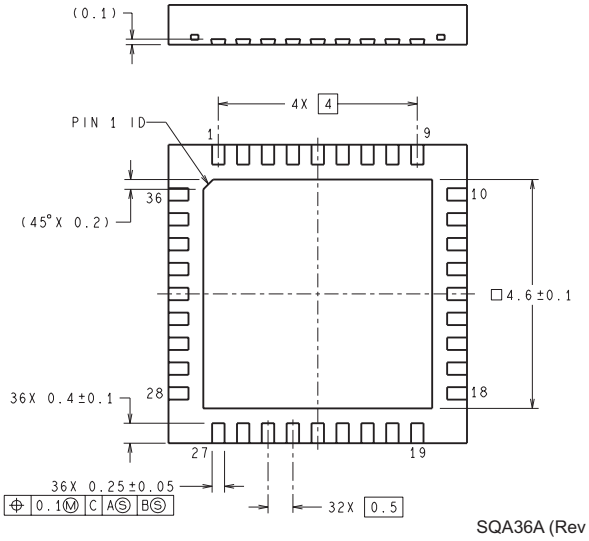


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







SQA36A (Rev A)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UR907QSQ/NOPB	ACTIVE	WQFN	NJK	36	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR907QSQ	Samples
DS90UR907QSQE/NOPB	ACTIVE	WQFN	NJK	36	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR907QSQ	Samples
DS90UR907QSQX/NOPB	ACTIVE	WQFN	NJK	36	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UR907QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

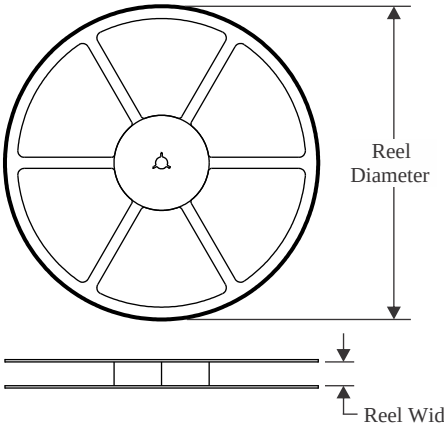
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

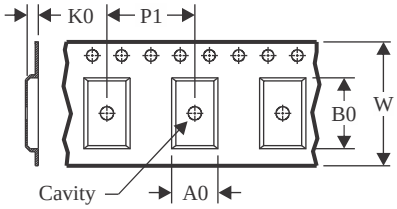
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

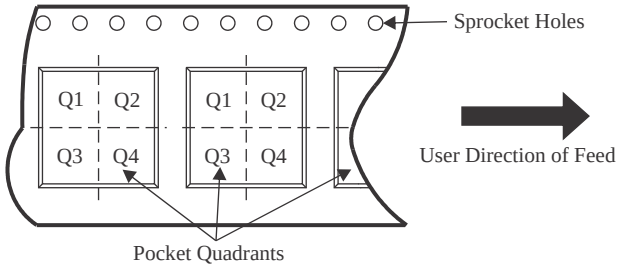


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

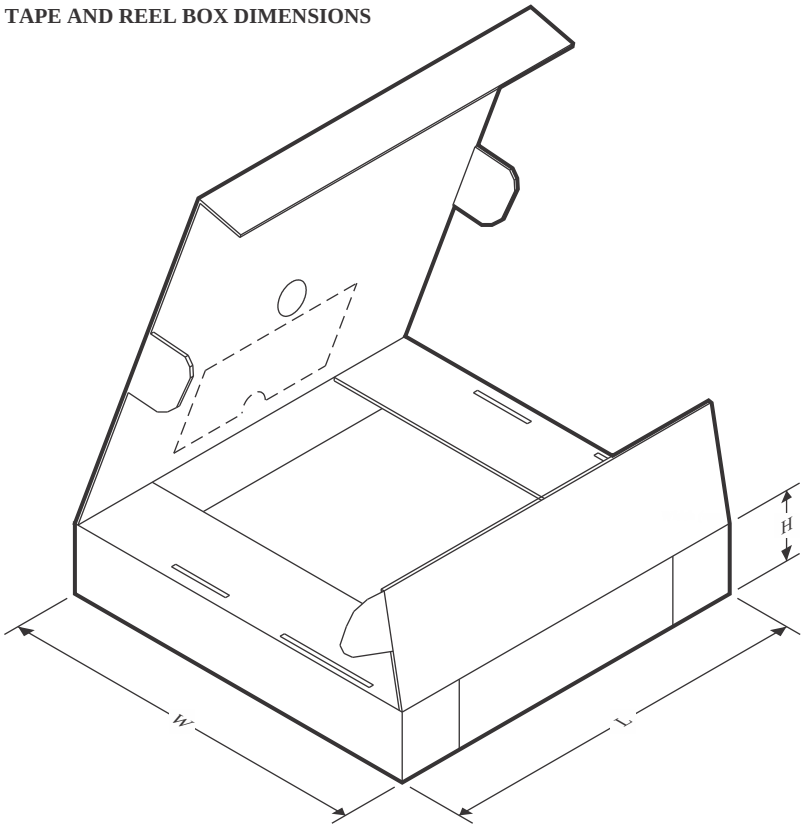
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UR907QSQ/NOPB	WQFN	NJK	36	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UR907QSQE/NOPB	WQFN	NJK	36	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UR907QSQX/NOPB	WQFN	NJK	36	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UR907QSQ/NOPB	WQFN	NJK	36	1000	356.0	356.0	36.0
DS90UR907QSQE/NOPB	WQFN	NJK	36	250	208.0	191.0	35.0
DS90UR907QSQX/NOPB	WQFN	NJK	36	2500	356.0	356.0	36.0

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- Alternative Solution
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