



THE DATASHEET OF CL21B103KC65PNC



Specification of Automotive MLCC

- Supplier : Samsung electro-mechanics
- Product : Multi-layer Ceramic Capacitor

- Samsung P/N : **CL21B103KC65PNC**
- Description : **CAP, 10nF, 100V, ±10%, X7R, 0805**
- AEC-Q 200 Specified

A. Samsung Part Number

CL 21 B 103 K C 6 5 P N C
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

① Series	Samsung Multi-layer Ceramic Capacitor		
② Size	0805 (inch code)	L: 2.0 ± 0.1 mm	W: 1.25 ± 0.1 mm
③ Dielectric	X7R	⑧ Inner electrode Termination	Ni , Open mode Cu , Ag-epoxy
④ Capacitance	10 nF	⑨ Plating	Sn 100% (Pb Free)
⑤ Capacitance tolerance	±10 %	⑩ Product	Automotive
⑥ Rated Voltage	100 V	⑪ Grade code	Standard
⑦ Thickness	0.6 ± 0.1 mm		⑪ Packaging Cardboard Type, 7" reel

B. Reliability Test and Judgement condition

	Performance	Test condition
High Temperature Exposure	Appearance : No abnormal exterior appearance Capacitance Change : Within ±10% Tan δ : 0.03 max IR : More than 10,000MΩ or 500MΩ×μF Whichever is Smaller	Unpowered, 1000hrs@T=150°C Measurement at 24±2hrs after test conclusion
Temperature Cycling	Appearance : No abnormal exterior appearance Capacitance Change : Within ±10% Tan δ : 0.03 max IR : More than 10,000MΩ or 500MΩ×μF Whichever is Smaller	1000Cycles Measurement at 24±2hrs after test conclusion 1 cycle condition : -55+0/-3°C (15±3min) -> Room Temp(1min.) -> 125+3/-0°C (15±3min) -> Room Temp(1min.)
Destructive Physical Analysis	No Defects or abnormalities	Per EIA 469
Moisture Resistance	Appearance : No abnormal exterior appearance Capacitance Change : Within ±12.5% Tan δ : 0.03 max IR : More than 10,000MΩ or 500MΩ×μF Whichever is Smaller	10Cycles, t=24hrs/cycle Heat (25~65°C) and humidity (80~98%), Unpowered measurement at 24±2hrs after test conclusion
Humidity Bias	Appearance : No abnormal exterior appearance Capacitance Change : Within ±12.5% Tan δ : 0.035 max IR : More than 500MΩ or 25MΩ×μF Whichever is Smaller	1000hrs 85°C/85%RH, Rated Voltate and 1.3~1.5V, Add 100kohm resistor Measurement at 24±2hrs after test conclusion The charge/discharge current is less than 50mA.
High Temperature Operating Life	Appearance : No abnormal exterior appearance Capacitance Change : Within ±12.5% Tan δ : 0.035 max IR : More than 1000MΩ or 50MΩ×μF Whichever is Smaller	1000hrs @ TA=125°C, 200% Rated Voltage, Measurement at 24±2hrs after test conclusion The charge/discharge current is less than 50mA.

	Performance	Test condition								
External Visual	No abnormal exterior appearance	Microscope ($\times 10$)								
Physical Dimensions	Within the specified dimensions	Using The calipers								
Mechanical Shock	Appearance : No abnormal exterior appearance Capacitance Change : Within $\pm 10\%$ Tan δ , IR : initial spec.	Three shocks in each direction should be applied along 3 mutually perpendicular axes of the test specimen (18 shocks) <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Peakvalue</th> <th>Duration</th> <th>Wave</th> <th>Velocity</th> </tr> </thead> <tbody> <tr> <td>1,500G</td> <td>0.5ms</td> <td>Half sine</td> <td>4.7m/sec.</td> </tr> </tbody> </table>	Peakvalue	Duration	Wave	Velocity	1,500G	0.5ms	Half sine	4.7m/sec.
Peakvalue	Duration	Wave	Velocity							
1,500G	0.5ms	Half sine	4.7m/sec.							
Vibration	Appearance : No abnormal exterior appearance Capacitance Change : Within $\pm 10\%$ Tan δ , IR : initial spec.	5g's for 20min., 12cycles each of 3 orientations, Use 8"x5" PCB 0.031" Thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10~2000Hz.								
Resistance to Solder Heat	Appearance : No abnormal exterior appearance Capacitance Change : Within $\pm 10\%$ Tan δ , IR : initial spec.	Solder pot : $260\pm 5^{\circ}\text{C}$, $10\pm 1\text{sec}$.								
Thermal Shock	Appearance : No abnormal exterior appearance Capacitance Change : Within $\pm 10\%$ Tan δ , IR : initial spec.	$-55^{\circ}\text{C}/+125^{\circ}\text{C}$. Note: Number of cycles required-300, Maximum transfer time-20 sec, Dwell time-15min. Air-Air								
ESD	Appearance : No abnormal exterior appearance Capacitance Change : Within $\pm 10\%$ Tan δ , IR : initial spec.	AEC-Q200-002								
Solderability	95% of the terminations is to be soldered evenly and continuously	a) Preheat at 155°C for 4 hours, Immerse in solder for 5s at $245\pm 5^{\circ}\text{C}$ b) Steam aging for 8 hours, Immerse in solder for 5s at $245\pm 5^{\circ}\text{C}$ c) Steam aging for 8 hours, Immerse in solder for 120s at $260\pm 5^{\circ}\text{C}$ solder : a solution ethanol and rosin								
Electrical Characterization	Capacitance : Within specified tolerance Tan δ (DF) : 0.025 max. IR(25°C) : More than $10,000\text{M}\Omega$ or $500\text{M}\Omega \times \mu\text{F}$ IR(125°C) : More than $1,000\text{M}\Omega$ or $10\text{M}\Omega \times \mu\text{F}$ Whichever is Smaller Dielectric Strength	The Capacitance /D.F. should be measured at 25°C , $1\text{kHz} \pm 10\%$, $1.0 \pm 0.2\text{Vrms}$ I.R. should be measured with a DC voltage not exceeding Rated Voltage @ 25°C , @ 125°C for 60~120 sec. Dielectric Strength : 250% of the rated voltage for 1~5 seconds								
Board Flex	Appearance : No abnormal exterior appearance Capacitance Change : Within $\pm 10\%$	Bending to the limit (2mm) for 5 seconds								
Terminal Strength(SMD)	Appearance : No abnormal exterior appearance Capacitance Change : Within $\pm 10\%$	18N, for 60 ± 1 sec.								
Beam Load	Destruction value should not be exceed Chip Length < 2.5mm a) Chip Thickness > 0.5mm : 20N b) Chip Thickness \leq 0.5mm : 8N	Beam speed $0.5 \pm 0.05\text{mm}/\text{sec}$								
Temperature Characterisitcs	X7R (From -55°C to 125°C , Capacitance change should be within $\pm 15\%$)									

C. Recommended Soldering method :

Reflow (Reflow Peak Temperature : $260+0/-5^{\circ}\text{C}$, 10sec. Max)

Meet IPC/JEDEC J-STD-020 D Standard

* For the more detail Specification, Please refer to the Samsung MLCC catalogue.

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