



**THE DATASHEET OF
BU26156RFS-E2**



24bit Audio CODEC series

3W+3W Class AB/D Speaker AMP Stereo Audio CODEC

BU26156RFS

General Description

BU26156RFS is Low Power Stereo Audio CODECs with built-in various acoustic effects. BU26156RFS has stereo line and monaural mic inputs that can input to 2Vrms, stereo speaker amplifier that can change Class AB / D and stereo Headphone Outputs. BU26156 also has built-in voltage regulator for the stability of CODEC characteristic that is sensitive to the outside noise.

Features

- 24bit Stereo ADC, DAC
- 2Vrms Input available, Stereo Line Input with ALC
- Monoraul MIC Input with ALC
- Switch Class AB/D 3W Stereo Speaker Amplifier
- AM Avoidance Function
- Stereo Headphone Output Amplifier
- Digital signal processing
- High Power Supply Rejection Ratio characteristic

Applications

- Radio cassette recorder
- PC Speaker

Important Characteristic

- Supply Voltage
 - SPLVDD,SPRVDD: 2.7V to 5.5V
 - HVDD1: 2.7V to 3.6V
 - HPVDD: 2.7V to 3.6V
 - IOVDD: 1.65V to 5.5V
- Mic-ADC SNR: 87[dB](Typ.)
- Line-ADC SNR: 93[dB](Typ.)
- DAC-SP SNR: 86[dB](Typ.)
- DAC-LOUT SNR: 95[dB](Typ.)
- Operating Temperature: -20°C to +85°C

Package

HTSSOP-A44R

W(Typ.) x D(Typ.) x H(Max.)
18.50mm x 9.50mm x 1.00mm



Figure 1. HTSSOP-A44R

Basic Block Diagram

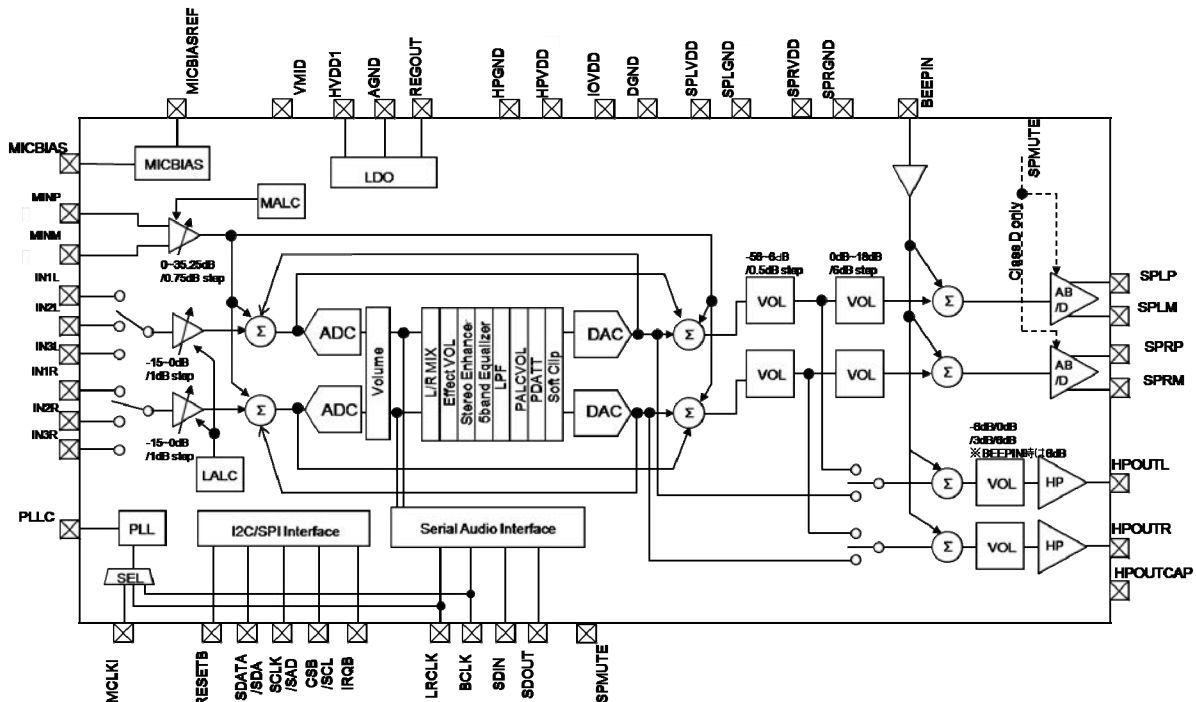


Figure 2.

Pin Layout HTSSOP-A44R

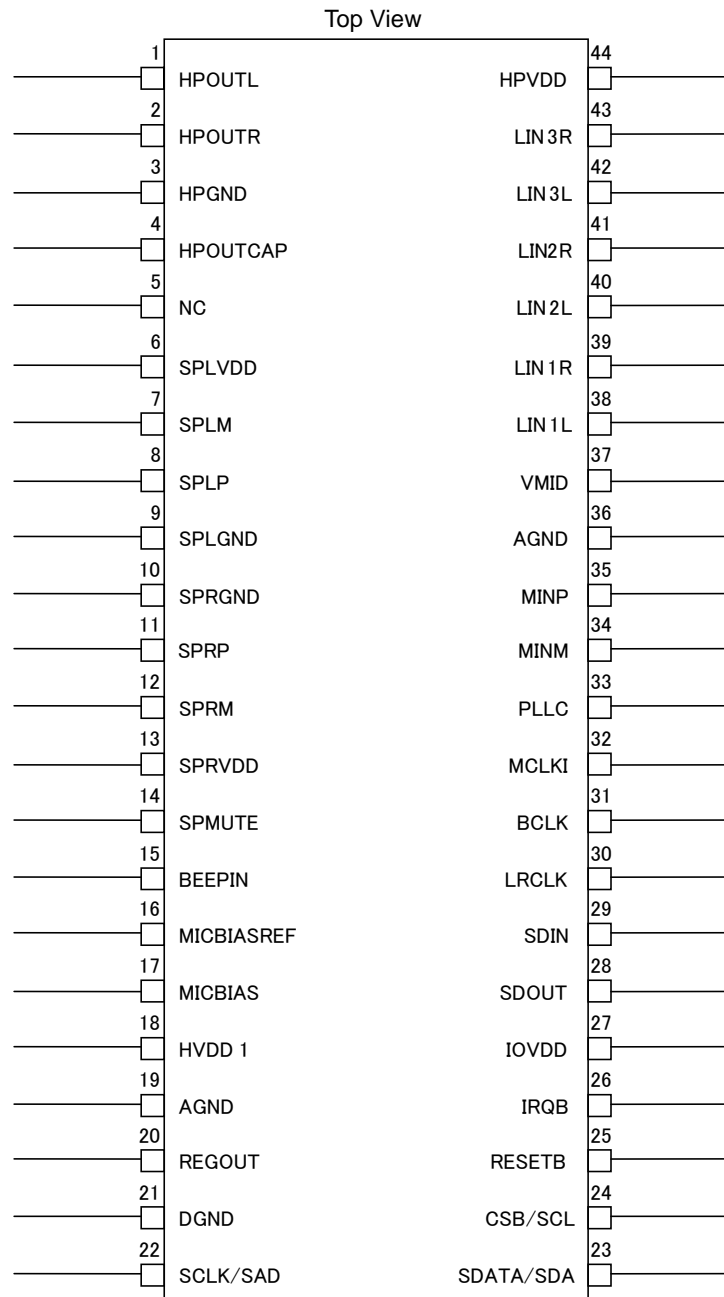


Figure 3.

Pin Description

| No | Name | I/O | Power | Function | Reset | No use |
|----|------------|-----|-------|--|---------|--------|
| 25 | RESETB | I | IOVDD | Reset pin “L” level : Reset enable. “H” level : Reset disable. | (input) | - |
| 23 | SDATA /SDA | IO | IOVDD | 3 wire interface: data input output pin It is indicated as SDATA on the description of AC characteristics. 2 wire interface : data input output pin ^(Note1) It is indicated as SDA on the description of AC characteristics. | (input) | - |
| 22 | SCLK /SAD | I | IOVDD | 3 wire interface : Serial clock input pin It is indicated as SCLK on the description of AC characteristics. 2 wire interface: Slave address pin Future explanation indicates SAD. Choose from the following two kinds. SAD Pin=HGND : "0011010" | (input) | DGND |

| | | | | SAD Pin=IOVDD : "0011011" | | |
|--------|------------|----|--------|---|---------|--|
| 24 | CSB /SCL | I | IOVDD | 3 wire interface : chip select input pin It is indicated as CSB on the description of AC characteristics. 2 wire interface : Serial clock input pin (Note1) It is indicated as SCL on the description of AC characteristics. | (input) | - |
| 30 | LRCLK | IO | IOVDD | SAI LR clock input/output pin | (input) | DGND |
| 31 | BCLK | IO | IOVDD | SAI bit clock input/output pin | (input) | DGND |
| 29 | SDIN | I | IOVDD | SAI serial data input pin | (input) | DGND |
| 28 | SDOUT | O | IOVDD | SAI serial data output pin | DGND | Open |
| 32 | MCLKI | I | IOVDD | Master Clock pin | (input) | DGND |
| 26 | IRQB | O | IOVDD | Interrupt output Pin | IOVDD | Open |
| 38 | LIN1L | I | REGOUT | Line analog input Lch pin 1 | (input) | Open, or coupling capacitor connected to AGND near by BU26156 |
| 39 | LIN1R | I | REGOUT | Line analog input Rch pin 1 | (input) | |
| 40 | LIN2L | I | REGOUT | Line analog input Lch pin 2 | (input) | |
| 41 | LIN2R | I | REGOUT | Line analog input Rch pin 2 | (input) | |
| 42 | LIN3L | I | REGOUT | Line analog input Lch pin 3 | (input) | |
| 43 | LIN3R | I | REGOUT | Line analog input Rch pin 3 | (input) | |
| 35 | MINP | I | REGOUT | Analog microphone + input | (input) | |
| 34 | MINM | I | REGOUT | Analog microphone - input | (input) | |
| 15 | BEEPIN | I | REGOUT | Line input pin. The input signal for this pin can output Headphone output pins or Speaker output pins. | (input) | |
| 16 | MICBIASREF | O | HVDD1 | External filter pin for microphone bias. A capacitor is connected between MICBIASREF and AGND. | ANGD | Open |
| 1 | MICBIAS | O | HVDD1 | Microphone bias voltage output pin A capacitor is connected between MICBIASREF and AGND. | AGND | Open |
| 37 | VMID | O | REGOUT | Analog reference voltage pin A capacitor is connected between VMID and AGND. | AGND | - |
| 20 | REGOUT | O | HVDD1 | Regulator output pin A capacitor is connected between REGOUT and HGND1. Please put in the chip close as much as possible. | AGND | - |
| 8 | SPLP | O | SPLVDD | speaker Lch output + pin | SPLGND | Open |
| 7 | SPLM | O | SPLVDD | speaker Lch output - pin | SPLGND | Open |
| 11 | SPRP | O | SPRVDD | speaker Rch output + pin | SPRGND | Open |
| 12 | SPRM | O | SPRVDD | speaker Rch output - pin | SPRGND | Open |
| 14 | SPMUTE | I | IOVDD | Test control pin "L" level : Release MUTE "H" level : MUTE | DGND | Open |
| 1 | HPOUTL | O | HPVDD | Headphone Lch output pin | HPGND | Open |
| 2 | HPOUTR | O | HPVDD | Headphone Rch output pin | HPGND | Open |
| 32 | LOUTCAP | O | HVDD1 | Headphone Output capacitance pin | AGND | Open |
| 33 | PLL | O | REGOUT | PLL filter pin The width of the clock frequency to input can be expanded. | AGND | Open |
| 27 | IOVDD | P | - | Interface Power Supply pin A capacitor is connected between IOVDD and HGND1. | - | - |
| 6 | SPLVDD | P | - | Speaker Lch Power Supply pin It is used on the same voltage as SPRVDD. A capacitor is connected between SPLVDD and SPLGND. | - | - |
| 9 | SPLGND | P | - | Speaker Lch ground pin | - | - |
| 13 | SPRVDD | P | - | Speaker Rch Power Supply pin It is used on the same voltage as SPLVDD. A capacitor is connected between SPRVDD and SPRGND. | - | - |
| 10 | SPRGND | P | - | Speaker Rch ground pin | - | - |
| 18 | HVDD1 | P | - | High voltage power supply 1 pin A capacitor is connected between HVDD1 and HGND1. | - | - |
| 19, 36 | AGND | P | - | Analog ground pin | - | - |
| 21 | DGND | P | - | Digital ground pin | | |

| | | | | |
|----|-------|---|--|------|
| 44 | HPVDD | P | Headphone Power Supply pin. A capacitor is connected between HPVDD and HPGND. | |
| 3 | HPGND | P | Headphone ground pin. | |
| 5 | NC | - | No Connection pin. Set open this pin. | Open |

(Note1) In case of 2 wire serial, if this pin is used with external pull-up resistor, it possibly gets noise from power. Therefore tamper noise design is required in the noisy environment.

Application Examples

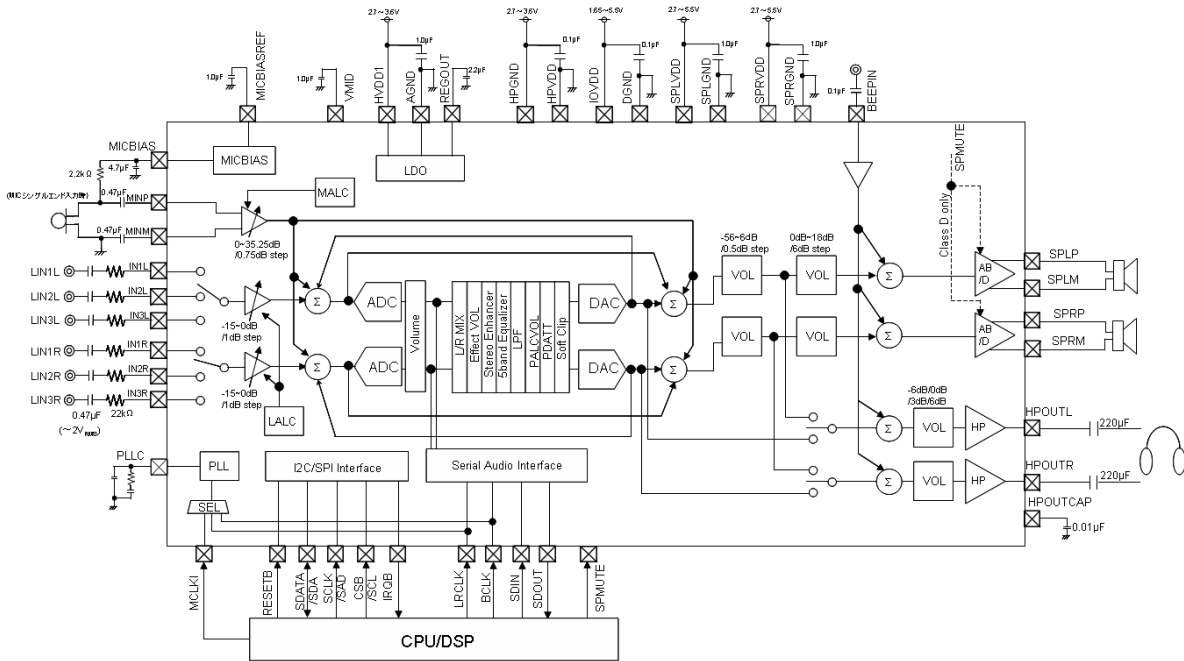


Figure 4. Application Examples1(Use internal speaker amplifier)

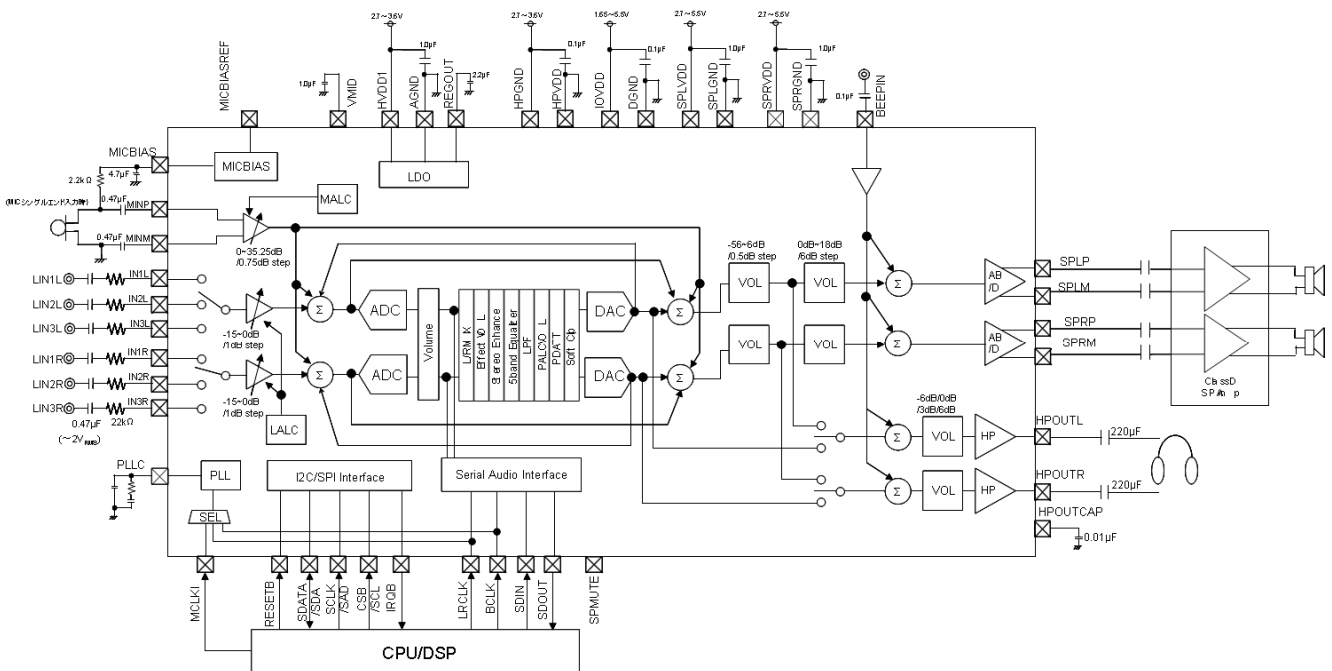


Figure 5. Application Examples2 (Use external speaker amplifier)

Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|-------------------------------|------------------|--|---|------|
| SPLVDD, SPRVDD Supply Voltage | SPLVDD SPRVDD | - | -0.3 to 7.0 | V |
| HPVDD Supply Voltage | HPVDD | - | -0.3 to 4.5 | V |
| HVDD1 Supply Voltage | HVDD1 | - | -0.3 to 4.5 | V |
| IOVDD Supply Voltage | IOVDD | - | -0.3 to 7.0 | V |
| Input Voltage | V _{IN} | MCLKI, LRCLK, BCLK, SDIN, SDATA/SDA, SCLK/SAD, CSB/SCL, SPMUTE | -0.3 to IOVDD+0.3 | V |
| | | LIN1L, LIN1R, LIN2L, LIN2R, MINL, MINR, BEEPIN | -0.3 to REGOUT+0.3 | V |
| Storage Temperature | T _{stg} | - | -55 to +150 | °C |
| Package power dissipation | θ _{jc} | HTSSOP-A44R | ² (T _{jmax} =+125°C) | °C/W |
| Output Current 1 | IOSP | SPLM, SPLP, SPRM, SPRP | -1.0 to +1.0 | A |
| Output Current 2 | IOLO | HPOUTL, HPOUTR | -100 to +100 | mA |
| Output Current 3 | IOREGO | REGOUT | -30 to 0 | mA |
| Output Current 4 | IOO | All digital pins | -8 to +8 | mA |

Do not short the output pin to another output pin, power supply pin or GND pin.
(Output pin includes an IO pin which is in output mode)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Condition

| Parameter | Symbol | Condition | Rating | Unit |
|-------------------------------|------------------|---------------|-------------|------|
| SPLVDD, SPRVDD Supply Voltage | SPLVDD SPRVDD | SPLVDD=SPRVDD | 2.7 to 5.5 | V |
| HPVDD Supply Voltage | HPVDD | - | 2.7 to 3.6 | V |
| HVDD1 Supply Voltage | HVDD1 | - | 2.7 to 3.6 | V |
| IOVDD Supply Voltage | IOVDD | - | 1.65 to 5.5 | V |
| Operating Temperature | T _{op} | - | -20 to +85 | °C |

*The radiation-proof design is not carried out.

Electrical Characteristics

DC Characteristics

(ALL GND terminals=0V, HVDD1=3.3V, IOVDD=3.3V, SPLVDD=SPRVDD=HPVDD=3.3V, Ta=25°C)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Related Pin |
|---|-----------|--|------------|--------|------------------|------|--|
| "H" Input Voltage 1 | VIH1 | DGND=0V | IOVDD×0.8 | - | IOVDD+0.3 | V | RESETB, SDATA/SDA, SCLK/SAD, CSB/SCL, SPMUTE and MCLKI pins. |
| "H" Input Voltage 2 | VIH2 | DGND=0V | IOVDD×0.7 | - | IOVDD+0.3 | V | LRCLK, BCLK and SDIN pins. |
| "L" Input Voltage | VIL | DGND=0V | -0.3 | - | IOVDD×0.2 | V | All Digital Input |
| "H" Output Voltage | VOH | IOH=-1mA | IOVDD×0.85 | - | - | V | Except SDA |
| "L" Output Voltage 1 | VOL1 | IOL=1mA | - | - | IOVDD×0.15 | V | Except SDA |
| "L" Output Voltage 2 | VOL2 | IOL=3mA, IOVDD ≥2V IOVDD <2V | - - | - - | 0.4 IOVDD×0.2 | V | SDA |
| "H" Input Leakage Current 1 | I IH1 | VIH= IOVDD | - | - | 10 | μA | Except SPMUTE |
| "L" Input Leakage Current | I IL | VIL=DGND | -10 | - | - | μA | All Digital Input |
| "Z" Output Leakage Current | IOZH | VOH=IOVDD | - | - | 10 | μA | SDA |
| "Z" Output Leakage Current | IOZL | VOL=DGND | -10 | - | - | μA | SDA |
| Stanby Current | | | | | | | |
| HVDD1 | IDDSH1 | RESETB="L" | - | 0.1 | 10 | μA | |
| SPLVDD+SPRVDD | IDDSPP | | - | 0.1 | 10 | μA | |
| HPVDD | IDDSHP | | - | 0.1 | 10 | μA | |
| IOVDD | IDDSIO | | - | 0.1 | 10 | μA | |
| Operating Current 1, DAC→mixvol→Headphone Output (fs48kHz, No Load, No signal input, Sound effect off) | | | | | | | |
| HVDD1 | IDDO1H1 | Headphone Output, No Load, No signal input, Sound effect off | - | 6.2 | 9.5 | mA | |
| SPLVDD+SPRVDD | IDDO1SP | | - | 0.02 | 0.1 | mA | |
| HPVDD | IDDO1HP | | - | 1.0 | 1.3 | mA | |
| IOVDD | IDDO1IO | | - | 0.03 | 0.1 | mA | |
| Operating Current 2, DAC→mixvol→D-class Speaker Output (fs48kHz, No Load, No signal input, Sound effect off) | | | | | | | |
| HVDD1 | IDDO2H1 | D-class Speaker Output, No Load, No signal input, Sound effect off | - | 6.2 | 8.2 | mA | |
| SPLVDD+SPRVDD | IDDO2SP | | - | 3.3 | 7.4 | mA | SPVDD=3.3V |
| SPLVDD+SPRVDD | IDDO2SP_5 | | - | 5.0 | - | mA | SPVDD=5V |
| HPVDD | IDDO2HP | | - | 0.03 | 0.1 | mA | |
| IOVDD | IDDO2IO | | - | 0.03 | 0.1 | mA | |
| Operating Current 3, DAC→mixvol→AB-class Speaker Output (fs48kHz, No Load, No signal input, Sound effect off) | | | | | | | |
| HVDD1 | IDDO3H1 | AB-class Speaker Output, No Load, No signal input, Sound effect off | - | 6.2 | 8.2 | mA | |
| SPLVDD+SPRVDD | IDDO3SP | | - | 5.0 | 9.6 | mA | SPVDD=3.3V |
| SPLVDD+SPRVDD | IDDO3SP_5 | | - | 6.0 | - | mA | SPVDD=5V |

| | | | | | | | |
|---|---------|---|---|------|------|----|--|
| HPVDD | IDDO3HP | | - | 0.03 | 0.1 | mA | |
| IOVDD | IDDO3IO | | - | 0.03 | 0.1 | mA | |
| Operating Current 4, MicIN→linemix→ADC (fs48kHz, Sin1kHz-Full Scale input, Micbias Enable, Mic ALC off, Sound Effect off) | | | | | | | |
| HVDD1 | IDDO4H1 | fs48kHz, No signal input,, Micbias Enable, Mic ALC off, Sound Effect off | - | 12.3 | 16.9 | mA | |
| SPLVDD+SPRVDD | IDDO4SP | | - | 0.02 | 0.1 | mA | |
| HPVDD | IDDO4HP | | - | 0.03 | 0.1 | mA | |
| IOVDD | IDDO4IO | | - | 0.03 | 0.1 | mA | |
| Operating Current 5, Lineln→llinemix→ADC (fs48kHz, Sin1kHz-Full Scale input, LineALC off, Sound Effect off) | | | | | | | |
| HVDD1 | IDDO5H1 | fs48kHz, No signal input, Line ALC off, Sound Effect off | - | 11.2 | 13.8 | mA | |
| SPLVDD+SPRVDD | IDDO5SP | | - | 0.02 | 0.1 | mA | |
| HPVDD | IDDO5HP | | - | 0.03 | 0.1 | mA | |
| IOVDD | IDDO5IO | | - | 0.03 | 0.1 | mA | |

Operating Power

(ALL GND terminals=0V, IOVDD=3.3V, HVDD1=3.3V, SPLVDD=SPRVDD=5.0V, HPVDD=3.3V, Ta=25°C)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|---------|--|-------------------|-------------------|-------------------|------|
| Regulator Output | | | | | | |
| REGOUT Output Level | VREGOUT | - | 1.7 | 1.8 | 1.9 | V |
| BEEP Input | | | | | | |
| Full Scale Input Signal Level | VBINFS | - | - | - | 1 | Vpp |
| Line Input (R _{LIN} =22 kΩ / Line Gain=-9dB / Digital Volume=0.0dB / Line ALC=OFF) | | | | | | |
| Full Scale Input Signal Level | VLINFS | LIN1L, LIN2L, LIN3L, LIN1R, LIN2R, LIN3R | - | - | 2.0 | Vrms |
| Mic Input (MIC Gain=20.25dB / Digital Volume=0.0dB / Mic ALC=OFF) | | | | | | |
| Full Scale Input Signal Level | VMINFS1 | MINP,MINM | - | - | 0.124 | Vp-p |
| Input Resistance | RMIN1 | MINP,MINM | 20 | 30 | 40 | kΩ |
| Mic Input (MIC Gain=9.0dB / Digital Volume=0.0dB / Mic ALC=OFF) | | | | | | |
| Full Scale Input Signal Level | VMINFS2 | MINP,MINM | - | - | 0.454 | Vp-p |
| Input Resistance | RMIN2 | MINP,MINM | 20 | 30 | 40 | kΩ |
| Analog Reference Level (VMID-pin) | | | | | | |
| Analog Reference Voltage | VREF | - | 0.9x REGOUT/2 | 1.0x REGOUT/2 | 1.1x REGOUT/2 | V |
| Microphone Bias (MICBIAS-pin) | | | | | | |
| Output Voltage (VMIC<HVDD1*0.85) | VMIC | IMIC = -2mA, MICBCON=0 | 1.51x REGOUT/2 | 1.67x REGOUT/2 | 1.83x REGOUT/2 | V |
| | | IMIC = -2mA, MICBCON=1 | 2.00x REGOUT/2 | 2.22x REGOUT/2 | 2.44x REGOUT/2 | V |
| | | IMIC = -2mA, MICBCON=2 | 2.51x REGOUT/2 | 2.78x REGOUT/2 | 3.05x REGOUT/2 | V |
| | | IMIC = -2mA, MICBCON=3 | 3.00x REGOUT/2 | 3.33x REGOUT/2 | 3.66x REGOUT/2 | V |
| Output Current | IMIC | - | - | - | 2 | mA |

(HGND1=0V, IOVDD=3.3V, HVDD1=3.3V, SPLVDD=SPRVDD=5.0V, HPVDD=3.3V, Ta=25°C, 1kHz signal, fs=48kHz)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------|--------------------|-----|-----|-----|------|
| Analog Line Input to ADC out (R _{LIN} =22kΩ / Line Gain=0dB / LineMix Gain = 0dB / Digital Volume=0.0dB / Line ALC=OFF) | | | | | | |
| S/(N+D) | SND1 | -1dBFS/ A-weighted | - | 81 | - | dB |
| S/N | SNR1 | A-weighted | - | 93 | - | dB |

| | | | | | | |
|---|-------|---|-----|-----|-----|-----|
| Power Supply Rejection Ratio | PSRR1 | HVDD1 on 100mVp-p, 1kHz ripple, no signal input | - | 90 | - | dB |
| Analog Mic Inputs to ADC out (MIC Gain=20.25dB / Line Mix Gain = 0dB / Digital Volume=0.0dB / Mic ALC=OFF) | | | | | | |
| S/(N+D) | SND2 | -1dBFS/ A-weighted | - | 79 | - | dB |
| S/N | SNR2 | A-weighted | - | 81 | - | dB |
| Power Supply Rejection Ratio | PSRR2 | HVDD1 on 100mVp-p, 1kHz ripple, no signal input | - | 89 | - | dB |
| Analog Mic Inputs to ADC out (MIC Gain=9.0dB / Digital Volume=0.0dB / Mic ALC=OFF) | | | | | | |
| S/(N+D) | SND3 | -1dBFS/ A-weighted | - | 80 | - | dB |
| S/N | SNR3 | A-weighted | - | 87 | - | dB |
| Power Supply Rejection Ratio | PSRR3 | HVDD1 on 100mVp-p, 1kHz ripple, no signal input | - | 90 | - | dB |
| DAC to Headphone OUT (HPOUTL/HPOUTR, with 220μFcuppling 16Ω load) | | | | | | |
| Output Power | Po4 | THD+N=1%, RL=16 Ω | - | 60 | - | mW |
| Total Harmonic Distortion | THD4 | -6dBFS input / A-weighted | - | 79 | - | dB |
| Signal to Noise Ratio | SNR4 | A-weighted | - | 90 | - | dB |
| Power Supply Rejection Ratio | PSRR4 | HPVDD on 100mVp-p,1kHz ripple, no signal input | - | 60 | - | dB |
| | | HVDD1 on 100mVp-p,1kHz ripple | - | 80 | - | dB |
| DAC to Class-AB Speaker OUT (SPLP/SPLM, SPRP/SPRM, with 8Ω / 50pF load) | | | | | | |
| Output Power | Po5-1 | SPMIXG=12dB, RL=8 Ω ,THD=1% | - | 1.4 | - | W |
| | Po5-2 | SPMIXG=12dB, RL=8 Ω ,THD=10% | - | 1.7 | - | W |
| | Po5-3 | SPMIXG=12dB, RL=4 Ω ,THD=1% | 1.5 | 2.5 | - | W |
| | Po5-4 | SPMIXG=12dB, RL=4 Ω ,THD=10% | 2 | 3 | - | W |
| Total Harmonic Distortion | THD5 | Po=1W, RL=8 Ω / A-weighted | - | 62 | - | dB |
| Signal to Noise Ratio | SNR5 | A-weighted | - | 91 | - | dB |
| Power Supply Rejection Ratio | PSRR5 | SPLVDD/SPRVDD on 100mVp-p,1kHz ripple | - | 60 | - | dB |
| | | HVDD1 on 100mVp-p,1kHz ripple | - | 80 | - | dB |
| DAC to Class-D Speaker OUT (SPLVDD=SPRVDD=5V,SPLP/SPLM, SPRP/SPRM, with 8Ω / 50pF load) | | | | | | |
| Output Power | Po6-1 | SPMIXG=12dB, RL=8 Ω ,THD=1% | - | 1.4 | - | W |
| | Po6-2 | SPMIXG=12dB, RL=8 Ω ,THD=10% | - | 1.7 | - | W |
| | Po6-3 | SPMIXG=12dB, RL=4 Ω ,THD=1% | 1.5 | 2.5 | - | W |
| | Po6-4 | SPMIXG=12dB, RL=4 Ω ,THD=10% | 2 | 3 | - | W |
| Total Harmonic Distortion | THD6 | Po=1W, RL=8 Ω / A-weighted | - | 62 | - | dB |
| Signal to Noise Ratio | SNR6 | A-weighted | - | 89 | - | dB |
| Power Supply Rejection Ratio | PSRR6 | SPLVDD/SPRVDD on 100mVp-p,1kHz ripple | - | 72 | - | dB |
| | | HVDD1 on 100mVp-p,1kHz ripple | - | 80 | - | dB |
| Class D oscillator frequency (AM Avoidance) | | | | | | |
| Oscillator frequency | AM0 | AMA[1:0]=0b00 | 360 | 400 | 440 | kHz |
| | AM1 | AMA[1:0]=0b01 | 450 | 500 | 550 | kHz |
| | AM2 | AMA[1:0]=0b10 | 540 | 600 | 660 | kHz |

| | AM3 | AMA[1:0]=0b11 | 630 | 700 | 770 | kHz |
|--------------------------------------|--------|---|-----|-----|-----|-----|
| Microphone Bias (MICBIAS-pin) | | | | | | |
| Output Noise Voltage | VMICN7 | 22Hz to 22kHz, VMIC =1.67 x REGOUT/2 | - | 5 | - | μV |
| Power Supply Rejection Ratio | PSRR7 | HVDD1 on 100mVp-p, 1kHz ripple Load=1mA | - | 80 | - | dB |

AC Characteristics

Clock
PLL not use

(DGND=0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C)

| Parameter | Symbol | Min | Max. | Unit |
|-----------------|--------|--------|---------|------|
| MCLKI Frequency | fC | 2.048M | 49.152M | Hz |
| MCLKI Period | tC | 1/fC | 1/fC | s |
| MCLKI Length | tCH | tC*0.4 | - | s |
| MCLKI Length | tCL | tC*0.4 | - | s |

PLL use (External Loop back filter not used)

(DGND =0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C)

| Parameter | Symbol | Min | Max. | Unit |
|-----------------|--------|--------|------|------|
| MCLKI Frequency | fC | 2M | 54M | Hz |
| MCLKI Period | tC | 1/fC | 1/fC | s |
| MCLKI Length | tCH | tC*0.4 | - | s |
| MCLKI Length | tCL | tC*0.4 | - | s |

PLL use (External Loop back filter used)

(DGND =0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C)

| Parameter | Symbol | Min | Max. | Unit |
|-----------------|--------|--------|------|------|
| MCLKI Frequency | fC | 32k | 2M | Hz |
| MCLKI Period | tC | 1/fC | 1/fC | s |
| MCLKI Length | tCH | tC*0.4 | - | s |
| MCLKI Length | tCL | tC*0.4 | - | s |

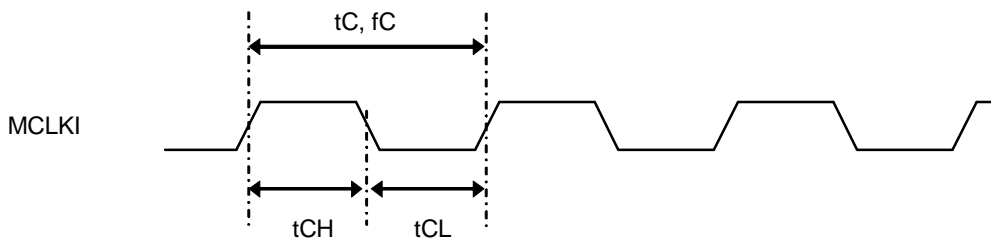


Figure 6.

Reset

(DGND =0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C)

| Parameter | Symbol | Min | Max. | Unit |
|--------------------|--------|-----|------|------|
| RESETB pulse width | tW_RST | 5 | - | μs |

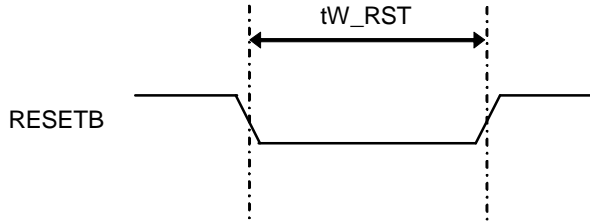


Figure 7.

When Reset pin is made Low level, internal LDO is power down mode. It is necessary for 1ms until REGOUT pin becomes Low level. The recommendation of tW_RST is 1ms over.

2 wire serial interface

(DGND =0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C, CL=30pF)

| Parameter | Symbol | Standard Mode | | Fast Mode | | Unit |
|--|---------------------|---------------|------|-----------|------|------|
| | | Min | Max. | Min | Max. | |
| SCL Frequency | f _{SCL} | - | 100 | - | 400 | kHz |
| SCL "L" Length | t _{LOW} | 4.7 | - | 1.3 | - | μs |
| SCL "H" Length | t _{HIGH} | 4.0 | - | 0.6 | - | μs |
| Hold time under Repeat [Start] Condition | t _{HD:STA} | 4.0 | - | 0.6 | - | μs |
| Setup Time under Repeat[Start] Condition | t _{SU:STA} | 4.0 | - | 0.6 | - | μs |
| Data Hold Time | t _{HD:DAT} | 0 | 3.45 | 0 | 0.9 | μs |
| Data Setup Time | t _{SU:DAT} | 250 | - | 100 | - | ns |
| Setup Time under [Stop] Condition | t _{SU:STO} | 4.0 | - | 0.6 | - | μs |

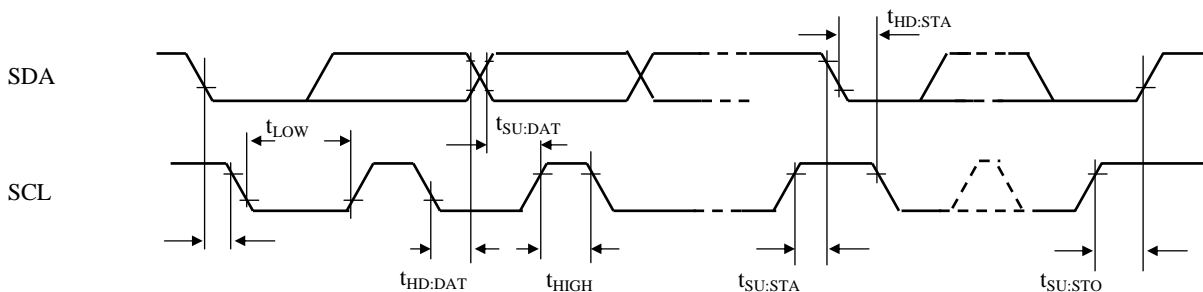


Figure 8.

3 wire serial interface

(DGND=0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C, CL=30pF)

| Parameter | Symbol | Min | Max. | Unit |
|---------------------------------------|--------|-----|------|------|
| SCLK Low to Chip Select enable | tSLCL | 100 | - | ns |
| Chip Select enable to SCLK Low | tCLSL | 100 | - | ns |
| Chip Select enable to SCLK High | tCLSH | 100 | - | ns |
| SCLK High to Chip Select enable | tSHCL | 100 | - | ns |
| SCLK High Pulse Width | tSH | 50 | - | ns |
| SCLK Low Pulse Width | tSL | 50 | - | ns |
| Input Data Setup time | tIDS | 30 | - | ns |
| Input Data Hold time | tIDH | 30 | - | ns |
| SCLK last edge to Chip Select disable | tCHS2 | 100 | - | ns |
| Chip Select High Pulse Width | tCH | 100 | - | ns |
| Output Data Valid | tODV | - | 40 | ns |
| Chip Select High to Data Transition | tCHDTS | - | 40 | ns |

Two kinds of timing is supported depends on the SCLK pin level at data transfer start. Read or Write is selected by LSB level of INDEX.

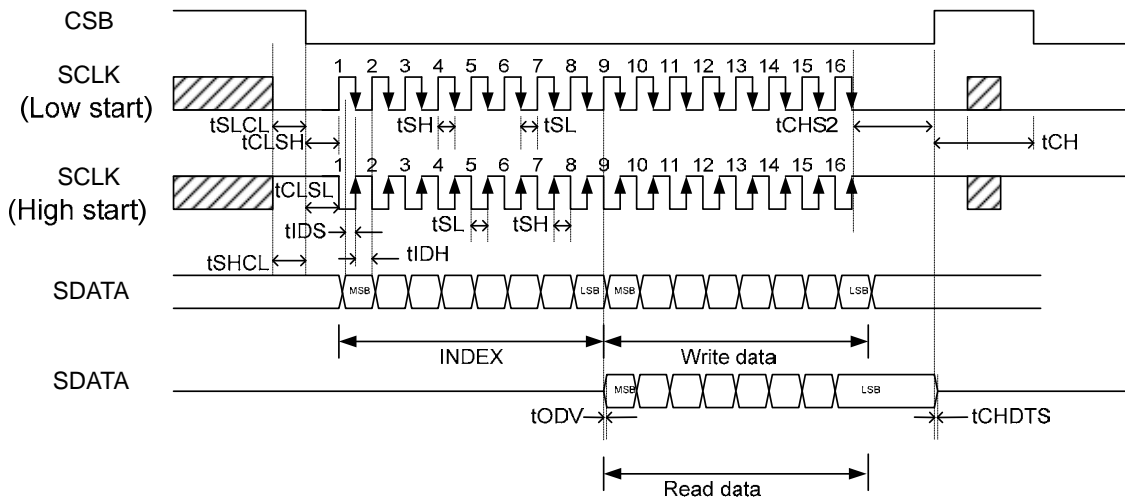


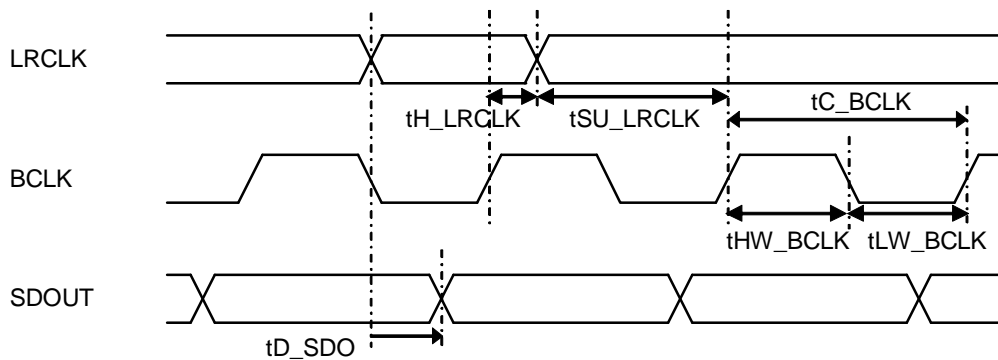
Figure 9.

Serial Audio Interface (Slave)

(DGND=0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C, CL=30pF)

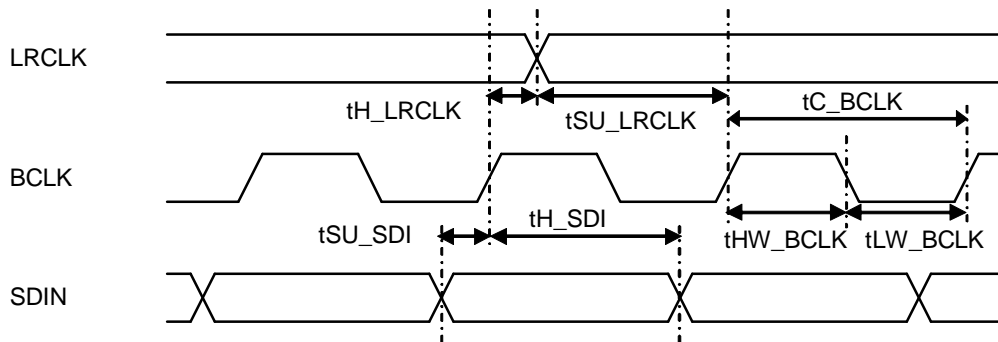
| Parameter | Symbol | Min | Max. | Unit |
|----------------------|----------------|------|-------|------|
| SAI_BCLK Period | tC_BCLK | 32fs | 128fs | Hz |
| SAI_BCLK "H" Length | tHW_BCLK | 73 | - | ns |
| SAI_BCLK "L" Length | tLW_BCLK | 73 | - | ns |
| SAI_LRCLK Hold Time | tH_LRCLK | 20 | - | ns |
| SAI_LRCLK Setup Time | tSU_LRCLK | 20 | - | ns |
| SAI_SDOUT Delay Time | tD_SDO (Note1) | - | 80 | ns |
| SAI_SDIN Setup Time | tSU_SDI | 20 | - | ns |
| SAI_SDIN Hold Time | tH_SDI | 20 | - | ns |

(Note1) tD_SDO is the delay time from later one of SAI_BCLK transition and SAI_LRCLK transition.



SAI Transmit

Figure 10.



SAI Receive

Figure 11.

Power Supply Sequence

Please power on/off the LSI with all kind of power at the same time.
 Each power supply should power up/down in 50ms. Also keep all power supply in the ON state or the OFF state.
 Please avoid partial ON or partial OFF states. Don't have to keep the sequence of power on/off

Please keep RESETB pin "L" level until all power supply become ON state. The CPU I/F available when all power supply are powered on, exceed t_{w_PURST} , RESET are disabled and exceed t_{w_REGU} . It is regardless that turn of power on and off of IOVDD and HVDD.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|----------------|-----|-----|-----|---------|
| Power On Delay Time | t_{VDD_ON} | 0 | - | 50 | ms |
| Power Down Delay Time | t_{VDD_OFF} | 0 | - | 50 | ms |
| Reset Time after Power ON | t_{w_PURST} | 1 | - | - | μs |
| Wait time for Regulator starting after reset release | t_{w_REGU} | 1 | - | - | ms |

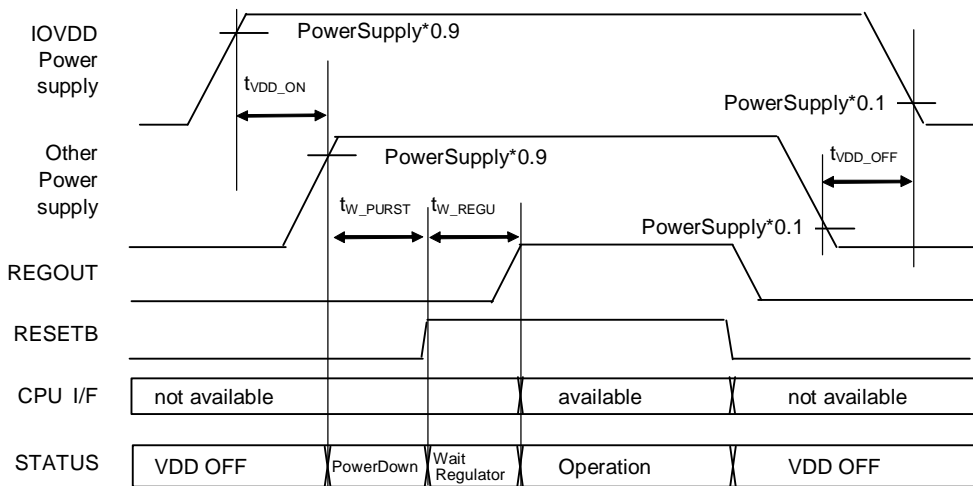


Figure 12.

Function Description

Clock control

Main modules that make up sound path of the LSI inside operate with 256fs Audio Clock.

Audio Clock can be selected whether divided clock of 256fs/512fs/1024fs from MCLKI or generated clock from Audio PLL. In case of used external loop filter of PLL, input clock must be 2MHz to 54MHz frequency. In case of not used external filter of PLL, input clock must be 32 kHz to 2MHz frequency. It is possible to select internal clock either MCLKI port or LRCLK port or BCLK port.

Internal Clock is selected Clock Input/Output Control Register. These frequency mean 512fs and master clock is divided by 2 from PLL output when sampling frequency is 16 kHz to 24 kHz, and these frequency mean 1024fs and master clock is divided by 4 from PLL output when sampling frequency is 8 kHz to 12 kHz.

· · PLL condition setting (changing) sequence

1. Stop PLL output by setting PLLOE bit to "0"
2. Disable PLL by setting PLEN bit to "0"
3. Set FPLLM, FPPNL, FPLLNH, FPLLD, FPLLFL, FPLLFH, FPLLFDL, FPLLFDH
4. Set PLEN bit to "1"
5. Wait for the PLL stabilizing time as the table "PLL Stabilizing Time"
6. Set PLLOE bit to "1"
7. Start recording or playback.

PLL Stabilizing Time

| PLL Stabilizing Time |
|----------------------|
| 10msec |

- Related Register

Sampling Rate Setting Register

FPLLM, FPPNL, FPLLNH, FPLLD, FPLLFL, FPLLFH, FPLLFDL, FPLLFDH Register

Clock Enable Register

Clock Input/Output Control Register

When pll is used.

The LSI support audio PLL function that can generate precise audio clock from wide range of clock frequency. Then, it can be realize audio function without external clock generator for audio. The LSI supports following cases.

- case 1: PLLISEL=0 or 2, MST=0, MCLKOE=0
Audio PLL generate system clock as 256fs from LRCLK

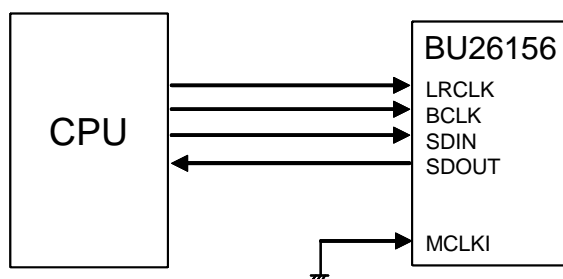


Figure 13.

When PLL is not used.

Please generate Audio clock on the CPU and supply to the LSI when PLL is not used. Then CPU and the LSI are synchronized.

■case 2: MST="0", MCLKOE="0"

Audio Clock is generated by the CPU and supplied to MCLKI pin of the LSI. LRCLK and BCLK are also provided from the CPU.

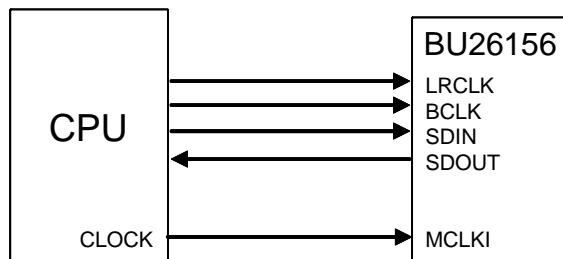


Figure 14.

Serial Audio Interface

The LSI supports SAI formats.

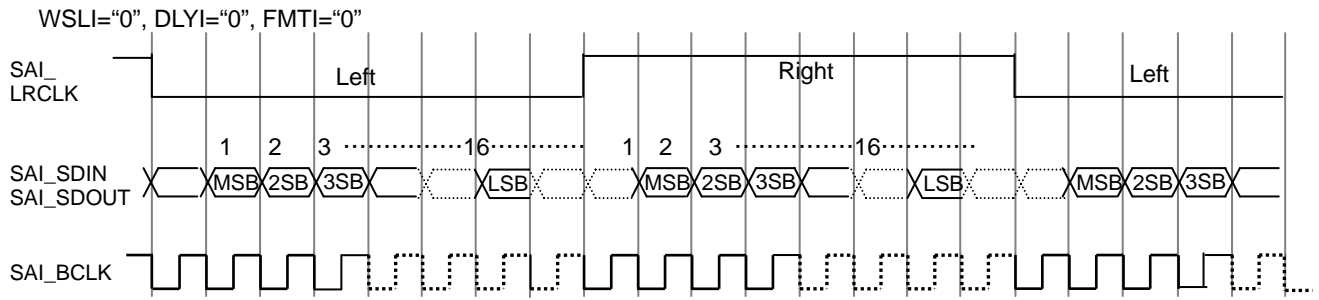


Figure 15.

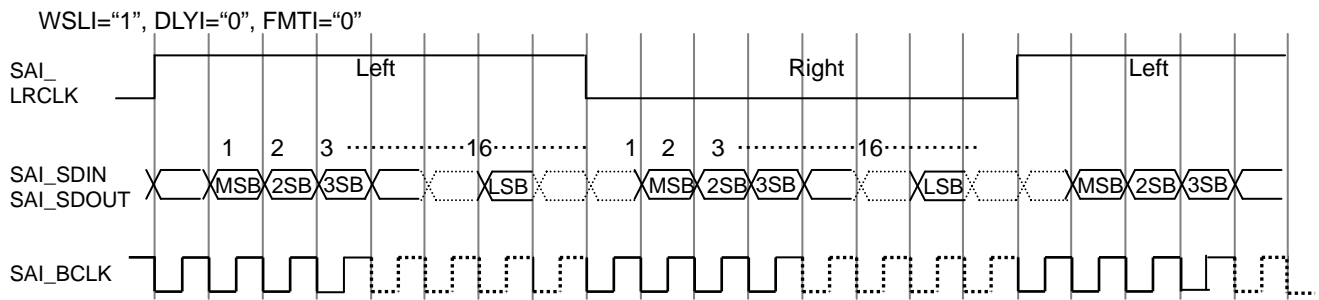


Figure 16.

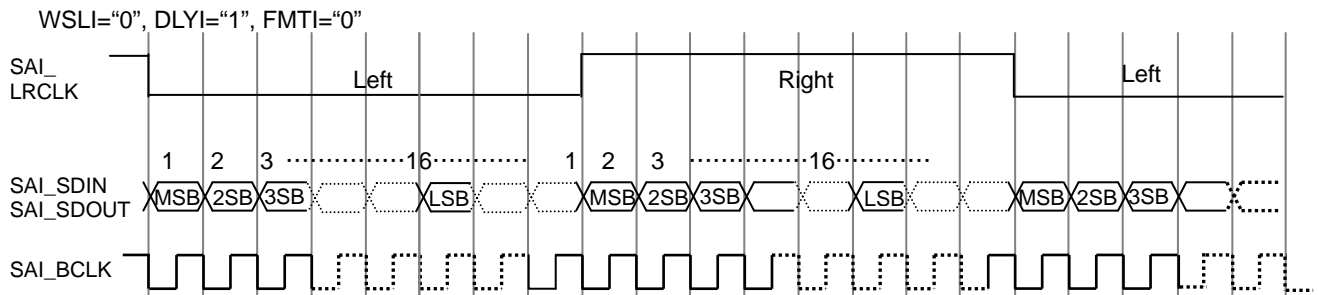


Figure 17.

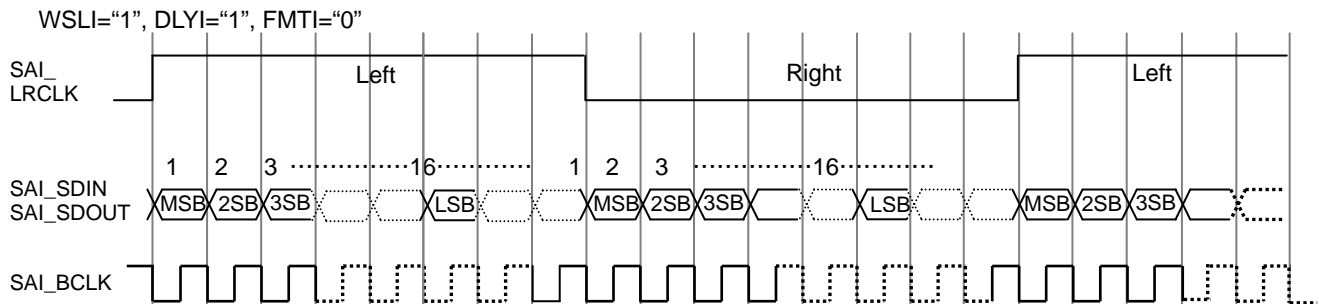


Figure 18.

DLYI="0", FMTI="1"

Flame synchronous transfer mode: R channel data is transferred right after L channel data.

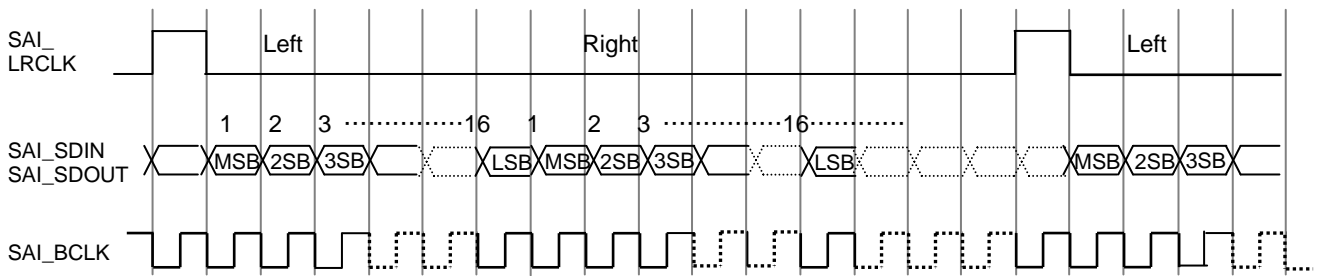


Figure 19.

DLYI="1", FMTI="1"

Flame synchronous transfer mode: R channel data is transferred right after L channel data.

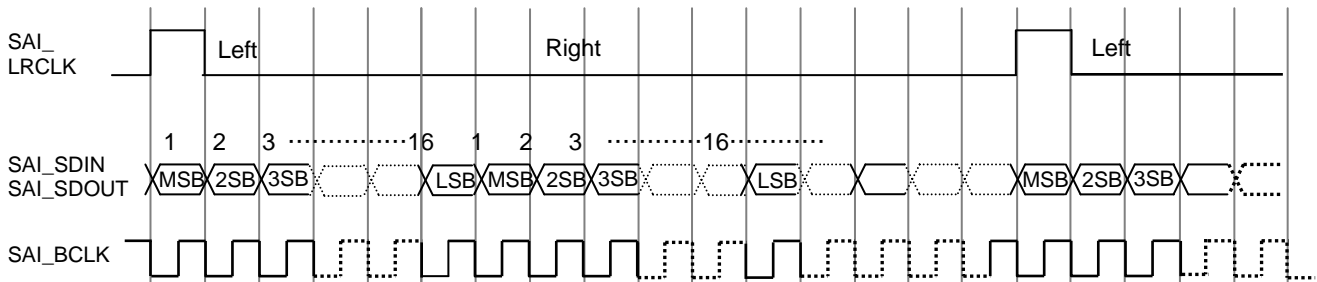


Figure 20.

- Related Register
- SAI Transmitter Control Register
- SAI Receiver Control Register

2 wire serial interface

This LSI has 2 wire serial interfaces. The LSI operates as a slave device. The address is fixed at "0011010".

- Format

The followings are the protocol of the LSI.

Write (MSB first)

- Start Condition (Set SDA level from "H" to "L" during SCL="H")
- Slave Address (0011010) +W (0) (8bit)
- Write Address (8bit)
- Write Data (8bit)
- ...
- Stop Condition (Set SDA level from "L" to "H" during SCL="H")

Read (MSB first)

- Start Condition
- Slave Address (0011010) +W (0) (8bit)
- Read Address (8bit)
- (Stop Condition) Start Condition
- Slave Address (0011010) +R (1) (8bit)
- Read Data (8bit)

The following shows the wave form of the LSI.
The yellow gridding shows that slave device drives the bus.
The symbol in the wave form means as following table.

| Unit | Description |
|--------|---|
| W/R | 0: Write 1: Read |
| A | 0: ACK(Acknowledge) 1: NAK(Not Acknowledge) |
| A[7-0] | Address (8bit) |
| D[7-0] | Data(8bit) |

Write

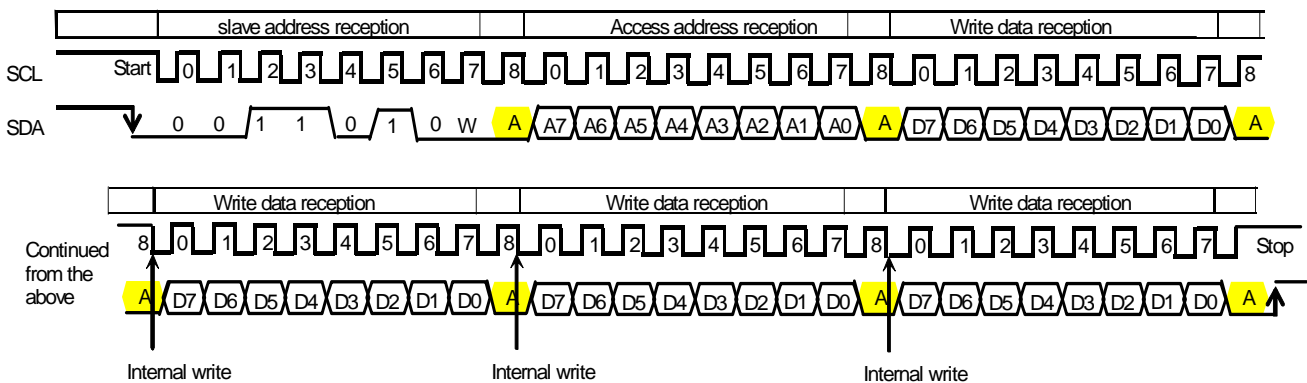


Figure 21.

In case there is no Stop or Start condition after internal register is written (Above figure: Internal Write), the slave device becomes continuous write mode and the next received 8 bits of data will be written into the internal register addressed by incremented by two to the current address.

Read

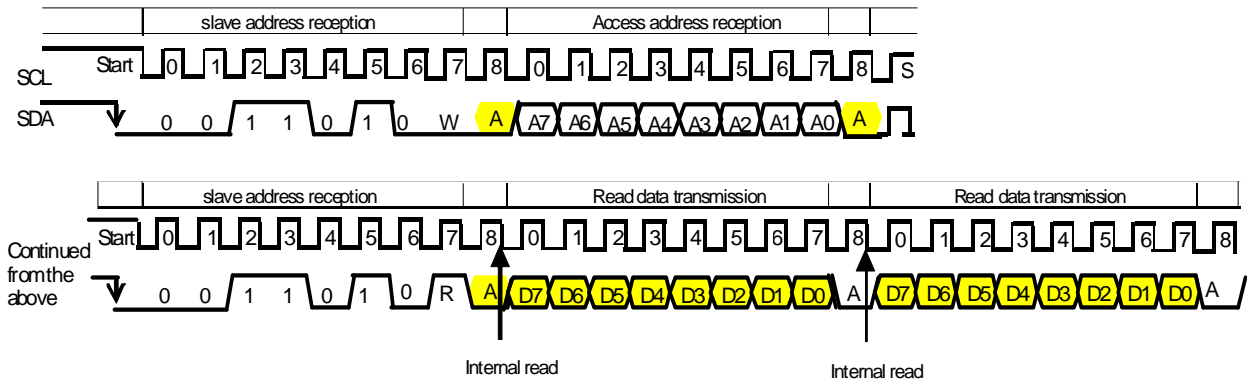


Figure 22.

If the Master device returns ACK (acknowledge) after the 8 bit data transferred from the LSI becomes continuous read mode. The next received 8 bits of data will be read from the internal register addressed by incremented by two to the current address.

Analog Block Gain Diagram

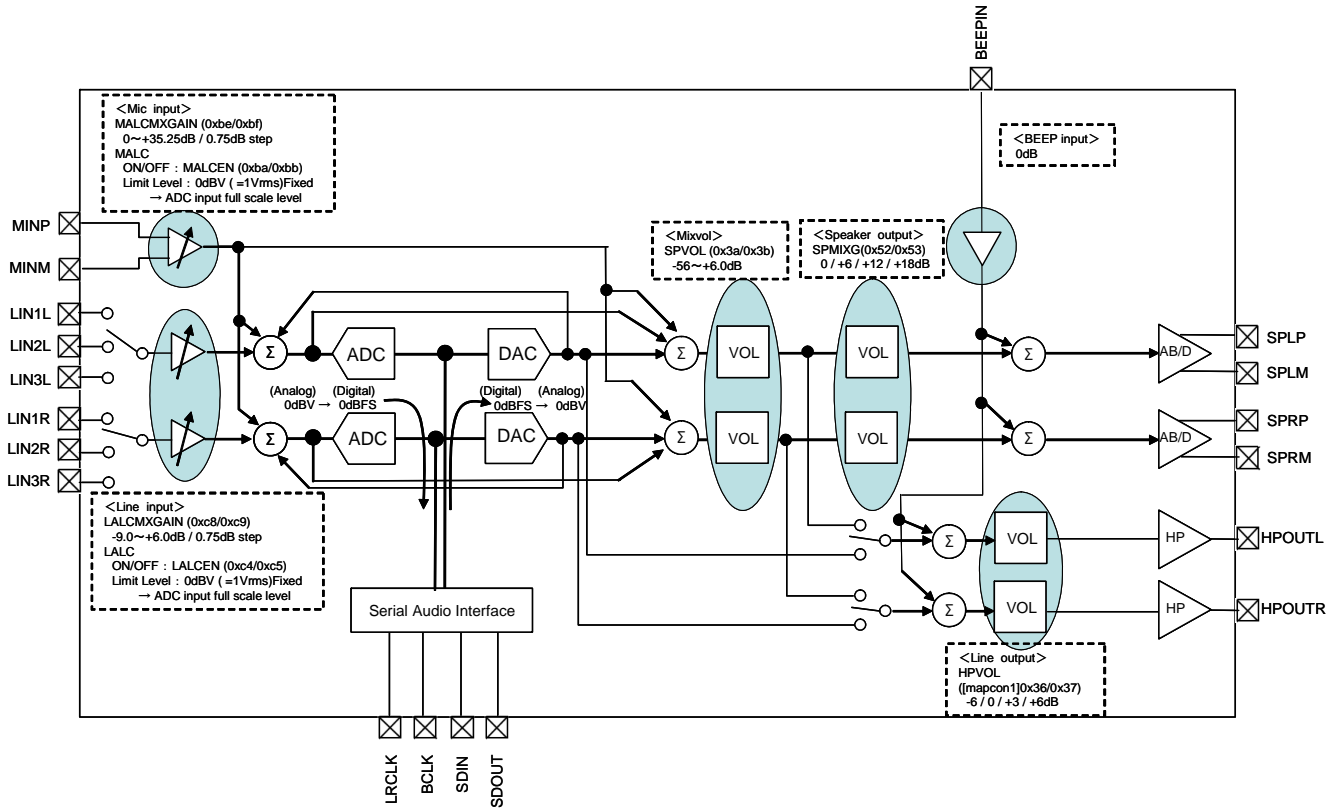


Figure 23.

State transition regarding SAI input and output control.

The following shows state transition about sound control. A change state is carried out by RECPLAY bit setup.

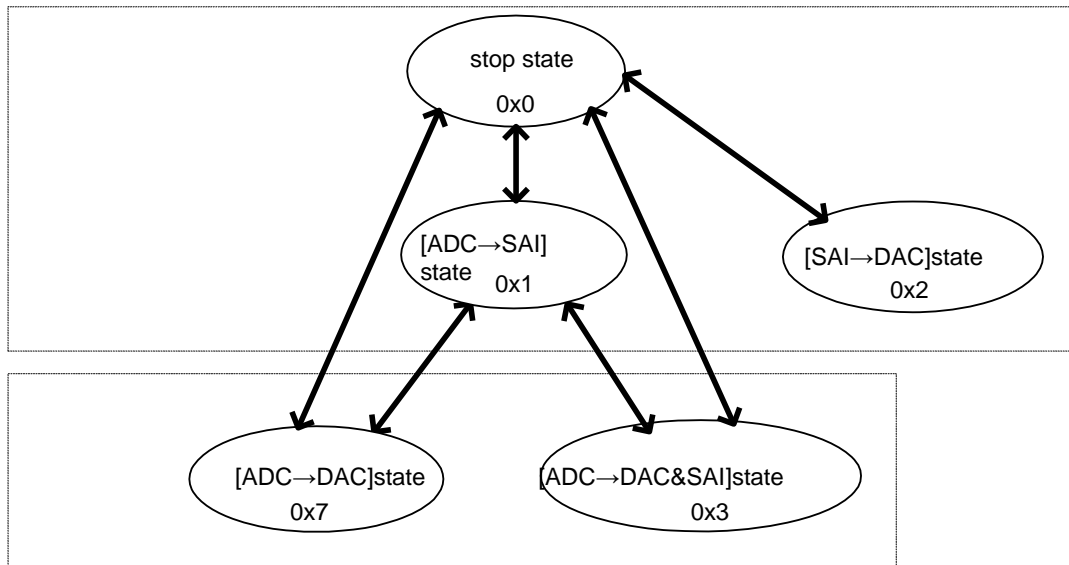


Figure 24.

- (1) Stop STATE (RECPLAY=0x0)
Sound activity is stopped.
- (2) [ADC→SAI] STATE (RECPLAY =0x1)
Analog input signal (MIC input/LINE input) is converted to digital data and outputted from SAI terminals.
- (3) [SAI→DAC] STATE (RECPLAY =0x2)
Digital signal from SAI is converted to analog data and it is outputted from speaker or line amplifier.
- (4) [ADC→DAC] STATE (RECPLAY =0x7)
Analog input signal (MIC input/LINE input) is converted to digital data and outputted speaker or line amplifier through DAC.
- (5) [ADC→DAC & SAI] STATE (RECPLAY =0x3)
Analog input signal (MIC input/LINE input) is converted to digital data and outputted from SAI terminals.
At one time, digital signal inputted from SAI is converted to analog data and it is outputted from speaker or line amplifier.
Set this state for using SDIN to SDOOUT path when LINDACEN bit enable.

*Please don't use "DAC output to LIMIX path" with path (4) and path (5).

Signal Flow

ADC used signal flow

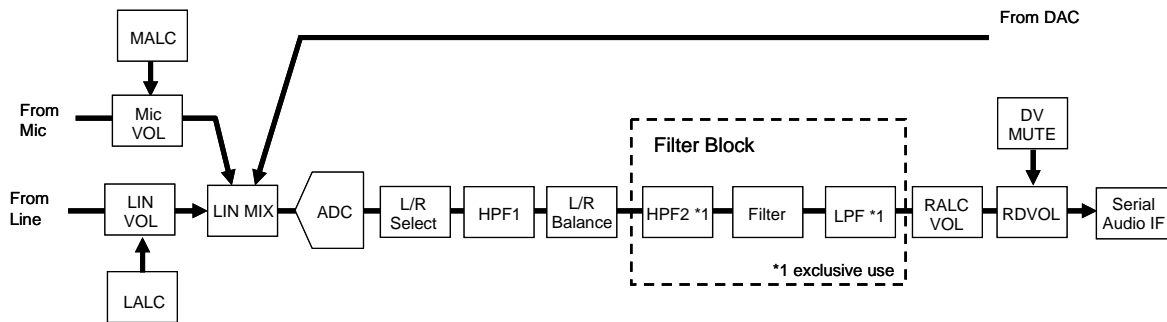


Figure 25.

| Name | Function | Related Register | Setting |
|----------------------|--|---|--|
| Mic ALC MICVOL | Analog Microphone volume and ALC | MIC ALC Control MIC ALC Max Gain Analog Input Power Management | 0dB to +35.25dB, 0.75dB step |
| LineIN ALC LINVOL | Analog line input volume and ALC | Line ALC Control Line ALC Max Gain Analog Input Power Management | -15 to +0dB, 1dB step |
| LIN MIX | Mixing the LINE input, MIC input and outputted signal from DAC | Line In Control Analog Path Control | Analog input control from Mic, Line and DAC. Mixing control |
| ADC | 24bit AD Converter | Analog Input Power Management | ADC Enable/Disable |
| L/R Select | ADC(Lch/Rch) to Audio Bass | [I2SL / I2SR / MONOREC] Record L/R Balance Volume Control | -6.0dB to 6.0dB(0.1step) |
| HPF1 | High path filter for DC cut | DSP Filter Function Enable | HPF Enable/Disable |
| L/R Balance | L/R balance volume control | [RBVOLL / RBVOLR] Record L/R Balance Volume Control | -6.0dB to 6.0dB(0.1step) |
| HPF2 | High pass filter for ADC | DSP Filter Function Enable High Pass Filter2 Cut-off Control | HPF Enable/Disable setting order setting Cut-off frequency setting |
| Filter | Sound filters setting | Sound Effect Mode DSP Filter Function Enable EQ Band N Gain Setting Programmable EQ Band N Coefficient-a0/1 | Sound effect mode setting. Each filters Enable/Disable. Each filter gain settings. Each sound effects characteristics setting |
| LPF | Programmable LPF setting for ADC | Rec Programmable LPF Setting Rec Programmable LPF Cutoff Coef | LPF Enable/Disable setting Order setting. Cut-off frequency setting |
| RALCVOL | Digital Boost Volume for ADC | Recording Digital Boost Volume Register | -12.000d to 35.625dB(0.375Step) |
| RDVOL | Digital attenuator and fader for ADC | Record Digital Attenuator Control Digital Volume Control Function Enable Mixer & Volume Control | Volume setting -71.5dB to 0dB (0.5dBstep) Fader enable/disenable setting (working together DVMUTE) |

*Filter Block can be used for either ADC path or DAC path.
For example, if Filter Block is connected to DAC, ADC is not effected by filter.
Regarding the detail of register setting, please refer to selection of [SEMODE] register.

DAC used signal flow

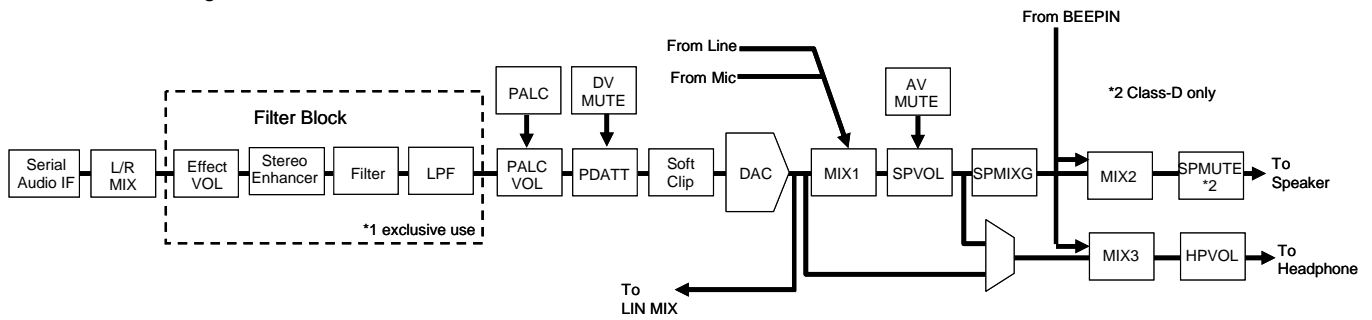


Figure 26.

| Name | Function | Related Register | Setting |
|-----------------|--|---|--|
| L/R MIX | Lch/Rch mixer for SAI input signal | Mixer & Volume Control | Mixer setting |
| Effect Vol | Digital volume in front of sound effect blocks. | Playback Effect Volume | -71.5dB to 0dB (0.5dBstep) |
| Stereo Enhancer | Stereo enhancer. | Stereo Gain | 3D effect |
| Filter | Each sound filters are enabled. | Sound Effect Mode DSP Filter Function Enable EQ Band N Gain Setting Programmable EQ Band N Coefficient-a0/1 | Sound effect mode setting. Each filters Enable/Disable Each filters gain setting Each sound effects characteristics setting |
| LPF | Programmable LPF for DAC path. | Play Programmable LPF Setting Play Programmable LPF Cutoff Coef | HPF Enable/Disable setting Order setting Cut-off frequency setting |
| PALC PALCVOL | Digital Playback ALC and Volume | Playback ALC Attack Time Control Playback ALC Decay Time Control Playback Target Level Control Playback ALC Min Gain Control Playback ALC Volume Control Playback ALC Zerocross Timeout Playback Limiter Fast Release Setting | ALC operation settings |
| PDATT | Digital Attenuator for DAC path. Fader for noise reduction at changing the digital volume | Playback Digital Attenuator Control Digital Volume Control Function Enable Mixer & Volume Control | Volume setting -71.5dB to 0.5dB (0.5dBstep) Fader ON/OFF setting Fade time setting |
| Soft Clip | Softclip limiter for output suppression | Soft Clip Enable Soft Clip Threshold Soft Clip Gain | Softclip Enable/Disable Threshold level, Gain setting |
| DAC | 24bit DA Converter | DAC Power Management | DAC Enable/Disable |
| MIX1 | Mixing DAC output and analog input. | Speaker Amplifier Output Control 2 | Gain setting Mixing paths setting |
| SPVOL | Analog Volume for DAC to analog output path. | Speaker Amplifier Volume Control Amplifier Volume Fader Control Amplifier Volume Control Function Enable | Volume setting -54 to +6dB Fader ON/OFF setting Fade time setting |
| SPMIXG | Analog Volume for Speaker output path | Speaker Amplifier Output Control 1 | Gain setting |
| MIX2 | Mixing Speaker output signal and BEEPIN input signal. | SPAMP input Control BEEPIN Amp Control | Mixing paths setting |
| MIX3 | Mixing Headphone output signal and BEEPIN input signal. | SPAMP input Control BEEPIN Amp Control | Mixing paths setting |
| HPVOL | Analog Volume for Headphone output path | Headphone output Gain Setting | Gain setting |

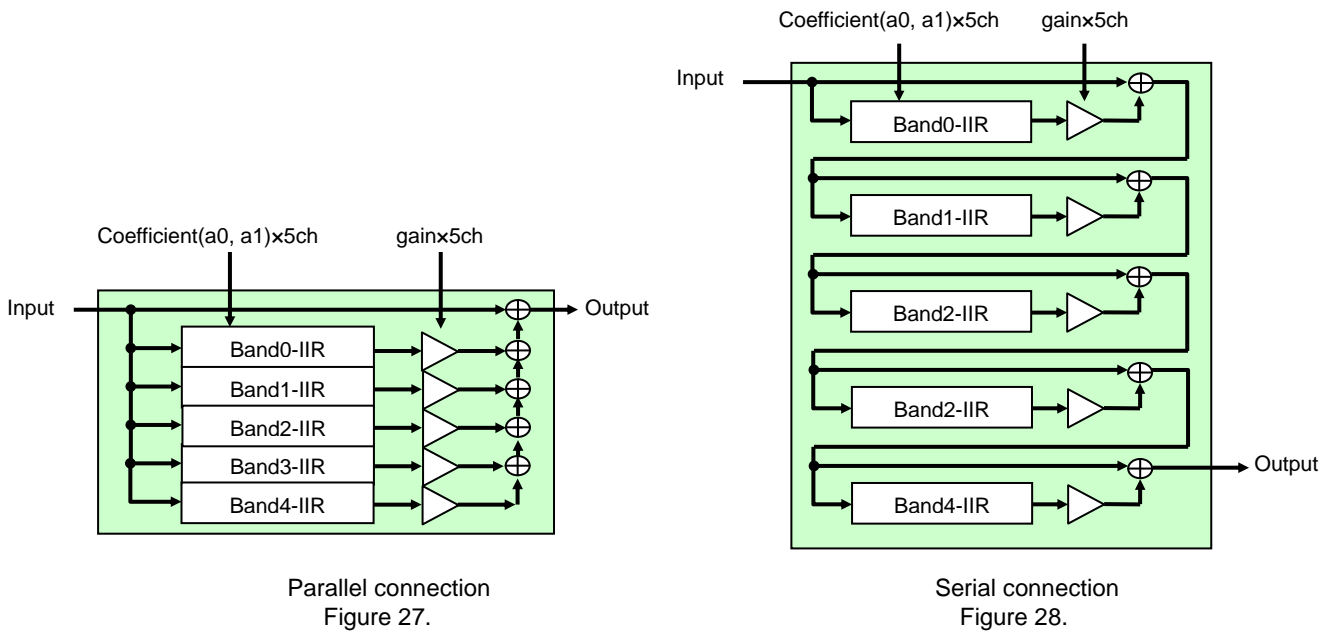
*Filter Block can be used for either ADC path or DAC path.
For example, if Filter Block is connectd to DAC, ADC is not effcted by filter.
Regardring the detail of register setting, please refer to selection of [SEMDE] register.

Filter (5bands-Programmable IIR Filter)

A five bands equalizer features a second-order IIR type Band Pass Filter. Volume control of MUTE, -71.5dB+12dB (0.5dB step) can be controlled at all paths.

Each channels of the filter can be selected parallel connection or serial connection

The followings are block diagrams at parallel connection and serial connection



The filter coefficient is programmable. From required center frequency and band width, Programmable Equalizer Coefficient-a0 Control Register and Programmable Notch Filter Coefficient-a1 Control Register value is decided. Followings are the setting formula.

$$a0 = (1 - \tan\pi f_b / f_s) / (1 + \tan\pi f_b / f_s)$$

$$a1 = -2\cos 2\pi f_0 / f_s / (1 + \tan\pi f_b / f_s)$$

- f0: Band center frequency [Hz]
- fb: -3dB band width [Hz]
- fs: Sampling frequency [Hz]

* Actual setting value is an integral number that the result of above formula multiplied by 2¹⁴ then round up numbers of five and above and round down anything under five to an integer.

DSP filtering function: ON / OFF

DSP Filter Function Enable register can set ON or OFF of each filter function. Please change this register when RECPLAY bit is 0x0. If this register is changed on playback or recording, the noise may be generated.

Stereo Enhancer

Please refer the application note "StereoEnhancerApplicationNote".

PALC (ALC fo DAC path)

Function outline

The PALC adjust a gain automatically from -12dB to 35.625dB in DAC path.

A small level singal is made easy listening because the small level signal is amplified to a target level and dynamic range is compressed when the gain setting is a plus gain

Or PALC can be used for a limiter when the gain setting is a minus gain. It protects a speaker from destruction.

Fast release function makes play sound natural by it release the gain fast when a big singal is suddenly input and a volume drops.

Operation outline

When output waveform level of ALC is under the target level, output waveform is increased. Maximum level of gain is MALCMXGAIN or LALCMXGAIN. Maximum alc gain is PALCVOL and minimum level is PALCMINGAIN.

PALCATKC is attack time. It is a time step of decreasing waveform level. PALCDCY is decay time. It is a time step of increasing waveform level.

These operations are the following.

*Note:When ALC is disable, output signal is also amplified to PALCVOL gain level.

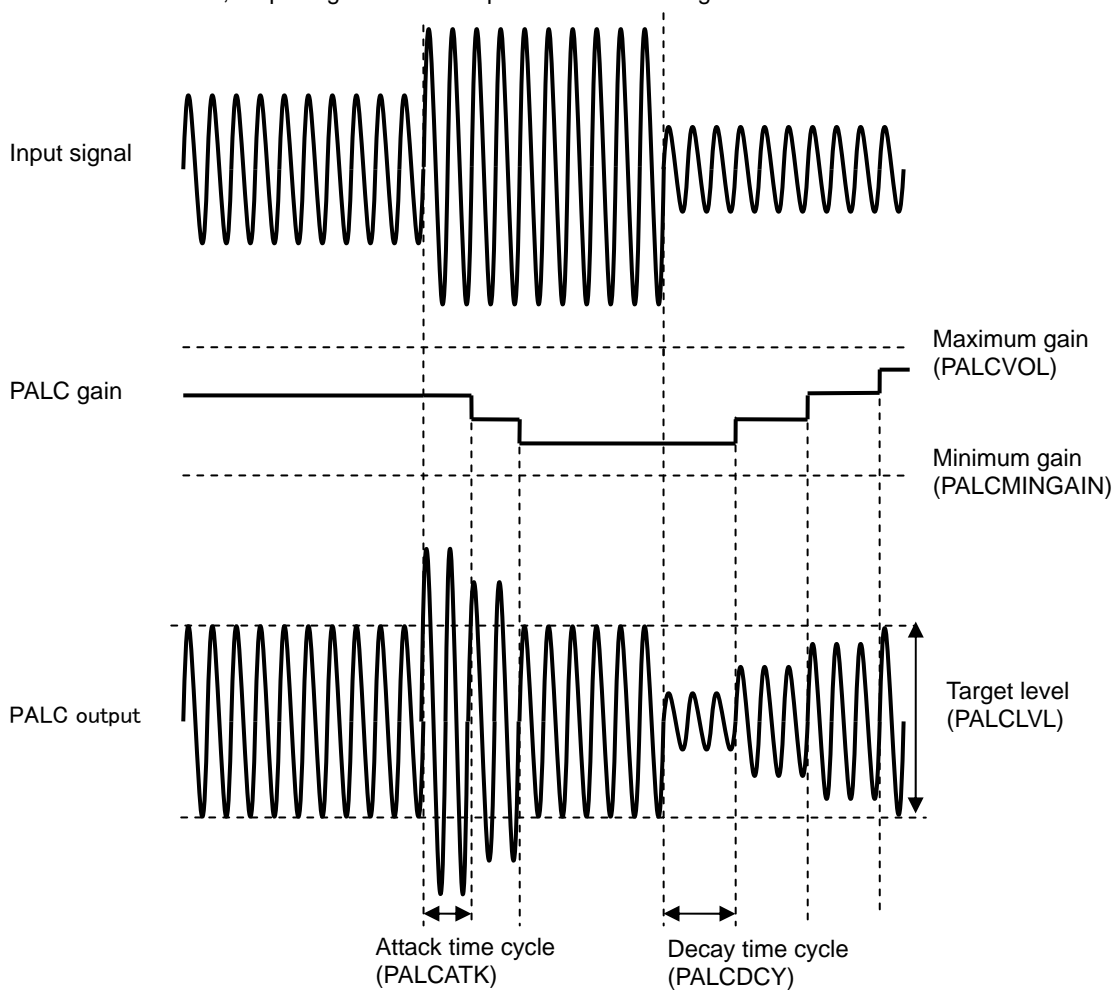


Figure 29.

A Peak Limiter function is carried in ALC. The Peak Limiter function short attack time and prevent clipping a wave. A threshold level is fixed at 87.5%(-1.16dBFS) and this function is priored the normal ALC operation when input level exceed the threshold level. The attack time is a minimum step, 1/fs, when the peak limiter operates. And this function cannot be turned off.

These operations level diagram is the following figure.

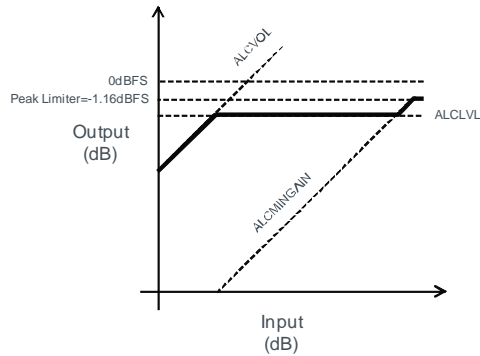


Figure 30. ALC Level diagram

Zero Cross

BU26156 combined Zerocross function for MALC, LALC. Zerocross is changed, when input waveform is crossed center level. In case of Zero Cross function is not occurred, BU26156 changes gain when time set by PALCZCTM is passed BU26156 also changes gain past that time when zerocross is enable (ZCEN=0x0). It is often caused POP noise to change gain without zero cross.

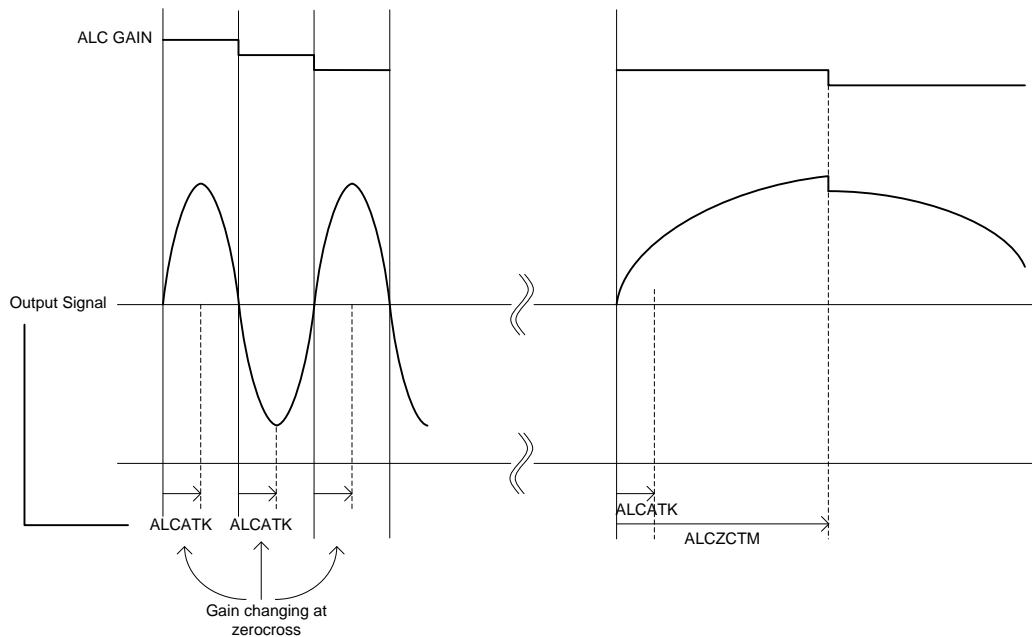


Figure 31.

Note:It is possible that a noise of changing the gain occur when ZCEN is disable.

Fast Release

In case of input impulse waveform is over target level of ALC, fast release function detects impulse waveform and LSI is returned until normal waveform level quickly. As result of quick return, output waveform of LSI is kept natural sound.

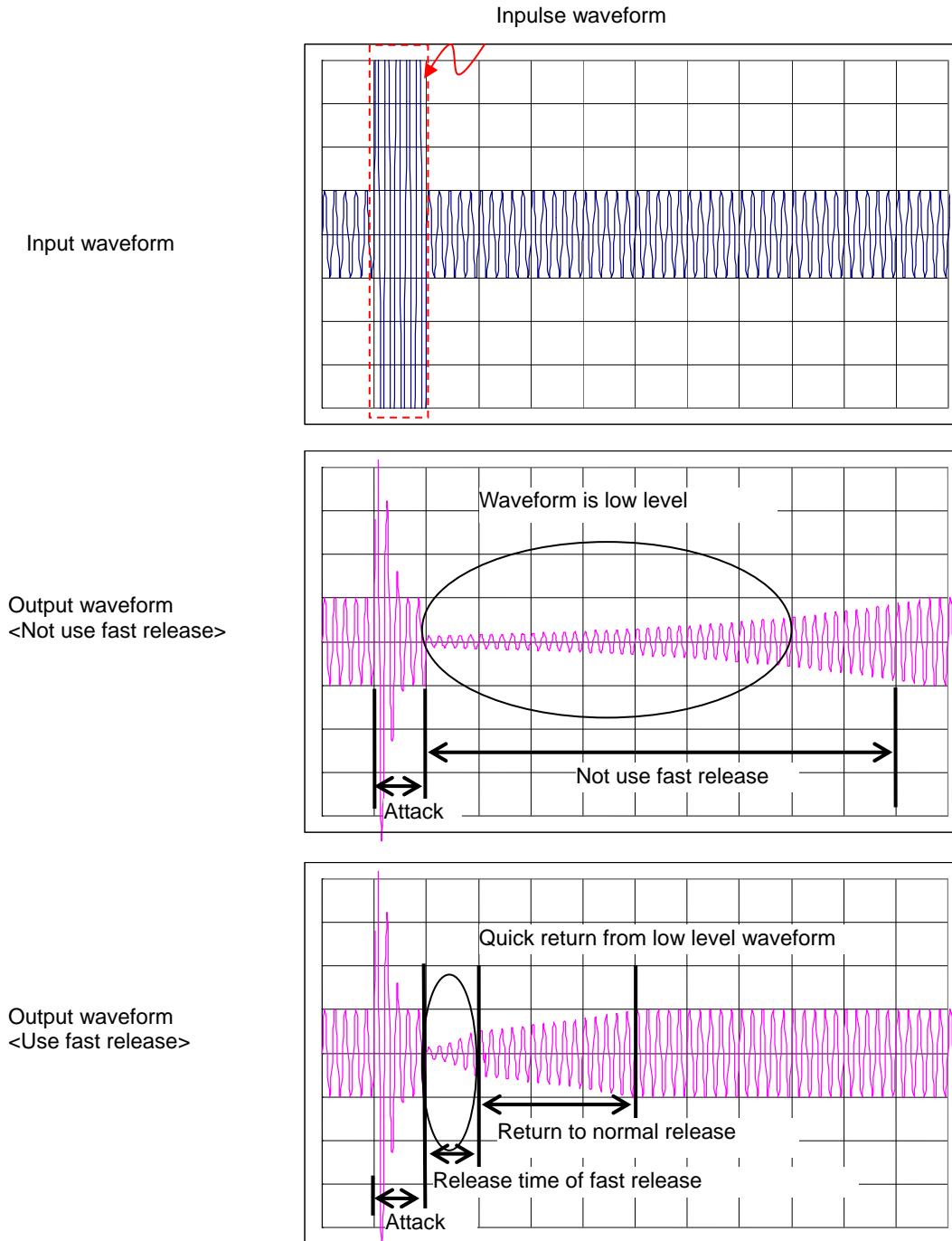


Figure 32. Not Fast release waveform and Fast release waveform

PALCFREN bit is setted enable of fast release function. When impulse waveform is over threshold of PALCFRTH level, fast release function is started and is returned waveform until detected level by fast release decay time. This decay time is selected PALFRSP bit.

MALC (Mic Input ALC)/LALC (Line input ALC)

Function general description

MALC can be adjusted mic input gain from 0dB to +35.25dB. LALC can be adjusted line input gain from -15dB to 0dB.

Operation general description

MALC and LALC are fixed ADC full-scale level. When output waveform level of ALC is under the target level, output waveform is increased. Maximum level of gain is MALCMXGAIN or LALCMXGAIN. Minimum level of gain is 0dB, when MALC is used. Minimum level of gain is -15dB, when LALC is used. MALCATK and LALCATK are attack time. It is a time step of decreasing waveform level. MALCDCY and LALCDCY is decay time. It is a time step of increasing waveform level. These operations are the following.

* In case of MALC, LALC are disabled, output waveform is effective MALCMXGAIN and LALCMXGAIN setting gain.

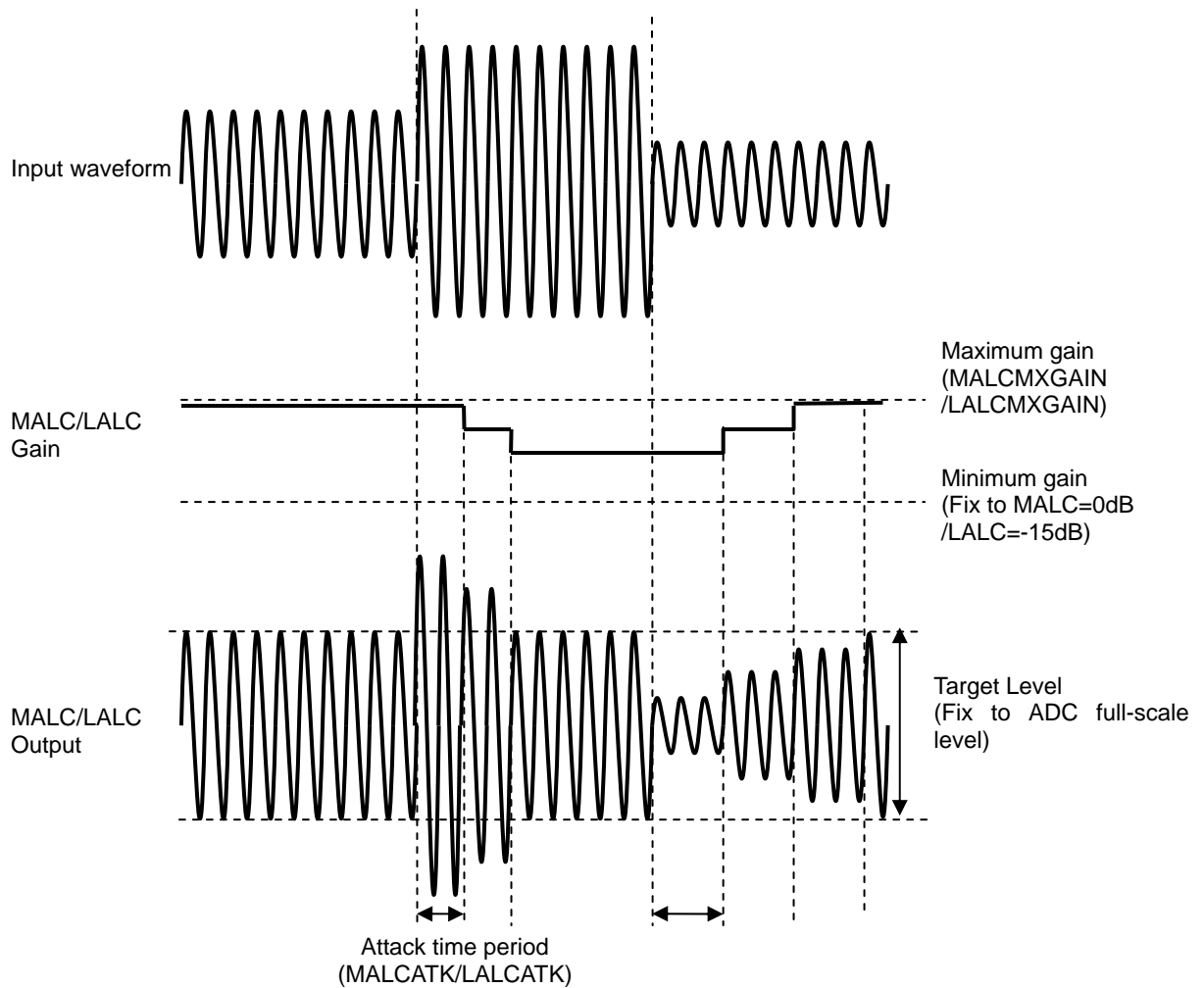


Figure 33.

Zero Cross

BU26156 combined Zerocross function for MALC, LALC. Zerocross is changed, when input waveform is crossed center level. In case of Zero Cross function is not occurred, BU26156 is changed gain after 2.7ms @Fs=48 kHz.

Clip reduction

Clip reduction function prevents clip waveform. When BU26156 is entered large waveform, BU26156 is shorted attack time. As result of this operation, output waveform is prevented clip waveform. When this function is enabled, attack time is fixed 2fs and zerocross is disabled. The difference between peak limiter and clip reduction is threshold and attacktime. Threshold of Clip deduction is ADC full scale level. Attack time of clip reduction is 2fs. It is possible to select ON/OFF register setting.

Soft clip limiter

Soft clip function is reduced power consumption. If ALC can not be responded to input waveform, soft clip function is reduced input waveform. In case of input waveform is overed threshold level, soft clip reduce output waveform.

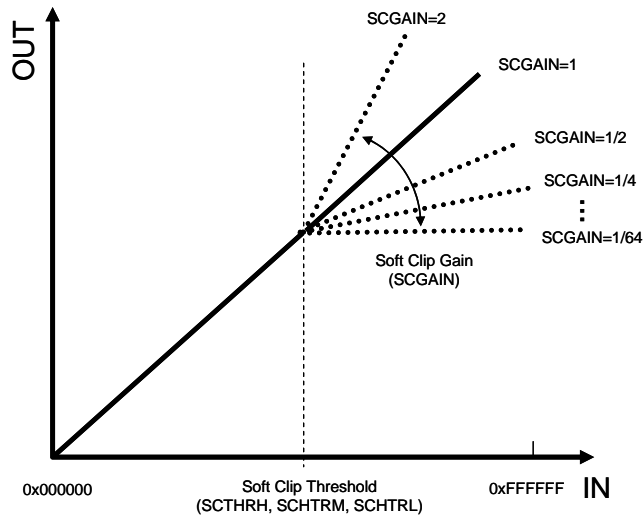


Figure 34.

Analog block

Analog Reference Voltage (VMID) Generation Circuit

VMID is used as analog circuit reference voltage for both recording path and playback path. Therefore, both case for recording and playback, VMID need to do power up. At the power up, the wait time in proportion to the capacitor value is needed to charge external capacitor connected with VMID pin. If recording and playback start before completion of charge, it may generate noise. The following is a sequence of recommendation. Refer to the Analog Reference Power Management Register for the function of VMIDCON.

VMID Power UP/DOWN Sequence (External capacitor 1uF)

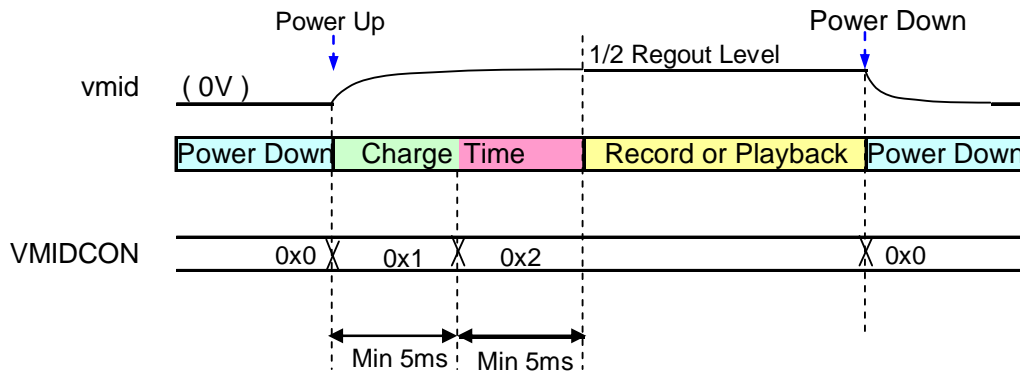


Figure 35.

Interrupt circuit

It is possible to check BU26156 operation by IRQ port. IRQ port polarity is changed by thermal protection operation and speaker short protection operation. It is possible to mask Interrupt function and select IRQ interrupt polarity. In case of BU26156 detects protection operation, BU26156 keeps interrupt status. In case of clear interrupt status, write to "1" to status register.

IRQB terminal outputs "L" level during RESETB equal "L" level (RESET state). Please mask IRQB signal in this period

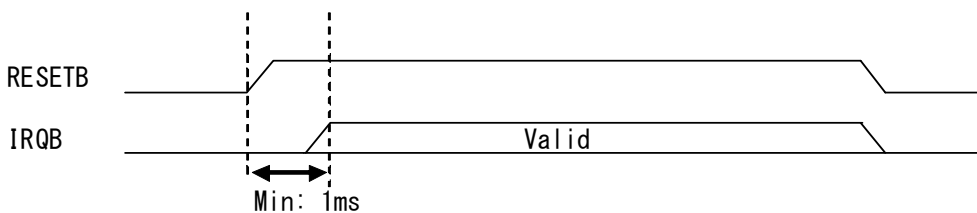


Figure 36.

Detailed Description of the Registers

Register map

Note: "-" indicates a reserved bit. They return "0" for reads. Write "0" to the bit every time. If "1" is written to this bit, the operations cannot be guaranteed.

Don't write the registers expect the map of below. If these register is written, the operations cannot be guaranteed.

About the register initial setting after starting this IC

After starting register access, according to following procedures at start-up, access register.

| Address (HEX) | Read/Write | Write Data (HEX) | Description |
|---------------|------------|------------------|---------------------------------|
| 1c | Write | 01 | MAPCON 1 |
| 39 | Write | 00 | For ADC parameter setting |
| 3b | Write | 01 | For ADC / Mic parameter setting |
| 3d | Write | 02 | For ADC parameter setting |
| 1c | Write | 00 | MAPCON 0 |

It is available at the MAPCON=0x0(Register Map Control Register 0x1c/0x1d)
 以下のレジスタは Register Map Control レジスタ (0x1c/0x1d) の MAPCON=0x0 のときにアクセス可能です。

| INDEX | | b07 | b06 | b05 | b04 | b03 | b02 | b01 | b00 | Register Name | Note | | | |
|-------|------|------------|---------|---------|---------|---------|---------|------------|---------|---------------|-------------------------|---|--|----------------------------|
| R | W | (Initial) | | | | | | | | | | | | |
| 0x00 | 0x01 | - | - | - | - | SR | | | 0 | 0 | 0 | Sampling Rate Setting | | |
| 0x06 | 0x07 | - | STEGAIN | | | | | | | 0 | 0 | 0 | Stereo Gain | |
| 0x08 | 0x09 | IRQPOLE | - | - | - | - | SHLIREN | SHRIREN | THRIREN | 0 | 0 | IRQ control | | |
| 0x0a | 0x0b | - | - | - | - | - | SHLSTS | SHRSTS | THRSTS | 0 | 0 | IRQ Status | | |
| 0x0c | 0x0d | - | - | - | - | MCLKOE | PLL0E | PLLEN | MCLKEN | 0 | 0 | Clock Enable | | |
| 0x0e | 0x0f | - | - | - | PLLISEL | | | CLKSEL | | | 0 | 0 | Clock Input/Output Control | |
| 0x10 | 0x11 | - | - | - | - | - | - | - | SOFRST | - | 0 | Software Reset | | |
| 0x12 | 0x13 | - | - | - | - | - | RECPLAY | | | 0 | 0 | Record/Playback Running Control | | |
| 0x14 | 0x15 | - | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Mic Input Charging Time | | | |
| 0x1c | 0x1d | - | - | - | - | - | - | - | MAPCON | - | 0 | RegisterMAP Control | | |
| 0x20 | 0x21 | LOREN | LOLEN | LOSEL | - | - | MICBEN | VMIDCON | | | 0 | 0 | Analog Reference Power Management | |
| 0x22 | 0x23 | - | - | - | - | PGAEN | ADCREN | ADCLEN | LIEN | 0 | 0 | Analog Input Power Management | | |
| 0x24 | 0x25 | - | - | - | - | - | DACREN | DACLEN | - | 0 | 0 | DAC Power Management | | |
| 0x26 | 0x27 | - | - | - | - | - | SPDEN | SPABEN | SPMVEN | 0 | 0 | Speaker Amplifier Power Management | | |
| 0x2a | 0x2b | TEST2 | - | BP2SPEN | MV2SPEN | TEST1 | TEST0 | AMA | | | 0 | 1 | AM avoidance Control / SPAMP input Control | |
| 0x2e | 0x2f | - | - | - | - | - | - | ZCEN | - | 0 | - | Zero Cross Comparator Power Management | | |
| 0x30 | 0x31 | - | - | - | BPINCON | | TEST3 | MICBCON18S | | | 0 | 0 | BEEPIN Amp Control / MICBIAS Voltage Control | |
| 0x32 | 0x33 | - | - | MXGAIN | LINMXEN | MICMXEN | LIN3EN | LIN2EN | LIN1EN | 0 | 1 | Line-In Control | | |
| 0x3a | 0x3b | - | - | SPVOL | | | | | | | 1 | 1 | Speaker Amplifier Volume Control | |
| 0x3e | 0x3f | PDATT | | | | | | | | | | 1 | 1 | Digital Attenuator Control |
| 0x48 | 0x49 | - | - | - | - | - | - | AVMUTE | AVFADE | 0 | 0 | Amplifier Volume Control | | |
| 0x4a | 0x4b | - | - | - | - | - | - | AVFCON | | | 0 | 0 | Function Enable | |
| 0x4c | 0x4d | PCMF024 | | FMTO | MSBO | ISSCKO | AFOO | DLYO | WSLO | 0 | 0 | Fader Control | | |
| 0x4e | 0x4f | PCMF124 | | FMTI | MSBI | ISSCKI | AFOI | DLYI | WSLI | 0 | 0 | SAI Transmitter Control | | |
| 0x50 | 0x51 | - | - | - | BSWP | - | - | - | MST | 0 | 0 | SAI Receiver Control | | |
| 0x52 | 0x53 | - | - | - | - | - | - | SPMIXG | | | 0 | 0 | SAI Mode select | |
| 0x54 | 0x55 | - | - | - | - | LINOE | MICOE | DACOE | LOMIXG | 0 | 0 | Speaker Amplifier output Control1 | | |
| 0x58 | 0x59 | - | - | OSRSEL | | - | - | - | - | - | - | Speaker Amplifier / Lineout Amplifier output Control2 | | |
| 0x5a | 0x5b | - | - | - | - | - | - | MINDIF | - | 1 | - | DAC Clock Setting | | |
| 0x5c | 0x5d | SEMODE | - | - | - | - | - | SEMODE | | | 0 | 0 | Mic Interface Control | |
| 0x5e | 0x5f | - | - | - | - | - | - | I2SR | I2SL | 0 | 0 | Mic Interface Control | | |
| 0x60 | 0x61 | RDVOL | | | | | | | | | | 1 | 1 | Sound Effect Mode |
| 0x62 | 0x63 | Effect VOL | | | | | | | | | | 1 | 1 | Record Path select |
| | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Record Digital Attenuator Control | | |
| | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Playback Effect Volume Control | | |

| INDEX | | b07 | b06 | b05 | b04 | b03 | b02 | b01 | b00 | Register Name | Note | | |
|-------|------|-----------|---------|-------|--------|--------|---------|--------|--------|--|--|---------------------------|--|
| R | W | (Initial) | | | | | | | | | | | |
| 0x66 | 0x67 | HPF2OD | EQ4EN | EQ3EN | EQ2EN | EQ1EN | EQ0EN | HPF2EN | HPF1EN | DSP Filter Function Enable | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | |
| 0x68 | 0x69 | - | - | - | DVMUTE | DVFADE | - | - | PALGEN | Digital Volume Control Function Enable | | | |
| | | - | - | - | 0 | 0 | - | - | 0 | | | | |
| 0x6a | 0x6b | DVFCON | | | RMCON | | | LMCON | | Mixer & Volume Control | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x74 | 0x75 | EQGAIN0 | | | | | | | | | EQ Band0 Gain Setting | | |
| | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | | | |
| 0x76 | 0x77 | EQGAIN1 | | | | | | | | | EQ Band1 Gain Setting | | |
| | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | | | |
| 0x78 | 0x79 | EQGAIN2 | | | | | | | | | EQ Band2 Gain Setting | | |
| | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | | | |
| 0x7a | 0x7b | EQGAIN3 | | | | | | | | | EQ Band3 Gain Setting | | |
| | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | | | |
| 0x7c | 0x7d | EQGAIN4 | | | | | | | | | EQ Band4 Gain Setting | | |
| | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | | | | |
| 0x7e | 0x7f | - | - | - | - | - | HPF2CUT | | | High Pass Filter2 Cut-off Control | | | |
| | | - | - | - | - | - | 0 | 0 | 0 | | | | |
| 0x80 | 0x81 | EQQA0L | | | | | | | | | Programable Equalizer Band0 Coefficient-a0 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x82 | 0x83 | EQQA0H | | | | | | | | | Programable Equalizer Band0 Coefficient-a0 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x84 | 0x85 | EQQA1L | | | | | | | | | Programable Equalizer Band0 Coefficient-a1 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x86 | 0x87 | EQQA1H | | | | | | | | | Programable Equalizer Band0 Coefficient-a1 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x88 | 0x89 | EQ1A0L | | | | | | | | | Programable Equalizer Band1 Coefficient-a0 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x8a | 0x8b | EQ1A0H | | | | | | | | | Programable Equalizer Band1 Coefficient-a0 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x8c | 0x8d | EQ1A1L | | | | | | | | | Programable Equalizer Band1 Coefficient-a1 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x8e | 0x8f | EQ1A1H | | | | | | | | | Programable Equalizer Band1 Coefficient-a1 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x90 | 0x91 | EQ2A0L | | | | | | | | | Programable Equalizer Band2 Coefficient-a0 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x92 | 0x93 | EQ2A0H | | | | | | | | | Programable Equalizer Band2 Coefficient-a0 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x94 | 0x95 | EQ2A1L | | | | | | | | | Programable Equalizer Band2 Coefficient-a1 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x96 | 0x97 | EQ2A1H | | | | | | | | | Programable Equalizer Band2 Coefficient-a1 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x98 | 0x99 | EQ3A0L | | | | | | | | | Programable Equalizer Band3 Coefficient-a0 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x9a | 0x9b | EQ3A0H | | | | | | | | | Programable Equalizer Band3 Coefficient-a0 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x9c | 0x9d | EQ3A1L | | | | | | | | | Programable Equalizer Band3 Coefficient-a1 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0x9e | 0x9f | EQ3A1H | | | | | | | | | Programable Equalizer Band3 Coefficient-a1 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0xa0 | 0xa1 | EQ4A0L | | | | | | | | | Programable Equalizer Band4 Coefficient-a0 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0xa2 | 0xa3 | EQ4A0H | | | | | | | | | Programable Equalizer Band4 Coefficient-a0 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0xa4 | 0xa5 | EQ4A1L | | | | | | | | | Programable Equalizer Band4 Coefficient-a1 (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0xa6 | 0xa7 | EQ4A1H | | | | | | | | | Programable Equalizer Band4 Coefficient-a1 (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0xac | 0xad | - | RALCVOL | | | | | | | | | Record ALC Volume Control | |
| | | - | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | | | |
| 0xae | 0xaf | - | - | - | - | - | - | - | RPPL | RecPlay Play Limiter Enable | | | |
| | | - | - | - | - | - | - | - | 0 | | | | |
| 0xb0 | 0xb1 | - | - | - | - | - | - | - | SCEN | Soft Clip Enable | | | |
| | | - | - | - | - | - | - | - | 0 | | | | |
| 0xb2 | 0xb3 | - | SCTHRH | | | | | | | | | Soft Clip Threshold H | |
| | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |

| INDEX | | b07 | b06 | b05 | b04 | b03 | b02 | b01 | b00 | Register Name | Note | |
|-------|------|-----------|---------|------------|---------|-------------|----------|-------|--------------------------------|-----------------------------|--|-------|
| R | W | (Initial) | | | | | | | | | | |
| 0xb4 | 0xb5 | SCTHRM | | | | | | | | Soft Clip Threshold M | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0xb6 | 0xb7 | SCTHRL | | | | | | | | Soft Clip Threshold L | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0xb8 | 0xb9 | - | - | - | - | - | SCGAIN | | | | Soft Clip Gain | |
| | | - | - | - | - | - | 0 | 0 | 1 | | | |
| 0xba | 0xbb | - | - | - | - | - | - | MCLEN | MALCEN | MIC ALC Control | | |
| | | - | - | - | - | - | - | 1 | 1 | | | |
| 0xbc | 0xbd | - | MALCDCY | | | - | MALCATK | | | MIC ALC Attack /Decay Time | | |
| | | - | 1 | 0 | 0 | - | 1 | 0 | 0 | | | |
| 0xbe | 0xbf | - | - | MALCMXGAIN | | | | | | MIC ALC Max Gain | | |
| | | - | - | 0 | 1 | 0 | 0 | 0 | 0 | | | |
| 0xc4 | 0xc5 | - | - | - | - | - | - | LCLEN | LALCEN | LINE ALC Control | | |
| | | - | - | - | - | - | - | 0 | 0 | | | |
| 0xc6 | 0xc7 | - | LALCDCY | | | - | LALCATK | | | LINE ALC Attack /Decay Time | | |
| | | - | 1 | 1 | 1 | - | 1 | 0 | 0 | | | |
| 0xc8 | 0xc9 | - | - | - | - | LALCMXGAIN | | | | | LINE ALC Max Gain | |
| | | - | - | - | - | 1 | 1 | 1 | 1 | | | |
| 0xdc | 0xdd | - | - | - | - | PALCATK | | | | | Playback ALC Attack Time Control | note1 |
| | | - | - | - | - | 0 | 1 | 0 | 0 | | | |
| 0xde | 0xdf | - | - | - | - | PALCDCY | | | | | Playback ALC Decay Time Control | note1 |
| | | - | - | - | - | 0 | 1 | 0 | 1 | | | |
| 0xe0 | 0xe1 | - | - | - | PALCLVL | | | | | | Playback ALC Target Level Control | note1 |
| | | - | - | - | 1 | 1 | 0 | 1 | 1 | | | |
| 0xe2 | 0xe3 | - | - | - | - | PALCMINGAIN | | | | | Playback ALC Min Gain Control | note1 |
| | | - | - | - | - | - | 0 | 0 | 0 | | | |
| 0xe4 | 0xe5 | - | PALCVOL | | | | | | Playback ALC Volume Control | note1 | | |
| | | - | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | | |
| 0xe6 | 0xe7 | - | - | - | - | - | PALCZCTM | | | | Playback ALC ZeroCross TimeOut | note1 |
| | | - | - | - | - | - | - | 0 | 0 | | | |
| 0xea | 0xeb | PALCFRTH | | | | PALCFREN | | - | PALCFRSP | | Playback Limiter Fast Release Setting | note1 |
| | | 0 | 0 | 0 | 1 | 0 | - | 0 | 1 | | | |
| 0xec | 0xed | - | - | LOPWTIM | | | | | - | - | HPOUT Power Up Control | |
| | | - | - | 0 | 0 | 0 | 0 | - | - | | | |

It is available at the MAPCON=0x1(Register Map Control Register 0x1c/0x1d)

| INDEX | | b07 | b06 | b05 | b04 | b03 | b02 | b01 | b00 | Register Name | Note | |
|-------|------|---------------|---------|------|--------|----------|--------|--------|--------|-------------------------------|---------------------------------|--|
| R | W | (Initial) | | | | | | | | | | |
| 0x02 | 0x03 | - | - | - | - | - | FPLLM | | | FPLL M setting | | |
| | | - | - | - | - | - | 0 | 0 | 0 | | | |
| 0x04 | 0x05 | FPLLNL | | | | | | | | FPLL N Setting(L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x06 | 0x07 | - | - | - | - | - | - | - | FPLLNH | FPLL N Setting(H) | | |
| | | - | - | - | - | - | - | - | 0 | | | |
| 0x08 | 0x09 | - | - | - | FPLLD | | | | | | FPLL D Setting | |
| | | - | - | - | 0 | 0 | 0 | 0 | 0 | | | |
| 0x0a | 0x0b | FPLLFL | | | | | | | | FPLL F Setting(L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x0c | 0x0d | FPLLFH | | | | | | | | FPLL F Setting(H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x0e | 0x0f | FPLLFDL | | | | | | | | FPLL F.D Setting(L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x10 | 0x11 | FPLLFDH | | | | | | | | FPLL F.D Setting(H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x12 | 0x13 | - | - | - | - | FPLLV | | | | | FPLL V setting | |
| | | - | - | - | - | 0 | 0 | 0 | 0 | | | |
| 0x16 | 0x17 | - | - | - | CPMODE | - | - | - | - | PLL CPMODE Setting | | |
| | | - | - | - | 0 | - | - | - | - | | | |
| 0x1c | 0x1d | - | - | - | - | - | - | - | MAPCON | RegisterMAP Control | | |
| | | - | - | - | - | - | - | - | 0 | | | |
| 0x36 | 0x37 | - | - | - | - | - | - | HPVOL | | HP output Gain Setting | | |
| | | - | - | - | - | - | - | 0 | 0 | | | |
| 0x3e | 0x3f | - | - | HALF | HPBPEN | LINDACEN | ADCSET | | | Analog Path Control | | |
| | | - | - | 1 | 0 | 0 | 1 | 1 | 1 | | | |
| 0x74 | 0x75 | - | RBLVOLL | | | | | | | | Record L Balance Volume Control | |
| | | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x76 | 0x77 | - | RBLVOLR | | | | | | | | Record R Balance Volume Control | |
| | | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x86 | 0x87 | - | - | - | - | - | - | STEEN | STEOD | Stereo Enhancer Control | | |
| | | - | - | - | - | - | - | 0 | 0 | | | |
| 0x88 | 0x89 | STE1CUT[7:0] | | | | | | | | Stereo Enhancer LPF1 CoefL | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x8a | 0x8b | STE1CUT[15:8] | | | | | | | | Stereo Enhancer LPF1 CoefH | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x8c | 0x8d | STE2CUT[7:0] | | | | | | | | Stereo Enhancer LPF2 CoefL | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0x8e | 0x8f | STE2CUT[15:8] | | | | | | | | Stereo Enhancer LPF2 CoefH | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0xa0 | 0xa1 | - | - | - | - | - | - | PLPFOD | PLPFEN | Play Programable LPF Setting | | |
| | | - | - | - | - | - | - | 0 | 0 | | | |
| 0xa2 | 0xa3 | PLPFC0L | | | | | | | | Play Programable LPF Coef (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0xa4 | 0xa5 | PLPFC0H | | | | | | | | Play Programable LPF Coef (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0xa6 | 0xa7 | - | - | - | - | - | - | RLPFOD | RLPFEN | Rec Programable LPF Setting | | |
| | | - | - | - | - | - | - | 0 | 0 | | | |
| 0xa8 | 0xa9 | RLPFC0L | | | | | | | | Rec Programable LPF Coef (L) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 0xaa | 0xab | RLPFC0H | | | | | | | | Rec Programable LPF Coef (H) | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |

Detailed Description of the Registers

Note: “-” indicates a reserved bit. They return “0” for reads. Write “0” to the bit every time. If “1” is written to this bit, the operations cannot be guaranteed.

Don't write the registers expect the map of below. If these register is written, the operations cannot be guaranteed.

“*” indicates that the register value is effective immediate without internal clock.

Sampling Rate Setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x00 | 0x01 | - | - | - | - | SR | | | |
| | | | - | - | - | - | 0 | 0 | 0 | 0 |

This register is to set the sampling rate of recording and playback. Please change this register value at recording and playback operation stop (\$12h/\$13h: RECPLAY=0h).

SR [3:0]

| SR [3:0] | Description |
|----------|-------------|
| 0x0 | 8 kHz |
| 0x1 | 11.025 kHz |
| 0x2 | 12 kHz |
| 0x3 | 16 kHz |
| 0x4 | 22.05 kHz |
| 0x5 | 24 kHz |
| 0x6 | 32 kHz |
| 0x7 | 44.1 kHz |
| 0x8 | 48 kHz |

Stereo Gain Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|---------|-----|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x06 | 0x07 | - | STEGAIN | | | | | | |
| | | | - | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

This register is to set the amount of effects of stereo emphasis. Please refer to "StereoEnhancerApplicationNote" for the details of setting.

STEGAIN[3:0]

| STEGAIN | Gain[times] | STEGAIN | Gain[times] | STEGAIN | Gain[times] | STEGAIN | Gain[times] |
|---------|-------------|---------|-------------|---------|-------------|---------|-------------|
| 0x00 | 0.000 | 0x10 | 1.000 | 0x20 | 2.000 | 0x30 | 3.000 |
| 0x01 | 0.063 | 0x11 | 1.063 | 0x21 | 2.063 | 0x31 | 3.063 |
| 0x02 | 0.125 | 0x12 | 1.125 | 0x22 | 2.125 | 0x32 | 3.125 |
| 0x03 | 0.188 | 0x13 | 1.188 | 0x23 | 2.188 | 0x33 | 3.188 |
| 0x04 | 0.250 | 0x14 | 1.250 | 0x24 | 2.250 | 0x34 | 3.250 |
| 0x05 | 0.313 | 0x15 | 1.313 | 0x25 | 2.313 | 0x35 | 3.313 |
| 0x06 | 0.375 | 0x16 | 1.375 | 0x26 | 2.375 | 0x36 | 3.375 |
| 0x07 | 0.438 | 0x17 | 1.438 | 0x27 | 2.438 | 0x37 | 3.438 |
| 0x08 | 0.500 | 0x18 | 1.500 | 0x28 | 2.500 | 0x38 | 3.500 |
| 0x09 | 0.563 | 0x19 | 1.563 | 0x29 | 2.563 | 0x39 | 3.563 |
| 0x0A | 0.625 | 0x1A | 1.625 | 0x2A | 2.625 | 0x3A | 3.625 |
| 0x0B | 0.688 | 0x1B | 1.688 | 0x2B | 2.688 | 0x3B | 3.688 |
| 0x0C | 0.750 | 0x1C | 1.750 | 0x2C | 2.750 | 0x3C | 3.750 |
| 0x0D | 0.813 | 0x1D | 1.813 | 0x2D | 2.813 | 0x3D | 3.813 |
| 0x0E | 0.875 | 0x1E | 1.875 | 0x2E | 2.875 | 0x3E | 3.875 |
| 0x0F | 0.938 | 0x1F | 1.938 | 0x2F | 2.938 | 0x3F | 3.938 |

IRQ control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|---------|---------|---------|
| | R | W | | | | | | | | |
| 0x0 | 0x08 | 0x09 | IRQPOLE(*) | - | - | - | - | SHLIREN | SHRIREN | THRIREN |
| | | | 0 | - | - | - | - | 0 | 0 | 0 |

This register controls the interrupt enable or disable.

THRIREN

This bit controls thermal error interrupt.

| THRIREN | Description |
|---------|--|
| 0 | If thermal error occurs, interrupt is not generated. |
| 1 | If thermal error occurs, interrupt is generated. |

SHRIREN

This bit controls interrupt of left speaker short error.

| SHRIREN | Description |
|---------|---|
| 0 | If left speaker short error occurs, interrupt is not generated. |
| 1 | If left speaker short error occurs, interrupt is generated. |

SHLIREN

This bit controls interrupt of right speaker short error.

| SHLIREN | Description |
|---------|--|
| 0 | If right speaker short error occurs, interrupt is not generated. |
| 1 | If right speaker short error occurs, interrupt is generated. |

IRQPOLE

This bit specifies polarity of interrupt pin (IRQB).

| IRQPOLE | Description |
|---------|--|
| 0 | If interrupt occur, IRQB pin output L level. |
| 1 | If interrupt occur, IRQB pin output H level. |

IRQ Status Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|--------|--------|--------|
| | R | W | | | | | | | | |
| 0x0 | 0x0a | 0x0b | - | - | - | - | - | SHLSTS | SHRSTS | THRSTS |
| | | | - | - | - | - | - | 0 | 0 | 0 |

This register can check the interrupt status. If writing "1", state is clearable.

THRSTS

This bit can check thermal error interrupt state.

| THRSTS | Description |
|--------|-------------------------|
| 0 | No thermal error. |
| 1 | Thermal error occurred. |

SHRSTS

This bit can check left speaker short error interrupt status.

| SHRSTS | Description |
|--------|------------------------------------|
| 0 | No left speaker short error. |
| 1 | Left speaker short error occurred. |

SHLSTS

This bit can check right speaker short error interrupt status.

| SHLSTS | Description |
|--------|-------------------------------------|
| 0 | No right speaker short error. |
| 1 | Right speaker short error occurred. |

Clock Enable Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----------|----------|----------|-----------|
| | R | W | | | | | | | | |
| 0x0 | 0x0c | 0x0d | - | - | - | - | MCLKOE(*) | PLLOE(*) | PLLEN(*) | MCLKEN(*) |
| | | | - | - | - | - | 0 | 0 | 0 | 0 |

This register controls clock operation.

MCLKEN

This bit is to set the MCLKI pin enable or disable. A clock is not transmitted to an inside in case of the disable.

| MCLKEN | Description |
|--------|--|
| 0 | MCLKI pin input disabled. The clock stops at the first input buffer of the MCLKI pin. |
| 1 | MCLKI pin input enabled |

PLLEN

This bit is to set the status of PLL.

| PLLEN | Description |
|-------|----------------|
| 0 | PLL power down |
| 1 | PLL power up |

At the first, set PLL Setting registers. After that, set PLLEN bit to "1".

PLLOE

This bit is to set the status of PLL output. Set this bit to "1" after PLL operation has stabilized. Also, this bit must be set to "1" if PLL is not used, otherwise internal clock can not be provided.

| PLLOE | Description |
|-------|--------------------|
| 0 | PLL output disable |
| 1 | PLL output enable |

MCLKOE

This bit is to set the status of output signal from MCLKO pin.

| MCLKOE | Description |
|--------|--------------------|
| 0 | Normally Operation |
| 1 | Prohibited |

Clock Input/Output Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|------------|-----|-----------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x0e | 0x0f | - | - | - | PLLISEL(*) | | CLKSEL(*) | | |
| | | | - | - | - | 0 | 0 | 0 | 0 | 0 |

This register is to select internal clock. It is to use or not use and to create MCLKI input or internal clock divided PLL.

CLKSEL[2:0]

These bits are to select the internal clock.

| CLKSEL[2:0] | Description |
|-------------|--|
| 0x0 | Use PLL output clock.(256fs) |
| 0x2 | Use PLL output clock.(512fs) PLL output clock is divided by 2 in the LSI. |
| 0x3 | Use PLL output clock.(1024fs) PLL output clock is divided by 4 in the LSI. |
| 0x4 | 256fs external clock from MCLKI pin input. MCLKI pin input is directly used in the LSI. |
| 0x6 | 512fs external clock from MCLKI pin input. MCLK pin input is divided by 2 in the LSI. |
| 0x7 | 1024fs external clock from MCLKI pin input. MCLK pin input is divided by 4 in the LSI. |

PLLISEL[1:0]

This bit is to select the input clock to Audio PLL. If not use PLL, it is to set 0x0.

| PLLISEL[1:0] | Description |
|--------------|---------------------|
| 0x0 | Use LRCLK input pin |
| 0x1 | Use MCLKI input pin |
| 0x2 | Use BCLK input pin |

Software Reset Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----|------------|
| | R | W | | | | | | | | |
| 0x0 | 0x10 | 0x11 | - | - | - | - | - | - | - | SOFTRST(*) |
| | | | - | - | - | - | - | - | - | 0 |

This register is for software reset. CPU interface and this register are reset by writing SOFTRST bit to "1". And then, write "0" for releasing reset.

Record/Playback Running Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|---------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x12 | 0x13 | - | - | - | - | - | RECPLAY | | |
| | | | - | - | - | - | - | 0 | 0 | 0 |

This register controls SAI input/output for ADC and DAC.

RECPLAY[2:0]

This bit controls SAI input/output for ADC and DAC. ADC and DAC can be executed at same time. ADC output data can be directly outputted to DAC path. And about the transition of SAI input/output for ADC and DAC, please refer to Chapter “State Transition about Sound Control”. It is prohibited the other direct transition. So it is recommended that transition may be changed via Sound Stop (RECPLAY=0x0).

| RECPLAY[2:0] | Description |
|--------------|---|
| 0x0 | SAI input/output for ADC and DAC stop state |
| 0x1 | ADC enable, SAI output state Analog input (Microphone/Line) is converted from analog to digital, and transferred through SAI. |
| 0x2 | DAC enable, SAI input state. SAI received data is converted from digital to analog and output from analog output path (Speaker/Headphone Output). |
| 0x3 | ADC enable, SAI output state and DAC enable, SAI input state. Analog input (Microphone/Line) is converted from analog to digital, and transferred through SAI and SAI received data is converted from digital to analog and output from analog output path (Speaker/Headphone Output). |
| 0x7 | ADC enable, SAI output state and DAC enable state. Analog input (Microphone/Line) input is converted from analog to digital, and transferred through SAI and this data is converted from digital to analog and output from analog output path (Speaker/Headphone Output). |

Mic Input Charging Time Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|--------|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x14 | 0x15 | - | - | MCTIME | | | | | |
| | | | - | - | 0 | 0 | 0 | 0 | 0 | 0 |

This register is to select the wait time for microphone input load charge. The LSI work recording signal are mute when from RECPLAY is changed from 0x0 until MCTIME. This time contains required time of initializing internal circuit that is 40/fs. It must be waited the setting time to start recording or playback. In addition the wait time at starting playback is always 40/fs regardless of the setting value of this register.

MCTIME[5:0]

These bits are to set the wait time for Mic input charging time at starting recording. The wait time is available 40/fs and 128/fs to 8064/fs every 128fs. According to following table, this time is proportional to sampling frequency (fs).

| MCTIME[5:0] | fs equivalent | Time(fs=48kHz) |
|-------------|-----------------|----------------|
| 0x00 | 40/fs | 0.8ms |
| 0x01 | 128/fs | 2.7ms |
| 0x02 | 256/fs | 5.3ms |
| 0x03 | 384/fs | 8.0ms |
| 0x04 - 0x3D | (128/fs / step) | : |
| 0x3E | 7936/fs | 165.3ms |
| 0x3F | 8064/fs | 168.0ms |

Note) the wait time for microphone input load charge

The wait time can be optionally to set with Mic Input Charging Time register. It is a recommended value of MIN1 coupling capacitor at the charge time.

Charge time

| Capacity of Capacitor | Charge time (minimum) | MCTIME setting time (fs=48kHz) |
|-----------------------|-----------------------|--------------------------------|
| 0.1µF | 16ms | 0x09 |
| 0.22µF | 36ms | 0x14 |

* Charge time is proportional to Capacity of Capacitor.

Register MAP Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----------|
| | R | W | | | | | | | | |
| ALL | 0x1c | 0x1d | - | - | - | - | - | - | - | MAPCON(*) |
| | | | - | - | - | - | - | - | - | 0 |

MAPCON

The register is to set register map. Please refer register map about the map of the changing object.

| MAPCON | Description |
|--------|-----------------------------|
| 0 | Register MAP0 access enable |
| 1 | Register MAP1 access enable |

Analog Reference Power Management Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-------|-------|-----|-----|--------|------------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x20 | 0x21 | LOREN | LOLEN | LOSEL | - | - | MICBEN | VMIDCON(*) | |
| | | | 0 | 0 | 0 | - | - | 0 | 0 | 0 |

This register controls power up and down of the Headphone Output amplifier and the analog reference voltage generation circuit.

VMIDCON[1:0]

These bits control power up and down of the VMID generation circuit. Power up time can be reduced by using high speed power up mode. VMID generation circuit should be changed to normal mode after power up is completed. About the timing of setting, please refer to the section of "Analog Reference Voltage (VMID) generation circuit".

| VMIDCON[1:0] | Description |
|--------------|---|
| 0x0 | VMID generation circuit power down |
| 0x1 | VMID generation circuit power up high speed power up mode |
| 0x2 | VMID generation circuit power up normal mode |

MICBEN

This bit controls power up and down of the MICBIAS generation circuit.

| MICBEN | Description |
|--------|---------------------------------------|
| 0 | MICBIAS generation circuit power down |
| 1 | MICBIAS generation circuit power up |

LOSEL

This bit specify input path to Headphone Output amplifier. It is available DAC output or SPVOL output.

| LOSEL | Description |
|-------|---|
| 0 | DAC output is directly outputted from HPOUT. |
| 1 | DAC output is outputted from HPOUT through SPVOL block. |

LOLEN

This bit controls HPOUT left output enable or disable.

| LOLEN | Description |
|-------|----------------------------|
| 0 | HPOUT left output disabled |
| 1 | HPOUT left output enabled |

LOREN

This bit controls HPOUT right output enable or disable.

| LOREN | Description |
|-------|-----------------------------|
| 0 | HPOUT right output disabled |
| 1 | HPOUT right output enabled |

Analog Input Power Management Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|----------|--------|--------|------|
| | R | W | | | | | | | | |
| 0x0 | 0x22 | 0x23 | - | - | - | - | PGAEN(*) | ADCREN | ADCLEN | LIEN |
| | | | - | - | - | - | 0 | 0 | 0 | 0 |

This register controls power up and down of the input part of the analog circuit.

LIEN

This bit controls power up and down of the Line input amplifier.

| LIEN | Description |
|------|---------------------------------|
| 0 | Line input amplifier power down |
| 1 | Line input amplifier power up |

This LSI charge the coupling capacitor of LIN pins, when LIEN bit is changed from 0 to 1. This period's time is counted by master clock which is between about 97ms and about 142ms. In this period, the output path of LINVOL amplifier is open, so input signal is muted for next part amplifier. It does n't depend on LIN1EN,LIN2EN,LIN3EN,LINMXEN and MICMXEN registers.

*Pleas set this register to "1" at MIC recording.

ADCLEN

This bit controls power up and down of the ADC left.

| ADCLEN | Description |
|--------|---------------------|
| 0 | ADC left power down |
| 1 | ADC left power up |

ADCREN

This bit controls power up and down of the ADC right.

| ADCREN | Description |
|--------|----------------------|
| 0 | ADC right power down |
| 1 | ADC right power up |

PGAEN

This bit controls power up and down of the MIC input amplifier.

| PGAEN | Description |
|-------|--------------------------------|
| 0 | Mic input amplifier power down |
| 1 | Mic input amplifier power up |

DAC Power Management Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|--------|--------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x24 | 0x25 | - | - | - | - | - | DACREN | DACLEN | - |
| | | | - | - | - | - | - | 0 | 0 | - |

This register controls power up and down of the DAC

DACLEN

This bit controls power ON and OFF of the DAC left

| DACLEN | Description |
|--------|---------------------|
| 0 | DAC left power down |
| 1 | DAC left power up |

DACREN

This bit controls power ON and OFF of the DAC right

| DACREN | Description |
|--------|----------------------|
| 0 | DAC right power down |
| 1 | DAC right power up |

Speaker Amplifier Power Management Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-------|--------|--------|
| | R | W | | | | | | | | |
| 0x0 | 0x26 | 0x27 | - | - | - | - | - | SPDEN | SPABEN | SPMVEN |
| | | | - | - | - | - | - | 0 | 0 | 0 |

This register controls power up and down of the speaker amplifier and volume amplifier.

SPMVEN

This bit controls power up and down of the MIXVOL (MIXER and SPVOL volume) block.

| SPMVEN | Description |
|--------|-------------------------|
| 0 | MIXVOL block power down |
| 1 | MIXVOL block power up |

SPABEN

This bit controls power up and down of the Class-AB speaker amplifier.

| SPABEN | Description |
|--------|---------------------------------------|
| 0 | Class-AB speaker amplifier power down |
| 1 | Class-AB speaker amplifier power up |

SPDEN

This bit controls power up and down of the Class-D speaker amplifier.

| SPDEN | Description |
|-------|--------------------------------------|
| 0 | Class-D speaker amplifier power down |
| 1 | Class-D speaker amplifier power down |

*If SPABEN and SPDEN are set to 1 at once, SPABEN is effective.

AM avoidance Control / SPAMP input Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|---------|---------|-------|-------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x2a | 0x2b | TEST2 | - | BP2SPEN | MV2SPEN | TEST1 | TEST0 | AMA | |
| | | | 0 | - | 0 | 1 | 1 | 1 | 1 | 1 |

This register controls input path of speaker amplifier, select operation frequency of Class-D speaker amplifier, and for shipment test.

AMA

This bits control operation frequency of Class-D speaker amplifier by AM avoidance function.

| AMA[1:0] | Description |
|----------|-------------|
| 0x0 | 700kHz |
| 0x1 | 600kHz |
| 0x2 | 500kHz |
| 0x3 | 400kHz |

TEST0

This bit is for shipment test. Don't change from initial value.

| TEST0 | Description |
|-------|-------------------------|
| 1 | Test register. Use by 1 |

TEST1

This bit is for shipment test. Don't change from initial value.

| TEST1 | Description |
|-------|-------------------------|
| 1 | Test register. Use by 1 |

MV2SPEN

This bit controls the input signal of speaker amplifier from mixer volume.

| MV2SPEN | Description |
|---------|--|
| 0 | Don't input the signal from mixer volume to speaker amplifier. |
| 1 | Input the signal from mixer volume to speaker amplifier. |

BP2SPEN

This bit controls the input signal of speaker amplifier from mixer volume.

| BP2SPEN | Description |
|---------|--|
| 0 | Don't input the signal from BEEPIN amplifier to speaker amplifier. |
| 1 | Input the signal from BEEPIN amplifier to speaker amplifier. |

TEST2

This bit is for shipment test. Don't change from initial value.

| TEST2 | Description |
|-------|--------------------------|
| 0 | Test register. Use by 0. |

Zero Cross Comparator Power Management Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x2e | 0x2f | - | - | - | - | - | - | ZCEN | - |
| | | | - | - | - | - | - | - | 0 | - |

This register is to set ON and OFF of zerocross function about refreshing PLAYVOL setting by PALC controller.

ZCEN

The zero cross is applied to refreshing PLAYVOL settings when zero cross detection operation is effective.

| ZCEN | Description |
|------|--|
| 0 | Zerocross detection operation is invalid. The gain setting of PLAYVOL is immediately reflected when the settings are changed. |
| 1 | Zerocross detection operation is effective. The gain setting of PLAYVOL is reflected after zerocross detection. |

BEEPIN Amp Control / MICBIAS Voltage Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|---------|-----|-------|------------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x30 | 0x31 | - | - | - | BPINCON | | TEST3 | MICBCON18S | |
| | | | - | - | - | 0 | 0 | 1 | 0 | 0 |

This register controls voltage value of microphone bias, and controls BEEPIN amplifier and for shipment test.

MICBCON18S[1:0]

These bits are to set the MICBIAS. Set the MICBIAS voltage less than HVDD x 0.85.

| MICBCON18S | Output Voltage (the case of REGOUT =1.8V) |
|------------|---|
| 0x0 | 1.50V |
| 0x1 | 2.00V |
| 0x2 | 2.50V |
| 0x3 | 3.00V |

TEST3

This bit is for shipment test. Don't change from initial value.

| TEST3 | Description |
|-------|-------------------------|
| 1 | Test register. Use by 1 |

BPINCON[1:0]

These bits

| BPINCON | Output Voltage (the case of REGOUT =1.8V) |
|---------|---|
| 0x0 | BEEPIN amplifier power down |
| 0x1 | Prohibited |
| 0x2 | BEEPIN amplifier power up at normal mode |
| 0x3 | BEEPIN amplifier power up at high speed power up mode |

Line-In Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|--------|---------|---------|--------|--------|--------|
| | R | W | | | | | | | | |
| 0x0 | 0x32 | 0x33 | - | - | MXGAIN | LINMXEN | MICMXEN | LIN3EN | LIN2EN | LIN1EN |
| | | | - | - | 0 | 1 | 0 | 0 | 0 | 1 |

This register controls the operation of Line input amplifier path and Mixer (LineMix)

LIN1EN

| LIN1EN | Description |
|--------|---------------------------------------|
| 0 | Line input amplifier LIN1 path is OFF |
| 1 | Line input amplifier LIN1 path is ON |

LIN2EN

| LIN2EN | Description |
|--------|---------------------------------------|
| 0 | Line input amplifier LIN2 path is OFF |
| 1 | Line input amplifier LIN2 path is ON |

LIN3EN

| LIN3EN | Description |
|--------|---------------------------------------|
| 0 | Line input amplifier LIN3 path is OFF |
| 1 | Line input amplifier LIN3 path is ON |

MICMXEN

| MICMXEN | Description |
|---------|--------------------------------------|
| 0 | Mixing of MIC path in LineMix is OFF |
| 1 | Mixing of MIC path in LineMix is ON |

LINMXEN

| LINMXEN | Description |
|---------|--------------------------------------|
| 0 | Mixing of LIN path in LineMix is OFF |
| 1 | Mixing of LIN path in LineMix is ON |

MXGAIN

| MXGAIN | Description |
|--------|----------------------------------|
| 0 | Mixing Gain in LineMix is 0dB |
| 1 | Mixing g Gain in LineMix is -6dB |

Speaker Amplifier Volume Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-------|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x3a | 0x3b | - | - | SPVOL | | | | | |
| | | | - | - | 1 | 1 | 0 | 0 | 1 | 1 |

This register is to set the Mixvol volume Gain.

SPVOL[5:0]

| SPVOL[5:0] | Gain[dB] | MEMO | Value | Gain[dB] | MEMO |
|------------|----------|-------------|-------|----------|-----------|
| 0x3F | 6.0 | ↓0.5dB step | 0x1F | -14.0 | |
| 0x3E | 5.5 | | 0x1E | -15.0 | |
| 0x3D | 5.0 | | 0x1D | -16.0 | |
| 0x3C | 4.5 | | 0x1C | -17.0 | |
| 0x3B | 4.0 | | 0x1B | -18.0 | |
| 0x3A | 3.5 | | 0x1A | -19.0 | |
| 0x39 | 3.0 | | 0x19 | -20.0 | |
| 0x38 | 2.5 | | 0x18 | -21.0 | |
| 0x37 | 2.0 | | 0x17 | -22.0 | |
| 0x36 | 1.5 | | 0x16 | -23.0 | |
| 0x35 | 1.0 | | 0x15 | -24.0 | |
| 0x34 | 0.5 | | 0x14 | -25.0 | |
| 0x33 | 0.0 | | 0x13 | -26.0 | |
| 0x32 | -0.5 | | 0x12 | -27.0 | |
| 0x31 | -1.0 | | 0x11 | -28.0 | |
| 0x30 | -1.5 | | 0x10 | -29.0 | |
| 0x2F | -2.0 | | 0x0F | -30.0 | |
| 0x2E | -2.5 | | 0x0E | -31.0 | |
| 0x2D | -3.0 | | 0x0D | -32.0 | ↓2dB step |
| 0x2C | -3.5 | | 0x0C | -34.0 | |
| 0x2B | -4.0 | | 0x0B | -36.0 | |
| 0x2A | -4.5 | | 0x0A | -38.0 | |
| 0x29 | -5.0 | | 0x09 | -40.0 | |
| 0x28 | -5.5 | | 0x08 | -42.0 | |
| 0x27 | -6.0 | | 0x07 | -44.0 | |
| 0x26 | -7.0 | ↓1dB step | 0x06 | -46.0 | |
| 0x25 | -8.0 | | 0x05 | -48.0 | |
| 0x24 | -9.0 | | 0x04 | -50.0 | |
| 0x23 | -10.0 | | 0x03 | -52.0 | |
| 0x22 | -11.0 | | 0x02 | -54.0 | |
| 0x21 | -12.0 | | 0x01 | -56.0 | |
| 0x20 | -13.0 | | 0x00 | MUTE | |

Playback Digital Attenuator Control Register

| Playback Digital Attenuator Control Register | | | | | | | | | | | |
|--|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|--|
| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 | |
| | R | W | | | | | | | | | |
| 0x0 | 0x3e | 0x3f | PDATT | | | | | | | | |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

This register is to set the digital VolumeGain on DAC path.
It is available MUTE and -71.5dB to 0.5dB every 0.5dB.

PDATT[7:0]

These bits are to set PLAYDATT : digital VolumeGain.

| PDATT[7:0] | Gain[dB] | Value | Gain[dB] | Value | Gain[dB] | Value | Gain[dB] |
|--------------|------------|-------|----------|-------|----------|-------|-------------------|
| 0x00 to 0x6E | Prohibited | 0x93 | -54.0 | 0xB8 | -35.5 | 0xDD | -17.0 |
| 0x6F | MUTE | 0x94 | -53.5 | 0xB9 | -35.0 | 0xDE | -16.5 |
| 0x70 | -71.5 | 0x95 | -53.0 | 0xBA | -34.5 | 0xDF | -16.0 |
| 0x71 | -71.0 | 0x96 | -52.5 | 0xBB | -34.0 | 0xE0 | -15.5 |
| 0x72 | -70.5 | 0x97 | -52.0 | 0xBC | -33.5 | 0xE1 | -15.0 |
| 0x73 | -70.0 | 0x98 | -51.5 | 0xBD | -33.0 | 0xE2 | -14.5 |
| 0x74 | -69.5 | 0x99 | -51.0 | 0xBE | -32.5 | 0xE3 | -14.0 |
| 0x75 | -69.0 | 0x9A | -50.5 | 0xBF | -32.0 | 0xE4 | -13.5 |
| 0x76 | -68.5 | 0x9B | -50.0 | 0xC0 | -31.5 | 0xE5 | -13.0 |
| 0x77 | -68.0 | 0x9C | -49.5 | 0xC1 | -31.0 | 0xE6 | -12.5 |
| 0x78 | -67.5 | 0x9D | -49.0 | 0xC2 | -30.5 | 0xE7 | -12.0 |
| 0x79 | -67.0 | 0x9E | -48.5 | 0xC3 | -30.0 | 0xE8 | -11.5 |
| 0x7A | -66.5 | 0x9F | -48.0 | 0xC4 | -29.5 | 0xE9 | -11.0 |
| 0x7B | -66.0 | 0xA0 | -47.5 | 0xC5 | -29.0 | 0xEA | -10.5 |
| 0x7C | -65.5 | 0xA1 | -47.0 | 0xC6 | -28.5 | 0xEB | -10.0 |
| 0x7D | -65.0 | 0xA2 | -46.5 | 0xC7 | -28.0 | 0xEC | -9.5 |
| 0x7E | -64.5 | 0xA3 | -46.0 | 0xC8 | -27.5 | 0xED | -9.0 |
| 0x7F | -64.0 | 0xA4 | -45.5 | 0xC9 | -27.0 | 0xEE | -8.5 |
| 0x80 | -63.5 | 0xA5 | -45.0 | 0xCA | -26.5 | 0xEF | -8.0 |
| 0x81 | -63.0 | 0xA6 | -44.5 | 0xCB | -26.0 | 0xF0 | -7.5 |
| 0x82 | -62.5 | 0xA7 | -44.0 | 0xCC | -25.5 | 0xF1 | -7.0 |
| 0x83 | -62.0 | 0xA8 | -43.5 | 0xCD | -25.0 | 0xF2 | -6.5 |
| 0x84 | -61.5 | 0xA9 | -43.0 | 0xCE | -24.5 | 0xF3 | -6.0 |
| 0x85 | -61.0 | 0xAA | -42.5 | 0xCF | -24.0 | 0xF4 | -5.5 |
| 0x86 | -60.5 | 0xAB | -42.0 | 0xD0 | -23.5 | 0xF5 | -5.0 |
| 0x87 | -60.0 | 0xAC | -41.5 | 0xD1 | -23.0 | 0xF6 | -4.5 |
| 0x88 | -59.5 | 0xAD | -41.0 | 0xD2 | -22.5 | 0xF7 | -4.0 |
| 0x89 | -59.0 | 0xAE | -40.5 | 0xD3 | -22.0 | 0xF8 | -3.5 |
| 0x8A | -58.5 | 0xAF | -40.0 | 0xD4 | -21.5 | 0xF9 | -3.0 |
| 0x8B | -58.0 | 0xB0 | -39.5 | 0xD5 | -21.0 | 0xFA | -2.5 |
| 0x8C | -57.5 | 0xB1 | -39.0 | 0xD6 | -20.5 | 0xFB | -2.0 |
| 0x8D | -57.0 | 0xB2 | -38.5 | 0xD7 | -20.0 | 0xFC | -1.5 |
| 0x8E | -56.5 | 0xB3 | -38.0 | 0xD8 | -19.5 | 0xFD | -1.0 |
| 0x8F | -56.0 | 0xB4 | -37.5 | 0xD9 | -19.0 | 0xFE | -0.5 |
| 0x90 | -55.5 | 0xB5 | -37.0 | 0xDA | -18.5 | 0xFF | 0.0 Prohibited |
| 0x91 | -55.0 | 0xB6 | -36.5 | 0xDB | -18.0 | | |
| 0x92 | -54.5 | 0xB7 | -36.0 | 0xDC | -17.5 | | |

*Set 0xFF is prohibited. It has possibilities that DAC output waveform has distorted.

Amplifier Volume Control Function Enable Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|--------|--------|
| | R | W | | | | | | | | |
| 0x0 | 0x48 | 0x49 | - | - | - | - | - | - | AVMUTE | AVFADE |
| | | | - | - | - | - | - | - | 0 | 0 |

This register is to set the Mixvol volume fade function and mute function.

AVFADE

This bit is to set the ON and OFF of the Mixvol volume fade function.

| AVFADE | Description |
|--------|--|
| 0 | Fade function OFF The register setting value of SPVOL is used actual volume value as it is. Therefore the value is effective immediate. |
| 1 | Fade function ON The volume is changing to the register setting value of SPVOL with 1 step per AVFCON register step time. |

AVMUTE

This bit is to set the volume to the mute state. The fade function by AVFADE is effective against the volume change by this bit. And MixVol Volume value by SPVOL is held and return to setting Volume on release AVMUTE

| Value | Description |
|-------|--|
| 0 | MixVol volume is set to MUTE OFF. Register value of SPVOL is effective for MixVol volume. |
| 1 | MixVol volume is set to MUTE. Register value of SPVOL cannot be changed by this bit, the volume is resumed by releasing this bit (AVMUTE=0) to the original setting value of SPVOL. |

* Related Register

SPVOL: MixVolVolume Control Register (0x3a/0x3b)

AVFCON: MixVol Volume Fader Control Register (0x4a/0x4b)

Amplifier Volume Fader Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|--------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x4a | 0x4b | - | - | - | - | - | AVFCON | | |
| | | | - | - | - | - | - | 0 | 0 | 0 |

This register controls the MixVol volume fade function.

AVFCON[2:0]

These bits are to set the volume change step time of the MixVol volume fade function. The volume changes step by step with this setting period. Step time is in proportion to sampling frequency (fs) as following table.

| AVFCON[2:0] | fs equivalent | Time(fs=48kHz) |
|-------------|---------------|----------------|
| 0x0 | 1/fs | 20.8µs |
| 0x1 | 4/fs | 83.3µs |
| 0x2 | 16/fs | 333µs |
| 0x3 | 64/fs | 1.33ms |
| 0x4 | 256/fs | 5.33ms |
| 0x5 | 1024/fs | 21.3ms |
| 0x6 | 4096/fs | 85.3ms |
| 0x7 | 16384/fs | 341.ms |

SAI Transmitter Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|------|------|--------|------|------|------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x4c | 0x4d | PCMFO24 | FMT0 | MSBO | ISSCKO | AFOO | DLYO | WSLO | |
| | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

This register controls the SAI transmit format setting. This register setting must not be changed during SAI operation. Set this register as same as SAI Receiver Control Register.

WSLO

This bit specifies the LRCLK polarity at this LSI's transmission. This bit must be set at "1" when the Flame synchronous transfer mode (FMT0 is "1").

| WSLO | Description |
|------|--|
| 0 | Left channel transmission at LRCLK is "L" level; right channel transmission at LRCLK is "H" level. |
| 1 | Left channel transmission at LRCLK is "H" level; right channel transmission at LRCLK is "L" level. |

DLYO

This bit specifies the existence for serial output data one clock delay of master device.

| DLYO | Description |
|------|--------------------------|
| 0 | Serial data delay exists |
| 1 | No serial data delay |

AFOO

This bit specifies left-justify or right-justify. In case of the slave mode, this bit is ignored and fixed at left-justify. This bit must be set at "0" when the Flame synchronous transfer mode (FMT0 is "1").

| AFOO | Description |
|------|---------------|
| 0 | Left-justify |
| 1 | Right-justify |

ISSCKO

This bit specifies 32fs or 64fs.

| ISSCKO | Description |
|--------|-------------|
| 0 | 32fs |
| 1 | 64fs |

MSBO

This bit specifies MSB-first or LSB-first of the SAI transmission data.

| MSBO | Description |
|------|-------------|
| 0 | MSB-first |
| 1 | LSB-first |

FMT0

This bit specifies transmission mode.

| FMT0 | Description |
|------|---------------------------------|
| 0 | SAI_LRCLK transfer mode |
| 1 | Flame synchronous transfer mode |

PCMFO24

This bit specifies PCM format of SAI transmission data.

| PCMFO24 | Description |
|---------|-------------|
| 0x2 | 16bit PCM |
| 0x3 | 24bit PCM |
| Other | Prohibited |

SAI Receiver Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|------|------|--------|------|------|------|
| | R | W | | | | | | | | |
| 0x0 | 0x4e | 0x4f | PCMF124 | | FMTI | MSBI | ISSCKI | AFOI | DLYI | WSLI |
| | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

This register controls the setting for the SAI receive format. Do not change this register during operation of the SAI. Set this register as same as SAI Transmitter Control Register.

WSLI

This bit is to select LRCLK polarity of this LSI. This bit must be set at "1" when the Flame synchronous transfer mode (FMTI is "1").

| WSLI | Description |
|------|--|
| 0 | LEFT channel is received when LRCLK is "L" level, right channel is received at LRCLK is "H" level. |
| 1 | LEFT channel is received when LRCLK is "H" level, right channel is received at LRCLK is "L" level. |

DLYI

This bit specifies the existence for serial input data one clock delay of master device.

| DLYI | Description |
|------|--------------------------|
| 0 | Serial data delay exists |
| 1 | No serial data delay |

AFOI

This bit specifies the receiving data of Left-justify or Right-justify. This bit must be set at "0" when the Flame synchronous transfer mode (FMTI is "1").

| AFOI | Description |
|------|---------------|
| 0 | Left-justify |
| 1 | Right-justify |

ISSCKI

This bit specifies the sampling frequency of SAI_BCLK pin.

| ISSCKI | Description |
|--------|-------------|
| 0 | 32fs |
| 1 | 64fs |

MSBI

This bit specifies the SAI receiving data of MSB-first or LSB-first.

| Value | Description |
|-------|-------------|
| 0 | MSB-first |
| 1 | LSB-first |

FMTI

This bit specifies the receiving mode

| FMTI | Description |
|------|---------------------------------|
| 0 | LRCLK transfer mode |
| 1 | Flame synchronous transfer mode |

PCMF124

This bit specifies the PCM format of SAI receiving.

| Value | Description |
|-------|-------------|
| 0x2 | 16bit PCM |
| 0x3 | 24bit PCM |
| other | Prohibited |

SAI Mode select Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|------|-----|-----|-----|--------|
| | R | W | | | | | | | | |
| 0x0 | 0x50 | 0x51 | - | - | - | BSWP | - | - | - | MST(*) |
| | | | - | - | - | 0 | - | - | - | 0 |

This register is to set master mode or slave mode of the SAI. Do not change this register during SAI operation.

MST

This bit use by 0.

| MST | Description |
|-----|-------------|
| 0 | Slave mode |

BSWP

This bit is selected of the SAI output data format.

| BSWP | Description |
|------|--|
| 0 | SAI output data format (16bit Audio Data:15bit-8bit,7bit-0bit) (24bit Audio Data:23bit-16bit,15bit-8bit,7bit-0bit) |
| 1 | SAI output data format (16bit Audio Data:7bit-0bit,15bit-8bit) (24bit Audio Data:7bit-0bit,15bit-8bit 23bit-16bit) |

Speaker Amplifier output Control1 Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|--------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x52 | 0x53 | - | - | - | - | - | - | SPMIXG | |
| | | | - | - | - | - | - | - | 0 | 0 |

This register sets the gain of the speaker amplifier.

SPMIXG[1:0]

This bits sets the gain of the speaker amplifier.

| SPMIXG | Description |
|--------|-------------|
| 0 | 0dB |
| 1 | 6dB |
| 2 | 12dB |
| 3 | 18dB |

Speaker Amplifier / Lineout Amplifier output Control2 Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-------|-------|-------|--------|
| | R | W | | | | | | | | |
| 0x0 | 0x54 | 0x55 | - | - | - | - | LINOE | MICOE | DACOE | LOMIXG |
| | | | - | - | - | - | 0 | 0 | 0 | 0 |

This register sets the input signal path to a MixVol part mixer

LOMXG

This sets a mixing gain of the DAC output and the MIC output.
The Line-input is 0dB fix.

| LOMXG | Description |
|-------|--|
| 0 | The amplitude of a DAC output and the MIC output is added to MIXVOL in 0dB. |
| 1 | The amplitude of a DAC output and the MIC output is added to MIXVOL in -6dB. |

DACOE

| DACOE | Description |
|-------|---|
| 0 | The connection of DAC and MIXVOL is disable |
| 1 | The connection of DAC and MIXVOL is enable |

MICOE

| MICOE | Description |
|-------|---|
| 0 | The connection of MIC-input and MIXVOL is disable |
| 1 | The connection of MIC-input and MIXVOL is enable |

LINOE

| LINOE | Description |
|-------|--|
| 0 | The connection of Line-input and MIXVOL is disable |
| 1 | The connection of Line-input and MIXVOL is enable |

DAC Clock Setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|--------|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x58 | 0x59 | - | - | OSRSEL | | - | - | - | - |
| | | | - | - | 0 | 0 | - | - | - | - |

This register performs clock setting to use in DAC

OSRSEL[1:0]

| PLL use or nonuse | CLKSEL | Sampling Frequency | | |
|---------------------------|--------|----------------------------|----------------------------|---------------------------|
| | | 8kHz 11.025kHz 12kHz | 16kHz 22.05kHz 24kHz | 32kHz 44.1kHz 48kHz |
| PLL use | 0x0 | Prohibited | Prohibited | 0x00 |
| | 0x2 | Prohibited | 0x10 | Prohibited |
| | 0x3 | 0xe0 | Prohibited | Prohibited |
| PLL not use (MCLKI input) | 0x4 | Prohibited | 0x10 | 0x00 |
| | 0x6 | 0xa0 | 0x10 | 0x00 |
| | 0x7 | 0xe0 | 0x10 | 0x00 |

Mic Interface Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x5a | 0x5b | - | - | - | - | - | - | MINDIF(*) | - |
| | | | - | - | - | - | - | - | 1 | - |

This register controls microphone input interface.

MINDIF

| MINDIF | Description |
|--------|--|
| 0 | Use analog microphone as single-ended input. |
| 1 | Use analog microphone as differential input. |

Sound Effect Mode Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|--------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x5c | 0x5d | SEMODE | - | - | - | - | SEMODE | | |
| | | | 0 | - | - | - | - | 0 | 0 | 0 |

This register sets the filter block

SEMODE[7]

BU26156 can use the filter block in ADC path or DAC path. Filter Block can set on only ADC path or DAC path.

Please refer "Single flow section on Function Description about Filter Block.

| SEMODE[7] | Description |
|-----------|-------------------------------|
| 0 | use Filter Block in Recording |
| 1 | use Filter Block in Playback |

SEMODE[2:0]

This chooses the number of the Filter bands

| SEMODE[2:0] | Description |
|-------------|------------------------|
| 0x0 | Notch5 band / EQ0 band |
| 0x1 | Notch4 band / EQ1 band |
| 0x2 | Notch3 band / EQ2 band |
| 0x3 | Notch2 band / EQ3 band |
| 0x4 | Notch1 band / EQ4 band |
| 0x5 | Notch0 band / EQ5 band |

Record Path select Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|---------|------|------|
| | R | W | | | | | | | | |
| 0x0 | 0x5e | 0x5f | - | - | - | - | - | MONOREC | I2SR | I2SL |
| | | | - | - | - | - | - | 0 | 0 | 0 |

This register is to control recording path.

In case of changing this register setting, you must stop this LSI by RECPLAY bit in Record/Playback Running Control Register. A setup of I2SL=1 and I2SR=1 is prohibition.

I2SL

This bit is to select the path to Left channel of SAI transmit data.

| I2SL | Description |
|------|--|
| 0 | SAI left channel data is from left channel analog microphone input. |
| 1 | SAI left channel data is from right channel analog microphone input. |

I2SR

This bit is to select the path to Right channel of SAI transmit data.

| I2SR | Description |
|------|---|
| 0 | SAI right channel data is from right channel analog microphone input. |
| 1 | SAI right channel data is from left channel analog microphone input. |

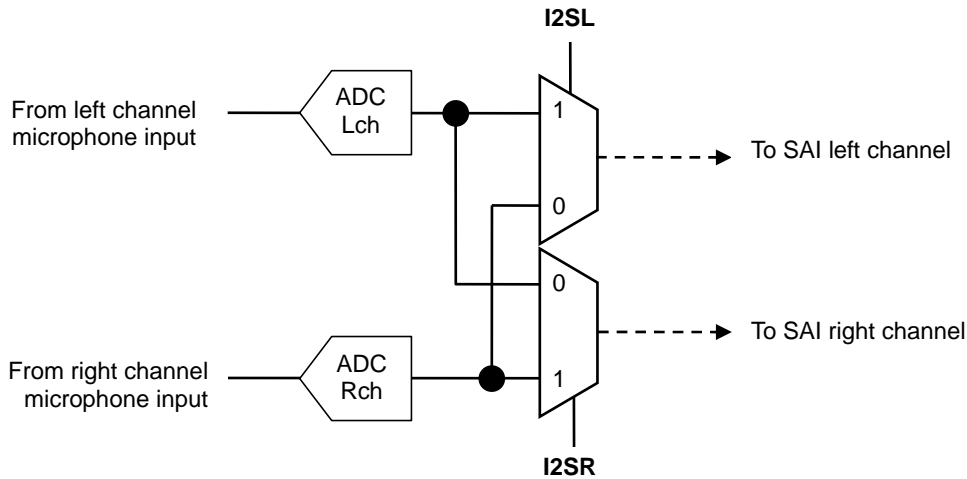


Figure 37

MONOREC

This bit chooses whether ADC output data connects in stereo, or it changes and connects in monaural.

| MONOREC | Description |
|---------|---|
| 0 | ADC output data connects in stereo Lch Output is Lch-ADC data Rch Output is Rch-ADC data |
| 1 | ADC output data changes and connects in monaural. Lch Output is (Lch-ADC data + Rch-ADC data) / 2 Rch Output is (Lch-ADC data + Rch-ADC data) / 2 |

Record Digital Attenuator Control Register

| Record Digital Attenuator Control Register | | | | | | | | | | | |
|--|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|--|
| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 | |
| | R | W | | | | | | | | | |
| 0x0 | 0x60 | 0x61 | RDVOL | | | | | | | | |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

This register is to set the digital volume of the recording path.
 Their values are 0.5dB step from -71.5dB to 0.0dB, and mute.

RDVOL[7:0]

| RDVOL | Gain(dB) | RDVOL | Gain(dB) | RDVOL | Gain(dB) | RDVOL | Gain(dB) |
|--------------|----------------|-------|----------|-------|----------|-------|----------|
| 0x00 to 0x6E | Write prohibit | 0x93 | -54.0 | 0xB8 | -35.5 | 0xDD | -17.0 |
| 0x6F | MUTE | 0x94 | -53.5 | 0xB9 | -35.0 | 0xDE | -16.5 |
| 0x70 | -71.5 | 0x95 | -53.0 | 0xBA | -34.5 | 0xDF | -16.0 |
| 0x71 | -71.0 | 0x96 | -52.5 | 0xBB | -34.0 | 0xE0 | -15.5 |
| 0x72 | -70.5 | 0x97 | -52.0 | 0xBC | -33.5 | 0xE1 | -15.0 |
| 0x73 | -70.0 | 0x98 | -51.5 | 0xBD | -33.0 | 0xE2 | -14.5 |
| 0x74 | -69.5 | 0x99 | -51.0 | 0xBE | -32.5 | 0xE3 | -14.0 |
| 0x75 | -69.0 | 0x9A | -50.5 | 0xBF | -32.0 | 0xE4 | -13.5 |
| 0x76 | -68.5 | 0x9B | -50.0 | 0xC0 | -31.5 | 0xE5 | -13.0 |
| 0x77 | -68.0 | 0x9C | -49.5 | 0xC1 | -31.0 | 0xE6 | -12.5 |
| 0x78 | -67.5 | 0x9D | -49.0 | 0xC2 | -30.5 | 0xE7 | -12.0 |
| 0x79 | -67.0 | 0x9E | -48.5 | 0xC3 | -30.0 | 0xE8 | -11.5 |
| 0x7A | -66.5 | 0x9F | -48.0 | 0xC4 | -29.5 | 0xE9 | -11.0 |
| 0x7B | -66.0 | 0xA0 | -47.5 | 0xC5 | -29.0 | 0xEA | -10.5 |
| 0x7C | -65.5 | 0xA1 | -47.0 | 0xC6 | -28.5 | 0xEB | -10.0 |
| 0x7D | -65.0 | 0xA2 | -46.5 | 0xC7 | -28.0 | 0xEC | -9.5 |
| 0x7E | -64.5 | 0xA3 | -46.0 | 0xC8 | -27.5 | 0xED | -9.0 |
| 0x7F | -64.0 | 0xA4 | -45.5 | 0xC9 | -27.0 | 0xEE | -8.5 |
| 0x80 | -63.5 | 0xA5 | -45.0 | 0xCA | -26.5 | 0xEF | -8.0 |
| 0x81 | -63.0 | 0xA6 | -44.5 | 0xCB | -26.0 | 0xF0 | -7.5 |
| 0x82 | -62.5 | 0xA7 | -44.0 | 0xCC | -25.5 | 0xF1 | -7.0 |
| 0x83 | -62.0 | 0xA8 | -43.5 | 0xCD | -25.0 | 0xF2 | -6.5 |
| 0x84 | -61.5 | 0xA9 | -43.0 | 0xCE | -24.5 | 0xF3 | -6.0 |
| 0x85 | -61.0 | 0xAA | -42.5 | 0xCF | -24.0 | 0xF4 | -5.5 |
| 0x86 | -60.5 | 0xAB | -42.0 | 0xD0 | -23.5 | 0xF5 | -5.0 |
| 0x87 | -60.0 | 0xAC | -41.5 | 0xD1 | -23.0 | 0xF6 | -4.5 |
| 0x88 | -59.5 | 0xAD | -41.0 | 0xD2 | -22.5 | 0xF7 | -4.0 |
| 0x89 | -59.0 | 0xAE | -40.5 | 0xD3 | -22.0 | 0xF8 | -3.5 |
| 0x8A | -58.5 | 0xAF | -40.0 | 0xD4 | -21.5 | 0xF9 | -3.0 |
| 0x8B | -58.0 | 0xB0 | -39.5 | 0xD5 | -21.0 | 0xFA | -2.5 |
| 0x8C | -57.5 | 0xB1 | -39.0 | 0xD6 | -20.5 | 0xFB | -2.0 |
| 0x8D | -57.0 | 0xB2 | -38.5 | 0xD7 | -20.0 | 0xFC | -1.5 |
| 0x8E | -56.5 | 0xB3 | -38.0 | 0xD8 | -19.5 | 0xFD | -1.0 |
| 0x8F | -56.0 | 0xB4 | -37.5 | 0xD9 | -19.0 | 0xFE | -0.5 |
| 0x90 | -55.5 | 0xB5 | -37.0 | 0xDA | -18.5 | 0xFF | 0.0 |
| 0x91 | -55.0 | 0xB6 | -36.5 | 0xDB | -18.0 | | |
| 0x92 | -54.5 | 0xB7 | -36.0 | 0xDC | -17.5 | | |

Playback Effect Volume Control Register

| Playback Effect Volume Control Register | | | | | | | | | | | |
|---|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|--|
| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 | |
| | R | W | | | | | | | | | |
| 0x0 | 0x62 | 0x63 | Effect VOL | | | | | | | | |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

This register is to set the digital volume of the playback path.
 Their values are 0.5dB step from -71.5dB to 0.0dB, and mute.

Effect Vol[7:0]

| Effect Vol | Gain(dB) | Effect Vol | Gain(dB) | Effect Vol | Gain(dB) | Effect Vol | Gain(dB) |
|--------------|----------------|------------|----------|------------|----------|------------|----------|
| 0x00 to 0x6E | Write prohibit | 0x93 | -54.0 | 0xB8 | -35.5 | 0xDD | -17.0 |
| 0x6F | MUTE | 0x94 | -53.5 | 0xB9 | -35.0 | 0xDE | -16.5 |
| 0x70 | -71.5 | 0x95 | -53.0 | 0xBA | -34.5 | 0xDF | -16.0 |
| 0x71 | -71.0 | 0x96 | -52.5 | 0xBB | -34.0 | 0xE0 | -15.5 |
| 0x72 | -70.5 | 0x97 | -52.0 | 0xBC | -33.5 | 0xE1 | -15.0 |
| 0x73 | -70.0 | 0x98 | -51.5 | 0xBD | -33.0 | 0xE2 | -14.5 |
| 0x74 | -69.5 | 0x99 | -51.0 | 0xBE | -32.5 | 0xE3 | -14.0 |
| 0x75 | -69.0 | 0x9A | -50.5 | 0xBF | -32.0 | 0xE4 | -13.5 |
| 0x76 | -68.5 | 0x9B | -50.0 | 0xC0 | -31.5 | 0xE5 | -13.0 |
| 0x77 | -68.0 | 0x9C | -49.5 | 0xC1 | -31.0 | 0xE6 | -12.5 |
| 0x78 | -67.5 | 0x9D | -49.0 | 0xC2 | -30.5 | 0xE7 | -12.0 |
| 0x79 | -67.0 | 0x9E | -48.5 | 0xC3 | -30.0 | 0xE8 | -11.5 |
| 0x7A | -66.5 | 0x9F | -48.0 | 0xC4 | -29.5 | 0xE9 | -11.0 |
| 0x7B | -66.0 | 0xA0 | -47.5 | 0xC5 | -29.0 | 0xEA | -10.5 |
| 0x7C | -65.5 | 0xA1 | -47.0 | 0xC6 | -28.5 | 0xEB | -10.0 |
| 0x7D | -65.0 | 0xA2 | -46.5 | 0xC7 | -28.0 | 0xEC | -9.5 |
| 0x7E | -64.5 | 0xA3 | -46.0 | 0xC8 | -27.5 | 0xED | -9.0 |
| 0x7F | -64.0 | 0xA4 | -45.5 | 0xC9 | -27.0 | 0xEE | -8.5 |
| 0x80 | -63.5 | 0xA5 | -45.0 | 0xCA | -26.5 | 0xEF | -8.0 |
| 0x81 | -63.0 | 0xA6 | -44.5 | 0xCB | -26.0 | 0xF0 | -7.5 |
| 0x82 | -62.5 | 0xA7 | -44.0 | 0xCC | -25.5 | 0xF1 | -7.0 |
| 0x83 | -62.0 | 0xA8 | -43.5 | 0xCD | -25.0 | 0xF2 | -6.5 |
| 0x84 | -61.5 | 0xA9 | -43.0 | 0xCE | -24.5 | 0xF3 | -6.0 |
| 0x85 | -61.0 | 0xAA | -42.5 | 0xCF | -24.0 | 0xF4 | -5.5 |
| 0x86 | -60.5 | 0xAB | -42.0 | 0xD0 | -23.5 | 0xF5 | -5.0 |
| 0x87 | -60.0 | 0xAC | -41.5 | 0xD1 | -23.0 | 0xF6 | -4.5 |
| 0x88 | -59.5 | 0xAD | -41.0 | 0xD2 | -22.5 | 0xF7 | -4.0 |
| 0x89 | -59.0 | 0xAE | -40.5 | 0xD3 | -22.0 | 0xF8 | -3.5 |
| 0x8A | -58.5 | 0xAF | -40.0 | 0xD4 | -21.5 | 0xF9 | -3.0 |
| 0x8B | -58.0 | 0xB0 | -39.5 | 0xD5 | -21.0 | 0xFA | -2.5 |
| 0x8C | -57.5 | 0xB1 | -39.0 | 0xD6 | -20.5 | 0xFB | -2.0 |
| 0x8D | -57.0 | 0xB2 | -38.5 | 0xD7 | -20.0 | 0xFC | -1.5 |
| 0x8E | -56.5 | 0xB3 | -38.0 | 0xD8 | -19.5 | 0xFD | -1.0 |
| 0x8F | -56.0 | 0xB4 | -37.5 | 0xD9 | -19.0 | 0xFE | -0.5 |
| 0x90 | -55.5 | 0xB5 | -37.0 | 0xDA | -18.5 | 0xFF | 0.0 |
| 0x91 | -55.0 | 0xB6 | -36.5 | 0xDB | -18.0 | | |
| 0x92 | -54.5 | 0xB7 | -36.0 | 0xDC | -17.5 | | |

DSP Filter Function Enable Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-------|-------|-------|-------|-------|--------|--------|
| | R | W | | | | | | | | |
| 0x0 | 0x66 | 0x67 | HPF2OD | EQ4EN | EQ3EN | EQ2EN | EQ1EN | EQ0EN | HPF2EN | HPF1EN |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

This register is to set ON or OFF for DSP filtering function.

HPF1EN

This bit is to set ON or OFF of a first-order high pass filter for DC cut. Do not change this bit during operation of the recording (0x13/0x14: RECPLAY=0x1, 0x3, or 0x7). If this bit is changed, the noise may be generated.

| HPF1EN | Description |
|--------|---|
| 0 | DC cut first-order high pass filter OFF |
| 1 | DC cut first-order high pass filter ON |

HPF2EN

This bit is to set ON or OFF of a second-order high pass filter for noise cut. (0x13h/0x14h: RECPLAY=1 or 2). If this bit is changed, the noise may be generated.

| HPF2EN | Description |
|--------|---|
| 0 | Noise cut second-order high pass filter OFF |
| 1 | Noise cut second-order high pass filter ON |

EQ0EN

This bit is to set ON or OFF of equalizer band 0. In case of changing this bit during recording and playback operation (0x13/0x14: RECPLAY=0x1, 0x2, 0x3, or 0x7), enables digital volume fade function (0x68/0x69: DVFADE=1) and then change the gain to 0dB.

| EQ0EN | Description |
|-------|--------------------------|
| 0 | equalizer band 0 disable |
| 1 | equalizer band 0 enable |

EQ1EN

This bit is to set ON or OFF of equalizer band 1. In case of changing this bit during recording and playback operation (0x13/0x14: RECPLAY=0x1, 0x2, 0x3, or 0x7), enables digital volume fade function (0x68/0x69: DVFADE=1) and then change the gain to 0dB.

| EQ1EN | Description |
|-------|--------------------------|
| 0 | equalizer band 1 disable |
| 1 | equalizer band 1 enable |

EQ2EN

This bit is to set ON or OFF of equalizer band 2. In case of changing this bit during recording and playback operation (0x13/0x14: RECPLAY=0x1, 0x2, 0x3, or 0x7), enables digital volume fade function (0x68/0x69: DVFADE=1) and then change the gain to 0dB.

| EQ2EN | Description |
|-------|--------------------------|
| 0 | equalizer band 2 disable |
| 1 | equalizer band 2 enable |

EQ3EN

This bit is to set ON or OFF of equalizer band 3. In case of changing this bit during recording and playback operation (0x13/0x14: RECPLAY=0x1, 0x2, 0x3, or 0x7), enables digital volume fade function (0x68/0x69: DVFADE=1) and then change the gain to 0dB.

| EQ3EN | Description |
|-------|--------------------------|
| 0 | equalizer band 3 disable |
| 1 | equalizer band 3 enable |

EQ4EN

This bit is to set ON or OFF of equalizer band 4. In case of changing this bit during recording and playback operation (0x13/0x14: RECPLAY=0x1, 0x2, 0x3, or 0x7), enables digital volume fade function (0x68/0x69: DVFADE=1) and then change the gain to 0dB.

| EQ4EN | Description |
|-------|--------------------------|
| 0 | equalizer band 4 disable |
| 1 | equalizer band 4 enable |

HPF2OD

This bit is to set number of high pass filter order(HPF2EN bit) for noise cut. In recording or playback operation(RECPLAY≠0x0), do not change this bit. If this bit is changed, the noise may be generated.

| HPF2OD | Description |
|--------|-------------------------------|
| 0 | second-order high pass filter |
| 1 | first-order high pass filter |

Digital Volume Control Function Enable Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|--------|--------|-----|-----|--------|
| | R | W | | | | | | | | |
| 0x0 | 0x68 | 0x69 | - | - | - | DVMUTE | DVFADE | - | - | PALCEN |
| | | | - | - | - | 0 | 0 | - | - | 0 |

This register is to set ON or OFF for digital volume control function.

PALCEN

This bit is to set ON or OFF of limiter at playback.

Set this register at stop state. (RECPLAY=0x0)

Set PALCEN register' value same as RPPL register (0xae/0xaf)

| setting | Description |
|---------|----------------------|
| 0 | PALC OFF at playback |
| 1 | PALC ON at playback |

DVFADE

This bit is to set ON or OFF of digital volume fade function. The fade function is effective for the recording and playback digital volume and the equalizer gain.

| setting | Description |
|---------|--|
| 0 | Fade function OFF: The register setting value of RDATT, PDATT and EQGAIN0 to 3 is used actual volume value as it is. Therefore the value is effective immediate. |
| 1 | Fade function ON: The volume is changing to the register setting value of RDATT, PDATT and EQGAIN0 to 3 with 1 step per DVFCON register step time. |

DVMUTE

This bit is to set MUTE of the digital volume. This mute function is effective for the recording digital volume at recording and effective for playback digital volume at playback. The fade function by DVFADE is effective against the volume change by this bit.

| setting | Description |
|---------|--|
| 0 | Register value of RDVOL and PDATT is effective. |
| 1 | Digital volume is set to MUTE. Register value of RDVOL and PDATT cannot be changed by this bit, the volume is resumed by releasing this bit(DVMUTE=0) to the original setting value of RDVOL and PDVOL. |

Mixer & Volume Control Register

| Mixer & Volume Control Register | | | | | | | | | | |
|---------------------------------|-------|------|------------------|-----|-----|-----|-------|-----|-------|-----|
| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
| | R | W | | | | | | | | |
| 0x0 | 0x6a | 0x6b | DVFCN | | | | RMCON | | LMCON | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register is to control the SAI receive data L channel plus R channel mixer and the digital volume fade control.

LMCON[1:0]

These bits are to control the SAI receive data L channel plus R channel mixer

| LMCON | Description |
|-------|-----------------|
| 0x0 | Use L Discard R |
| 0x1 | Use R Discard L |
| 0x2 | Use (L+R) |
| 0x3 | Use (L+R)/2 |

RMCON[1:0]

These bits are to control the SAI receive data R channel plus L channel mixer

| RMCON | Description |
|-------|-----------------|
| 0x0 | Use R Discard L |
| 0x1 | Use L Discard R |
| 0x2 | Use (L+R) |
| 0x3 | Use (L+R)/2 |

DVFCN[3:0]

These bits are to set the volume change step time of the digital volume fade function. The volume changes step by step (0.5dB) with this setting period. Step time is in proportion to sampling frequency (fs) as following table.

| DVFCN | fs equivalent | Time(fs=48kHz) |
|-------|---------------|----------------|
| 0x0 | 1/fs | 20.8µs |
| 0x1 | 2/fs | 41.7µs |
| 0x2 | 4/fs | 83.3µs |
| 0x3 | 8/fs | 167µs |
| 0x4 | 16/fs | 333µs |
| 0x5 | 32/fs | 667µs |
| 0x6 | 64/fs | 1.33ms |
| 0x7 | 128/fs | 2.67ms |
| 0x8 | 256/fs | 5.33ms |
| 0x9 | 512/fs | 10.7ms |
| 0xA | 1024/fs | 21.3ms |
| 0xB | 2048/fs | 42.7ms |
| 0xC | 4096/fs | 85.3ms |
| 0xD | 8192/fs | 171ms |
| 0xE | 16384/fs | 341ms |

EQ Band0 Gain Setting Register
 EQ Band1 Gain Setting Register
 EQ Band2 Gain Setting Register
 EQ Band3 Gain Setting Register
 EQ Band4 Gain Setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x74 | 0x75 | EQGAIN0 | | | | | | | |
| | | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0x0 | 0x76 | 0x77 | EQGAIN1 | | | | | | | |
| | | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0x0 | 0x78 | 0x79 | EQGAIN2 | | | | | | | |
| | | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0x0 | 0x7a | 0x7b | EQGAIN3 | | | | | | | |
| | | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0x0 | 0x7c | 0x7d | EQGAIN4 | | | | | | | |
| | | | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

These registers are to set the gain of each band equalizer.

(*)Index values are different by setting sound effect mode register. See Sound Effect Mode register description.

| EQGAIN 0 to 4[7:0] | Gain (0dB) | EQGAIN 0 to 4[7:0] | Gain (0dB) | EQGAIN 0 to 4[7:0] | Gain (dB) | EQGAIN 0 to 4[7:0] | Gain (dB) |
|-----------------------|---------------|-----------------------|---------------|-----------------------|--------------|-----------------------|--------------|
| 0x00 to 0x57 | MUTE | 0x82 | -50.5 | 0xAD | -29.0 | 0xD8 | -7.5 |
| 0x58 | -71.5 | 0x83 | -50.0 | 0xAE | -28.5 | 0xD9 | -7.0 |
| 0x59 | -71.0 | 0x84 | -49.5 | 0xAF | -28.0 | 0xDA | -6.5 |
| 0x5A | -70.5 | 0x85 | -49.0 | 0xB0 | -27.5 | 0xDB | -6.0 |
| 0x5B | -70.0 | 0x86 | -48.5 | 0xB1 | -27.0 | 0xDC | -5.5 |
| 0x5C | -69.5 | 0x87 | -48.0 | 0xB2 | -26.5 | 0xDD | -5.0 |
| 0x5D | -69.0 | 0x88 | -47.5 | 0xB3 | -26.0 | 0xDE | -4.5 |
| 0x5E | -68.5 | 0x89 | -47.0 | 0xB4 | -25.5 | 0xDF | -4.0 |
| 0x5F | -68.0 | 0x8A | -46.5 | 0xB5 | -25.0 | 0xE0 | -3.5 |
| 0x60 | -67.5 | 0x8B | -46.0 | 0xB6 | -24.5 | 0xE1 | -3.0 |
| 0x61 | -67.0 | 0x8C | -45.5 | 0xB7 | -24.0 | 0xE2 | -2.5 |
| 0x62 | -66.5 | 0x8D | -45.0 | 0xB8 | -23.5 | 0xE3 | -2.0 |
| 0x63 | -66.0 | 0x8E | -44.5 | 0xB9 | -23.0 | 0xE4 | -1.5 |
| 0x64 | -65.5 | 0x8F | -44.0 | 0xBA | -22.5 | 0xE5 | -1.0 |
| 0x65 | -65.0 | 0x90 | -43.5 | 0xBB | -22.0 | 0xE6 | -0.5 |
| 0x66 | -64.5 | 0x91 | -43.0 | 0xBC | -21.5 | 0xE7 | 0.0 |
| 0x67 | -64.0 | 0x92 | -42.5 | 0xBD | -21.0 | 0xE8 | 0.5 |
| 0x68 | -63.5 | 0x93 | -42.0 | 0xBE | -20.5 | 0xE9 | 1.0 |
| 0x69 | -63.0 | 0x94 | -41.5 | 0xBF | -20.0 | 0xEA | 1.5 |
| 0x6A | -62.5 | 0x95 | -41.0 | 0xC0 | -19.5 | 0xEB | 2.0 |
| 0x6B | -62.0 | 0x96 | -40.5 | 0xC1 | -19.0 | 0xEC | 2.5 |
| 0x6C | -61.5 | 0x97 | -40.0 | 0xC2 | -18.5 | 0xED | 3.0 |
| 0x6D | -61.0 | 0x98 | -39.5 | 0xC3 | -18.0 | 0xEE | 3.5 |
| 0x6E | -60.5 | 0x99 | -39.0 | 0xC4 | -17.5 | 0xEF | 4.0 |
| 0x6F | -60.0 | 0x9A | -38.5 | 0xC5 | -17.0 | 0xF0 | 4.5 |
| 0x70 | -59.5 | 0x9B | -38.0 | 0xC6 | -16.5 | 0xF1 | 5.0 |
| 0x71 | -59.0 | 0x9C | -37.5 | 0xC7 | -16.0 | 0xF2 | 5.5 |
| 0x72 | -58.5 | 0x9D | -37.0 | 0xC8 | -15.5 | 0xF3 | 6.0 |
| 0x73 | -58.0 | 0x9E | -36.5 | 0xC9 | -15.0 | 0xF4 | 6.5 |
| 0x74 | -57.5 | 0x9F | -36.0 | 0xCA | -14.5 | 0xF5 | 7.0 |
| 0x75 | -57.0 | 0xA0 | -35.5 | 0xCB | -14.0 | 0xF6 | 7.5 |
| 0x76 | -56.5 | 0xA1 | -35.0 | 0xCC | -13.5 | 0xF7 | 8.0 |
| 0x77 | -56.0 | 0xA2 | -34.5 | 0xCD | -13.0 | 0xF8 | 8.5 |
| 0x78 | -55.5 | 0xA3 | -34.0 | 0xCE | -12.5 | 0xF9 | 9.0 |
| 0x79 | -55.0 | 0xA4 | -33.5 | 0xCF | -12.0 | 0xFA | 9.5 |
| 0x7A | -54.5 | 0xA5 | -33.0 | 0xD0 | -11.5 | 0xFB | 10.0 |
| 0x7B | -54.0 | 0xA6 | -32.5 | 0xD1 | -11.0 | 0xFC | 10.5 |
| 0x7C | -53.5 | 0xA7 | -32.0 | 0xD2 | -10.5 | 0xFD | 11.0 |
| 0x7D | -53.0 | 0xA8 | -31.5 | 0xD3 | -10.0 | 0xFE | 11.5 |
| 0x7E | -52.5 | 0xA9 | -31.0 | 0xD4 | -9.5 | 0xFF | 12.0 |
| 0x7F | -52.0 | 0xAA | -30.5 | 0xD5 | -9.0 | | |
| 0x80 | -51.5 | 0xAB | -30.0 | 0xD6 | -8.5 | | |
| 0x81 | -51.0 | 0xAC | -29.5 | 0xD7 | -8.0 | | |

High Pass Filter2 Cut-off Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|---------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x7e | 0x7f | - | - | - | - | - | HPF2CUT | | |
| | | | - | - | - | - | - | 0 | 0 | 0 |

HPF2CUT[2:0]

This register is to set the cut off frequency of the high pass filter for noise reduction. Do not change this register setting at filtering operation.

These bits are to set the cut-off frequency of noise reduction high pass filter.

The following table shows that the frequency decreases 3dB at second order filter selected (HPF2OD=0) and decreases 1.5dB at first order filter selected (HPF2OD=1).

| setting | Cut-off Frequency(Hz) | | |
|---------|-----------------------------|---------------------------------------|------------------------------|
| | fs=8kHz, 16kHz, 32kHz | fs=11.025kHz, 22.05kHz, 44.1kHz | fs=12kHz, 24kHz, 48kHz |
| 0x0 | 80 | 110 | 120 |
| 0x1 | 100 | 138 | 150 |
| 0x2 | 130 | 179 | 195 |
| 0x3 | 160 | 221 | 240 |
| 0x4 | 200 | 276 | 300 |
| 0x5 | 260 | 358 | 390 |
| 0x6 | 320 | 441 | 480 |
| 0x7 | 400 | 551 | 600 |

Programable Equalizer Band0 Coefficient-a0 (L) Register
 Programable Equalizer Band0 Coefficient-a0 (H) Register
 Programable Equalizer Band0 Coefficient-a1 (L) Register
 Programable Equalizer Band0 Coefficient-a1 (H) Register
 Programable Equalizer Band1 Coefficient-a0 (L) Register
 Programable Equalizer Band1 Coefficient-a0 (H) Register
 Programable Equalizer Band1 Coefficient-a1 (L) Register
 Programable Equalizer Band1 Coefficient-a1 (H) Register
 Programable Equalizer Band2 Coefficient-a0 (L) Register
 Programable Equalizer Band2 Coefficient-a0 (H) Register
 Programable Equalizer Band2 Coefficient-a1 (L) Register
 Programable Equalizer Band2 Coefficient-a1 (H) Register
 Programable Equalizer Band3 Coefficient-a0 (L) Register
 Programable Equalizer Band3 Coefficient-a0 (H) Register
 Programable Equalizer Band3 Coefficient-a1 (L) Register
 Programable Equalizer Band3 Coefficient-a1 (H) Register
 Programable Equalizer Band4 Coefficient-a0 (L) Register
 Programable Equalizer Band4 Coefficient-a0 (H) Register
 Programable Equalizer Band4 Coefficient-a1 (L) Register
 Programable Equalizer Band4 Coefficient-a1 (H) Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0x80 | 0x81 | EQ0A0L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x82 | 0x83 | EQ0A0H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x84 | 0x85 | EQ0A1L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x86 | 0x87 | EQ0A1H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x88 | 0x89 | EQ1A0L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x8a | 0x8b | EQ1A0H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x8c | 0x8d | EQ1A1L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x8e | 0x8f | EQ1A1H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x90 | 0x91 | EQ2A0L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x92 | 0x93 | EQ2A0H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x94 | 0x95 | EQ2A1L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x96 | 0x97 | EQ2A1H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x98 | 0x99 | EQ3A0L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x9a | 0x9b | EQ3A0H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x9c | 0x9d | EQ3A1L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0x9e | 0x9f | EQ3A1H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0xa0 | 0xa1 | EQ4A0L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0xa2 | 0xa3 | EQ4A0H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0xa4 | 0xa5 | EQ4A1L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0xa6 | 0xa7 | EQ4A1H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

These registers are to set the coefficients a0 and a1 of each five band programmable equalizer. One coefficients value is specified by two bytes data. The centre frequency and band width of the filter can be set by changing these register value.

Please do not change the register setting during corresponding filter operation (*).The detailed setting value is described in the Filter function.

(*) (RECPLAY is not 0x0) and (EQ0EN=1 or EQ1EN=1 or EQ2EN=1 or EQ3EN=1)

RecPlay Play Limiter Enable Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----|------|
| | R | W | | | | | | | | |
| 0x0 | 0xae | 0xaf | - | - | - | - | - | - | - | RPPL |
| | | | - | - | - | - | - | - | - | 0 |

RPPL

This bit is to set ON or OFF of limiter at playback.

Set this register at stop state. (RECPLAY=0x0)

Set RPPL register' value same as PLACEN register (0x68/0x69)

| setting | Description |
|---------|----------------------|
| 0 | PALC OFF at playback |
| 1 | PALC ON at playback |

Soft Clip Enable Register
 Soft Clip Threshold H Register
 Soft Clip Threshold M Register
 Soft Clip Threshold L Register
 Soft Clip Gain Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|--------|-----|-----|-----|--------|-----|------|
| | R | W | | | | | | | | |
| 0x0 | 0xb0 | 0xb1 | - | - | - | - | - | - | - | SCEN |
| | | | - | - | - | - | - | - | - | 0 |
| 0x0 | 0xb2 | 0xb3 | - | SCTHRH | | | | | | |
| | | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0xb4 | 0xb5 | SCTHRM | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0xb6 | 0xb7 | SCTHRL | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0 | 0xb8 | 0xb9 | - | - | - | - | - | SCGAIN | | |
| | | | - | - | - | - | - | 0 | 0 | 1 |

This register is setting of the "SoftClip" block.

SCEN

| setting | Description |
|---------|-----------------------|
| 0 | SoftClip Function OFF |
| 1 | SoftClip Function ON |

SCTHRH
 SCTHRM
 SCTHRL

This register sets a soft clip threshold level.
 When PCM signal with more than of this bit is input, the LSI clips it according to a value of SCGAIN and works.
 The value of threshold level is 23bit(SCTHRM[6:0], SCTHRM[7:0], SCTHRL[7:0])
 Please do not change the value of this bit during SoftClip function movement.

SCGAIN[2:0]

This register is setting the gain at SoftClip. This register setting must not be changed during SoftClip function is active.

| setting | Description |
|---------|-----------------|
| 0x0 | 2 time |
| 0x1 | 1 time(default) |
| 0x2 | 1/2 time |
| 0x3 | 1/4 time |
| 0x4 | 1/8 time |
| 0x5 | 1/16 time |
| 0x6 | 1/32 time |
| 0x7 | 1/64 time |

MIC ALC Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-------|--------|
| | R | W | | | | | | | | |
| 0x0 | 0xba | 0xbb | - | - | - | - | - | - | MCLEN | MALCEN |
| | | | - | - | - | - | - | - | 1 | 1 |

This register sets the ALC for MIC input
Please refer to function explanation for the details of this function

MALCEN

This sets the MIC ALC.
In the case of OFF, MIC ALC suffers from Gain of MICAMP with a value of MALCMXGAIN

| setting | Description |
|---------|----------------------------|
| 0 | MALC Function OFF |
| 1 | MALC Function ON (default) |

MCLEN

This sets the MIC Clip reduction.

| setting | Description |
|---------|---------------------------------|
| 0 | MIC Clip reduction OFF |
| 1 | MIC Clip reduction ON (default) |

MIC ALC Attack /Decay Time Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|---------|-----|-----|-----|---------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xbc | 0xbd | - | MALCDCY | | | - | MALCATK | | |
| | | | - | 1 | 0 | 0 | - | 1 | 0 | 0 |

This register sets Decay Time in Attack Time of the MIC ALC.

MALCATK[2:0]

MIC ALC Attack Time

| setting | 8kHz | 11.025k Hz | 12kHz | 16kHz | 22.05kH z | 24kHz | 32kHz | 44.1kHz | 48kHz | Unit |
|---------|------|---------------|-------|-------|--------------|-------|-------|---------|-------|------|
| 0 | 0.25 | 0.18 | 0.17 | 0.13 | 0.09 | 0.08 | 0.06 | 0.05 | 0.04 | ms |
| 1 | 0.5 | 0.36 | 0.33 | 0.25 | 0.18 | 0.17 | 0.13 | 0.09 | 0.08 | ms |
| 2 | 1.0 | 0.73 | 0.67 | 0.5 | 0.36 | 0.33 | 0.25 | 0.18 | 0.17 | ms |
| 3 | 2.0 | 1.45 | 1.33 | 1.0 | 0.73 | 0.67 | 0.5 | 0.36 | 0.33 | ms |
| 4 | 4.0 | 2.9 | 2.67 | 2.0 | 1.45 | 1.33 | 1.0 | 0.73 | 0.67 | ms |
| 5 | 8.0 | 5.8 | 5.33 | 4.0 | 2.9 | 2.67 | 2.0 | 1.45 | 1.33 | ms |
| 6 | 16.0 | 11.61 | 10.67 | 8.0 | 5.8 | 5.33 | 4.0 | 2.9 | 2.67 | ms |
| 7 | 32.0 | 23.22 | 21.33 | 16.0 | 11.61 | 10.67 | 8.0 | 5.8 | 5.33 | ms |

MALCDCY[2:0]

MIC ALC Decay Time

| setting | 8kHz | 11.025k Hz | 12kHz | 16kHz | 22.05kH z | 24kHz | 32kHz | 44.1kHz | 48kHz | Unit |
|---------|------|---------------|-------|-------|--------------|-------|-------|---------|-------|------|
| 0 | 64 | 46 | 43 | 32 | 23 | 21 | 16 | 12 | 11 | ms |
| 1 | 128 | 93 | 85 | 64 | 46 | 43 | 32 | 23 | 21 | ms |
| 2 | 256 | 186 | 171 | 128 | 93 | 85 | 64 | 46 | 43 | ms |
| 3 | 512 | 372 | 341 | 256 | 186 | 171 | 128 | 93 | 85 | ms |
| 4 | 1024 | 743 | 683 | 512 | 372 | 341 | 256 | 186 | 171 | ms |
| 5 | 2048 | 1486 | 1365 | 1024 | 743 | 683 | 512 | 372 | 341 | ms |
| 6 | 4096 | 2972 | 2731 | 2048 | 1486 | 1365 | 1024 | 743 | 683 | ms |
| 7 | 8192 | 5944 | 5461 | 4096 | 2972 | 2731 | 2048 | 1486 | 1365 | ms |

MIC ALC Max Gain Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|------------|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xbe | 0xbf | - | - | MALCMXGAIN | | | | | |
| | | | - | - | 0 | 1 | 0 | 0 | 0 | 0 |

This register sets the ALC MAX GAIN for MIC input

MALCGAIN[5:0]

MIC ALC Max Gain.

| setting | Description |
|---------|---------------|
| 0x3F | 35.25dB |
| 0x3E | 34.50dB |
| : | (0.75dB/step) |
| 0x28 | 18.00dB |
| : | (0.75dB/step) |
| 0x11 | 0.75dB |
| 0x10 | 0.00dB |
| : | Prohibited |
| 0x00 | Prohibited |

LINE ALC Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|--------|--------|
| | R | W | | | | | | | | |
| 0x0 | 0xc4 | 0xc5 | - | - | - | - | - | - | LCLLEN | LALCEN |
| | | | - | - | - | - | - | - | 0 | 0 |

This register sets the ALC for Line input

Please refer to function explanation for the details of this function

LALCEN

This sets the Line ALC.

| setting | Description |
|---------|-----------------------------|
| 0 | LALC Function OFF (default) |
| 1 | LALC Function ON |

LCLLEN

This sets the Line Clip reduction.

| setting | Description |
|---------|-----------------------------------|
| 0 | Line Clip reduction OFF (default) |
| 1 | Line Clip reduction ON |

LINE ALC Attack /Decay Time Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|---------|-----|-----|-----|---------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xc6 | 0xc7 | - | LALCDCY | | | - | LALCATK | | |
| | | | - | 1 | 1 | 1 | - | 1 | 0 | 0 |

This register sets Decay Time in Attack Time of the Line ALC.

LALCATK[2:0]

Line ALC Attack Time

| setting | 8kHz | 11.025k Hz | 12kHz | 16kHz | 22.05kH z | 24kHz | 32kHz | 44.1kHz | 48kHz | Unit |
|---------|------|---------------|-------|-------|--------------|-------|-------|---------|-------|------|
| 0 | 0.5 | 0.4 | 0.3 | 0.3 | 0.2 | 0.2 | 0.1 | 0.1 | 0.1 | ms |
| 1 | 1.0 | 0.7 | 0.7 | 0.5 | 0.4 | 0.3 | 0.3 | 0.2 | 0.2 | ms |
| 2 | 2.0 | 1.5 | 1.3 | 1.0 | 0.7 | 0.7 | 0.5 | 0.4 | 0.3 | ms |
| 3 | 4.0 | 2.9 | 2.7 | 2.0 | 1.5 | 1.3 | 1.0 | 0.7 | 0.7 | ms |
| 4 | 8.0 | 5.8 | 5.3 | 4.0 | 2.9 | 2.7 | 2.0 | 1.5 | 1.3 | ms |
| 5 | 16.0 | 11.6 | 10.7 | 8.0 | 5.8 | 5.3 | 4.0 | 2.9 | 2.7 | ms |
| 6 | 32.0 | 23.2 | 21.3 | 16.0 | 11.6 | 10.7 | 8.0 | 5.8 | 5.3 | ms |
| 7 | 64.0 | 46.4 | 42.7 | 32.0 | 23.2 | 21.3 | 16.0 | 11.6 | 10.7 | ms |

LALCDCY[2:0]

Line ALC Decay Time

| setting | 8kHz | 11.025k Hz | 12kHz | 16kHz | 22.05kH z | 24kHz | 32kHz | 44.1kHz | 48kHz | Unit |
|---------|------|---------------|-------|-------|--------------|-------|-------|---------|-------|------|
| 0 | 64 | 46 | 43 | 32 | 23 | 21 | 16 | 12 | 11 | ms |
| 1 | 128 | 93 | 85 | 64 | 46 | 43 | 32 | 23 | 21 | ms |
| 2 | 256 | 186 | 171 | 128 | 93 | 85 | 64 | 46 | 43 | ms |
| 3 | 512 | 372 | 341 | 256 | 186 | 171 | 128 | 93 | 85 | ms |
| 4 | 1024 | 743 | 683 | 512 | 372 | 341 | 256 | 186 | 171 | ms |
| 5 | 2048 | 1486 | 1365 | 1024 | 743 | 683 | 512 | 372 | 341 | ms |
| 6 | 4096 | 2972 | 2731 | 2048 | 1486 | 1365 | 1024 | 743 | 683 | ms |
| 7 | ∞ | ∞ | ∞ | ∞ | ∞ | ∞ | ∞ | ∞ | ∞ | ms |

LINE ALC Max Gain Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|------------|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xc8 | 0xc9 | - | - | - | - | LALCMXGAIN | | | |
| | | | - | - | - | - | 1 | 1 | 1 | 1 |

This register sets the ALC MAX GAIN for Line input

LALCGAIN[3:0]

Line ALC Max Gain.

| setting | Description |
|---------|-------------|
| 0xF | 6dB |
| 0xE | 5dB |
| : | (1dB/step) |
| 0x1 | -8dB |
| 0x0 | -9dB |

Playback ALC Attack Time Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|---------|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xdc | 0xdd | - | - | - | - | PALCATK | | | |
| | | | - | - | - | - | 0 | 1 | 0 | 0 |

This register is to set the attack time that is the step period for the playback ALC volume down.

PALCATK[3:0]

These bits are to set the playback ALC attack time. The playback ALC volume downs step by step per this attack time period. Attack time is in proportion to sampling frequency(fs) as following table.

| setting | fs equivalent | Time(fs=48kHz) |
|---------|---------------|----------------|
| 0x0 | 1/fs | 20.8us |
| 0x1 | 2/fs | 41.7us |
| 0x2 | 4/fs | 83.3us |
| 0x3 | 8/fs | 167us |
| 0x4 | 16/fs | 333us |
| 0x5 | 32/fs | 667us |
| 0x6 | 64/fs | 1.33ms |
| 0x7 | 128/fs | 2.67ms |
| 0x8 | 256/fs | 5.33ms |
| 0x9 | 512/fs | 10.7ms |
| 0xA | 1024/fs | 21.3ms |
| 0xB | 2048/fs | 42.7ms |
| 0xC | 4096/fs | 85.3ms |
| 0xD | 8192/fs | 171ms |
| 0xE | 16384/fs | 341ms |
| 0xF | 32768/fs | 683ms |

Playback ALC Decay Time Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|---------|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xde | 0xdf | - | - | - | - | PALCDCY | | | |
| | | | - | - | - | - | 0 | 1 | 0 | 1 |

This register is to set the decay time that is the step period for the playback ALC volume up.

PALCDCY[3:0]

These bits are to set the playback ALC decay time. The playback ALC volume ups step by step per this decay time period. Decay time is in proportion to sampling frequency(fs) as following table.

| setting | fs equivalent | Time(fs=48kHz) |
|---------|---------------|----------------|
| 0x0 | 4/fs | 83.3us |
| 0x1 | 8/fs | 167us |
| 0x2 | 16/fs | 333us |
| 0x3 | 32/fs | 667us |
| 0x4 | 64/fs | 1.33ms |
| 0x5 | 128/fs | 2.67ms |
| 0x6 | 256/fs | 5.33ms |
| 0x7 | 512/fs | 10.7ms |
| 0x8 | 1024/fs | 21.3ms |
| 0x9 | 2048/fs | 42.7ms |
| 0xA | 4096/fs | 85.3ms |
| 0xB | 8192/fs | 171ms |
| 0xC | 16384/fs | 341ms |
| 0xD | 32768/fs | 683ms |
| 0xE | 65536/fs | 1.37s |
| 0xF | 131072/fs | 2.73s |

Playback ALC Target Level Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|---------|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xe0 | 0xe1 | - | - | - | PALCLVL | | | | |
| | | | - | - | - | 1 | 1 | 0 | 1 | 1 |

This register is to set the target level of the playback ALC.

PALCLVL[4:0]

These bits are to set the target level of the playback ALC.

| setting | Target Level (dBFS) | setting | Target Level (dBFS) |
|---------|---------------------|---------|---------------------|
| 0x00 | -23.25 | 0x10 | -11.25 |
| 0x01 | -22.50 | 0x11 | -10.50 |
| 0x02 | -21.75 | 0x12 | -9.75 |
| 0x03 | -21.00 | 0x13 | -9.00 |
| 0x04 | -20.25 | 0x14 | -8.25 |
| 0x05 | -19.50 | 0x15 | -7.50 |
| 0x06 | -18.75 | 0x16 | -6.75 |
| 0x07 | -18.00 | 0x17 | -6.00 |
| 0x08 | -17.25 | 0x18 | -5.25 |
| 0x09 | -16.50 | 0x19 | -4.50 |
| 0x0A | -15.75 | 0x1A | -3.75 |
| 0x0B | -15.00 | 0x1B | -3.00 |
| 0x0C | -14.25 | 0x1C | -2.25 |
| 0x0D | -13.50 | 0x1D | -1.50 |
| 0x0E | -12.75 | | |
| 0x0F | -12.00 | | |

Playback ALC Min Gain Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-------------|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xe2 | 0xe3 | - | - | - | - | - | PALCMINGAIN | | |
| | | | - | - | - | - | - | 0 | 0 | 0 |

This register is to set the upper limit and the lower limit at the playback ALC operation.

PALCMINGAIN[2:0]

These bits are to set the lower limit at the playback ALC operation.

| setting | Min Gain (dB) |
|---------|---------------|
| 0x00 | -12.0 |
| 0x01 | -6.0 |
| 0x02 | 0.0 |
| 0x03 | +6.0 |
| 0x04 | +12.0 |
| 0x05 | +18.0 |
| 0x06 | +24.0 |
| 0x07 | +30.0 |

Playback ALC Volume Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|---------|-----|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xe4 | 0xe5 | - | PALCVOL | | | | | | |
| | | | - | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

This register is to set the volume that is used in the PALC. It can be set the volume up to +35.625dB. Also this volume can be used as a playback path boost volume when the PALC is not used.

PALCVOL[6:0]

PALCVOL becomes a fixed gain at the time of "PALCEN=0".

PALCVOL becomes a PALC Maximum gain at the time of "PALCEN=1".

| PALCVOL | Gain (dB) | PALCVOL | Gain (dB) | PALCVOL | Gain (dB) | PALCVOL | Gain (dB) |
|---------|-----------|---------|-----------|---------|-----------|---------|-----------|
| 0x00 | -12.000 | 0x20 | 0.000 | 0x40 | 12.000 | 0x60 | 24.000 |
| 0x01 | -11.625 | 0x21 | 0.375 | 0x41 | 12.375 | 0x61 | 24.375 |
| 0x02 | -11.250 | 0x22 | 0.750 | 0x42 | 12.750 | 0x62 | 24.750 |
| 0x03 | -10.875 | 0x23 | 1.125 | 0x43 | 13.125 | 0x63 | 25.125 |
| 0x04 | -10.500 | 0x24 | 1.500 | 0x44 | 13.500 | 0x64 | 25.500 |
| 0x05 | -10.125 | 0x25 | 1.875 | 0x45 | 13.875 | 0x65 | 25.875 |
| 0x06 | -9.750 | 0x26 | 2.250 | 0x46 | 14.250 | 0x66 | 26.250 |
| 0x07 | -9.375 | 0x27 | 2.625 | 0x47 | 14.625 | 0x67 | 26.625 |
| 0x08 | -9.000 | 0x28 | 3.000 | 0x48 | 15.000 | 0x68 | 27.000 |
| 0x09 | -8.625 | 0x29 | 3.375 | 0x49 | 15.375 | 0x69 | 27.375 |
| 0x0A | -8.250 | 0x2A | 3.750 | 0x4A | 15.750 | 0x6A | 27.750 |
| 0x0B | -7.875 | 0x2B | 4.125 | 0x4B | 16.125 | 0x6B | 28.125 |
| 0x0C | -7.500 | 0x2C | 4.500 | 0x4C | 16.500 | 0x6C | 28.500 |
| 0x0D | -7.125 | 0x2D | 4.875 | 0x4D | 16.875 | 0x6D | 28.875 |
| 0x0E | -6.750 | 0x2E | 5.250 | 0x4E | 17.250 | 0x6E | 29.250 |
| 0x0F | -6.375 | 0x2F | 5.625 | 0x4F | 17.625 | 0x6F | 29.625 |
| 0x10 | -6.000 | 0x30 | 6.000 | 0x50 | 18.000 | 0x70 | 30.000 |
| 0x11 | -5.625 | 0x31 | 6.375 | 0x51 | 18.375 | 0x71 | 30.375 |
| 0x12 | -5.250 | 0x32 | 6.750 | 0x52 | 18.750 | 0x72 | 30.750 |
| 0x13 | -4.875 | 0x33 | 7.125 | 0x53 | 19.125 | 0x73 | 31.125 |
| 0x14 | -4.500 | 0x34 | 7.500 | 0x54 | 19.500 | 0x74 | 31.500 |
| 0x15 | -4.125 | 0x35 | 7.875 | 0x55 | 19.875 | 0x75 | 31.875 |
| 0x16 | -3.750 | 0x36 | 8.250 | 0x56 | 20.250 | 0x76 | 32.250 |
| 0x17 | -3.375 | 0x37 | 8.625 | 0x57 | 20.625 | 0x77 | 32.625 |
| 0x18 | -3.000 | 0x38 | 9.000 | 0x58 | 21.000 | 0x78 | 33.000 |
| 0x19 | -2.625 | 0x39 | 9.375 | 0x59 | 21.375 | 0x79 | 33.375 |
| 0x1A | -2.250 | 0x3A | 9.750 | 0x5A | 21.750 | 0x7A | 33.750 |
| 0x1B | -1.875 | 0x3B | 10.125 | 0x5B | 22.125 | 0x7B | 34.125 |
| 0x1C | -1.500 | 0x3C | 10.500 | 0x5C | 22.500 | 0x7C | 34.500 |
| 0x1D | -1.125 | 0x3D | 10.875 | 0x5D | 22.875 | 0x7D | 34.875 |
| 0x1E | -0.750 | 0x3E | 11.250 | 0x5E | 23.250 | 0x7E | 35.250 |
| 0x1F | -0.375 | 0x3F | 11.625 | 0x5F | 23.625 | 0x7F | 35.625 |

Playback ALC ZeroCross TimeOut Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|----------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xe6 | 0xe7 | - | - | - | - | - | - | PALCZCTM | |
| | | | - | - | - | - | - | - | 0 | 0 |

PALCZCTM[1:0]

This register is to set the value of Zero Cross time out in Playback ALC.

| setting | fs equivalent | Time(fs=48kHz) |
|---------|---------------|----------------|
| 0x0 | 128/fs | 2.67ms |
| 0x1 | 256/fs | 5.33ms |
| 0x2 | 512/fs | 10.7ms |
| 0x3 | 1024/fs | 21.3ms |

Playback Limiter Fast Release Setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|----------|-----|----------|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xea | 0xeb | PALCFRTH | | | | PALCFREN | - | PALCFRSP | |
| | | | 0 | 0 | 0 | 1 | 0 | - | 0 | 1 |

This register is to set the fast release in Playback ALC.

PALCFREN

This is to set the Fast Release enable in Playback ALC.

| setting | Description |
|---------|-------------|
| 0 | Disable |
| 1 | Enable |

PALCFRSP[1:0]

These bits are to set the release speed in Playback ALC.

Release speed is expressed with PALCDCY.

| setting | Release Speed |
|---------|--------------------|
| 0x0 | (1 / 4) * PALCDCY |
| 0x1 | (1 / 8) * PALCDCY |
| 0x2 | (1 / 16) * PALCDCY |
| 0x3 | (1 / 32) * PALCDCY |

PALCFRTH[3:0]

This bit can set the threshold in Fast Release (Playback ALC).

Whether to make Fast Release effective by the gain down in which extent.

| setting | Threshold (1Step=0.375dB) | setting | Threshold (1Step=0.375dB) |
|---------|------------------------------|---------|------------------------------|
| 0x0 | 13step = 4.875dB | 0x8 | 24step = 9.000dB |
| 0x1 | 15step = 5.625dB | 0x9 | 25step = 9.375dB |
| 0x2 | 16step = 6.000dB | 0xA | 27step = 10.125dB |
| 0x3 | 17step = 6.375dB | 0xB | 28step = 10.500dB |
| 0x4 | 19step = 7.125dB | 0xC | 29step = 10.875dB |
| 0x5 | 20step = 7.500dB | 0xD | 31step = 11.625dB |
| 0x6 | 21step = 7.875dB | 0xE | 32step = 12.000dB |
| 0x7 | 23step = 8.625dB | 0xF | 33step = 12.375dB |

LOUT Power Up Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|---------|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x0 | 0xec | 0xed | - | - | LOPWTIM | | | | - | - |
| | | | - | - | 0 | 0 | 0 | 0 | - | - |

This register controls function for pop noise reducer of line amplifier power up and down.

LOPWTIM [3:0]

It is the setting for start/stop time of pop noise reducer. This register setting must not be changed during line amplifier active.

According to LOPWTIM setting and sampling frequency, the start/stop time of lineamp is changed as below.

Please change LOPWTIM when it changes sampling frequency.

Evaluate it enough for the decision of the value.

| | Start-up/shut-down time [ms] | | |
|---------------|-------------------------------|---|--------------------------------|
| | fs=8kHz / 16kHz / 32kHz | fs=11.025kHz / 22.05kHz / 44.1kHz | fs=12kHz / 24kHz / 48kHz |
| 0x0 | 0.2 | 0.3 | 0.3 |
| 0x1 | 0.4 | 0.6 | 0.5 |
| 0x2 | 0.8 | 1.1 | 1.0 |
| 0x3 | 1.6 | 2.3 | 2.1 |
| 0x4 | 3.1 | 4.6 | 4.2 |
| 0x5 | 6.3 | 9.1 | 8.4 |
| 0x6 | 12.6 | 18.2 | 16.8 |
| 0x7 | 25.1 | 36.5 | 33.5 |
| 0x8 | 50.3 | 72.9 | 67.0 |
| 0x9 | 100.5 | 145.9 | 134.0 |
| 0xA | 201.1 | 291.8 | 268.1 |
| 0xB to 0xF | Write prohibit | | |

FPLL M setting Register
 FPLL N Setting(L) Register
 FPLL N Setting(H) Register
 FPLL D Setting Register
 FPLL F Setting(L) Register
 FPLL F Setting(H) Register
 FPLL F_D Setting(L) Register
 FPLL F_D Setting(H) Register
 FPLL V setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 | |
|--------|-------|------|------------------|-----|-----|----------|----------|----------|-----|-----------|--|
| | R | W | | | | | | | | | |
| 0x1 | 0x02 | 0x03 | - | - | - | - | - | FPLLM(*) | | | |
| | | | - | - | - | - | - | 0 | 0 | 0 | |
| 0x1 | 0x04 | 0x05 | FPLLNL(*) | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 0x1 | 0x06 | 0x07 | - | - | - | - | - | - | - | FPLLNH(*) | |
| | | | - | - | - | - | - | - | - | 0 | |
| 0x1 | 0x08 | 0x09 | - | - | - | FPLLD(*) | | | | | |
| | | | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| 0x1 | 0x0a | 0x0b | FPLLFL(*) | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 0x1 | 0x0c | 0x0d | FPLL FH(*) | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 0x1 | 0x0e | 0x0f | FPLLF DL(*) | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 0x1 | 0x10 | 0x11 | FPLLF DH(*) | | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 0x1 | 0x12 | 0x13 | - | - | - | - | FPLLV(*) | | | | |
| | | | - | - | - | - | 0 | 0 | 0 | 0 | |

This register is to set PLL output clock frequency.

Please use PLL Setting Calculation program. The program outputs PLL register setting values.
 PLL output frequency gets decided by FPLL Registers as the following expression.

$$\text{PLL output frequency (Hz)} = \text{PLL input frequency} / \text{FPLLM} \times (\text{FPLLN} + \text{FPLLD}/16 + \text{FPLLF}/\text{FPLLF_D}/16) \times 2 / \text{FPLLV}$$

PLL CPMODE setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----------|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x1 | 0x16 | 0x17 | - | - | - | CPMODE(*) | | | | |
| | | | - | - | - | 0 | 0 | 1 | 1 | 0 |

CPMODE[4:0]

This bit is to set the ON and OFF of the PLL external loop-filter function.
 If PLL is used on condition input frequency is lower than 2MHz, the external loop-filter is necessary.
 Set this bit ,if the external loop-filter is necessary.
 Recommended external circuit of the loop-filter is decided by PLL frequency. Please ask recommended circuit, if you need.

| Setting | Description |
|---------|---|
| 0x00110 | Not use PLL chip external loop-filter (Default) |
| 0x10110 | Use PLL chip external loop-filter |

Headphone Output Gain Setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-------|-----|
| | R | W | | | | | | | | |
| 0x1 | 0x36 | 0x37 | - | - | - | - | - | - | HPVOL | |
| | | | - | - | - | - | - | - | 0 | 0 |

This register is to set the gain of Headphone Output.

HPVOL[1:0]

This bit is to set the gain of Headphone Output. When beep input is used, please set data to 0x3.

| Setting | Description |
|---------|---|
| 0x0 | -6dB (It is prohibition to use with beep input) |
| 0x1 | 0dB (It is prohibition to use with beep input) |
| 0x2 | 3dB (It is prohibition to use with beep input) |
| 0x3 | 6dB |

Analog Path Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|------|--------|----------|--------|-----|-----|
| | R | W | | | | | | | | |
| 0x1 | 0x3e | 0x3f | - | - | HALF | HPBPEN | LINDACEN | ADCSET | | |
| | | | - | - | 1 | 0 | 0 | 1 | 1 | 1 |

This register adjusts ADC characteristics, and set signal path of analog section.

ADCSET

This register adjust ADC characteristics. Use by 0x7

| ADCSET | Description |
|--------|-------------|
| 0x7 | Use by 0x7 |

LINDACEN

Set signal path about from DAC to LINMIX amplifier.

*Please set to "0" with recording monitor mode (0x13=0x07)

| LINDACEN | Description |
|----------|---|
| 0 | Don't connect DAC output to LINMIX amplifier. |
| 1 | Connect DAC output to LINMIX amplifier. |

HPBPEN

Set signal path about from BEEPIN amplifier to Head phone amplifier.

| HPBPEN | Description |
|--------|--|
| 0 | Don't connect BEEPIN amplifier output to Head phone amplifier. |
| 1 | Connect BEEPIN amplifier output to Head phone amplifier. |

HALF

Set the gain of MIC amplifier on input block.

| HALF | Description |
|------|-------------|
| 0 | 0dB |
| 1 | -6dB |

Record L Balance Volume Control Register
 Record R Balance Volume Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|---------|-----|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x1 | 0x74 | 0x75 | - | RBLVOLL | | | | | | |
| | | | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x1 | 0x76 | 0x77 | - | RBLVOLR | | | | | | |
| | | | - | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

This register is to set "L/R Balance" block in digital signal flow, when ADC-path is used.
 Left and Right volume are available to be set from -6.0dB to 6.0dB at 0.1dB step each.

RBLVOLL, RBLVOLR[6:0]

| Setting | Gain(dB) | Setting | Gain(dB) | Setting | Gain(dB) | Setting | Gain(dB) |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 0x04 | -6.0 | 0x24 | -2.8 | 0x44 | 0.4 | 0x64 | 3.6 |
| 0x05 | -5.9 | 0x25 | -2.7 | 0x45 | 0.5 | 0x65 | 3.7 |
| 0x06 | -5.8 | 0x26 | -2.6 | 0x46 | 0.6 | 0x66 | 3.8 |
| 0x07 | -5.7 | 0x27 | -2.5 | 0x47 | 0.7 | 0x67 | 3.9 |
| 0x08 | -5.6 | 0x28 | -2.4 | 0x48 | 0.8 | 0x68 | 4.0 |
| 0x09 | -5.5 | 0x29 | -2.3 | 0x49 | 0.9 | 0x69 | 4.1 |
| 0x0A | -5.4 | 0x2A | -2.2 | 0x4A | 1.0 | 0x6A | 4.2 |
| 0x0B | -5.3 | 0x2B | -2.1 | 0x4B | 1.1 | 0x6B | 4.3 |
| 0x0C | -5.2 | 0x2C | -2.0 | 0x4C | 1.2 | 0x6C | 4.4 |
| 0x0D | -5.1 | 0x2D | -1.9 | 0x4D | 1.3 | 0x6D | 4.5 |
| 0x0E | -5.0 | 0x2E | -1.8 | 0x4E | 1.4 | 0x6E | 4.6 |
| 0x0F | -4.9 | 0x2F | -1.7 | 0x4F | 1.5 | 0x6F | 4.7 |
| 0x10 | -4.8 | 0x30 | -1.6 | 0x50 | 1.6 | 0x70 | 4.8 |
| 0x11 | -4.7 | 0x31 | -1.5 | 0x51 | 1.7 | 0x71 | 4.9 |
| 0x12 | -4.6 | 0x32 | -1.4 | 0x52 | 1.8 | 0x72 | 5.0 |
| 0x13 | -4.5 | 0x33 | -1.3 | 0x53 | 1.9 | 0x73 | 5.1 |
| 0x14 | -4.4 | 0x34 | -1.2 | 0x54 | 2.0 | 0x74 | 5.2 |
| 0x15 | -4.3 | 0x35 | -1.1 | 0x55 | 2.1 | 0x75 | 5.3 |
| 0x16 | -4.2 | 0x36 | -1.0 | 0x56 | 2.2 | 0x76 | 5.4 |
| 0x17 | -4.1 | 0x37 | -0.9 | 0x57 | 2.3 | 0x77 | 5.5 |
| 0x18 | -4.0 | 0x38 | -0.8 | 0x58 | 2.4 | 0x78 | 5.6 |
| 0x19 | -3.9 | 0x39 | -0.7 | 0x59 | 2.5 | 0x79 | 5.7 |
| 0x1A | -3.8 | 0x3A | -0.6 | 0x5A | 2.6 | 0x7A | 5.8 |
| 0x1B | -3.7 | 0x3B | -0.5 | 0x5B | 2.7 | 0x7B | 5.9 |
| 0x1C | -3.6 | 0x3C | -0.4 | 0x5C | 2.8 | 0x7C | 6.0 |
| 0x1D | -3.5 | 0x3D | -0.3 | 0x5D | 2.9 | | |
| 0x1E | -3.4 | 0x3E | -0.2 | 0x5E | 3.0 | | |
| 0x1F | -3.3 | 0x3F | -0.1 | 0x5F | 3.1 | | |
| 0x20 | -3.2 | 0x40 | 0.0 | 0x60 | 3.2 | | |
| 0x21 | -3.1 | 0x41 | 0.1 | 0x61 | 3.3 | | |
| 0x22 | -3.0 | 0x42 | 0.2 | 0x62 | 3.4 | | |
| 0x23 | -2.9 | 0x43 | 0.3 | 0x63 | 3.5 | | |

Stereo Enhancer Control Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-------|-------|
| | R | W | | | | | | | | |
| 0x1 | 0x86 | 0x87 | - | - | - | - | - | - | STEEN | STEOD |
| | | | - | - | - | - | - | - | 0 | 0 |

This register is to set "Stereo Enhancer" block in digital signal flow. This is to control Stereo enhancer function. This function is effective for DAC-path(playback) at "STEEN=1" and "SEMODE[7]=1".

STEOD

This bit is to set number of low pass filter order for Stereo enhancer.

| setting | Description |
|---------|---|
| 0 | second-order , LPF1 and LPF2 are effective. |
| 1 | first-order , only LPF1 is effective. |

STEEN

This bit is to set Enable/Disable of low pass filter for Stereo enhancer.

| setting | Description |
|---------|-------------------------|
| 0 | Stereo enhancer Disable |
| 1 | Stereo enhancer Enable |

- Stereo Enhancer LPF1 CoefL Register
- Stereo Enhancer LPF1 CoefH Register
- Stereo Enhancer LPF2 CoefL Register
- Stereo Enhancer LPF2 CoefH Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x1 | 0x88 | 0x89 | STE1CUT[7:0] | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x1 | 0x8a | 0x8b | STE1CUT[15:8] | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x1 | 0x8c | 0x8d | STE2CUT[7:0] | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x1 | 0x8e | 0x8f | STE2CUT[15:8] | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register is to set "Stereo Enhancer" block in digital signal flow. This is to set LPF of Stereo enhancer function.

STE1CUT[15:0]

This bit is to set the first low pass filter cut off frequency for Stereo enhancer.

STE2CUT[15:0]

This bit is to set the second low pass filter cut off frequency for Stereo enhancer.

Play Programmable LPF Setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|--------|--------|
| | R | W | | | | | | | | |
| 0x1 | 0xa0 | 0xa1 | - | - | - | - | - | - | PLPFOD | PLPFEN |
| | | | - | - | - | - | - | - | 0 | 0 |

This register is to set "LPF" block for DAC-path(playback) in digital signal flow. This is to set Enable/Disable and filter order. This function is effective for DAC-path(playback) at "PLPFEN=1" and "SEMODE[7]=1".

PLPFEN

This bit is to set Enable/Disable of low pass filter for DAC-path.

| setting | Description |
|---------|-----------------------------|
| 0 | LPF for DAC-path is Disable |
| 1 | LPF for DAC-path is Enable |

PLPFOD

This bit is to set number of low pass filter order for DAC-path.

| setting | Description |
|---------|----------------------------------|
| 0 | LPF for DAC-path is second-order |
| 1 | LPF for DAC-path is first-order |

Play Programmable LPF Coef (L) Register

Play Programmable LPF Coef (H) Register

| MAPCON | INDEX | | b7 (Initial) | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|--------|-------|------|-----------------|----|----|----|----|----|----|----|
| | R | W | | | | | | | | |
| 0x1 | 0xa2 | 0xa3 | PLPFC0L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x1 | 0xa4 | 0xa5 | PLPFC0H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register is to set "LPF" block for DAC-path(playback) in digital signal flow. This is to set Enable/Disable and filter order.

PLPFC0L [7:0] / PLPFC0H [7:0]

This bit is to set low pass filter cut off frequency for DAC-path.

This value has to change by Sampling frequency.

Please use Filter Setting Calculation program for *PLPFC0L / PLPFC0H setting.

Rec Programable LPF Setting Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|--------|--------|
| | R | W | | | | | | | | |
| 0x1 | 0xa6 | 0xa7 | - | - | - | - | - | - | RLPFOD | RLPFEN |
| | | | - | - | - | - | - | - | 0 | 0 |

This register is to set “LPF” block for ADC-path(record) in digital signal flow. This is to set Enable/Disable and filter order.
 This function is exclusive to “HPF2” controlled by HPF2EN of DSP Filter Function Enable register.
 This function is effective for ADC-path(record) at “RLPFEN=1” and “SEMODE[7]=1”.

RLPFEN

This bit is to set Enable/Disable of low pass filter for ADC-path.

| RLPFEN | Description |
|--------|--|
| 0 | LPF for DAC-path is Disable (HPF2 is available) |
| 1 | LPF for DAC-path is Enable(HPF2 is not available. HPF2EN-bit is not valid) |

RLPFOD

This bit is to set number of low pass filter order for ADC-path.

| RLPFOD | Description |
|--------|----------------------------------|
| 0 | LPF for ADC-path is second-order |
| 1 | LPF for ADC-path is first-order |

Rec Programable LPF Coef (L) Register
 Rec Programable LPF Coef (H) Register

| MAPCON | INDEX | | b07 (Initial) | b06 | b05 | b04 | b03 | b02 | b01 | b00 |
|--------|-------|------|------------------|-----|-----|-----|-----|-----|-----|-----|
| | R | W | | | | | | | | |
| 0x1 | 0xa8 | 0xa9 | RLPFC0L | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x1 | 0xaa | 0xab | RLPFC0H | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register is to set “LPF” block for ADC-path(playback) in digital signal flow.

RLPFC0L [7:0] / RLPFC0H [7:0]

This bit is to set low pass filter cut off frequency for ADC-path.
 This value has to change by Sampling frequency.
 Please use Filter Setting Calculation program for *RLPFC0L / RLPFC0H setting.

Typical Performance Curves (Reference data)

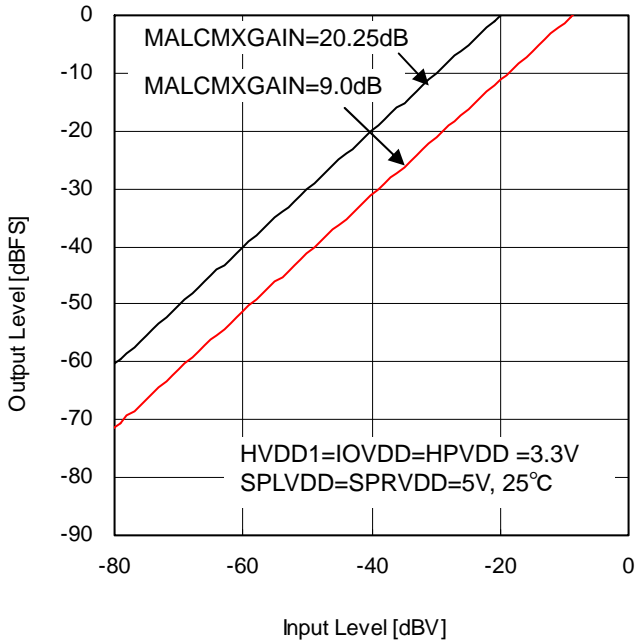


Figure 38.

Input Level [dBV] vs Output Level [dBFS]
Analog Mic Input tot ADC out, MALCEN=0

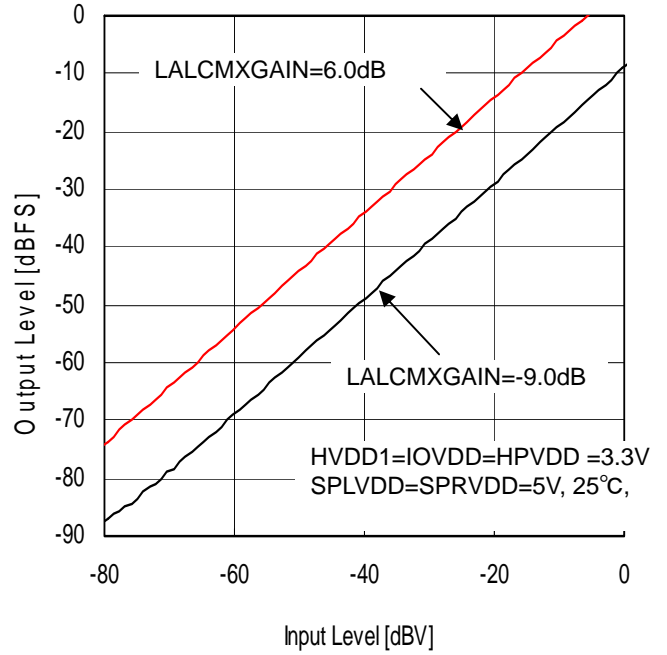


Figure 39.

Input Level [dBV] vs Output Level [dBFS]
Analog Line Input tot ADC out, LALCEN=0

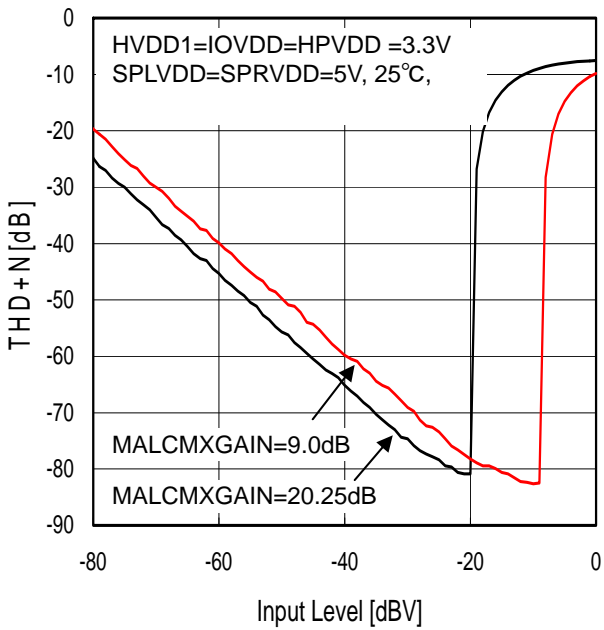


Figure 40.

Input Level [dBV] vs THD+N [dB]
Analog Mic Input tot ADC out, MALCEN=0

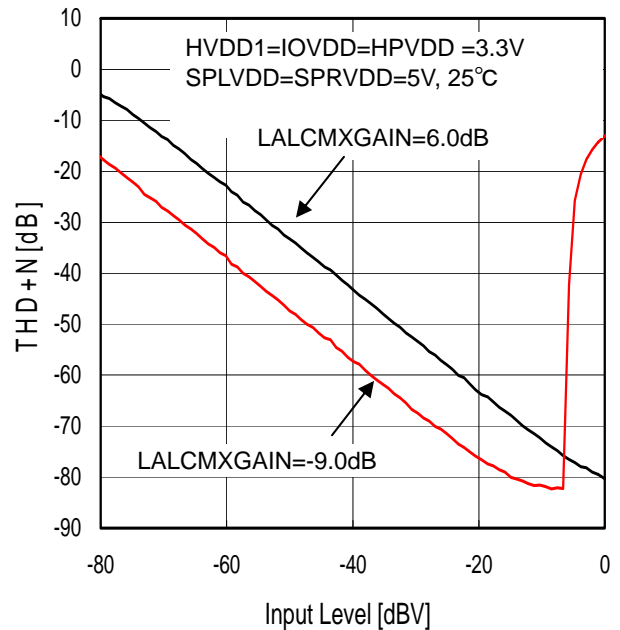


Figure 41.

Input Level [dBV] vs THD+N [dB]
Analog Line Input tot ADC out, LALCEN=0

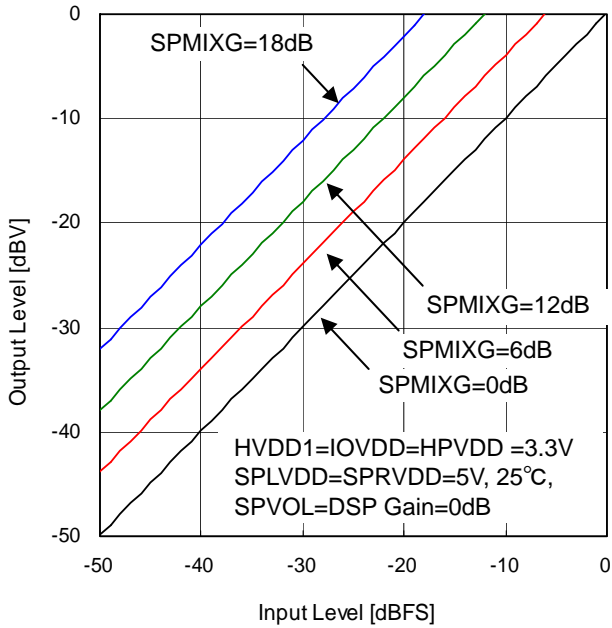


Figure 42.

Input Level [dBFS] vs Output Level [dBV]
Digital DAC Input to Class-D Speaker output

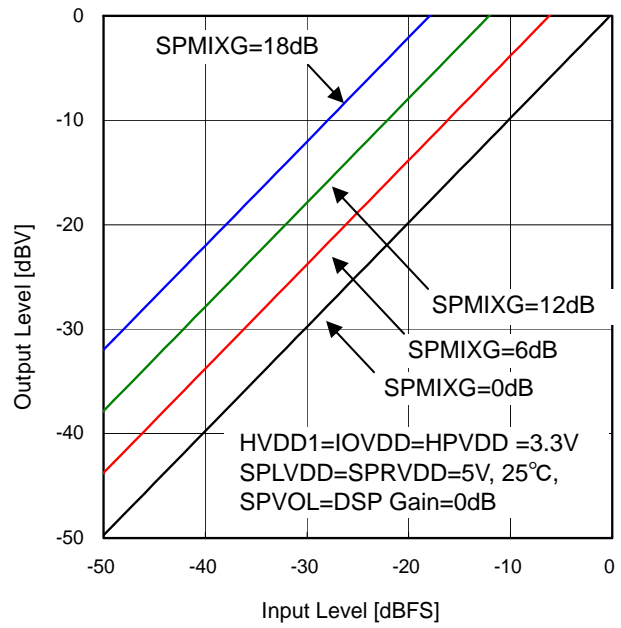


Figure 43.

Input Level [dBFS] vs Output Level [dBV]
Digital DAC Input to Class-AB Speaker output

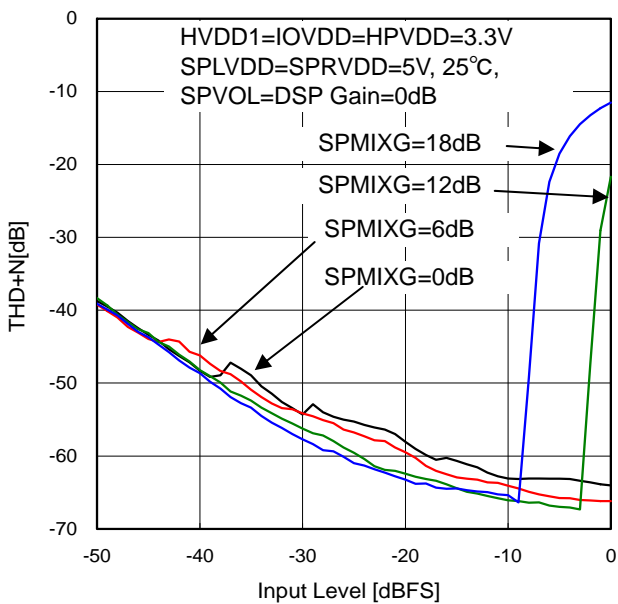


Figure 44.

Input Level [dBFS] vs THD+N [dB]
Digital DAC Input to Class-D Speaker output

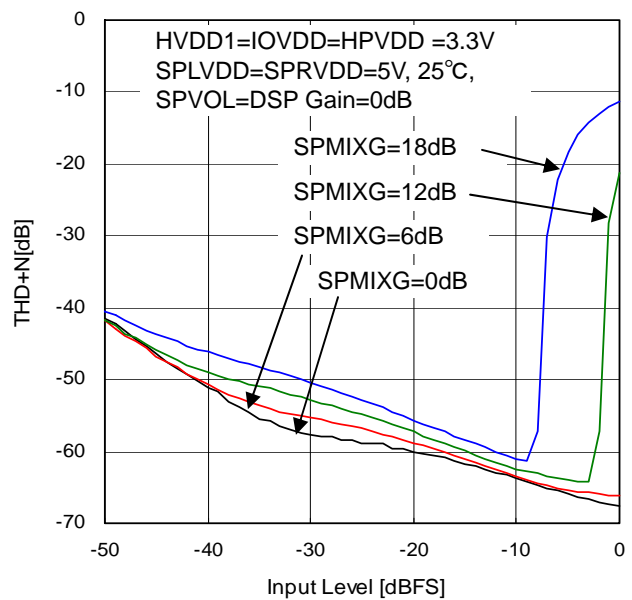


Figure 45.

Input Level [dBFS] vs THD+N [dB]
Digital DAC Input to Class-AB Speaker output

I/O equivalence circuits

| No. | Name | I/O | Power | I/O equivalence circuits |
|-----|------------|-----|--------|--------------------------|
| 17 | MICBIAS | O | HVDD1 | |
| 37 | VMID | O | REGOUT | |
| 33 | PLL | O | REGOUT | |
| 15 | BEEPIN | I | REGOUT | |
| 16 | MICBIASREF | O | HVDD1 | |

| No. | Name | I/O | Power | I/O equivalence circuits |
|----------------------------|---|-----|--------|---|
| 32 29 24 22 | MCLKI SDIN CSB/SCL SCLK/SAD | I | IOVDD | <p>The diagram shows an input pin connected to an IOVDD supply through a pull-up resistor. The signal path includes a Schmitt trigger. Two diodes are connected to the pin: one pointing towards IOVDD and one pointing towards DGND.</p> |
| 31 30 26 23 28 | BCLK LRCLK IRQB SDATA/SDA SDOUT | IO | IOVDD | <p>The diagram shows a bidirectional pin with an IOVDD supply, a pull-up resistor, and a Schmitt trigger. It includes two diodes (one to IOVDD, one to DGND) and a CMOS output stage with PMOS and NMOS transistors.</p> |
| 25 | RESETB | I | IOVDD | <p>The diagram shows the RESETB pin connected to IOVDD through a pull-up resistor. It features a Schmitt trigger and two diodes (one to IOVDD, one to DGND).</p> |
| 20 | REGOUT | O | HVDD1 | <p>The diagram shows the REGOUT pin connected to HVDD1 through a PMOS transistor. It includes a pull-up resistor, an NMOS transistor, and a diode connected to AGND.</p> |
| 11 12 | SPRP SPRM | O | SPRVDD | <p>The diagram shows the SPRP/SPRM pins connected to SPRVDD through a PMOS transistor. It includes a pull-up resistor, an NMOS transistor, and a diode connected to SPRGND.</p> |

| No. | Name | I/O | Power | I/O equivalence circuits |
|----------------------------------|--|-----|--------|--------------------------|
| 14 | SPMUTE | I | IOVDD | |
| 8 7 | SPLP SPLM | O | SPLVDD | |
| 2 1 | HPOUTR HPOUTL | O | HPVDD | |
| 4 | HPOUTCAP | O | HPVDD | |
| 38 40 42 39 41 43 | LIN1L LIN2L LIN3L LIN1R LIN2R LIN3R | I | REGOUT | |
| 35 34 | MINP MINM | I | REGOUT | |

Cautions on use

- 1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus don't exceed the absolute maximum ratings of supply voltage, temperature. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.
- 2) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.
- 3) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.
- 4) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.
- 5) Thermal design
If use speaker amplifier function, please consider power dissipation by an actual using status, and perform the thermal design which have a margin enough. If an input signal is made excessive in the state with insufficient heat dissipation, desired output power may not only be securable, but the thermal shutdown may operate.
- 6) Thermal shutdown
This IC has the thermal shutdown circuit. If the thermal shutdown operates, speaker output terminal and Headphone Output terminal will stop in the open state(high impedance state).The thermal shutdown is only a function for suspending the output operation of IC to the last at the time of the thermal run-away under the abnormal condition in which chip temperature(T_{jmax}) exceeded 170 degrees. It is a circuit to protect IC, and the purpose is not offering protection and a guarantee of the set.
- 7) Short protection of output terminals
This IC has the short protect function for output terminals. If the short protect function operates, output terminal will be latched and stop in the open state(high impedance state).After a stop, even if a short state is removed, it does not return to normal operation automatically. Please once write speaker amplifier enable register to make it return.
- 8) Operating condition
Operating voltage and operating temperature are ranges which perform basic function. Electrical characteristics and absolute maximum rating are not guaranteed in full voltage range or full temperature range.
- 9) Electrical characteristics specification
Each audio characteristic specification, such as limit output power, total harmonic distortion, the maximum gain, an ALC limit level, and an ALC release level, shows the standard performance of the device, and depends for it on board layout / use parts / power supply part greatly.
Typical specification value is a value when a device and each parts are directly mounted in the board of Rohm's standard.
- 10) Power supply
Since the speaker L power supply (SPLVDD) and the speaker R power supply (SPRVDD) are shorted inside IC, please use them as a same power supply.
Moreover, large peak current rushes into a power supply line at the time of ClassD speaker amplifier use.
The audio characteristic is affected by the value of a power supply decoupling capacitor, and layout.
The power supply decoupling capacitor should be layouted (1uF or more) with sufficiently low ESR (equivalent series resistance) to most close of IC terminal.
Moreover, in the design of a board pattern, the wiring of a power supply / GND line should become low impedance. In that case, even if digital power supply and analog power supply are same potential, please divide the digital power pattern and the analog power pattern and reduce a surroundings lump of the digital noise to the analog power supply by the common impedance of a wiring pattern.
Please take the same pattern design into consideration also about a GND line. Moreover, while inserting a capacitor between power supply-GND terminals about all the power supply terminals of LSI, and please determine the value of capacitor after sufficient confirmation that there is no problem in the characteristics of capacitors to be used (a capacity omission happens at low temperature) in the case of electrolytic capacitors use.
- 11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

12) Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

Ordering Information

B U 2 6 1 5 6 R F S

E 2

Package
RFS:HTSSOP-A44R

Packaging and forming specification
E2: Embossed tape and reel

Physical Dimension Tape and Reel Information

| | |
|---------------------|---------------------|
| Package Name | VQFN040V6060 |
|---------------------|---------------------|

<包装仕様>

| | |
|------|--|
| 包装形態 | エンボステーピング(防湿仕様) |
| 包装数量 | 1500pcs |
| 包装方向 | E2 (リールを左手に持ち、右手でテープを引き出したときに 製品の1番ピンが左上にくる方向) |

※ご発注の際は、包装数量の倍数でお願い致します。

(UNIT : mm)
PKG : HTSSOP-A44R
Drawing No. EX197-5002

Marking Diagram

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TSZ22111 · 15 · 001

91/92

TSZ02201-0V1V0E502570-1-2
Jul.1.2014 Rev.001

Revision History

| Date | Revision | Page | Item | Changes |
|-------------|----------|------|------|-------------------|
| Jun.24.2014 | Rev.001 | - | - | Rev.001. Release. |

Notice

Precaution on using ROHM Products

- Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

- ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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General Precaution






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