THE DATASHEET OF

BM1C101F-GE2

AC/DC Drivers

Power Factor Correction and Quasi-Resonant DC/DC converter IC

BM1C101F

General Description

The compounded LSI of the Power Factor Correction (PFC) converter and Quasi-Resonant (QR) controller type DC/DC converter IC provides an optimum system for all products that include an electrical outlet. BM1C101F has a built-in HV starter circuit that tolerates 650V and X-Cap discharge function, and contributes to low power consumption and high speed start.

The PFC part operates by Boundary Conduction Mode (BCM). It reduces the switching loss and the switching noise.

Because of zero current detection (ZCD) by a resistance, this solution achieves no auxiliary winding and reduces external parts and the bias current.

The DC/DC part operates by Quasi-Resonant Mode This method enables soft switching and helps to keep the EMI low. With MOSFET for switching and current detection resistors as external devices, a higher degree of design freedom is achieved.

This IC has over voltage protection for the PFC output terminal, which protects electrolytic capacitor by stopping switching and makes the standby power consumption low by the PFC ON/OFF control function. The IC includes various protective functions such as VCC over voltage protection, external latch protection, brown out protection, soft start function, per-cycle current limiter and over load protection.

Features

- ■PFC+QR Combo IC
- ■Built-in 650V tolerance start circuit
- ■VCC pin: under and over voltage protection
- ■Brown out function
- ■External latch terminal function
- ■PFC boundary conduction mode (voltage control)
- ■PFC Zero Cross Detection
- ■PFC variable max frequency
- ■PFC Dynamic & Static OVP function
- ■PFC Output level switched function
- ■PFC ON/OFF setting
- ■QR low power when load is light (Burst operation) and frequency decrease function
- ■QR maximum frequency control (120kHz)
- ■QR_CS pin open protection and OCP function
- ■QR Over-Current Protection with AC compensation
- ■QR Soft Start function
- ■QR secondary side protection circuit of over-current
- ■QR_ZT pin 2 step timeout function and OVP function

Applications

AC adapters, TV, Lighting, Household appliances (Vacuum cleaners, Air cleaners, Air conditioners, IH cooking heaters, Rice cookers, etc.).

Key Features

Operating Power Supply:	VCC	8.9V to 26.0V
Voltage Range:	VH_IN	80V to 500V
Operating Current:	Normal	1.2mA (Typ)
	Burst	0.6mA (Typ)
Max frequency:	PFC	External setting
	QR	120kHz (Typ)
The range of temperature:		-40°C to+105°C

Package W(Typ) x D(Typ) x H(Max)

SOP18 11.20mm × 7.80mm × 2.01mm pitch 1.27mm

SOP18

Typical Application Circuit

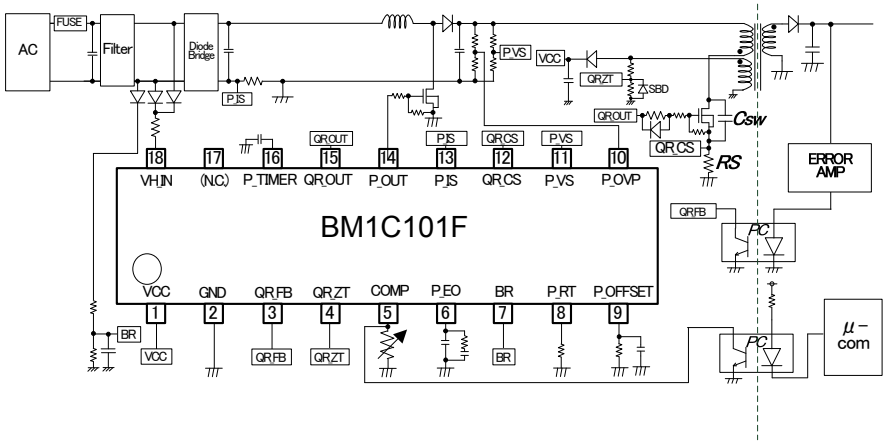


Figure 1. Application circuit

Pin Configuration

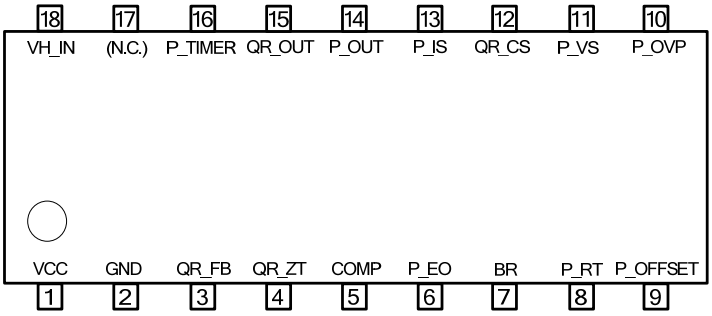


Figure 2. Pin Layout (Top View)

Pin Description

Table 1. I/O Pin Functions

Pin Name	I/O	Pin No.	Function	ESD Diode	
				VCC	GND
VCC	I/O	1	[General] Power supply pin	-	○
GND	I/O	2	[General] GND pin	○	-
QR_FB	I	3	[QR] Feedback detection pin	−	○
QR_ZT	I	4	[QR] Zero cross detection pin	-	○
COMP	I	5	[General] External latch input pin	−	○
P_EO	O	6	[PFC] Error amplifier output pin	−	○
BR	I	7	[General] Input AC voltage monitor pin	−	○
P_RT	I	8	[PFC] Max frequency setting pin	−	○
P_OFFSET	I	9	[PFC] ON/OFF setting voltage	−	○
P_OVP	I	10	[PFC] Over voltage detection pin	−	○
P_VS	I	11	[PFC] Feedback signal input pin	−	○
QR_CS	I	12	[QR] Over-current detection pin	−	○
P_IS	I	13	[PFC] Zero cross detection pin	−	○
P_OUT	O	14	[PFC] External MOS drive pin	○	○
QR_OUT	O	15	[QR] External MOS drive pin	○	○
P_TIMER	I	16	[PFC] OFF time setting pin	−	○
N.C.	-	17	-	-	-
VH_IN	I	18	[General] Starter circuit pin	-	○

Block Diagram

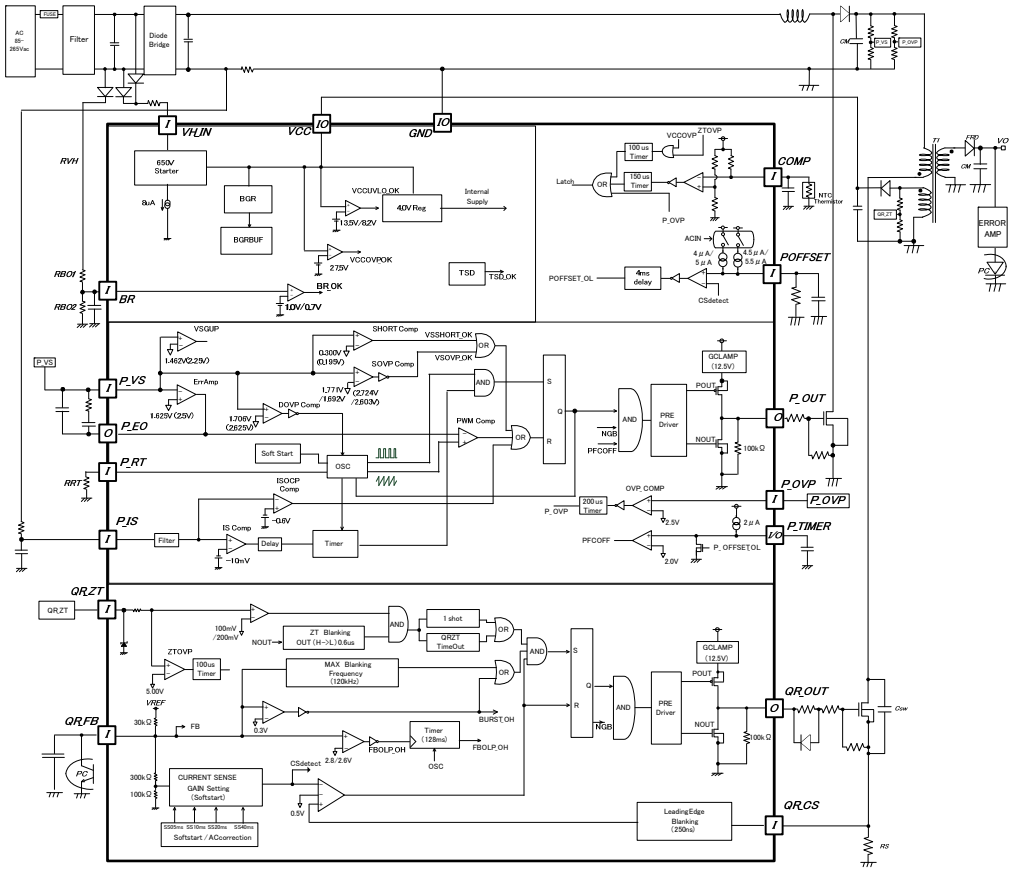


Figure 3. Block Diagram

Description of Blocks

(1) Starter Block (VH_IN Pin)

The IC builds in starter circuit which tolerates 650V. It is shown in Figure-4. For that it enables low standby mode current consumption and high speed starting.
After starting, current consumption is idle I_{START3} (typ=8uA) only. (Shown in Figure-5)
To supply electric power from AC supply to VH_IN pin, diode rectification connection is needed from both AC input.
It is shown in Figure-4.

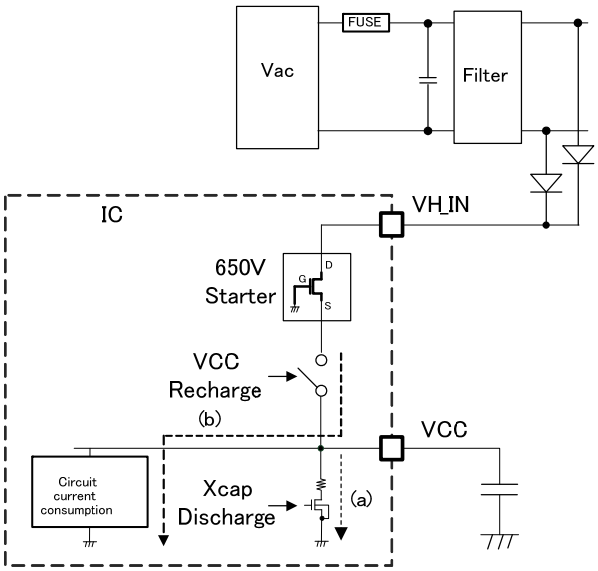


Figure 4. Starter Circuit Block Diagram

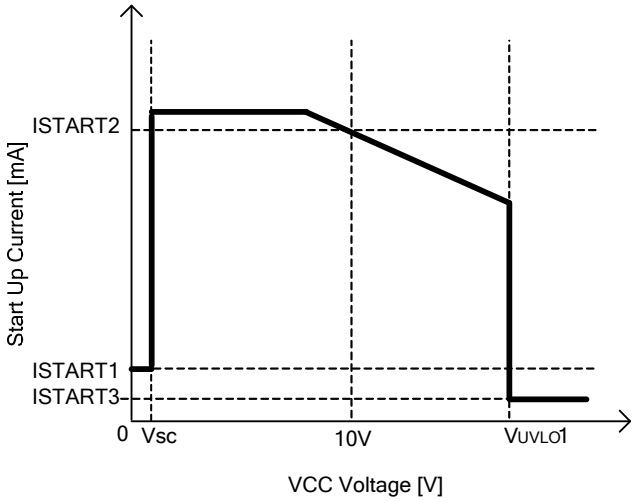


Figure 5. Start-up Current vs VCC Voltage

In addition, VH_IN pin has an X-Cap discharge function. If the input voltage peak of BR pin goes below 1.0V, discharge function starts after passing 256ms. X-Cap discharge is the function that once VH_IN charge moves from VH_IN to VCC pin by VCC recharge function, IC discharges VCC charge by X-Cap discharge node(Figure-4(a)).
In the case there is no power supply from the auxiliary winding such as a light load, the OLP state of the secondary side output, the IC operates VCC recharge function. VCC recharge function charges VCC pin from VH_IN pin, VCC pin voltage rises. As the result, X-cap is discharged. When VCC recharge function operates, the current path is Figure 4 (b). After it past 256ms timer from pulling out the outlet, X-Cap function discharges the charge of X-cap by the current path of Figure-4(a).

(2) Start-Up Sequence

(Low temperature start up: Cold Start Function, Soft Start Operation)

This IC has a built-in AC voltage detection function and this switches the reference voltage magnification of PFC and CS over current detection voltage of QR and POFFSET pin current. When BR pin peak voltage > V_{ACIN1} (typ=2.5V), IC judges ACIN=H. When BR pin peak voltage <V_{ACIN1}, IC judges ACIN=L.

The reference magnification of PFC: The internal reference magnification of PFC changes.
ACIN=H: ×1.0, ACIN=L: ×0.65

The over current detection switching of QR: FB/CS gain of QR changes and
The over current detection voltage also changes.
ACIN=H: ×0.90, ACIN=L: ×1.00

The POFFSET current at PFC OFF : POFFSET current at PFC=OFF is changed
ACIN=H: 5.0uA, ACIN=L: 5.5uA

The POFFSET current at PFC ON : POFFSET current at PFC=ON is changed
ACIN=H: 4.0uA, ACIN=L: 4.5uA

At starting, IC initial condition is ACIN=L except cold start status.

When the VCCUVLO protection function and the brown out function are released, the IC starts to operate.

[Cold Start]

At the time of start-up, the IC operates under the condition: PFC reference voltage magnification = × 1.0 and QR over current detection voltage = × 1.0. This is the function that enables the stable start-up within required time by a momentary rising of PFC output voltage in order not to make start-up time longer during low temperature for applications with thermistor. At starting QR starts with a soft start. During this time PFC stops. And PFC can start operation after it passed 4ms from a soft start and P_EO voltage is charged more than about 0.8V.

About the above the cold start operation, PFC operates until P_VS voltage rises to 90% of AC 240V. When PFC output voltage rises to 90% the cold start is released. After cold start operation, the ACIN logic is set to ACIN=L when the detection of AC voltage hasn't finished yet. When the stable AC waveform is applied seven times in a row, the IC detects AC peak voltage by BR pin and the setting of ACIN=H/L is determined. When QR output is stable and A quarter of the QRFB voltage(CS detect voltage) is lower than POFFSET voltage, PFC stops after the time set at P_TIMER pin. Refer to Figure 6.

Operation explanation of Figure 6

A: Input voltage VH_IN is applied. Then the input voltage ×√2 is outputs from PFC.
B: Charge current flows from VH_IN pin to the VCC pin capacitor through the start circuit. Then VCC pin voltage rises.
C: When V_{UVLO1} (typ=13.5V) < VCC pin, VCC UVLO is released and the internal regulator rises.
D: When the IC detects BR pin voltage > 1.0V on the condition that VCC ULVO is released, and the brown out function is released.
E: QR DCDC starts operation. When QR switching operation starts, secondary output VOUT raises. After QR DC/DC starts up, secondary output voltage is needed to be stable within T_{FOLP}(typ=128ms).During the start-up the IC operates in below conditions by cold start function until PFC become 90% of AC230V.
Over current detection of QR = AC100V (QRFB/QRCS=4.0)
Output voltage of PFC = AC230V (PFC standard voltage=2.5V)
After the cold start, the IC operates under the status AC 100V until AC voltage is detected.
And if POFFSET pin voltage>CS detect voltage after the cold start, PFC stops after the setting time of PTIMER pin.

[QR Start-Up Operation]

E: IC adjusts the over-current limiter of QR DC/DC part during the operation of soft start1 against over voltage and current rising. IC operates in the soft start1 state for t_{ss1}(typ=0.5ms). Then maximum current of QR is limited to 12%.
F: IC adjusts the over-current limiter of QR DC/DC part during the operation of soft start2 against over voltage and current rising. IC operates in the soft start2 state for t_{ss2} (typ=1.0ms). Then maximum current of QR is limited to 25%.
G: IC adjusts the over-current limiter of QR DC/DC part during the operation of soft start3 against over voltage and current rising. IC operates in the soft start3 state for t_{ss3} (typ=2.0ms). Then maximum current of QR is limited to 50%.
H: IC adjusts the over-current limiter of QR DC/DC part during the operation of soft start4 against over voltage and current rising. IC operates in the soft start4 state for t_{ss4} (typ=4.0ms). Then maximum current of QR is limited to 75%.
I: When T_{SS4} (typ=4ms) passed from start-up, soft start function finishes.
J: When secondary output voltage is stable, the QR_FB voltage is also stable by constant value corresponding to flow current from photo coupler. At normal state, QR_FB voltage is QR_FB<$V_{FBOLP1B}$ (typ=2.60V).

[PFC Start-Up Operation]

I: When P_VS pin voltage is more than V_{P_SHORTH} (typ=0.3V), the IC judges that the PFC output is normal condition.After finishing the soft start of QR, PFC starts to operate when P_EO voltage is over 0.8V. At this time PFC output rises to 90% of setting voltage of ACIN=H.
K: After PFC output rise to 90%, the cold start is released and PFC reference voltage and QR gain is set to ACIN=L.
L: AC is detected seven consecutive by BR pin. The operation is started by ACIN setting controlled by AC voltage. The IC operates under the condition PFC reference voltage = 2.5V because ACIN=H is detected.

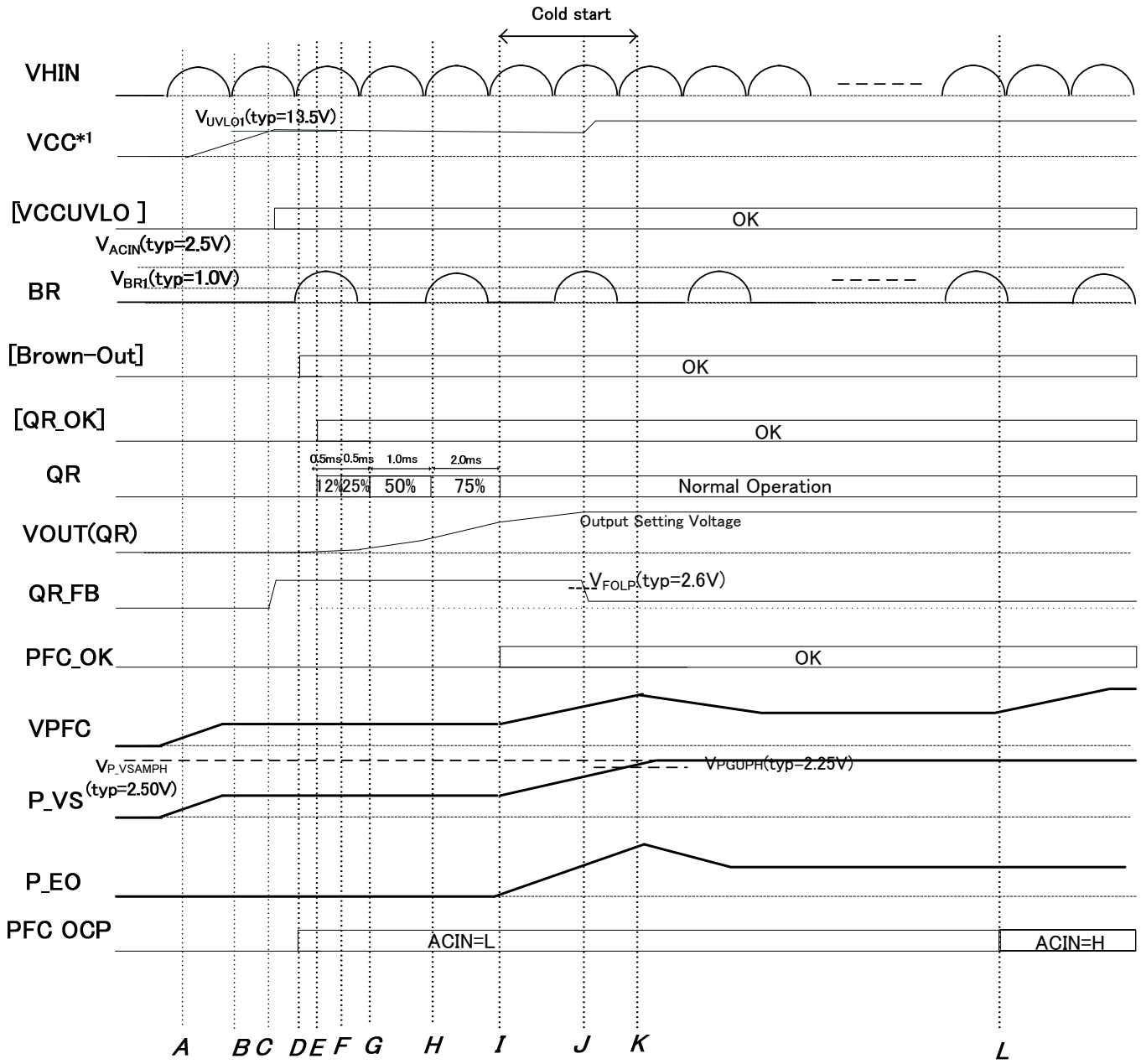


Figure 6. Start-up Sequence Timing Chart

(3) VCC Pin Protection Function

The IC builds in VCC low voltage protection function, "VCC UVLO (Under Voltage Lock Out)", VCC over voltage protection function, "VCC OVP (Over Voltage Protection)", and VCC CHARGE function that operates in case the VCC voltage drops. VCC UVLO and VCC OVP are for stopping switching to prevent the switching MOSFET from destroying at abnormal voltage. VCC charge function stabilizes the secondary output voltage by stabilizing VCC voltage to charge the power from the high voltage line to VCC pin through the starter circuit when the VCC voltage drops.

And VCC pin releases latch protection when VCC voltage is low.

(3-1) VCC UVLO／VCC OVP Function

VCC UVLO is an auto recovery comparator that has voltage hysteresis. VCC OVP is latch protection. VCCOVP has mask time to prevent a false detection by surge etc. When the situation of VCC pin voltage > V_{OVP} (typ=27.5) continues for T_{LACH} (typ=100us), OVP protection is operated.

(3-2) VCC Charge Function

After the VCC pin voltage >V_{UVLO1}, once VCC < V_{CHG1} VCC charge function operates. Then VCC pin is charged from VH_IN pin through starter circuit. The function prevents VCC starting failure. In charging VCC, PFC switching operation is stopped to stable VCC pin charge. When the VCC pin voltage rises to VCC >V_{CHG2}, VCC charging is stopped, and PFC starts to work. The operations are shown in figure-7. However, as VH_IN voltage is AC input, VCC is not charged in the range of low voltage. During this time, VCC charging function operates but VCC pin is not charged. Even If the AC voltage is low, adjust the value of VCC capacitor in order for VCC pin not to become lower than UVLO and more than 22uF is recommended as the value of VCC capacitor. And to prevent thermal runaway, this function also stops when the overheating of the IC operates.

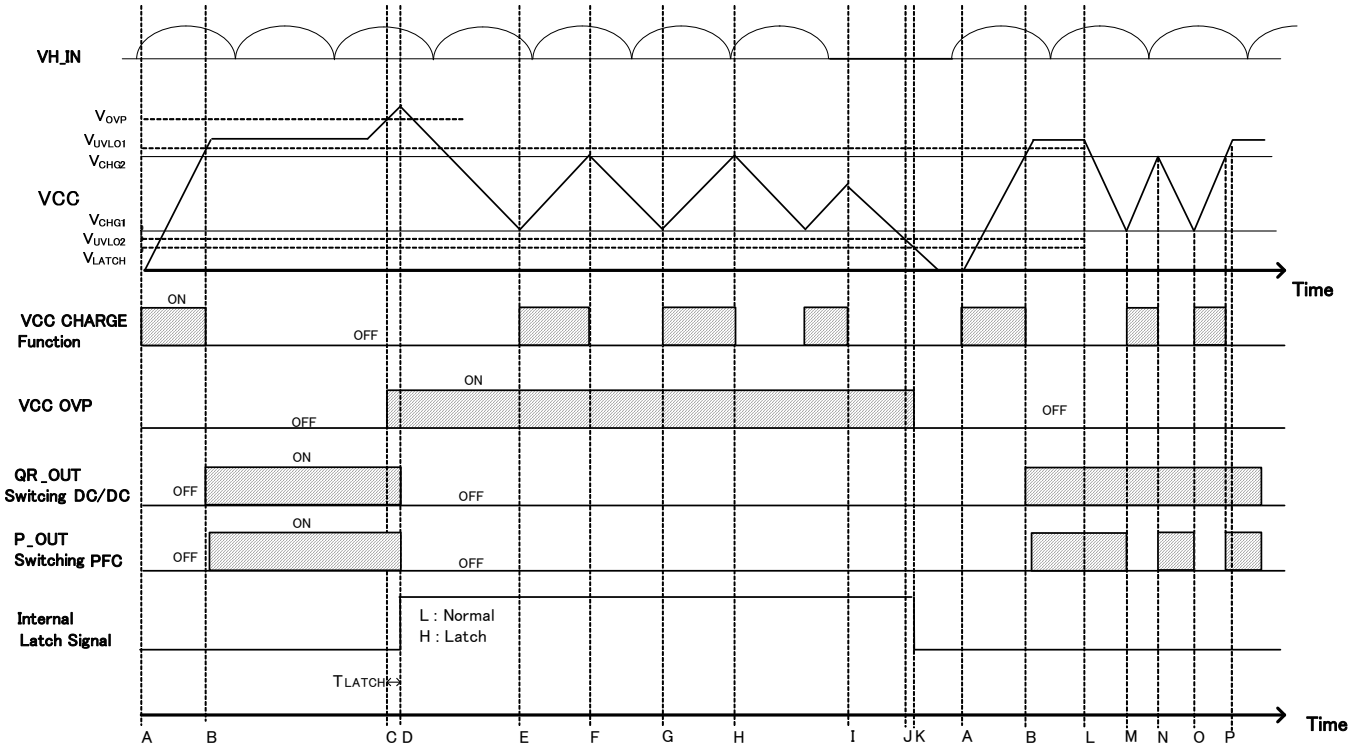


Figure 7. VCC UVLO / VCC OVP / VCC Charge Function Timing Chart

A: VH _IN pin voltage is applied, VCC pin voltage starts rising.
B: VCC > V_{UVLO1}, VCC UVLO is released, QR DC/DC operates. After that, PFC operation starts at QR soft-start finished.
C: VCC > V_{OVP}, VCC OVP detects the overvoltage in the IC.
D: If the state of VCC > V_{OVP} continues for T_{LATCH} (typ=100us) time, switching stops by the OVP function. (Latch mode).
E: Because of latch protection, PFC and QR don't operate switching. Then, VCC voltage decreases because there is supply from an auxiliary winding. If VCC pin voltage<V_{CHG1}, VCC pin voltage rises by operating VCC recharging function.
F: VCC pin voltage > V_{CHG2}, VCC recharge function stops. Because of latch protection, PFC and QR don't operate switching. By the operation of E and F, latch is not released since VCC voltage is stabilized. For that, latch protection is not released.
G: (The same as E.)
H: (The same as F.)
I: The voltage of VH_IN is stopped to supply. Then the brown out is detected and X-cap electrical discharge is started.
J: Because VH_IN is lost, VCC charging function operates but VCC is not charged. So VCC voltage decreases. If VCC pin voltage < V_{UVLO2}, VCC UVLO function operates.
K: VCC<V_{LATCH}, Latch is released.
L: When the secondary output has no load, QR DCDC works burst operation. VCC pin voltage drops because power does not supply from auxiliary winding
M: VCC<V_{CHG1}, VCC recharging function operates.
N: VCC> V_{CHG2}, VCC recharge function stops.
O: (The same as M.)
P: To increase a load, the power supply of the auxiliary winding starts.

However when the VCC recharge function operates, the standby power is increased because the loss of (VHIN voltage – VCC voltage) × VH current occurs. So design the application which supplies electricity from the auxiliary winding to VCC during no load. And operate VCC recharge function in time of a start-up assist, an over load protection, and a latch protection.

(4) COMP Pin (Outside forced stop function)

The COMP pin is used for forced stop function. When the COMP pin is lower than VCOMP (typ=0.5V), PFC part and QR DC/DC part stop. A detection timer T_{COMP} (typ=150us) is builds in to prevent detection errors caused by noise. The stop mode is latched.

The COMP pin is pulled up by R_{COMP} (typ=25.9kΩ), When the COMP pin is pulled down by a lower resistance value than R_T(3.70kΩ.typ), IC detects the abnormality and IC operates latch off. The application examples are shown in Figure 8, 9 and 10.

Overheating Protection by NTC Thermistor

When a thermistor is attached to the COMP pin, latch stop can be operated when overheating occurs. In the case of this application, it should be designed so that the thermistor resistance becomes R_T (typ=3.70kΩ) when overheating is detected.

(Figure 8, 9 are application circuit examples in which latching occurs when Ta = 110°C.)

Please set the capacitor value less than 0.01uF to stabilize COMP pin voltage if COMP pin is attached capacitor to GND.

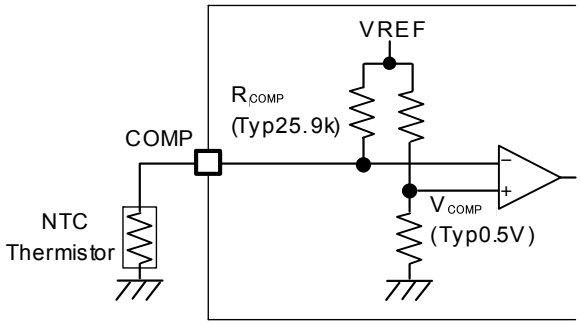


Figure 8. COMP Pin Overheating Protection Application

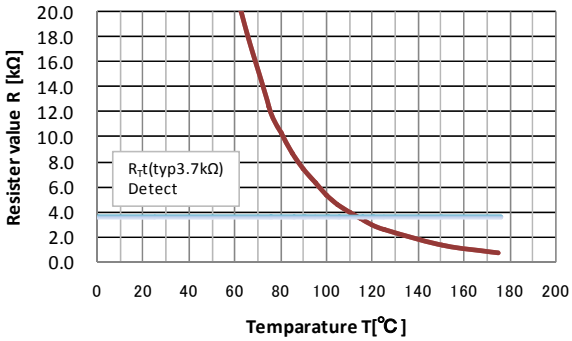


Figure 9. Temperature-Thermistor Resistance Value Characteristics

Secondary Output Voltage Overvoltage Protection

A photo-coupler is attached to the COMP pin to perform detection of secondary output overvoltage.

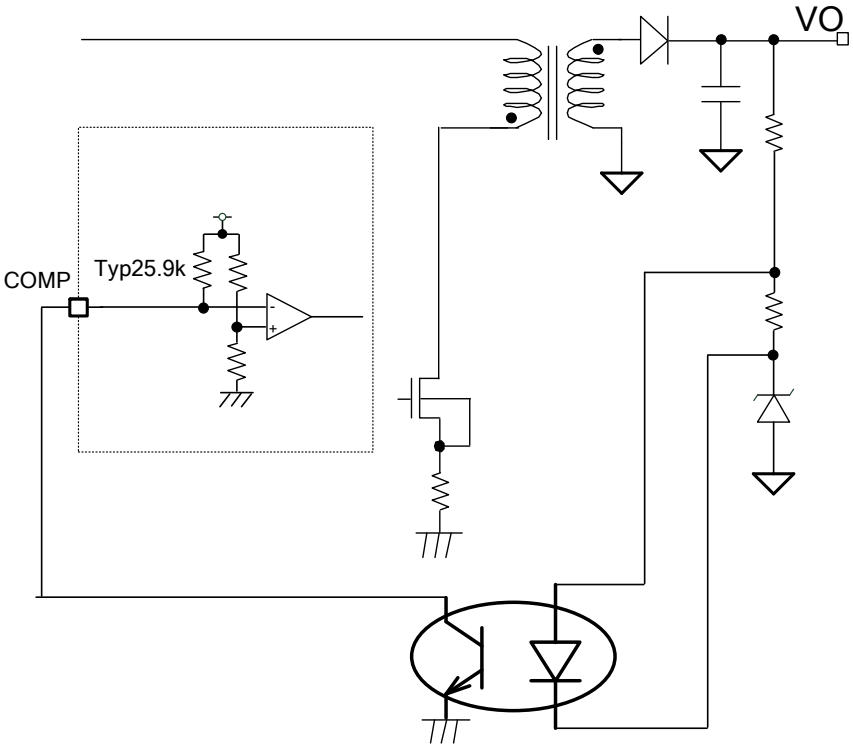


Figure 10. Output Overvoltage Protection Application

(5) BR Pin

The BR Pin has built-in three functions below. Usage example is shown in Figure 11.

1: Low AC voltage protection. (Blown IN/OUT) If BR pin voltage peak is lower than V_{BR1} (typ=1.0V), the operation is stopped.
2: When the condition is detected that BR pin voltage peak is lower than V_{BR1} (typ1.0V), and x-cap discharging function is operated from VH_IN pin.
3: AC input voltage judges whether 240V or 100V, and PFC reference voltage and voltage level of the QRCS over-current detection and POFFSET current are switched by ACIN logic. When the peak of BR pin voltage is higher than V_{ACIN}(typ=2.5V), IC judges ACIN=H. And when it is lower, it judges AC100V.

The Input voltage to the BR pin is the full-wave / half-wave rectified AC waveform of 50Hz/60Hz voltage divided by resistance. In addition, in order to stabilize the input waveform, the capacitor (0.1nF to 10nF) must be connected close to the BR pin.

(5-1) Low AC Voltage Protection (Blown IN/OUT)

When AC voltage is low, blown out function can stop the PFC block and QR block operation. The AC input voltage is connected to the BR pin through two divider resistors. When the peak voltage of the BR pin is higher than V_{BR1} (typ=1.0V), the IC judges normal state and QR DC/DC starts operation and QR and PFC start to operate.

If the AC outlet is plugged out after the IC operates, QR DCDC part stop after T_{BR} (typ=256ms) after the IC detects that BR pin exceeds V_{BR} (typ=1.0V) finally. Moreover, X capacitor discharge function is operated.

(5-2) X Capacitor Discharge Function

After it past T_{BR} (typ=256ms) from AC voltage dropping, X-capacitor discharge function is operated.
X-capacitor discharge function operates to be linked VCC recharge function after VCC is discharged.

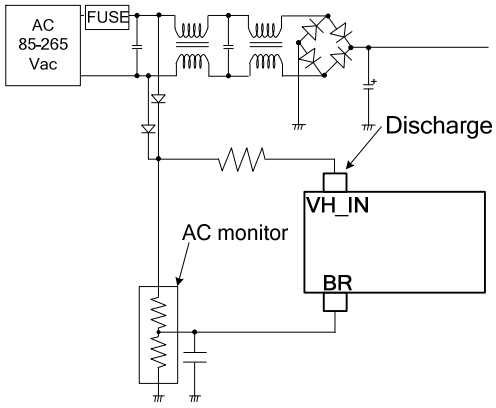
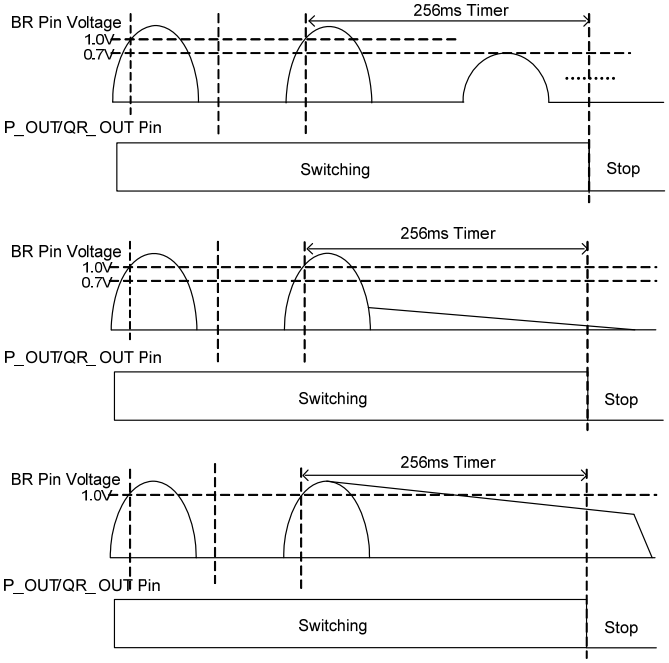


Figure 11. Blown IN/OUT Application Circuits



(1) When AC input voltage drops BR < V_{BR1}(typ=1.0V) for more than 256ms, QR DC/DC operation stops
In this case, X-cap discharge function starts to operate.

(2) When the AC outlet is pulled out, BR pin voltage < V_{BR1} (typ=1.0V), QR DC/DC output stops after 256ms from the time which the BR terminal voltage drops to 1.0V or less.
In this case, Xcap discharge function operates.

(3) If the AC outlet is pulled out, BR pin voltage is higher than V_{BR1} (typ=1.0V), QR DC/DC does not stop.
After T_{BR} (typ=256ms) from the time which the BR pin peak voltage drops to V_{BR1} (typ=1.0V), QR DC/DC stops and X-cap discharge function operates.

Figure 12. BR Pin Timing Chart

(5-3) PFC Output Voltage Switching Function

In order to make PFC boosting rate constant for AC input voltage that varies by region, PFC output voltage value is switched by AC100V or AC240V. For example, PFC output voltage is set to 260V in the case of AC100V-based input and PFC output voltage is set to 400V in the case of AC240V-based input. As a result, the PFC efficiency of AC100V is improved and the noise of AC100V is low.

This function is detected AC100V or AC240V by BR pin voltage divided resistor from AC input voltage. (Refer to Figure 13). See the timing chart of Figure 14, When the waveform (voltage higher than the voltage V_{ACIN} (typ=2.5V)) of 9 cycles is applied continuously, IC judges AC240V system. Then, GM amplifier reference voltage inside IC is changed from V_{P_VSAMPL} (typ=1.625V) to V_{P_VSAMPH} (typ=2.5V), and the PFC output voltage is changed from 260V to 400V.

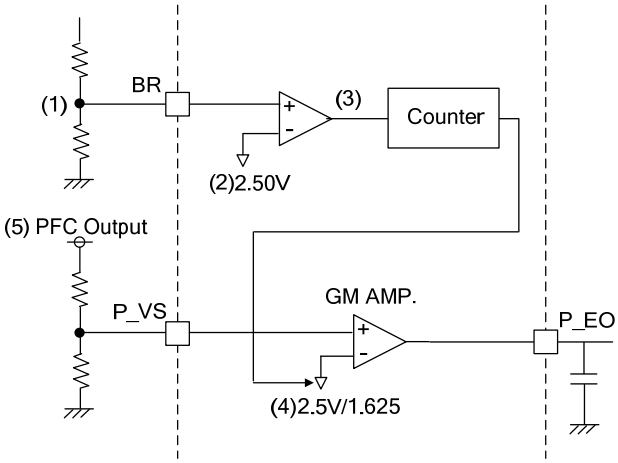


Figure 13. PFC output voltage switching function

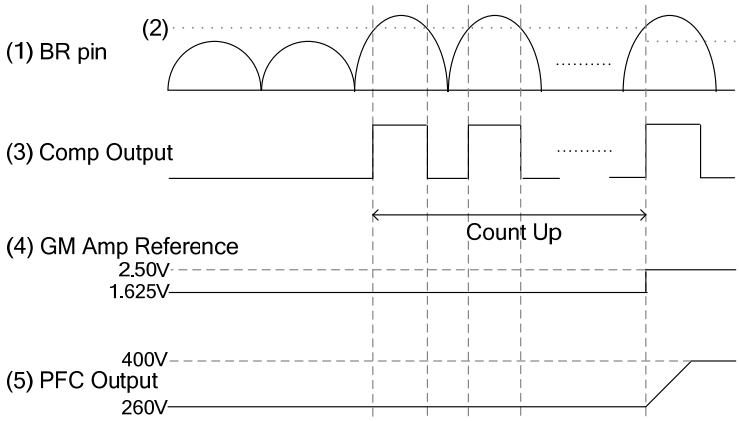


Figure 14. PFC output voltage switching Timing Chart

(6) The Quasi-Resonant DC/DC Driver

QR part of IC operates with PFM (Pulse Frequency Modulation) mode method. By monitoring the QR_FB pin, QR_ZT pin, and QR_CS pin, the IC supplies optimum system for QR DC/DC operation. IC controls ON width (Turn Off) of external MOSFET by QR_FB pin and QR_CS pin. And IC controls OFF width (Turn ON) of external MOSFET by QR_ZT pin. The details are shown below. (Refer to Figure 15)

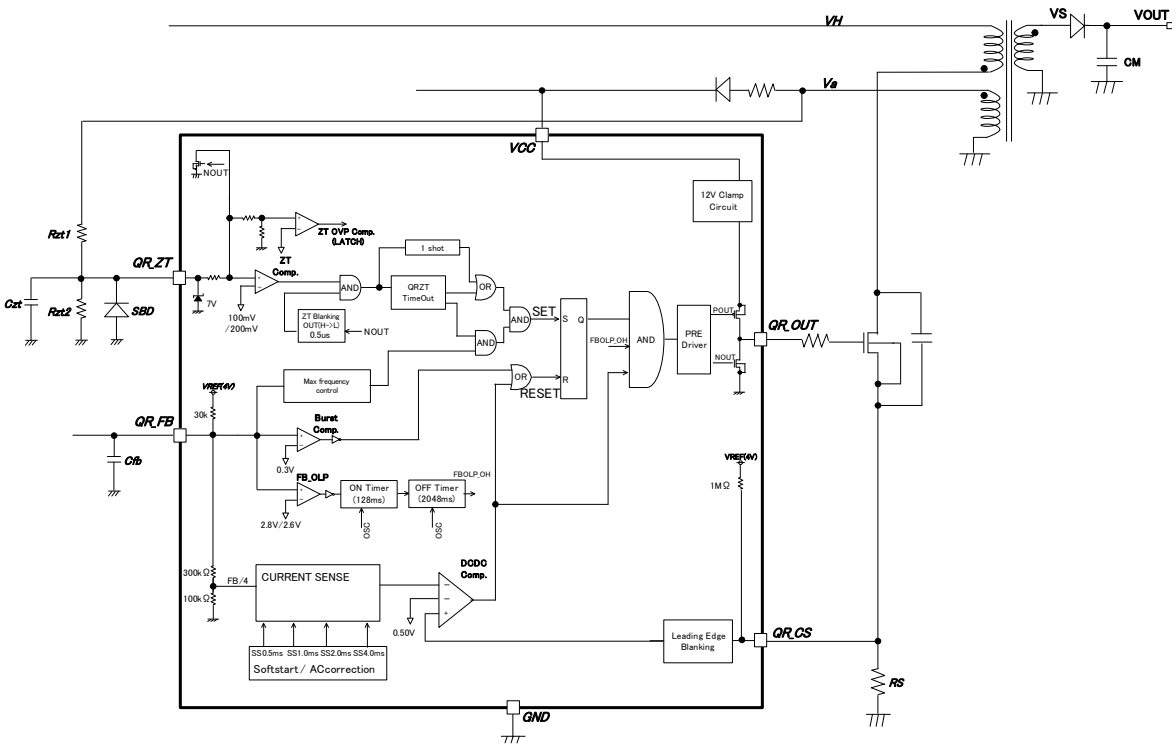


Figure 15. DC/DC Block Diagram

(6-1) Determination of ON width (Turn OFF)

ON width is controlled by QR_FB and QR_CS. The IC decides ON width by comparison between the value which divide QR_FB pin by AV_{CS1} (typ=4) voltage and QR_CS pin voltage. CS Limiter has changed comparator level lineally by QR_FB voltage shown in Figure-16. QR_CS voltage is also used over current limiter per pulse.
By change over current limiter level and maximum blanking frequency by QR_FB voltage, IC regulates output.

mode1: Burst operation
mode2: Frequency reduction operation (reduce max frequency)
mode3: Max frequency operation
mode4: Over load operation (To detect over load state, IC stops switching)

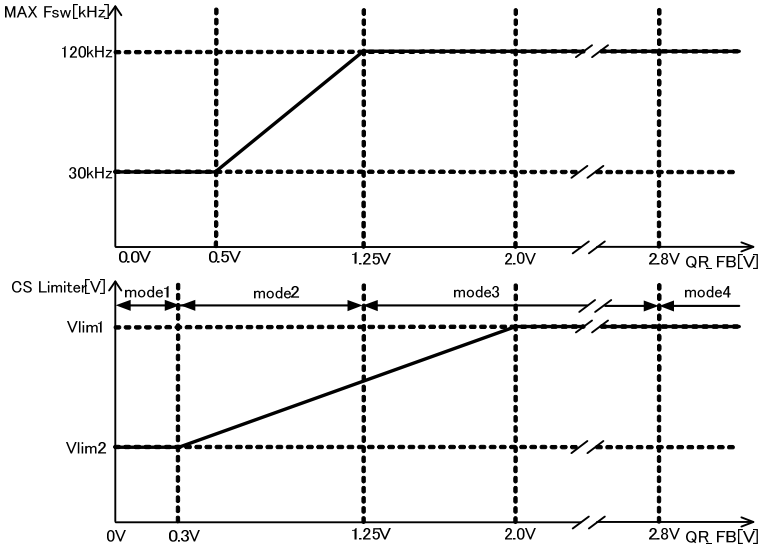


Figure 16. QR_FB Pin Voltage – Over-Current Limiter, Max Frequency Characteristics

To adjust over-current limiter level, CS Over-Current Protection voltage is switched in soft-start, AC voltage.
Vlim1 and Vlim2 are changed below.

Table 2. Over-Current Protection Voltage Detail

Soft Start	AC=100V AC=240V(PFC=OFF)		AC=240V(PFC=ON)	
	Vlim1	Vlim2	Vlim1	Vlim2
Start to 0.5ms	0.063V (12%)	0.009V (1.8%)	0.056V (11%)	0.008V (1.7%)
0.5ms to 1ms	0.125V (25%)	0.019V (3.8%)	0.113V (23%)	0.017V (3.4%)
1ms to 2ms	0.250V (50%)	0.038V (7.6%)	0.225V (45%)	0.034V (6.8%)
2ms to 4ms	0.375V (75%)	0.056V (19%)	0.338V (68%)	0.051V (10.1%)
4ms ≤	0.500V (100%)	0.75V (25%)	0.450V (90%)	0.068V (13.5%)

* (percent) is shown comparative value with Vlim1 (typ =0.5V) in normal operation.
The reason that distinguishes between AC100V and AC230V is by CS over-current protection voltage switch function which is shown in (6-3).

(6-2) LEB (Leading Edge Blanking) Function

When a MOSFET for switching is turned ON, surge current occurs because of capacitance or rush current. Therefore, when QR_CS voltage rises temporarily, the over-current limiter circuit may result to miss detections. To prevent miss detections, the IC has a built-in blanking function which masks for TLEB (typ=250ns) from switching QR_OUT pin from L to H. This blanking function enables to reduce noise filter of QR_CS pin.

(6-3) QR_CS Pin Over-Current Protection Switching Function

IC has changed PFC output voltage. When PFC output voltage changes high, ON time is short. As a result, maximum capable power increases for constant over-current limiter. For that while monitoring BR pin (ACIN detect voltage) the IC switches the over-current detection of the IC. In case of high voltage (AC230V) and PFC working, IC changes over-current comparator level to ×0.9 multiple of normal level.

(6-4) Determination of OFF Width (Turn on)

OFF width is controlled at the QR_ZT pin. When QR_OUT is Low, the power stored in the coil is supplied to the secondary-side output capacitor. When this power supply ends as there is no more current flowing to the secondary side, the drain pin voltage of switching MOSFET drops. Consequently, the voltage on the auxiliary winding also drops. A voltage that was resistance-divided by Rzt1 and Rzt2 is applied to QR_ZT pin. When this voltage level drops to VZT1 (typ=100mV) or below, MOSFET is turned ON by the ZT comparator. Since zero current status is detected at the QR_ZT pin, time constants are generated using Czt, Rzt1, and Rzt2. Additionally, a ZT trigger mask function (described in section 6-5) and a ZT timeout function (described in section 6-6) are built in IC.

In addition, the voltage on auxiliary winding becomes negative value while the switching is turned ON, When the surge voltage negative is input to the QR_ZT pin, IC may be mal-functioned. For this reason, preventing QR_ZT voltage is lower than -0.3V, Please connect a Schottky diode between the pin and GND. (Refer to Figure 15) And, when the diode flows large leak current, ZT voltage is changed, ZTOVP level has changed. For the reason, it needs to select low leakage current diode in high degree. The Schottky diode is recommended RB751CM-40, RB530VM-30, and RB751VM-40 (made by Rohm).

(6-5) ZT Trigger Mask Function

When MOSFET is switched from ON to OFF, surge noise may occur at the QR_ZT pin.
Then, the ZT comparator and ZTOVP comparator are masked for the T_{ZTMASK} time to prevent ZT comparator operation errors. (Figure 17)

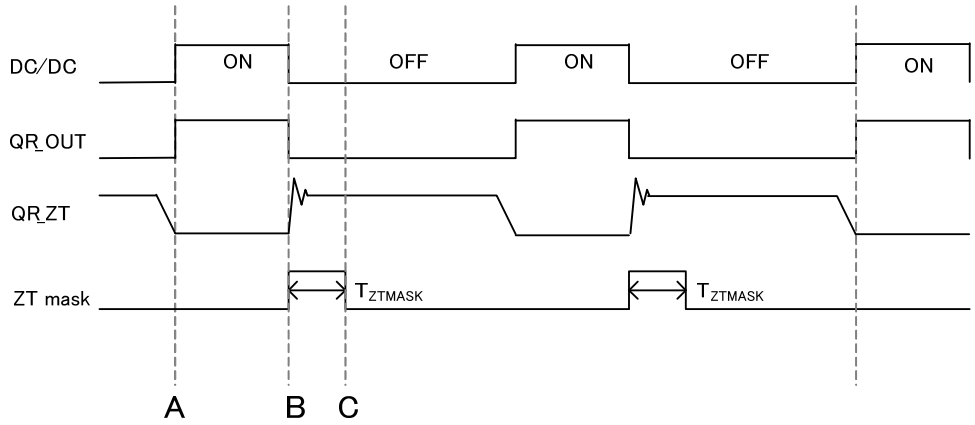


Figure 17. The Function of QR_ZT Trigger Mask.

A: DC/DC OFF => ON
B: DC/DC ON => OFF
C: Since a noise occurs to QR_ZT pin at B, IC masks ZT comparator and ZTOVP comparator detection for T_{ZTMASK} time.

(6-6) ZT Timeout Function

(6-6-1) ZT Timeout Function 1

When QR_ZT pin voltage is not higher than VZT2 (typ=200mV) for TZTOUT1 such as start or low output voltage, or QR_ ZT pin shorts to ground, IC turns on MOSFET by force. (Figure 18)

(6-6-2) ZT Timeout Function 2

After ZT comparator detects VZT1 low voltage level, when IC does not detect a following VZT1 low voltage level within TZTOUT2, IC turns on MOSFET by force. After ZT comparator detects one bottom per one pulse, the function operates. For that, it does not operate at start or at low output voltage. When IC turns on more than 2nd bottom number, IC cannot detect QR_ZT low voltage level by decreasing auxiliary winding voltage. Then, the function is operated.

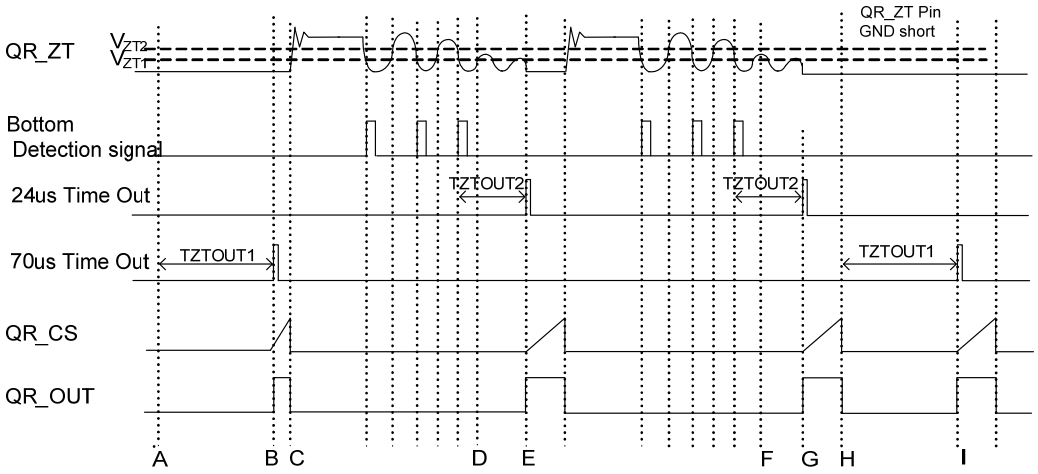


Figure 18. The Function of ZT Time Out

A: At the starting, IC starts to operate by ZT timeout function1 for QR_ZT=0V.
B: MOSFET turns ON
C: MOSFET turns OFF
D: QR_ZT voltage decreases but the IC is not turned on by the maximum frequency function. During this function operated, QR_ZT peak voltage is lower than V_{ZT2} (typ=200mV) because of a reduction of QR_ZT pin vibration. After this, the maximum frequency function is released.
E: MOSFET turns ON by ZT timeout fucntion2 after T_{ZTOUT2} (typ=24us) from D point.
F: QR_ZT voltage decreases but the IC is not turned on by the maximum frequency function. During this function operated, QR_ZT peak voltage is lower than V_{ZTOUT2} (typ=200mV) because of a reduction of QR_ZT pin vibration.
G: MOSFET turns ON by ZT timeout fucntion2 after T_{ZTOUT2} (typ=24us) from F point.
H: QR_ZT pin is short to GND.
I: MOSFET turns ON by ZT timeout function1 after T_{ZTOUT1} (typ=70us).

(6-7) Soft Start Sequence

Normally, when AC voltage is applied there is a large amount of current flow then secondary the output voltage and current overshoot. To prevent it, the IC has a built-in soft-start function. When VCC pin voltage is lower than V_{UVLO2} (typ=8.2V), IC is reset. After that, when AC voltage is applied, the IC operates soft-start. The soft start function is shown below:

start to 0.5ms	=>	Set QR_CS limiter to 12.5% of normal operation.
0.5ms to 1ms	=>	Set QR_CS limiter to 25% of normal operation.
1ms to 2ms	=>	Set QR_CS limiter to 50% of normal operation.
2ms to 4ms	=>	Set QR_CS limiter to 75% of normal operation.
4ms ≤	=>	normal operation

(6-8) QR_ZT OVP (Over Voltage Protection)

The built-in OVP function to QR_ZT pin of the IC has a protection type that is latch mode. ZTOVP corresponds to DC voltage detection and pulse detection for QR_ZT pin.

For DC detection, when the QR_ZT pin voltage is over V_{ZTL}(typ=5.0V) for T_{LATCH}(typ=100us), IC starts to detect ZTOVP function. For pulse detection, IC detects high voltage pulse of 3 count and T_{LATCH}(typ=100us) timer.

ZT OVP function operates in all states (normal state and over load state and burst state) after T_{ZTMASK}(typ=0.5us) to prevent ZT OVP from miss-detecting by surge noise,.

For pulse detection, ZT OVP operation starts detection after T_{ZTMASK} delay time from QR_OUT: H->L

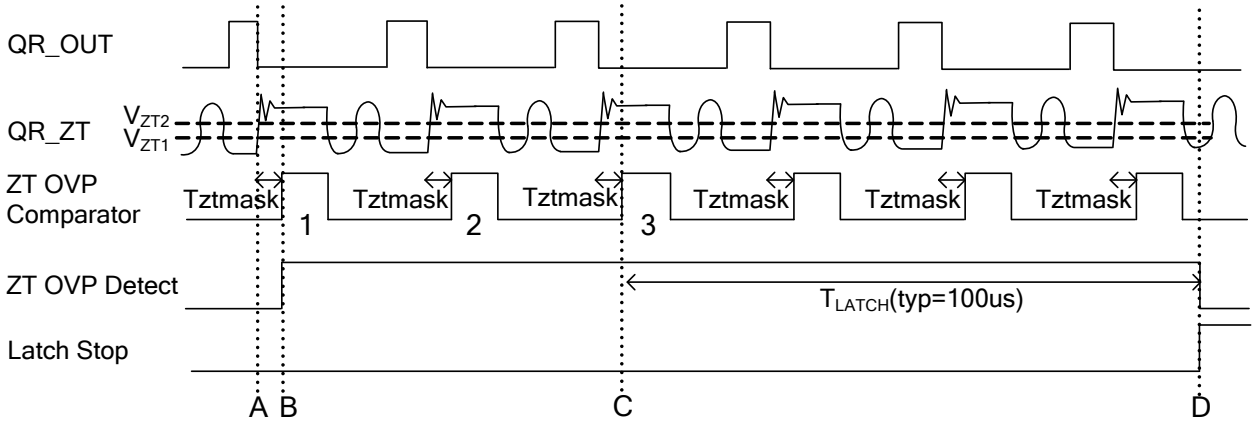


Figure 19. The Function of Latch Mask and ZT OVP

A: When QR_OUT voltage is changed from H to L, the surge occurs at QR_ZT pin. However, QR_ZT pin OVP is not detected by T_{ZTMASK} (typ=0.5us).

B: After it passes T_{ZTMASK} time (typ=0.5us) from A point, the IC detects QR_ZT pin OVP by ZT OVP comparator when QR_ZT voltage > V_{ZTL} (typ=5.0V).

C: When ZTOVP comparator counts 3 pulse, T_{LATCH} timer (typ=100us) operates.

D: When the situation of pulse or DC of QR_ZT pin voltage > VZTL (typ=5.0V) continues for T_{LATCH} timer (typ=100us) from C point, IC operates latch protection by QR_ZT OVP.

(6-9) QR_CS Open Protection

When QR_CS is OPEN, to prevent a malfunction of QR_OUT pin by a noise, the IC has built-in QR-CS pin open protection circuit. When QR_CS is open, QR_OUT switching is stopped by the function. (Auto-recovery protection.)

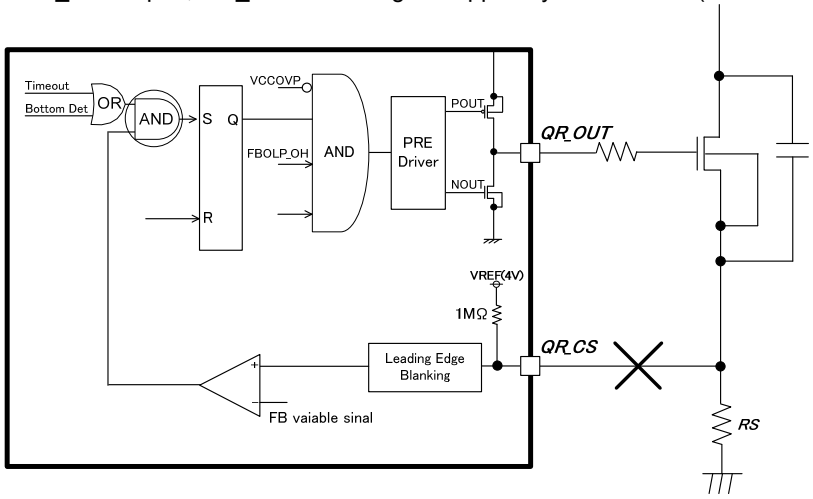


Figure 20. QR_CS Open Protection Circuit.

(6-10) OUTPUT over Load Protection (FB OLP Comparator)

Over load protection is the function that monitors the load state of secondary output by QR_FB pin, and fixes QR_OUT pin on L. In over load status, photo-coupler has no current flow and QR_FB pin rise, over load protection is detected. If the condition continues for T_{FOLP} (typ=128ms), IC judges it is over load state, and QR_OUT pin and P_OUT pin is fixed to L. After QR_FB voltage is over V_{FOLP1A} (typ=2.8V), if QR_FB voltage is lower than V_{FOLP1B} (typ=2.6V) within T_{FOLP} (typ=128ms), over load protection timer is reset.

Because QR_FB is pull-up by a resistor to internal voltage , QR_FB voltage starts to operate in the state which is more than V_{FOLP1A} (typ=2.8V) in starting. For that, please set the stable time of secondary output voltage within T_{FOLP} (typ=128ms) from the starting. After detecting over load, IC is stopped for T_{OLPST} (typ =2048ms), and it is on auto-recovery operation. At this moment, the IC operates a soft start. In stopping switching, though VCC voltage decreases, the IC keeps the condition VCC pin voltage > V_{UVLO2} because VCC recharging function charges VCC voltage from the starting circuit.

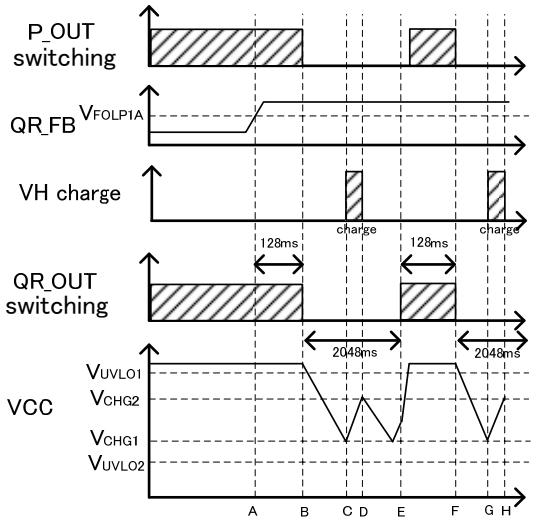


Figure 21. Auto Restart Operation by Over Load Protection.

A: Because of QR_FB > V_{FOLP1A}, FBOLP comparator detects over load.
B: When the state of A continues for T_{FOLP} (typ=128ms), the IC stops switching by over load protection.
C: During stopping switching by over load protection, VCC voltage drops. When VCC voltage is lower than V_{CHG1}, VCC re-charge function operates, and VCC voltage rises.
D: When VCC voltage is higher than V_{CHG2} by re-charge function, VCC recharge function is stopped.
E: It takes for T_{OLPST} (typ=2048ms) from B point until IC starts switching with soft-start.
F: While over load state continues, QR_FB voltage is over V_{FOLP1A}. When it passes for T_{FOLP} (typ=128ms) from E,IC stops switching.
G: During stopping switching, VCC voltage drops. When VCC voltage becomes lower than V_{CHG1}, VCC re-charge function operates and VCC voltage rises.
H: When VCC voltage is higher than V_{CHG2} by re-charge function, VCC recharge function is stopped.

(6-11) QR_OUT Pin Voltage Clamp Function

For the purpose of protecting the external MOSFET, H level of QR_OUT is clamped to V_{OUTH} (typ=12.5V)
It prevents gate destruction of MOSFET by rising VCC voltage. (refer to Figure 22)

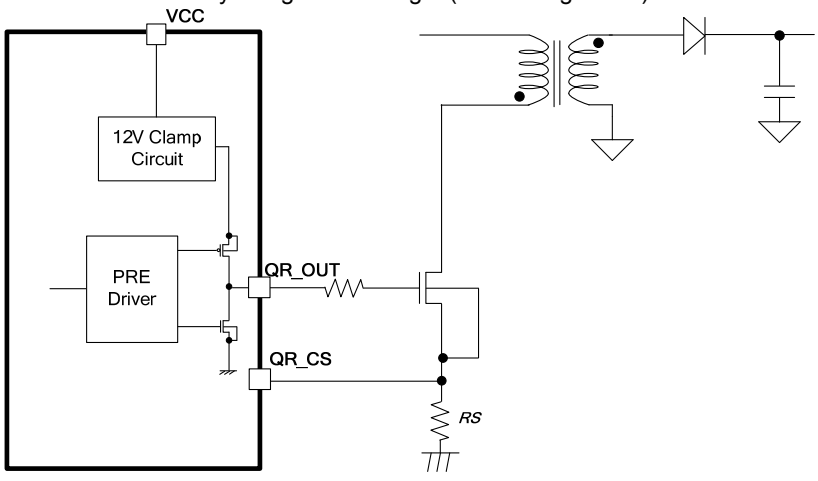


Figure 22. The Simple Circuit of QR_OUT Pin.

(7) Power Factor Correction (PFC: Power Factor Correction) Part

The Power Factor Correction Circuit is a voltage control method with the PFM boundary conduction mode. Because of this mode, ON width is fixed for a load. The operation circuit is shown is Figure 23 and Timing chart is shown in Figure 24.

Switching Operation

(1) Inductor current (I_L) increases after MOSFET changes to ON.
(2) When Vramp voltage becomes higher by comparing with the slope set by P_RT pin, MOSFET turns OFF.
(3) MOSFET is set to be ON after P_IS pin detects at the zero point.

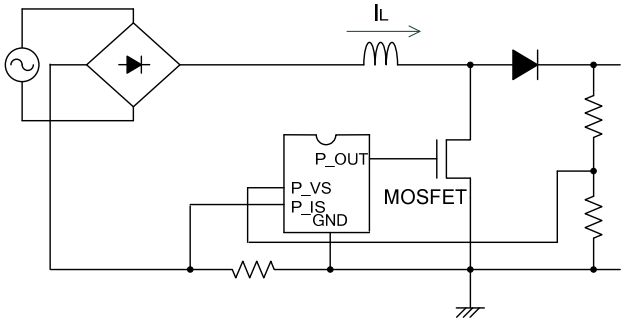


Figure 23. The Operation Circuit of PFC.

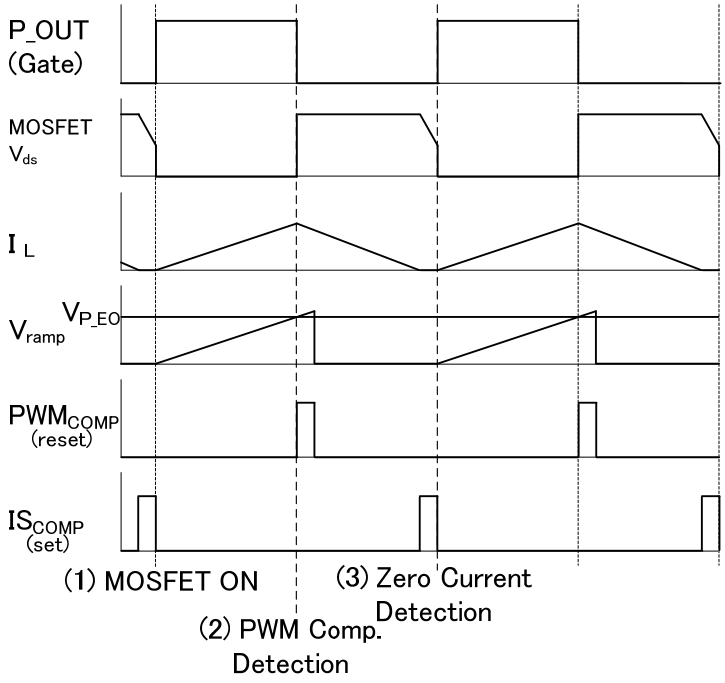


Figure 24. The Switching Timing Chart.

ON width is determined by Vramp voltage and VP_EO pin voltage which controlled by loads. Vramp waveform is generated in the inside of the IC. Using this ON width fixing operation, peak current is decided by the below formula.

IL = Vac × Ton/L1 (IL: coil current, Vac: input voltage, ton: ON width, L1: PFC inductance)

In case of constant loads, IL is determined according to the value of Vac because Ton and L1 are a fixing value. As a result, there is no phase difference between AC current and AC voltage, and a higher harmonic wave becomes smaller. Zero current detection operates with a negative voltage at P_IS pin. The current flowing in sense resistor is detected by voltage.

If currents except for PFC loop flow to this resistor by the pattern of application board, the operation becomes an unstable condition because it can't detect current accurately. For that, please pay attention to the pattern of boards making application boards.

(7-1) gmAMP

P_VS pin monitors a voltage divided resistors of PFC output voltage. P_VS voltage has the piled up ripple voltage of AC frequency (50Hz/60Hz).
The gmAMP filters this ripple voltage and controls the voltage level of P_EO, by responding to error of P_VS pin voltage and internal reference voltage V_{P_VSAMPH} / V_{P_VSAMPL} (typ=2.5V/1.625V).
Please remove the ripple of AC frequency by an error amp which is configured by P_EO pin shown in figure 25.
Gm constant is designed 44uA / V.

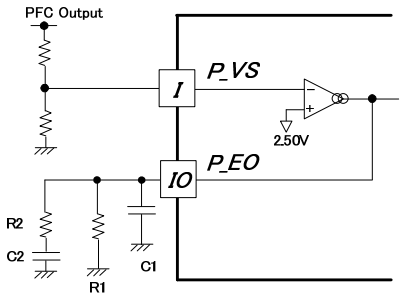


Figure 25. The Block Diagram of gmAMP.

PFC works switching operation within the P_EO voltage range from about 0.8V to 3.0V. As P_EO pin voltage rises, the ON width of P_OUT pin becomes longer. And when it becomes lower than about 0.8V, the switching operation is stopped. For that, as P_EO pin is shorted to GND forcibly by the exterior, it enables to stop the PFC operation.
The transfer function of an error amp is shown below.

$$G = \frac{Vout}{Vin} = gm \times Z = gm \times \frac{1}{\frac{1}{Rout} + \frac{1}{R1} + \frac{1}{R2 + \frac{1}{j\omega C2}} + j\omega C1}$$

(In this formula, Rout means an output impedance of an amp.)
In the case of attaching R1, P_EO voltage is clamped by the voltage which is multiplied by gm amplifier current and R1
If R1 is attached, R1 should be higher than 1MΩ. Basically, it is recommended that R1 is not attached.
Figure 26 shows this specific characteristic.

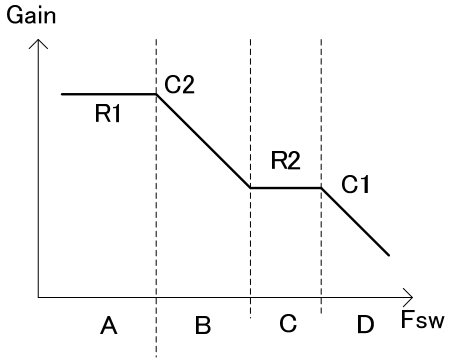


Figure 26. gmAMP specific characteristic of frequency

According to the transfer function and Figure 26,
If you want the gain of A area to rise, please raise R1.
If you want pole between A to B to lower, please raise C2
If you want the gain of C area to rise, please raise R2.
If you want pole between C to D to lower, please raise C1

The whole of the transfer function as PFC determined by not only error amp but also IC peculiar gain, LC resonance, and the voltage dividing resistor of PFC output. Please set the invariable of the error amp and regulate the AC frequency in order it not to appear at P_EO pin. And it is necessary to check in real applications.

(7-2) P_VS Short Protection

The PFC built-in short protection function at P_VS works by stopping switching at P_OUT when P_VS voltage < V_{P_SHORTH} / V_{P_SHORTL} (typ:0.3V/0.195V: -92% voltage of PFC output). The operation is shown is Figure 27.

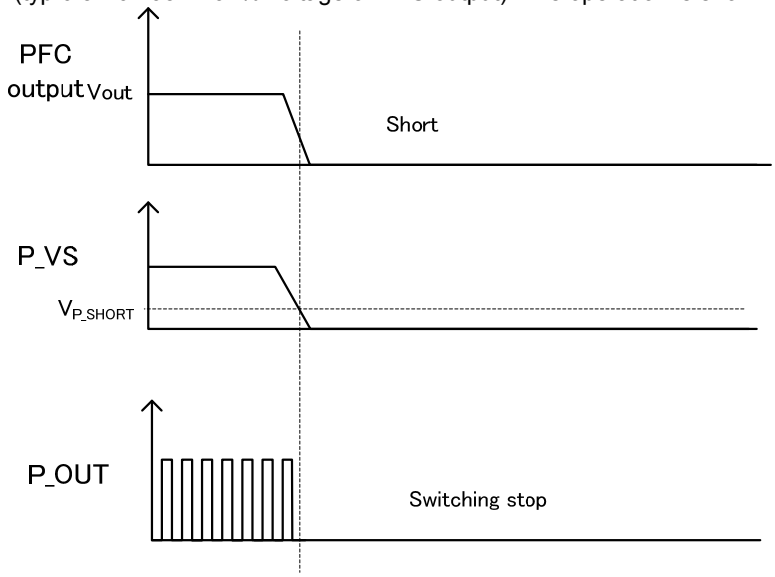


Figure 27. The Short Protection of P_VS Terminal

(7-3) Gain Boost Function in P_VS low Voltage

When the output voltage lowers by occurring sudden load changes, the tarn of a lowing output voltage becomes longer because of the slow voltage control loop. Therefore, when P_VS pin voltage lowers to V_{PGUP1} / V_{PGUP2} (typ=2.25V/1.462V), it is suitable for -10% of output voltage, and the IC speeds up the voltage control loop. In the operation, ON width at P_OUT pin increases, and PFC prevents output voltage from dropping for a long time. This operation is stopped when P_VS pin voltage is higher than V_{PGUP1} /V_{PGUP2} (typ=2.25V/1.462V).

(7-4) Gain Decrease Function in P_VS over Voltage (Dynamic OVP)

In case the output voltage rises by starting up or sudden output load changes, as PFC voltage response is slow, output voltage is high for a long time. Therefore, IC speeds up voltage control loop gain by P_VS first voltage protection function when P_VS pin voltage is higher than V_{P_OVP1H}/ V_{P_OVP1L}typ=2.625V/1.706V), it is suitable for +5% of the output voltage. In this operation, ON width at P_OUT pin decreases, IC prevents output voltage from rising for a long time. This operation is stopped when P_VS pin voltage is lower than $V_{P\_OVP1\ H}$/ V_{P_OVP1L} (typ=2.625V/1.706V).

(7-5) P_VS over Voltage Protection Function (Static OVP)

The IC has a second over voltage protection, for the case that P_VS voltage exceeds over the first over voltage protection voltage V_{P_OVP1H}/V_{P_OVP1L}. P_VS pin voltage is exceeded V_{P_OVP2H} / V_{P_OVP2L} (typ=2.725V/1.771V), PFC switching is stopped instantly. When P_VS pin voltage decrease lower than V_{P_OVP3H} / V_{P_OVP3L} (typ=2.625V / 1.706V), switching operation is re-start. Refer to Figure 28.

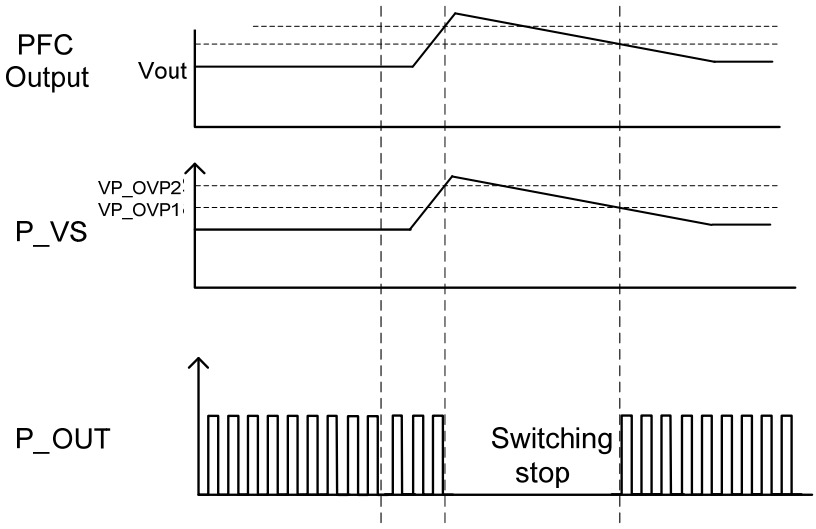


Figure 28. P_VS Over Voltage Protection (Auto Restart Mode).

(7-6) P_OVP Terminal over Voltage Protection Function

P_OVP pin is an over voltage protection function which is available in the case that the output of PFC rises more than P_VS over voltage protection function V_{P_OVP2} under an abnormal condition or is made latch. (Refer to Figure 29) This function makes it possible to protect PFC by double putting together with P_VS over voltage protection function.

The IC stops switching operation (latch mode) after timer (typ=200us), if P_OVP increases more than V_{POVP4} (typ=2.5V). By the internal timer, the IC avoids detection error. The operation is shown is Figure 30.

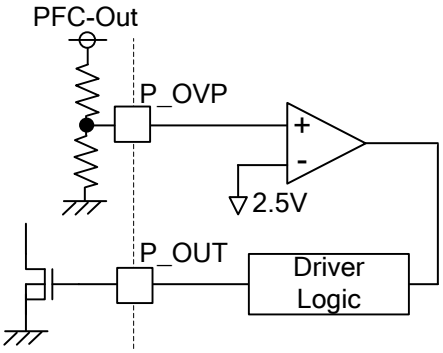


Figure 29. The Protection of P_POVP (Latch mode).

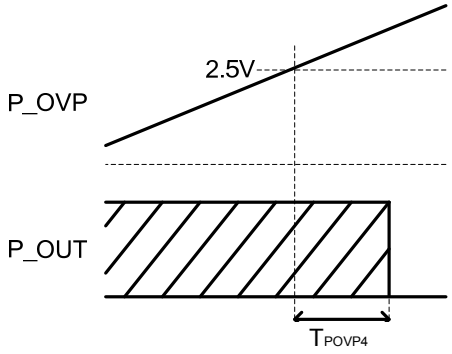


Figure 30. Timing Chart

(7-7) P_IS Pin: Zero Current Detection and Over-Current Detection Function

Zero current detection circuit is the function that detects zero cross of PFC inductor current (IL). (Shown in Figure32) The voltage of P_IS pin becomes more than the voltage of zero current detection and P_OUT output turn ON after it is passes for Delay time.

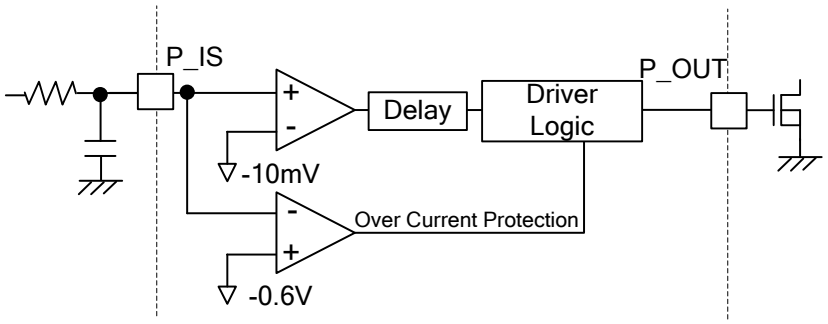


Figure 31. Current Detection Circuit of P_IS Terminal

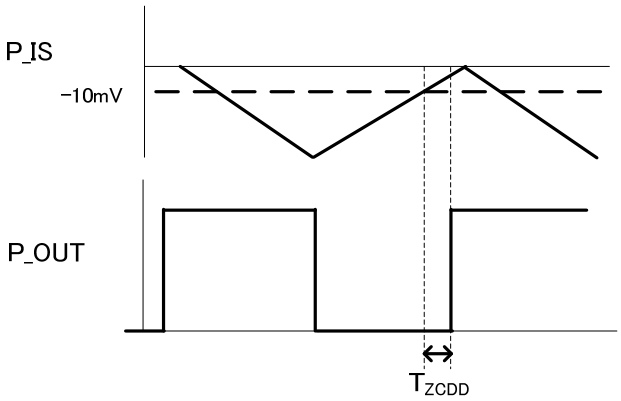


Figure 32. P_IS Zero Current Detection Delay Time

(7-8) P_IS pin over current detection protection function

In normal operation, turn OFF of PFC is controlled by the ON width determined by P_EO pin voltage. However, it turns OFF with pulse- by-pulse by operating over current protection when P_IS pin becomes lower than the voltage (IS over current detection voltage) V_{IS_OCP} (typ=-0.6V). This protection prevents the IC from flowing over current to MOSFET.

This function controls the ON width, so PFC voltage falls if it operates. Please decide the sense resistor of PFC within the range of AC voltage specification in order the function not to operate in normal operation. The level of over current detection protection detects AC voltage, and the level is switching.

(7-9)P_RT pin setting

This pin sets the maximum frequency by external resistor which generated in the interior of the IC.
By P_RT resistor value, maximum frequency, maximum ON width, and P_IS delay time are set. They are shown in Figure 33-35. The maximum ON width for minimum AC voltage is calculated by the following expression on application.
The maximum ON width set by P_RT resistance is shown in Figure-33

$$T_{MAXON}[s] = \frac{2 \times L \times P_O}{V_{ACMin}{}^2 \times \eta}$$

VAC Min: Minimum input power, L: Inductor, Po: Max output power (W), Efficiency η

The maximum ON width which set in Figure 31 needs to set more than T_{MAXON} width which shows above.
In order to improve the efficiency in a light load, the frequency rising in a light load is limited to set value at P_RT pin, by the maximum frequency of Figure 32.
Furthermore, Delay time from the comparator for zero cross detection V_{ZCD} (typ=-10mV) can be set in P_RT pin.
(Refer to Figure 33)
The IC can't operate in more 500kHz than maximum frequency because it has a peculiar delay time, external MOSFET delay and delay time of drive circuit even if P_RT resistor is attached less than 39kΩ..

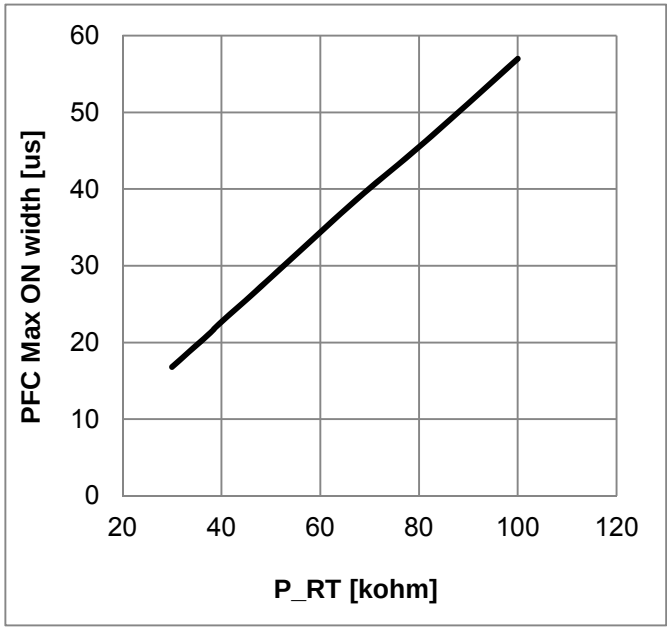


Figure 33. The Relationship of RT and Operation Frequency*

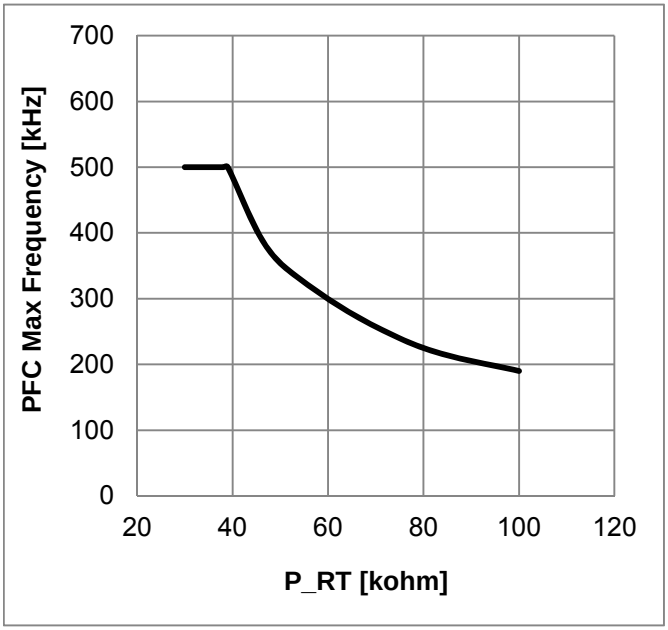


Figure 34. The Relationship of RT and ON Width*

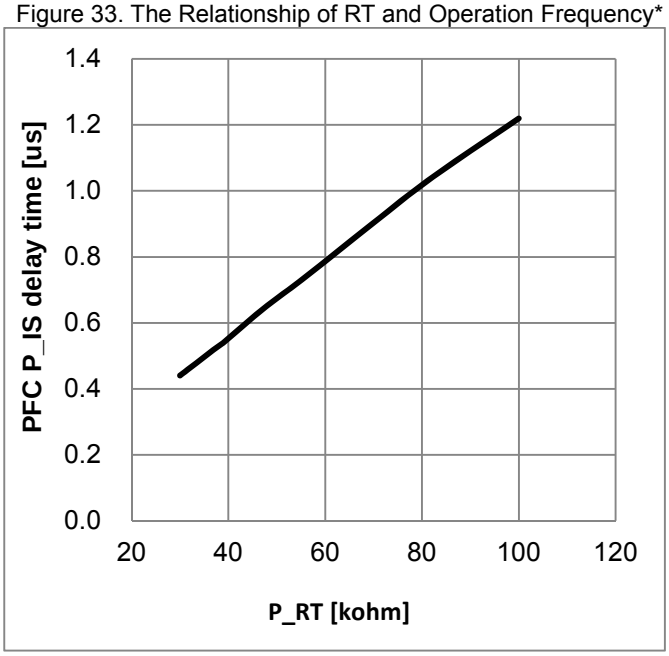


Figure 35. The Relationship of RT and PFC Zero Current Detection Delay*

*The above chart is for reference only. After confirmation of the actual device, please set the constant.

(7-10) PFC ON/OFF setting function

This is a function that stops PFC switching operation in a light load, and improve the efficiency of the whole of systems. PFC ON/OFF power is detected by a current limiter level of QR_CS pin (CS detection). (It is CS detect shown in Figure 38.)

CS detect = QR_FB voltage / AV_{CS1}

In application design, QR_FB voltage is needed to set to the power which hopes PFC ON/OFF. The POFFSET voltage is calculated by QR_FB voltage /4. It is set by POFFSET resistor that POFFSET voltage corresponds to the value.

With comparing the current limiter voltage with the voltage set POFFSET pin, PFC ON/OFF electric power is set. The relation of CS detection and QR_FB is shown in below. To set POFFSET voltage within the range of this CS detection enables the IC to operate PFC ON/OFF.

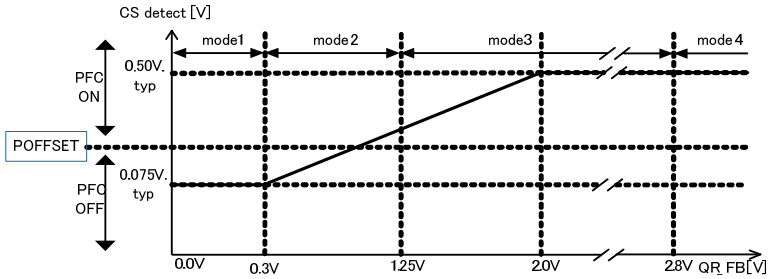


Figure 36. Relation of CS detection voltage –QR_FB voltage

The relation of CS detection voltage and output voltage is shown in below.

Output electric power: $Po=1/2\times Lp\times Ip^2\times Fsw\times\eta=1/2\times Lp\times (V_{CS}/Rs)^2\times F_{SW}\times\eta$

(Lp: QR primary side inductance, V_{CS}: over current detection voltage, Rs: sense resistor, Fsw: Switching frequency, η: efficiency)

VCS = CS detection + Vpfc × Tondelay Lp*Rs (Vpfc: input voltage of QR)

The CS detection voltage is detected PFC ON/OFF.

According to this formula the graph of the relation is shown in Figure 37.

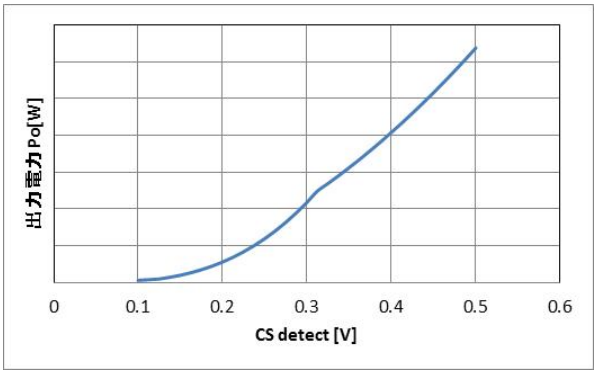


Figure 37. Relation of output electric power - CS detection

IC operates PFC ON/OFF comparing CS detect with POFFSET pin voltage. As a load increases in PFC OFF state, CS detect voltage increases. CS detect voltage increases than fixed POFFSET voltage for T_{PFCON}(typ=4ms), PFC turns from OFF to ON. While, as a load decreases in PFC ON state, CS detect voltage decreases. PFC turns OFF when the CS detect voltage lowers than the fixed POFFSET voltage.

It is expressed in electric specification that the P_OFFSET voltage turns PFC from ON to OFF in QR_CS = 0.15V (DC). It is regulated in P_OFFSET current in order to reduce the power varying of PFC ON/OFF($V_{\_OFSON}$, $V_{\_OFSOFF}$) by decreasing the difference between CS detection voltage and P_OFFSET voltage. So that, there is a large varying in POFFSET current, but it is designed that the varying of CS detection voltage and P_OFFFSET become to be small.

P_OFFSET pin current is determined below.

PFC OFF : ACIN=L => PFC current is $I_{\_OFFSET4}$(typ=5.5uA)
: ACIN=H => PFC current is $I_{\_OFFSET3}$(typ=5.0uA)
PFC ON : ACIN=L => PFC current is $I_{\_OFFSET2}$(typ=4.5uA)
: ACIN=H => PFC current is $I_{\_OFFSET1}$(typ=4.0uA)

For the current, PFC ON/OFF is needed to adjust POFFSET pin resistor.
To compensate PFC ON/OFF power variation by AC voltage, PFCOFF current is changed in ACIN=H/L.
An operation circuit diagrams shown in Figure 38, a resources operation circuit diagram is shown in Figure39, and a switching operation is shown in Figure 40.

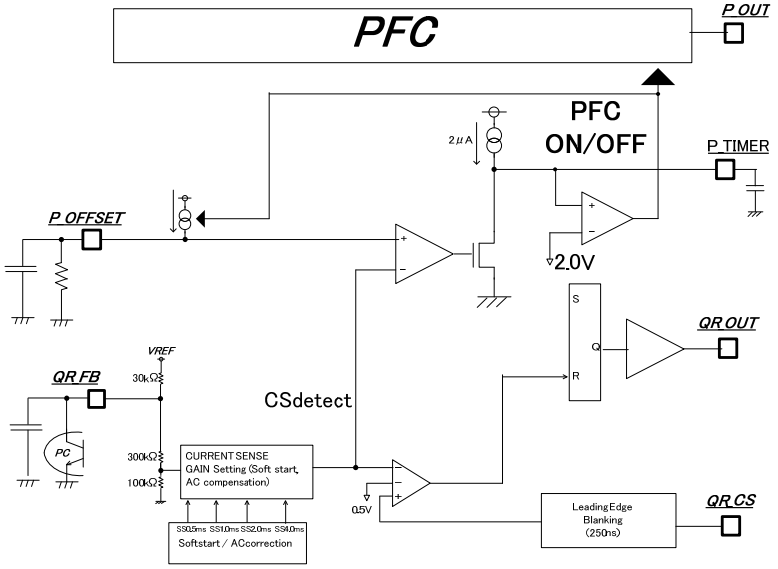


Figure 38. PFC ON/OFF operation circuit diagrams

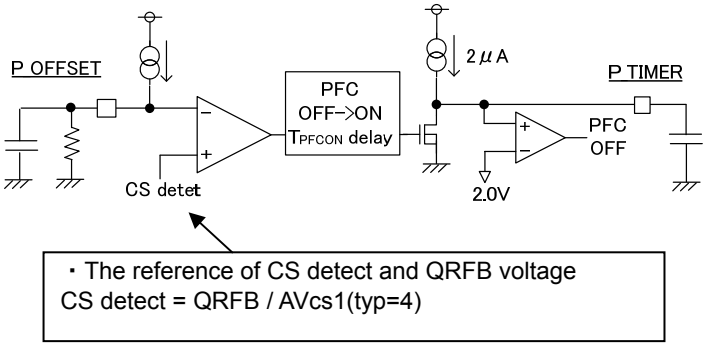


Figure 39. Resources Operation Circuit

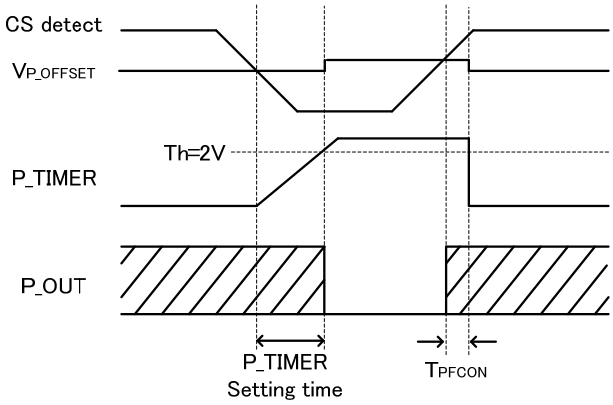


Figure 40. Timing Chart

Because CS detect voltage shown in Figure-39 is generated by QR_FB voltage. When QRFB voltage ripple is large, PFC ON/OFF may not be at target point because CS detect voltage is also piled up ripple. In this case, please regulate output capacitors or capacitors of QR_FB pin and so on.

P_TIMER pin is setting time pin which sets the time of detecting output electric power decline (CS limit voltage decline) to stopping PFC (PFC: ON to OFF). In order not to switch PFC by changing loads in such a case of pulse loads, please coordinate the time by this pin.

If the QR loads become to be light, peak current of QR is lower. Thus, if the voltage of CS limit lowers than DC voltage setting at P_OFFSET pin, the IC starts to charge to external capacity of P_TIMER pin. P_TIMER pin voltage rises, and PFC is stopped at the moment of exceeding the P_TIMER detection voltage (typ=2.0V).

To stabilize the P_OFFSET voltage, a capacitor 0.1uF is recommended at P_OFFSET pin.

When it wants to decrease PFC OFF power setting, it needs to decrease P_OFFSET resistor. Then, IC may be burst operation. When IC operates in burst operation, it needs to fit P_TIMER capacitor value because PFC ON/OFF is decided by burst frequency and P_TIMER setting time. And, please confirm operation in an actual application when setting.

And if you want PFC to continue operation without PFC=OFF function, please connect P_OFFSET pin and P_TIMER pin to GND. And if PFC is operated in a light load condition, there is a possibility that a current supply from an auxiliary winding fails. In

that case, please pay attention to VCC decreasing, and PFC and QR are stopping.
Furthermore, when it is set PFC ON/OFF by using external photo-coupler without using PFC ON/OFF function, set in below circuit.

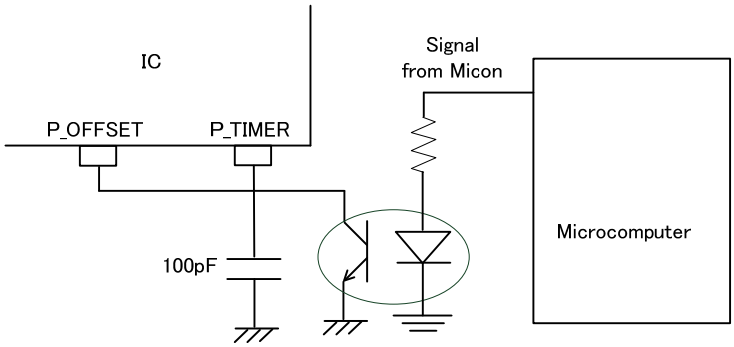


Figure 41. External PFC ON/OFF circuit

Operation Mode of Protection Circuit

Operation mode of protection functions are shown in Table 3.

Table 3. Operation Mode of Protection Circuit.

Item	Comments	Operation Mode			
		Detection Method	Operation At Detection	Release Method	Operation At Release
VCCUVLO	VCC Pin Low Voltage Protection	VCC<8.2V (VCC Falling)	PFC Part, DC/DC Part STOP	VCC>13.5V (VCC Rising)	PFC Part, DC/DC Part Start Up Operation
VCCOVP	VCC Pin Over Voltage Protection	VCC>27.5V During 100us (VCC Rising)	PFC Part, DC/DC Part Latch STOP	VCC<6.2V (VCC Falling)	PFC Part, DC/DC Part Latch released
Brown Out	Input AC Voltage Low Voltage Protection	BR＜1.0V During 256ms (BR Falling)	PFC Part and QR Part STOP, X-Cap Discharging	BR>1.0V (BR Rising)	Normal Operation
COMP	COMP Pin Protection	COMP<0.5V During 150us (COMP Falling)	PFC Part, DC/DC Part Latch Stop	VCC<6.2V (VCC Falling)	PFC Part, DC/DC Part Latch released
QR_FB_OLP	QR_FB Pin Over-Current Protection	QR_FB>2.8V During 128ms (QR_FB Rising)	DC/DC ,PFC Parts STOP	QR_FB<2.6V During 2048ms (QR_FB Falling)	Normal Operation
QR_ZT OVP	QR_ZT Pin Over Voltage Protection	QR_ZT>5.0V During 100us (QR_QR_ZT Rising)	DC/DC, PFC Parts Latch Stop	VCC<6.2V (VCC Falling)	PFC Part, DC/DC Part Latch released
P_IS OCP	P_IS Pin Short Protection	P_IS<-0.60V (P_IS Falling)	PFC Part Output STOP	Pulse by Pulse	Normal Operation
P_VS Short Protection 1(2)	P_VS Pin Short Protection	P_VS<0.300V(0.195V) (P_VS Falling)	PFC Part Operation STOP	P_VS>0.300V(0.195V) (P_VS Rising)	Normal Operation
P_VS Gain rise voltage1(2)	P_VS Pin Low Voltage Gain Boost Function	P_VS<2.250V(1.462V) (P_VS Falling)	Gm-Amp. GAIN Boost	P_VS>2.250V(1.462V) (P_VS Rising)	Normal Operation
P_VS Gain fall voltage1(2)	P_VS Pin Dynamic Over Voltage Protection	P_VS>2.625V(1.706V) (P_VS Rising)	Gm-Amp. GAIN Down	P_VS<2.625V(1.706V) (P_VS Falling)	Normal Operation
P_VS over voltage protection1(2)	P_VS Pin Static Over Voltage Protection	P_VS>2.725V(1.771V) (P_VS Rising)	PFC Part STOP	P_VS<2.603V(1.692V) (P_VS Falling)	Normal Operation
P_OVP OVP	P_OVP Pin Over Voltage Protection	P_OVP>2.5V (P_VS Rising)	PFC Part, DC/DC Part Latch Stop	VCC<6.2V (VCC Falling)	PFC Part, DC/DC Part Latch released

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{max1}	-0.3 to +30.0	V	VCC
Maximum Applied Voltage 2	V_{max2}	-0.3 to +650	V	VH_IN
Maximum Applied Voltage 3	V_{max3}	-0.3 to +15.0	V	P_OUT, QR_OUT
Maximum Applied Voltage 4	V_{max4}	-0.3 to +6.5	V	QR_FB, COMP, P_EO, BR, P_RT, P_OFFSET, P_OVP, P_VS, QR_CS, P_TIMER
Maximum Applied Voltage 5	V_{max5}	-0.3 to +7.0	V	QR_ZT
Maximum Applied Voltage 6	V_{max6}	-6.5 to +0.3	V	P_IS
P_OUT Pin Output Peak Current 1	I_{P_OUT1}	-0.5	A	source
P_OUT Pin Output Peak Current 2	I_{P_OUT2}	+1.0	A	sink
QR_OUT Pin Output Peak Current 1	I_{QR_OUT1}	-0.5	A	source
QR_OUT Pin Output Peak Current 2	I_{QR_OUT2}	+1.0	A	sink
Allowable Dissipation	P_d	0.68 (Note1)	W	mounted
Operating Temperature Range	T_{opr}	-40 to +105	°C	
Storage Temperature Range	T_{str}	-55 to +150	°C	

(Note1) Derate by 5.5 mW/°C when operating above Ta = 25°C when mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Power supply voltage range 1	V_{CC}	8.9 to 26.0	V	VCC Pin Voltage
Power supply voltage range 2	V_H	80 to 600	V	VH_IN Pin Voltage

Recommended External Parts (Ta = 25°C)

Parameter	Symbol	Rating	Unit
VCC Pin Capacitor	C_{VCC}	22.0～	μF
BR Pin Capacitor	C_{BR}	0.1 to 10	nF
P_OFFSET Pin Capacitor	C_{P_OFFSET}	0.1～	μF
COMP Pin Capacitor	C_{COMP}	to 0.01	μF
QR_ZT pin diode	D_{ZTD}	Schottkey diode	-

Electrical Characteristics (Unless otherwise noted, Ta=25°C, VCC=15V)

Parameter	Symbol	Specifications			Unit	Conditions
		Min	Typ	Max		
[Circuit Current]						
Circuit current (ON) 1	I_{ON1}	-	1.0	1.4	mA	PFC=OFF QR_FB=2.0V (During Pulse Operation)
Circuit current (ON) 2	I_{ON2}	-	1.2	1.7	mA	PFC=ON QR_FB=2.0V (During Pulse Operation)
Circuit current (ON) 3	I_{ON3}	-	600	780	μA	PFC=OFF FB=0.0V (During Burst Operation)
[Start-Up Circuit Block]						
Start current 1	I_{START1}	0.55	0.85	1.15	mA	VCC= 0V
Start current 2	I_{START2}	4.5	6.5	8.5	mA	VCC=10V
OFF Current	I_{START3}	-	8	16	μA	Input Current from VH _IN Terminal after Releasing UVLO
VH voltage switched start current	V_{SC}	0.8	1.5	2.1	V	
VH_IN minimum operation voltage	VHACT	30	-	-	V	VHIN start to flow
[VCC Pin Protection Function]						
VCC UVLO voltage1	V_{UVLO1}	12.5	13.5	14.5	V	VCC Rise
VCC UVLO voltage 2	V_{UVLO2}	7.5	8.2	8.9	V	VCC Drop
VCC UVLO hysteresis	V_{UVLO3}	-	5.3	-	V	V_{UVLO3} =V_{UVLO1} -V_{UVLO2}
VCC charge start voltage	V_{CHG1}	8.5	9.5	10.5	V	Start Circuit Operation Voltage
VCC charge end voltage	V_{CHG2}	9.5	10.5	11.5	V	Stop Voltage from V_{CHG1}
VCC OVP voltage	V_{OVP}	26.0	27.5	29.0	V	VCC Rise
[BR Pin (7pin)]						
BR detect voltage1	V_{BR1}	0.92	1.00	1.08	V	BR Rise
BR detect voltage 2	V_{BR2}	-	0.70	-	V	BR Fall
BR hysteresis	V_{BRHYS}	-	0.30	-	V	
BR timer	$T_{BRTIMER}$	204	256	307	ms	PFC, DCDC Stop, Discharge Start
ACIN switched voltage	V_{ACIN1}	2.3	2.5	2.7	V	ACIN switched BR peak voltage
[COMP Pin (5pin)]						
COMP pin detect voltage	V_{COMP}	0.37	0.50	0.63	V	
COMP pin pull-up resistor	R_{COMP}	19.4	25.9	32.3	kΩ	
Thermistor resistor detection value	R_T	3.32	3.70	4.08	kΩ	
Latch release voltage (VCC pin voltage)	V_{LATCH}	-	V_{UVLO2} – 2.00	-	V	
COMP Latch mask time	T_{COMP}	75	150	240	μs	

Electrical Characteristics – continued (Unless otherwise noted, Ta=25, VCC=15V)

Parameter	Symbol	Specifications			Unit	Conditions
		Min	Typ	Max		
[P_OFFSET block]						
P_OFFSET source current 1	$I_{OFFSET1}$	2.0	4.0	6.0	μA	At PFC ON ACIN=H
P_OFFSET source current 2	$I_{OFFSET2}$	2.5	4.5	7.0	μA	At PFC ON ACIN=L
P_OFFSET source current 3	$I_{OFFSET3}$	2.5	5.0	10.0	μA	At PFC OFF ACIN=H
P_OFFSET source current 4	$I_{OFFSET4}$	2.7	5.5	11.0	μA	At PFC OFF ACIN=L
P_OFFSET voltage At PFC OFF	V_{OFSON}	0.135	0.15	0.165	V	QR_CS=0.15V(DC) PFC OFF => ON Switched voltage
P_OFFSET voltage At PFC ON	V_{OFSOFF}	0.135	0.15	0.165	V	QR_CS=0.15V(DC) PFC ON => OFF Switched voltage
Delay time at PFC ON	TPFCON	2.60	4.00	5.40	ms	PFC ON delay time
[P_TIMER Pin]						
P_TIMER source current	I_{PTIMER}	1.8	2.0	2.2	μA	
P_TIMER detection voltage	V_{P_TIMER}	1.9	2.0	2.1	V	P_TIMER Rise
[PFC Part Gm Amplifier Block]						
P_VS pin pull-up current	I_{P_VS}	-	0.5	-	μA	
Gm Amp. normal voltage 1	V_{P_VSAMPH}	2.44	2.50	2.56	V	
Gm Amp. normal voltage 2	V_{P_VSAMPL}	1.544	1.625	1.706	V	
Gm Amp. trans conductance	T_{P_VS}	30.8	44.0	59.2	μA/V	
Maximum Gm amplifier source current	IP_EOsource	15	25	35	μA	P_VS=1.0V
Maximum Gm amplifier sink current	IP_EOsink	24	40	56	μA	P_VS=3.5V
[PFC Part OSC Block]						
Maximum ON width	T_{MAXON}	28	32	36	us	RT=56kΩ
Maximum oscillation frequency	FP_{MAX}	256	320	384	kHz	RT=56kΩ
[PFC Part P_IS Block]						
Zero current detection voltage	V_{ZCD}	-15	-10	-5	mV	
Zero current detection voltage Delay	T_{ZCDD}	0.4	0.8	1.2	μs	
IS over-current detection voltage	V_{IS_OCP}	-0.625	-0.600	-0.575	V	
[PFC Part protection Block]	**Figure of (%) is the ratio of VS standard voltage (1: 2.5V, 2:1.625V).**					
P_VS short protection voltage1	$V_{P\ SHORTH}$	0.200 (-92%)	0.300 (-88%)	0.400 (-84%)	V	ACIN=H
P_VS short protection voltage2	$V_{P\ SHORTL}$	0.130 (-92%)	0.195 (-88%)	0.260 (-84%)	V	ACIN=L
P_VS gain rise voltage1	V_{PGUP1}	2.050 (-18%)	2. 250 (-10%)	2.450 (-2%)	V	ACIN=H
P_VS gain rise voltage2	V_{PGUP2}	1.332 (-18%)	1.462 (-10%)	1.593 (-2%)	V	ACIN=L
P_VS gain fall voltage 1	$V_{P\ OVP1H}$	-	2.625 (+5%)	-	V	ACIN=H
P_VS gain fall voltage 2	$V_{P\ OVP1L}$	-	1.706 (+5%)	-	V	ACIN=L
P_VS over voltage protection detection voltage1	$V_{P\ OVP2H}$	-	2.725 (+9%)	-	V	ACIN=H
P_VS over voltage protection detection voltage2	$V_{P\ OVP2L}$	-	1.771 (+9%)	-	V	ACIN=L
P_VS over voltage protection release voltage1	$V_{P\ OVP3H}$	-	2.603 (+5%)	-	V	ACIN=H
P_VS over voltage protection release voltage2	$V_{P\ OVP3L}$	-	1.692 (+5%)	-	V	ACIN=L

* Definition of ACIN (L: BR Pin Voltage < 2.5V, H: BR Pin Voltage > 2.5V)

Electrical Characteristics – continued (Unless otherwise noted, Ta=25, VCC=15V)

Parameter	Symbol	Specifications			Unit	Conditions
		Min	Typ	Max		
[PFC Part OVP Block]						
PFC OVP pin detection voltage	V_{POVP4}	2.43	2.50	2.57	V	
PFC OVP pin detection timer	T_{POVP4}	100	200	350	us	
[PFC Part OUT Block]						
P_OUT pin H voltage	V_{POUTH}	10.5	12.5	14.5	V	IO = -20mA
P_OUT pin L voltage	V_{POUTL}	-	-	1.00	V	IO = +20mA
P_OUT pin pull down resistor	R_{PDOUT}	75	100	125	kΩ	
[DC/DC Convertor Block (Turn Off)]						
FB pin pull-up resistor	R_{FB}	22.5	30.0	37.5	kΩ	
CS over-current detect voltage 1A	V_{lim1A}	0.475	0.500	0.525	V	FB=2.2V (ACIN=L)
CS over-current detect voltage 1B	V_{lim1B}	0.410	0.450	0.490	V	FB=2.2V (ACIN＝H)
CS over-current detect voltage 2A	V_{lim2A}	0.150	0.200	0.250	V	FB=0.8V (ACIN＝L)
CS over-current detect voltage 2B	V_{lim2B}	0.130	0.180	0.230	V	FB=0.8V (ACIN＝H)
Voltage gain 1 (⊿VFB/⊿VCS)	AV_{CS1}	3.40	4.00	4.60	V/V	ACIN=L
Voltage gain 2 (⊿VFB/⊿VCS)	AV_{CS2}	3.77	4.44	5.11	V/V	ACIN=H
CS Leading Edge Blanking time	T_{LEB}	-	0.250	-	us	
Turn off time	T_{OFF}	-	0.250	-	us	PULSE is applied to CS Pin
Minimum ON width	T_{min}	-	0.500	-	us	$T_{LEB} + T_{OFF}$
Maximum ON width	T_{max}	29.0	43.0	57.2	us	
[DC/DC Convertor Block (Turn On)]						
Maximum operating frequency 1	F_{SW1}	108	120	132	kHz	FB=2.0V
Maximum operating frequency 2	F_{SW2}	20.5	30.0	39.5	kHz	FB=0.5V
Frequency reduction start FB voltage	V_{FBSW1}	1.10	1.25	1.40	V	
Frequency reduction end FB voltage	V_{FBSW2}	0.435	0.50	0.565	V	
ZT comparator voltage 1	V_{ZT1}	60	100	140	mV	ZT fall
ZT comparator voltage 2	V_{ZT2}	120	200	280	mV	ZT rise
ZT trigger mask time	T_{ZTMASK}	-	0.5	-	us	OUT H to L, for Protection Noise
ZT trigger timeout period 1	T_{ZTOUT1}	46.8	70.0	92.8	us	The Operation without Bottom Detection
ZT trigger timeout period 2	T_{ZTOUT2}	16.2	24	31.8	us	Count from Final ZT Trigger
[DC/DC Convertor Block (Protection)]						
Soft start time 1	T_{SS1}	0.35	0.50	0.65	ms	
Soft start time 2	T_{SS2}	0.70	1.00	1.30	ms	
Soft start time 3	T_{SS3}	1.40	2.00	2.60	ms	
Soft start time 4	T_{SS4}	2.80	4.00	5.20	ms	
FB burst voltage 1	V_{BURST1}	0.25	0.30	0.35	V	
FB OLP voltage a	V_{FOLP1A}	2.6	2.8	3.0	V	Over Load Detection (FB Fall)
FB OLP voltage b	V_{FOLP1B}	-	2.6	-	V	Over Load Detection (FB Rise)
FB OLP detection timer	T_{FOLP}	99	128	166	ms	
FB OLP stop timer	T_{OLPST}	1433	2048	2664	ms	
Latch release voltage (VCC pin voltage)	V_{LATCH}	-	V_{UVLO2} – 2.00	-	V	
Latch mask time	T_{LATCH}	50	100	200	μs	ZTOVP, VCCOVP
ZT OVP voltage	V_{ZTL}	4.64	5.00	5.36	V	
[DC/DC OUT Block]						
QR_OUT Pin H Voltage	V_{QROUTH}	10.5	12.5	14.5	V	IO=-20mA
QR_OUT Pin L Voltage	V_{QROUTL}	-	-	1.00	V	IO=+20mA
QR_OUT Pin Pull-Down Res.	R_{QRDOUT}	75	100	125	kΩ	

* Definition of ACIN (L: BR Pin Voltage < 2.5V, H: BR Pin Voltage > 2.5V)

Power Dissipation

The thermal design should set operation for the following conditions.
(Since the temperature shown below is the guaranteed temperature, be sure to take a margin into account.)

1. The ambient temperature Ta must be 105°C or less.
2. The IC's loss must be within the allowable dissipation Pd.

The thermal abatement characteristics are as follows.
(PCB: 70 mm × 70 mm × 1.6 mm, mounted on glass epoxy single-layer substrate)

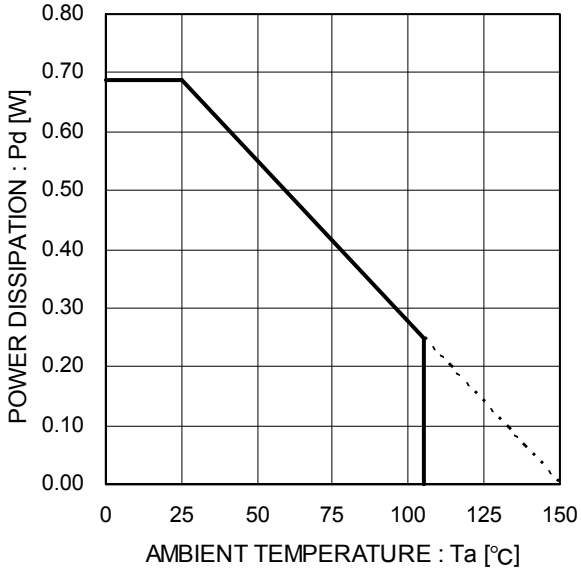
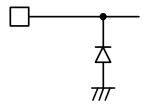
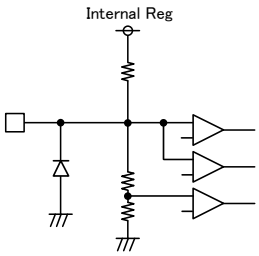
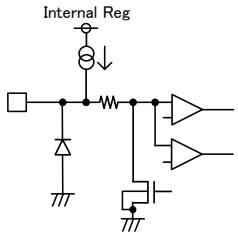
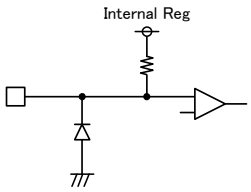
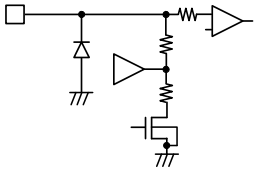
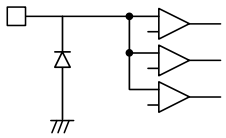
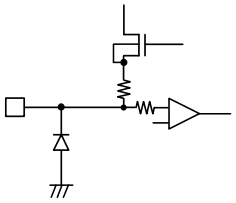


Figure 42. Thermal Abatement Characteristics

I/O Equivalence Circuits

1	VCC	2	GND	3	QR_FB	4	QR_ZT
							
5	COMP	6	P_EO	7	BR	8	P_RT
							
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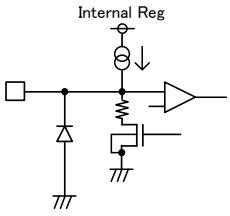		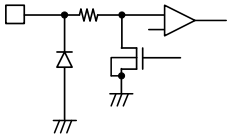		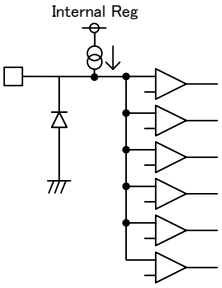		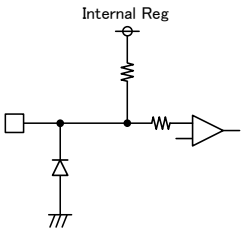	
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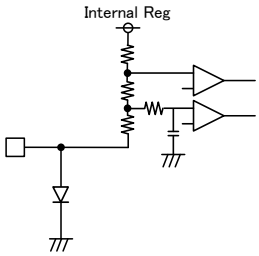
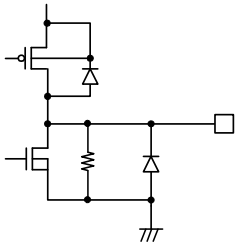
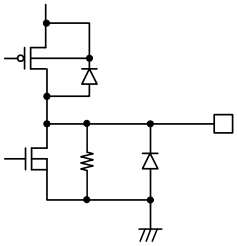
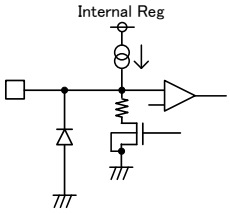
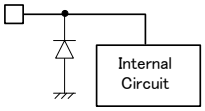
							
17	(N.C.)	18	VH_IN				
							

Figure 43. I/O Equivalent Circuit Diagram

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

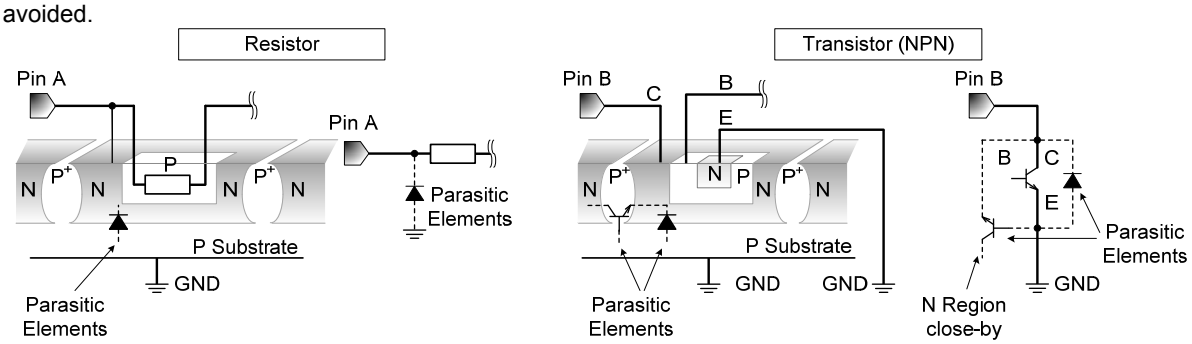


Figure 40. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

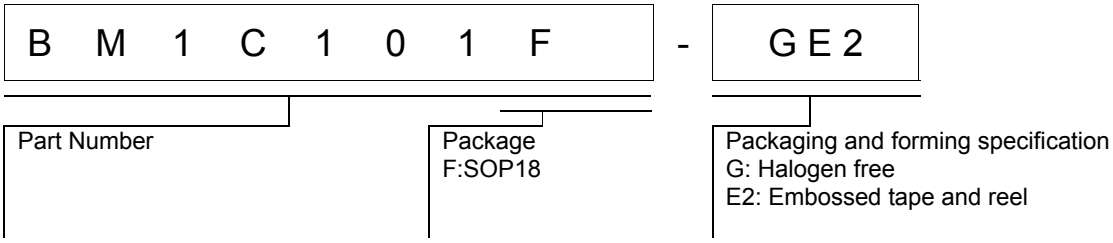
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

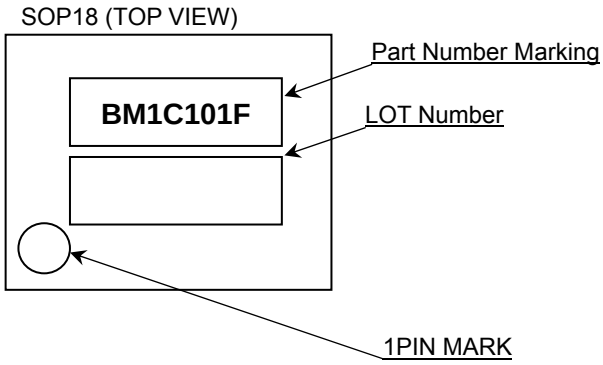
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

Ordering Information



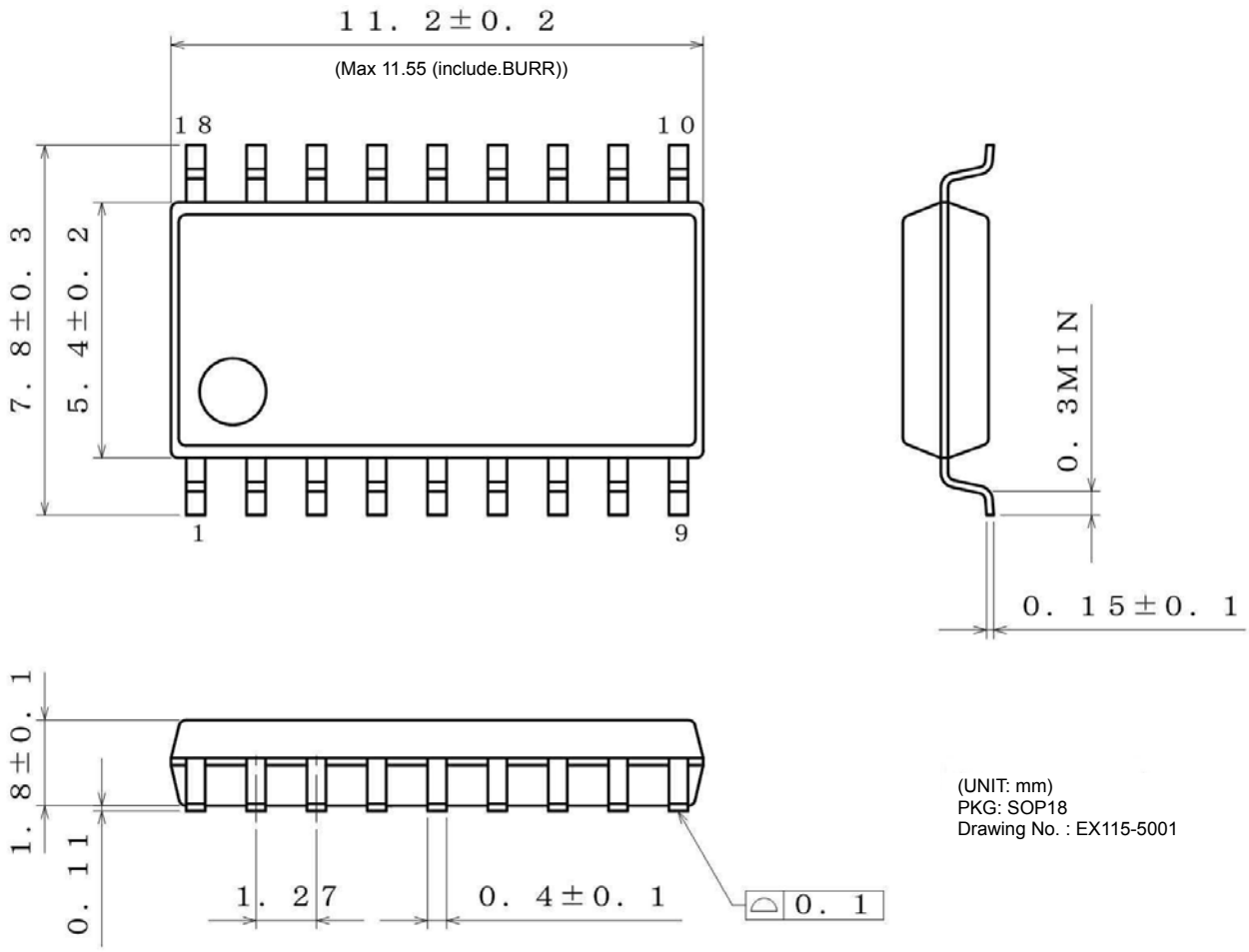
Marking Diagrams



Part Number Marking	Package	Orderable Part Number
BM1C101F	SOP18	BM1C101F-GE2

Physical Dimension, Tape and Reel Information

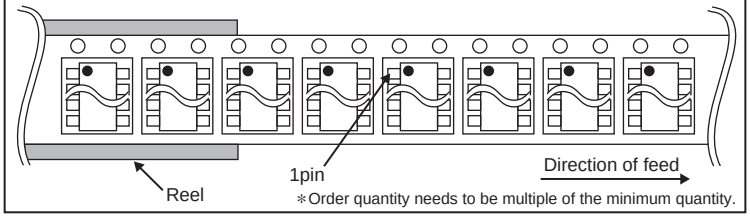
Package Name	SOP18



(UNIT: mm)
PKG: SOP18
Drawing No. : EX115-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
24.Nov.2015	001	New Release
22.Mar.2017	002	P11 the value in Figure 15

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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