THE DATASHEET OF

AS3728-BWLT

AS3728

8A Power Stage

General Description

The AS3728 is a companion power stage, intended to be used with AS372x products.

It cannot be used without a DCDC controller. It contains the power FETs for 2 phases and is capable to handle output currents up of 4A per phase.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3728, 8A Power Stage are listed below:

Figure 1:
Added Value of Using AS3728

Benefits	Features
• Support for single or dual phase operation	• 2 phases with separate control input
• 2 x 4A output stages are running on 1.3MHz	• Separate power low-side NMOS & high-side NMOS for 4A per phase • Separate coil current feedback per phase • Stand-alone zero-crossing operation
• Over – temperature protection	• Integrated temperature monitoring
• Cost effective, small package	• WL-CSP24 with 0.4mm pitch

Applications

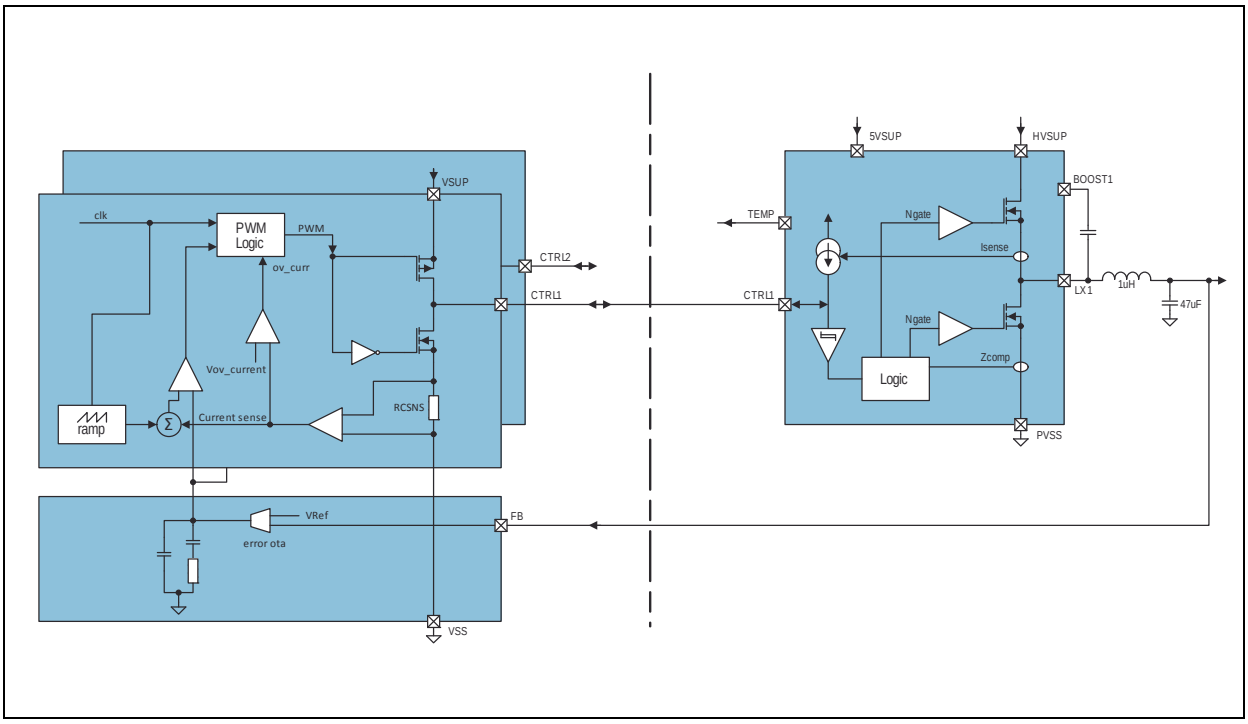
The device is a high current dual-phase DCDC and ideal for:

- Mobile phones
- Tablets
- Notebooks

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS3728 Block Diagram



AS3728 – Block Diagram: This figure shows the block diagram of the DCDC controller inside the Main PMIC and the AS3728 Power Stage with all relevant system components.

Pin Assignment

Figure 3:
Pin Diagram - 24 Balls WL-CSP with 0.4mm Pitch

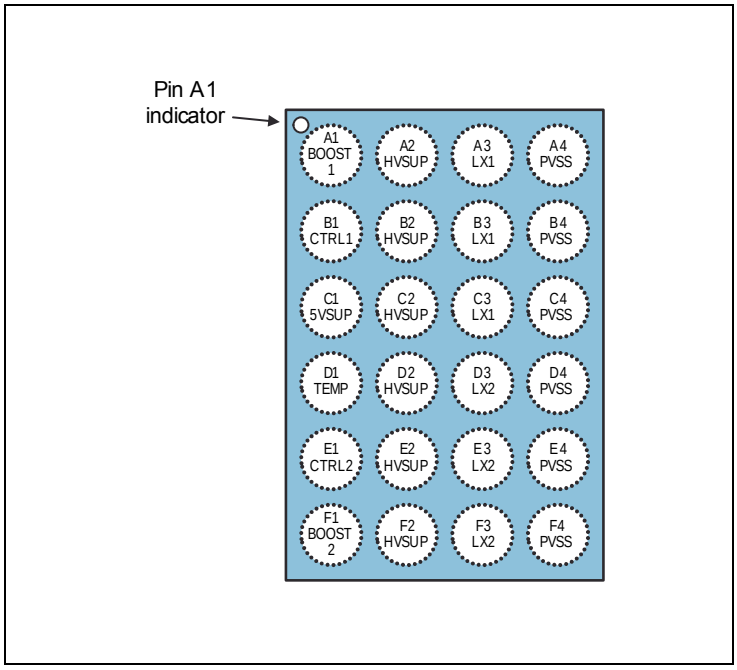


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
A1	BOOST1	AI	Supply pin for phase 1 high-side NMOS driver
B1	CTRL1	AIO	Control IO for phase 1
C1	5VSUP	S	5V supply pin
D1	TEMP	AIO	ON/OFF control and temperature feedback
E1	CTRL2	AIO	Control IO for phase 2
F1	BOOST2	AI	Supply pin for phase 2 high-side NMOS driver
A2, B2, C2	HVSUP	S	Phase 1 positive supply terminal
D2, E2, F2	HVSUP	S	Phase 2 positive supply terminal
A3, B3, C3	LX1	AIO	Phase 1 switching output to coil
D3, E3, F3	LX2	AIO	Phase 2 switching output to coil
A4, B4, C4	PVSS		Phase 1 negative supply terminal
D4, E4, F4	PVSS		Phase 2 negative supply terminal

Pin Description: Shows the pin number, type, name and description of every pin.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristicsis not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{GND}	Supply Voltage to Ground 14V pins	-0.5	16	V	Applicable for pins HVSUP, LX1, LX2
V_{GND}	Supply Voltage to Ground 20V pins	-0.5	22	V	Applicable for pins BOOST1, BOOST2
V_{GND}	Supply Voltage to Ground 5V pins	-0.5	7.0	V	Applicable for pins 5VSUP, CTRL1, CTRL2
V_{GND}	Supply Voltage to Ground 3V pins	-0.5	5.0	V	Applicable for pin TEMP
	Voltage Difference between Ground Terminals	-0.5	0.5	V	Applicable for pins PVSS
I_{SCR}	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous power dissipation		1.3	mW	P_T (1) for WL-CSP24 package (R_{THJA} ~ 42K/W)
Electrostatic Discharge					
ESD	Electrostatic Discharge HBM	±2		kV	Norm: JEDEC JESD22-A114F

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_A	Operating Temperature	-40	85	°C	
R_{THJA}	Junction to Ambient Thermal Resistance			°C/W	*R_{THJA} ~ 42K/W (typ)*
T_J	Junction Temperature		125	°C	
T_{STRG}	Storage Temperature Range	-55	125	°C	
T_{BODY}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020 (2)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	1			Represents an unlimited floor life time

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Note
V_{IN}	Input Voltage	4.5	12	14	V	Pin HVSUP
		4.5		5.5	V	Pin 5VSUP
		0		5.5	V	Pin CTRLx
		0		3.6	V	Pin TEMP
I_{LIMIT}	Peak coil current limit			5.6	A	Single phase
I_{LOAD}	Load current Single phase	0		3	A	Continuous load current
				4 (1)		Peak load current
$R_{HS-NMOS}$	N-switch ON resistance (2)		115	180	mΩ	Single phase
$R_{LS-NMOS}$	N-switch ON resistance (2)		30	40	mΩ	Single phase
f_{SW}	Switching frequency		1.3	3	MHz	Supplied by DCDC controller
I_{Q_HVSUP}	Quiescent current into HVSUP			2	µA	TEMP pin high, CTRLx pin high
I_{Q_5VSUP}	Quiescent current into 5VSUP	20		60	µA	TEMP pin high, CTRLx pin high
I_{power_off}	Power-Off current into HVSUP or 5VSUP			1	µA	No current into pin TEMP
$R_{discharge}$	Active discharge		28		Ω	Single phase

Electrical Characteristics: Shows the Electrical Characteristics of the Step Down DCDC Power Stage. HVSUP = 5VSUP = 5.0V, T_A = 25°C (unless otherwise specified)

Note(s) and/or Footnote(s):

1. Maximum value only for pulsed peak current
2. MOS transistor and package parasitic

Typical Operating Characteristics

Figure 7:
Efficiency vs. Output Current

AS3728 Step Down DCDC: Shows the Efficiency vs. Output Current for various V_{IN}/V_{OUT} conditions, 1.35MHz operation, T_{AMB} = 25°C

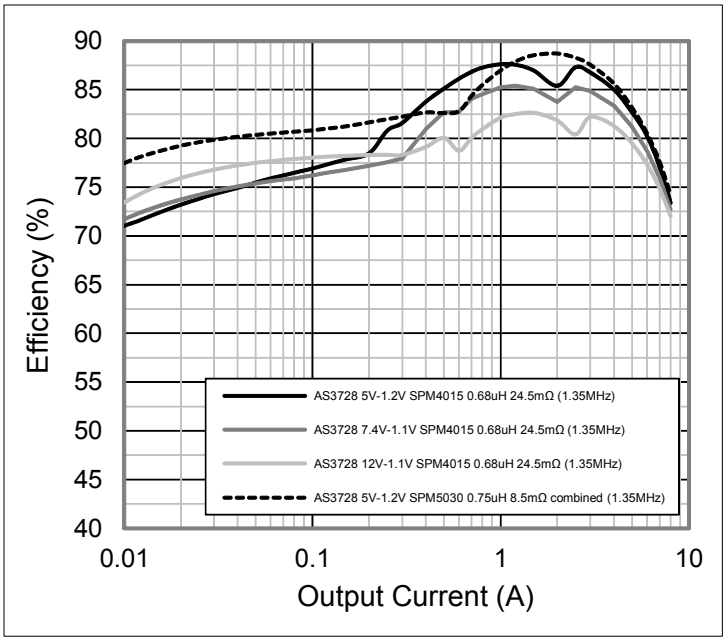


Figure 8:
Efficiency vs. Output Current

AS3728 Step Down DCDC: Shows the Efficiency vs. Output Current for various switching frequencies with V_{OUT} = 1.2V, V_{IN} = 5V, T_{AMB} = 25°C and TDK coil SPM4015 and Coilcraft coil XFL4015

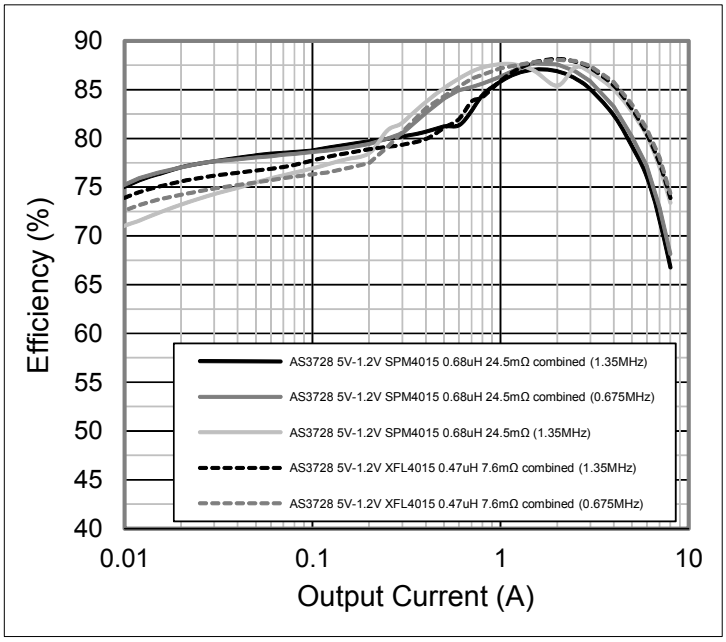


Figure 9:
Efficiency vs. Output Current

AS3728 Step Down DCDC: Shows the Efficiency vs. Output Current for various switching frequencies with V_{OUT} = 1.2V, V_{IN} = 5V, T_{AMB} = 25°C and TDK coil SPM5030

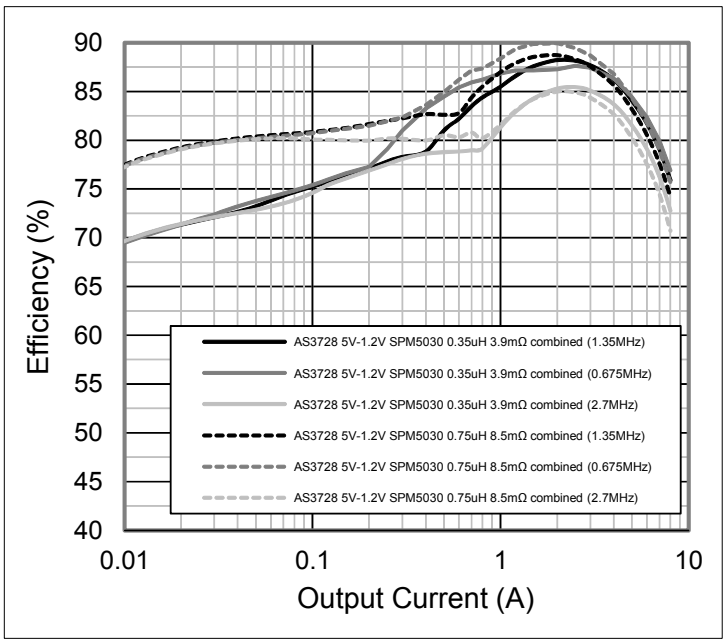
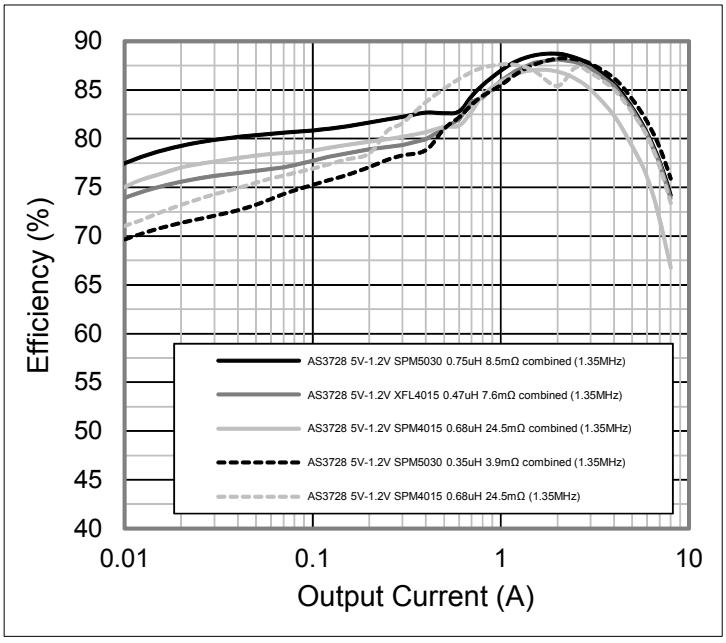


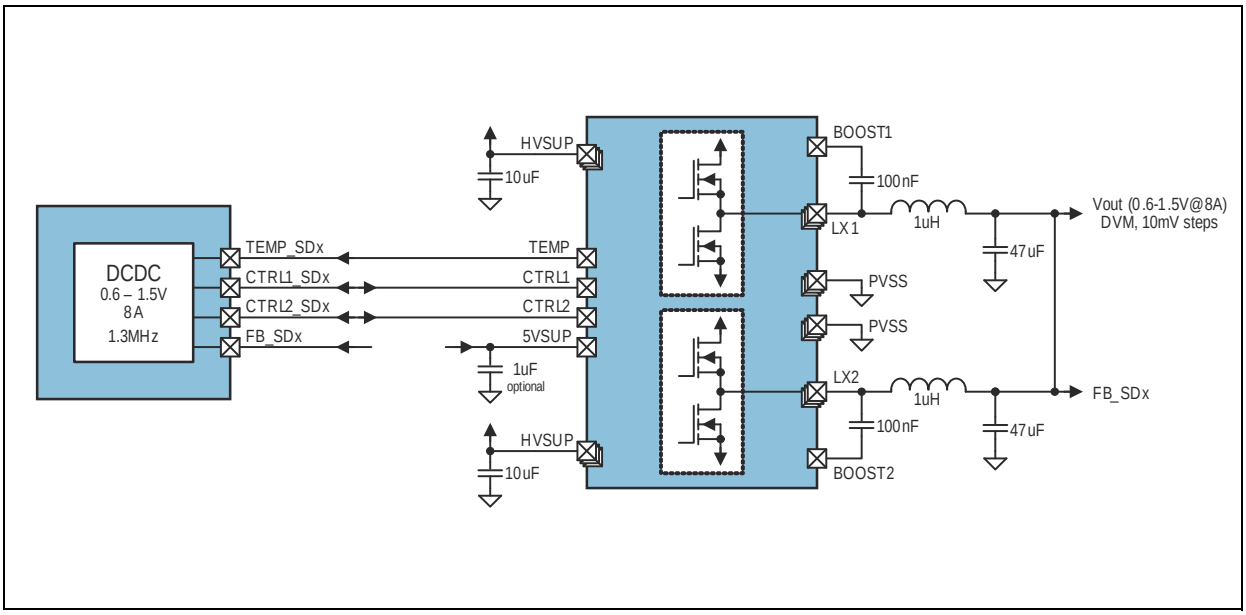
Figure 10:
Efficiency vs. Output Current

AS3728 Step Down DCDC: Shows the Efficiency vs. Output Current for various coil types with a switching frequency of 1.35MHz, V_{OUT} = 1.2V, V_{IN} = 5V, T_{AMB} = 25°C



Application Information

Figure 11:
Typical Application Circuit



Typical Application: This figure shows the connection of the DCDC controller and the AS3728 Power Stage.

External Components

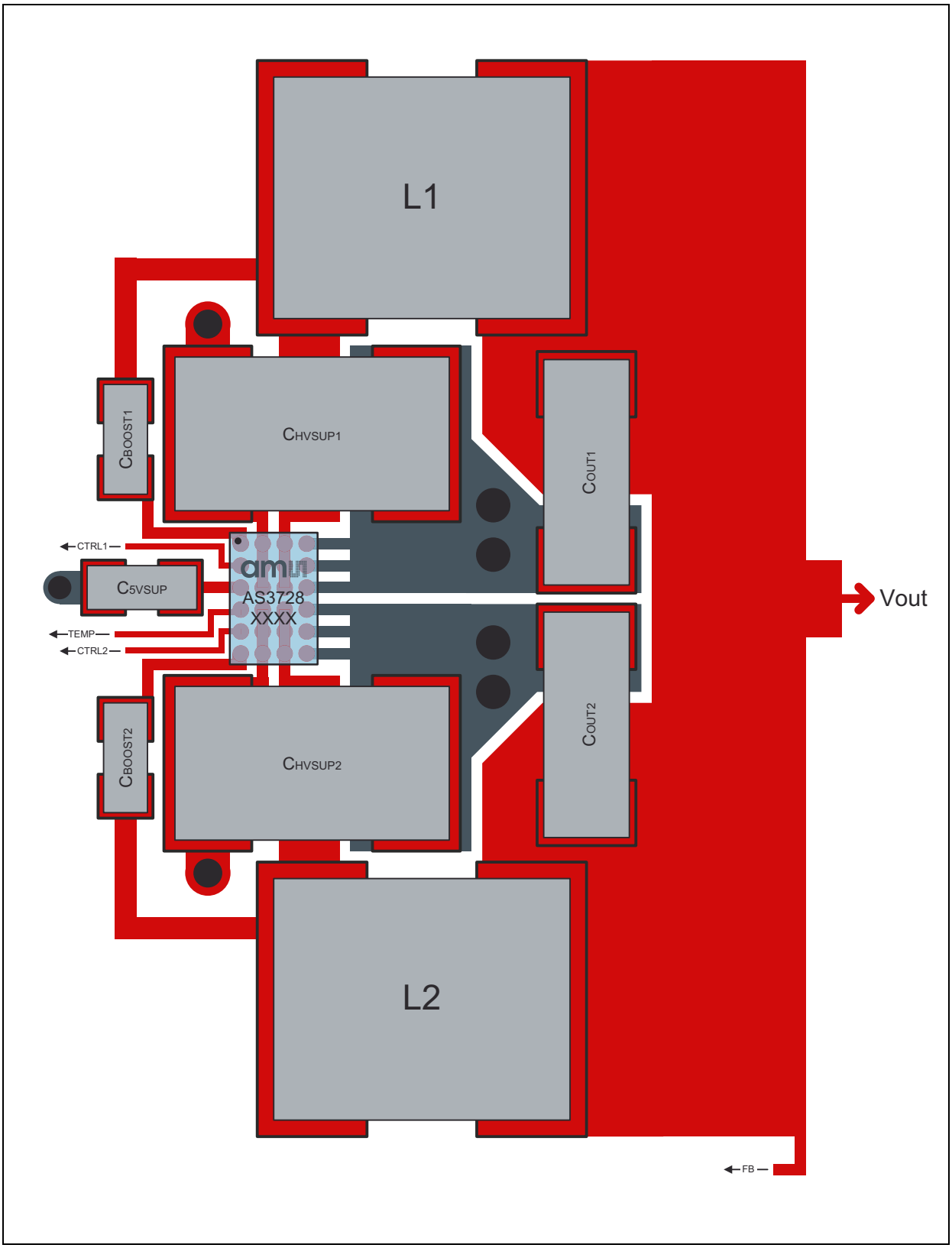
Figure 12:
Step Down DCDC Power Stage External Components

Symbol	Parameter	Min	Typ	Max	Units	Note
External Components Per Phase						
C_{FB}	Output Capacitor	64	82		µF	Ceramic X5R or X7R / 6.3V high performance
		32	47		µF	Ceramic X5R or X7R / 6.3V cost optimized
C_{HVSUP}	HV Input Capacitor	6	10		µF	Ceramic X5R or X7R / 25V
C_{BOOST}	Boost Capacitor		100		nF	Ceramic X5R or X7R / 6.3V
C_{5VSUP}	5V Supply Capacitor		1		µF	Ceramic X5R or X7R / 6.3V
L	Inductor	0.5	1		µH	5A rated, 1MHz operation, low R_{ON}

External Components: Shows the recommended values of the needed external components of the Step Down DCDC Power Stage.

PCB Layout

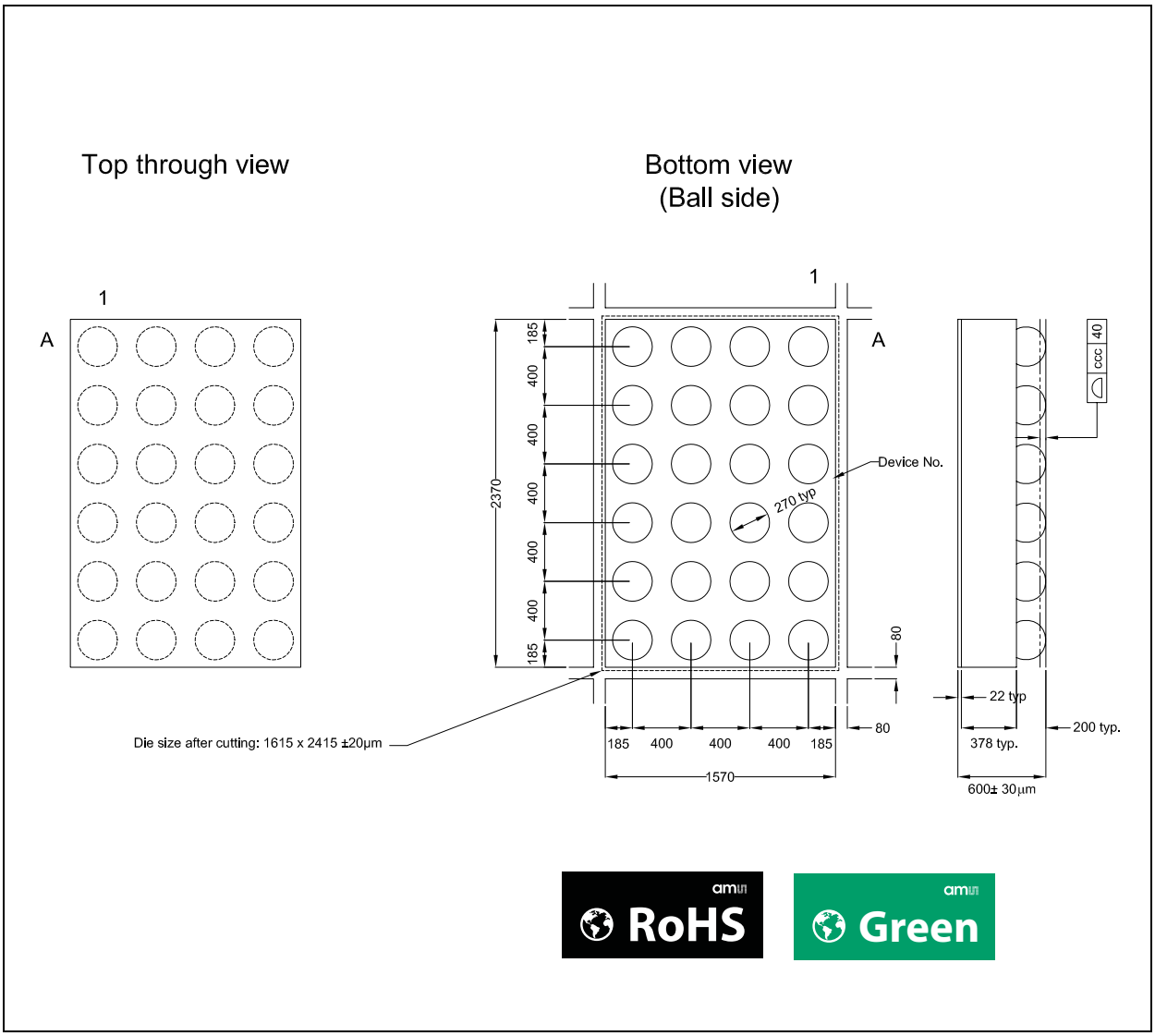
Figure 13:
Layout Guidelines



AS3728 – Layout Guidelines: This figure shows the recommended layout and placement of the external components for the 2-phase AS3728 Power Stage.

Package Drawings & Markings

Figure 14:
24 Balls WL-CSP With 0.4mm Pitch & Marking



Note(s) and/or Footnote(s):

1. Pin1 = A1.
2. ccc Coplanarity.
3. All dimensions are in µm.

Figure 15:
AS3728 Marking

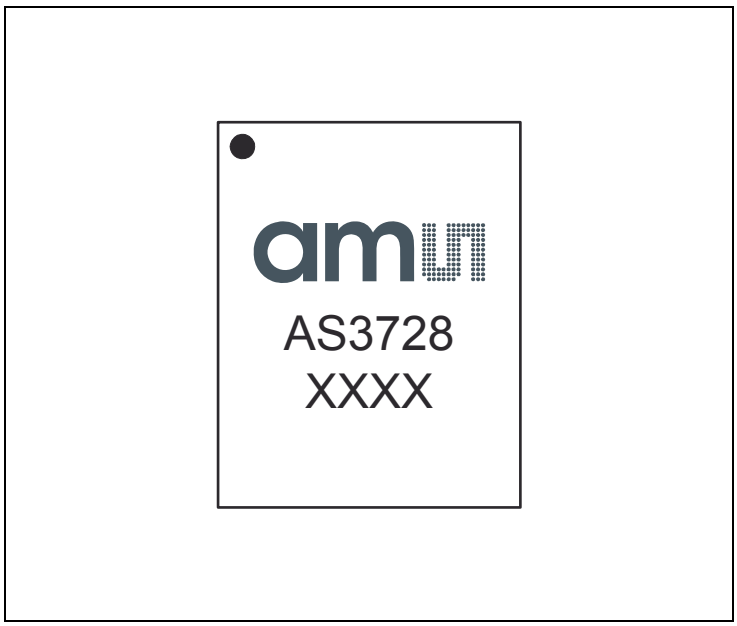


Figure 16:
AS3728 Package Code

XXXX
Tracecode

Ordering & Contact Information

Figure 17:
Ordering Information

Ordering Code	Description	Package	Delivery Form	Delivery Quantity
AS3728-BWLT	Power Stage for Multi-Phase DCDC	24-pin WL-CSP	Tape & Reel	12000 pcs/reel
AS3728-BWLM	Power Stage for Multi-Phase DCDC	24-pin WL-CSP	Mini T & R	500 pcs/reel

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Document Status	Product Status	Definition
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Revision Information

Changes from 1-02 (2014-Dec-16) to current revision 1-03 (2015-Aug-31)	Page
Updated Package Drawings & Markings section	11
Updated Figure 17	13

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide

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