



# THE DATASHEET OF ADG662BRUZ



### ADG661/ADG662/ADG663

#### FEATURES

- +5 V,  $\pm 5$  V Power Supplies
- Ultralow Power Dissipation ( $<0.5 \mu\text{W}$ )
- Low Leakage ( $<100 \text{ pA}$ )
- Low On Resistance ( $<50 \Omega$ )
- Fast Switching Times
- Low Charge Injection
- TTL/CMOS Compatible
- TSSOP Package

#### APPLICATIONS

- Battery Powered Instruments
- Single Supply Systems
- Remote Powered Equipment
- +5 V Supply Systems
- Computer Peripherals such as Disk Drives
- Precision Instrumentation
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Sample Hold Systems
- Communication Systems

#### GENERAL DESCRIPTION

The ADG661, ADG662 and ADG663 are monolithic CMOS devices comprising four independently selectable switches. These switches feature low, well-controlled on resistance and wide analog signal range, making them ideal for precision analog signal switching.

They are fabricated using Analog Devices' advanced linear compatible CMOS (LC<sup>2</sup>MOS) process, which offers benefits of low leakage currents, ultralow power dissipation and low capacitance for fast switching speeds with minimum charge injection.

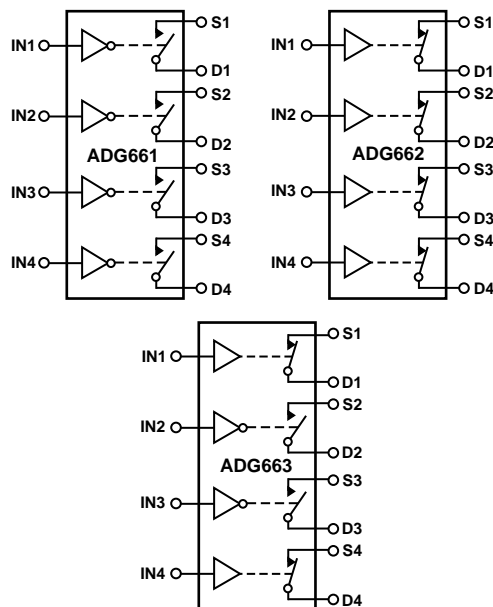
The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG661, ADG662 and ADG663 contain four independent SPST switches. The ADG661 and ADG662 differ only in that the digital control logic is inverted. The ADG661 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG662. The ADG663 has two switches with digital control logic similar to that of the ADG661, while the logic is inverted on the other two switches.

#### REV. 0

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#### FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

#### PRODUCT HIGHLIGHTS

1. +5 V Single Supply Operation  
The ADG661, ADG662 and ADG663 offer high performance, including low on resistance and wide signal range, fully specified and guaranteed with  $\pm 5$  V and +5 V supply rails.
2. Ultralow Power Dissipation  
CMOS construction ensures ultralow power dissipation.
3. Low  $R_{ON}$
4. Break-Before-Make Switching  
This prevents channel shorting when the switches are configured as a multiplexer.

# ADG661/ADG662/ADG663—SPECIFICATIONS<sup>1</sup>

Dual Supply ( $V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Versions		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analogue Signal Range		$V_{DD}$ to $V_{SS}$	V	
$R_{ON}$	30 38	50	$\Omega$ typ $\Omega$ max	$V_D = -3.5\text{ V}$ to $+3.5\text{ V}$ , $I_S = -10\text{ mA}$ ; $V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.025$ $\pm 0.1$	$\pm 2.5$	nA typ nA max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_D = \pm 4.5\text{ V}$ , $V_S = \pm 4.5\text{ V}$ ; Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.025$ $\pm 0.1$	$\pm 2.5$	nA typ nA max	$V_D = \pm 4.5\text{ V}$ , $V_S = \pm 4.5\text{ V}$ ; Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.05$ $\pm 0.2$	$\pm 5$	nA typ nA max	$V_D = V_S = \pm 4.5\text{ V}$ ; Test Circuit 3
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	150	275	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = \pm 3\text{ V}$ ; Test Circuit 4
$t_{OFF}$	55	120	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = \pm 3\text{ V}$ ; Test Circuit 4
Break-Before-Make Time Delay, $t_D$ (ADG663 Only)	80		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = +3\text{ V}$ ; Test Circuit 5
Charge Injection	6		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 10\text{ nF}$ ; Test Circuit 6
OFF Isolation	70		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
Channel-to-Channel Crosstalk	90		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8
$C_S$ (OFF)	9		pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	9		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	28		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$V_{DD}$		+4.5/5.5 -4.5/5.5	V min/max V min/max	
$I_{DD}$	0.0001	1	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5 V
$I_{SS}$	0.0001	1	$\mu\text{A}$ typ $\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Versions, -40°C to +85°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**Single Supply** ( $V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Versions		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH Analog Signal Range $R_{ON}$	45 68	0 V to $V_{DD}$ 75	V $\Omega$ typ $\Omega$ max	$V_D = 0\text{ V}$ to +3.5 V, $I_S = -10\text{ mA}$ ; $V_{DD} = +4.5\text{ V}$
LEAKAGE CURRENTS Source OFF Leakage $I_S$ (OFF) Drain OFF Leakage $I_D$ (OFF) Channel ON Leakage $I_D, I_S$ (ON)	$\pm 0.025$ $\pm 0.1$ $\pm 0.025$ $\pm 0.1$ $\pm 0.05$ $\pm 0.2$	$\pm 2.5$ $\pm 2.5$ $\pm 5$	nA typ nA max nA typ nA max nA typ nA max	$V_{DD} = +5.5\text{ V}$ $V_D = 4.5\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2 $V_D = 4.5\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2 $V_D = V_S = +4.5\text{ V}/+1\text{ V}$ ; Test Circuit 3
DIGITAL INPUTS Input High Voltage, $V_{INH}$ Input Low Voltage, $V_{INL}$ Input Current $I_{INL}$ or $I_{INH}$	0.005	2.4 0.8 $\pm 0.1$	V min V max $\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
DYNAMIC CHARACTERISTICS <sup>2</sup> $t_{ON}$ $t_{OFF}$ Break-Before-Make Time Delay, $t_D$ (ADG663 Only) Charge Injection OFF Isolation Channel-to-Channel Crosstalk $C_S$ (OFF) $C_D$ (OFF) $C_D, C_S$ (ON)	250 45 140 12 70 90 9 9 28	400 100	ns typ ns max ns typ ns max ns typ pC typ dB typ dB typ pF typ pF typ pF typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +2\text{ V}$ ; Test Circuit 4 $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +2\text{ V}$ ; Test Circuit 4 $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = +2\text{ V}$ ; Test Circuit 5 $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 10\text{ nF}$ ; Test Circuit 6 $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7 $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8 $f = 1\text{ MHz}$ $f = 1\text{ MHz}$ $f = 1\text{ MHz}$
POWER REQUIREMENTS $V_{DD}$ $I_{DD}$	0.0001	+4.5/5.5 1	V min/max $\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +5.5\text{ V}$ Digital Inputs = 0 V or 5 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Versions, -40°C to +85°C.<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG661/ADG662/ADG663

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	+44 V
V <sub>DD</sub> to GND .....	-0.3 V to +25 V
V <sub>SS</sub> to GND .....	+0.3 V to -25 V
Analog, Digital Inputs <sup>2</sup> .....	V <sub>SS</sub> -2 V to V <sub>DD</sub> +2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D .....	30 mA
Peak Current, S or D .....	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range	
Industrial (B Version) .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	+150°C
TSSOP Package, Power Dissipation .....	450 mW
θ <sub>JA</sub> Thermal Impedance .....	115°C/W
θ <sub>JC</sub> Thermal Impedance .....	35°C/W

## Lead Temperature, Soldering

Vapor Phase (60 secs) .....	+215°C
Infrared (15 secs) .....	+220°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## ORDERING GUIDE

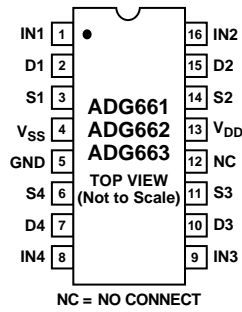
Model	Temperature Range	Package Description	Package Option
ADG661BRU	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG662BRU	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG663BRU	-40°C to +85°C	16-Lead TSSOP	RU-16

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG661/ADG662/ADG663 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION



**Table I. Truth Table (ADG661/ADG662)**

ADG661 In	ADG662 In	Switch Condition
0	1	ON
1	0	OFF

**Table II. Truth Table (ADG663)**

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

## TERMINOLOGY

$V_{DD}$	Most positive power supply potential.
$V_{SS}$	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
$R_{ON}$	Ohmic resistance between D and S.
$I_S$ (OFF)	Source leakage current with the switch "OFF."
$I_D$ (OFF)	Drain leakage current with the switch "OFF."
$I_D, I_S$ (ON)	Channel leakage current with the switch "ON."
$V_D$ ( $V_S$ )	Analog voltage on terminals D, S.
$C_S$ (OFF)	"OFF" Switch Source Capacitance.
$C_D$ (OFF)	"OFF" Switch Drain Capacitance.
$C_D, C_S$ (ON)	"ON" Switch Capacitance.
$t_{ON}$	Delay between applying the digital control input and the output switching on.
$t_{OFF}$	Delay between applying the digital control input and the output switching off.
$t_D$	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to analog output during switching.

Typical Performance Characteristics

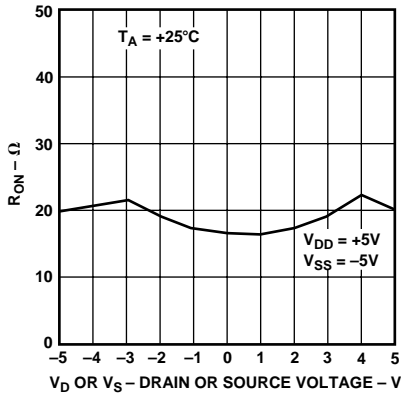


Figure 1. On Resistance as a Function of  $V_D$  ( $V_S$ ) Dual Supplies

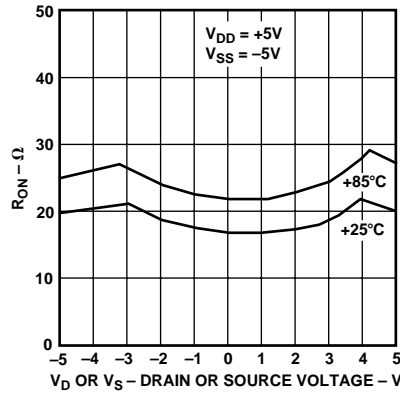


Figure 2. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

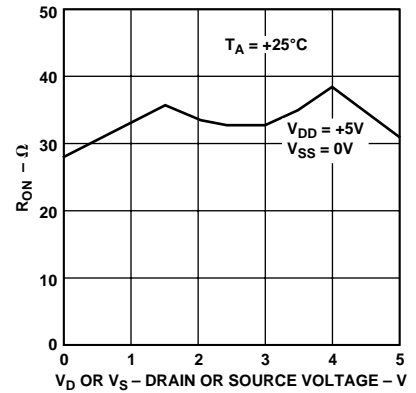


Figure 3. On Resistance as a Function of  $V_D$  ( $V_S$ ) Single Supply

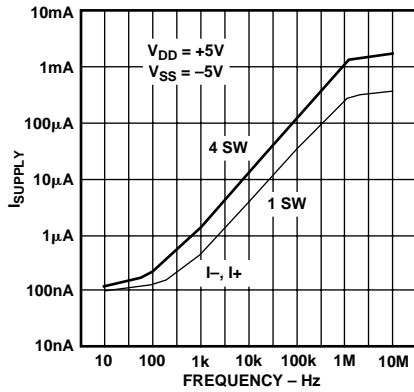


Figure 4. Supply Current vs. Input Switching Frequency

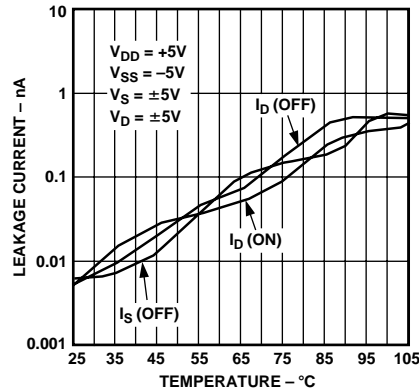


Figure 5. Leakage Currents as a Function of Temperature

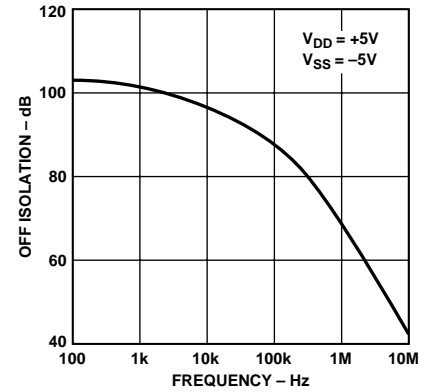


Figure 6. Off Isolation vs. Frequency

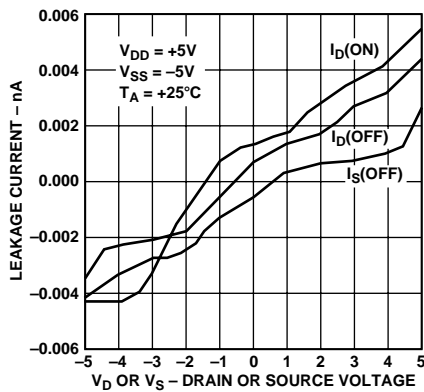


Figure 7. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

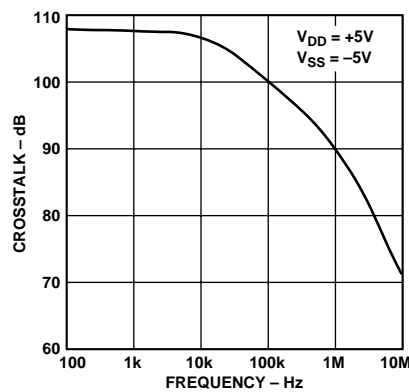
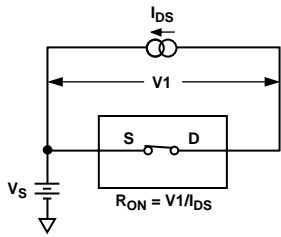
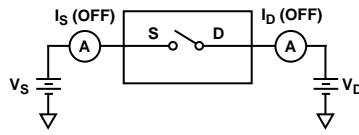


Figure 8. Crosstalk vs. Frequency

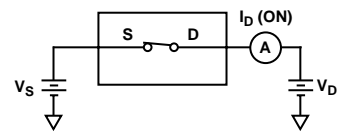
### Test Circuits



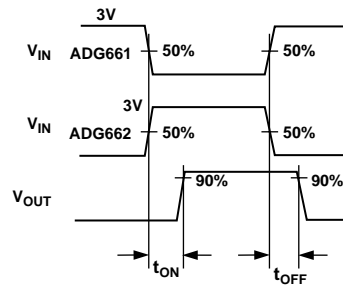
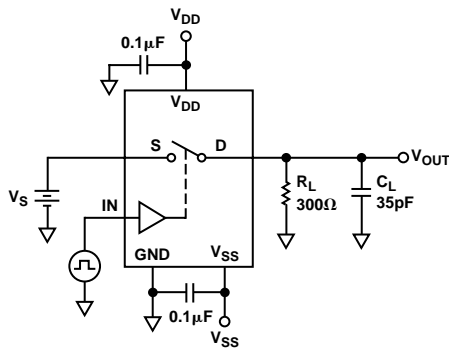
1. On Resistance



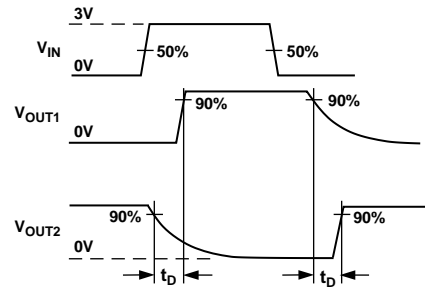
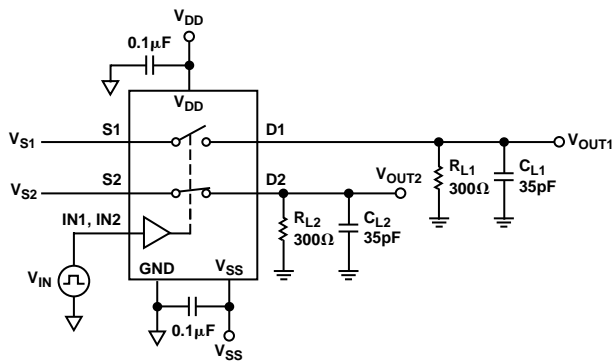
2. Off Leakage



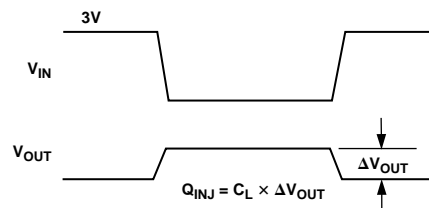
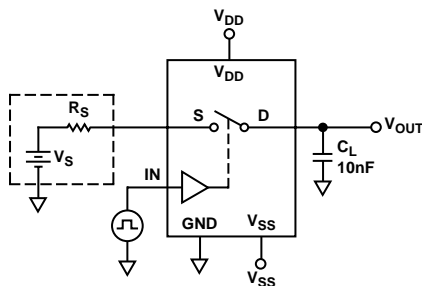
3. On Leakage



4. Switching Times

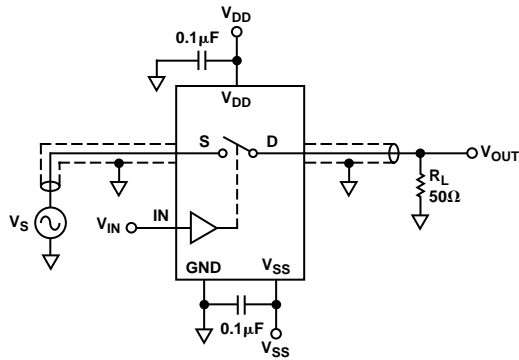


5. Break-Before-Make Time Delay

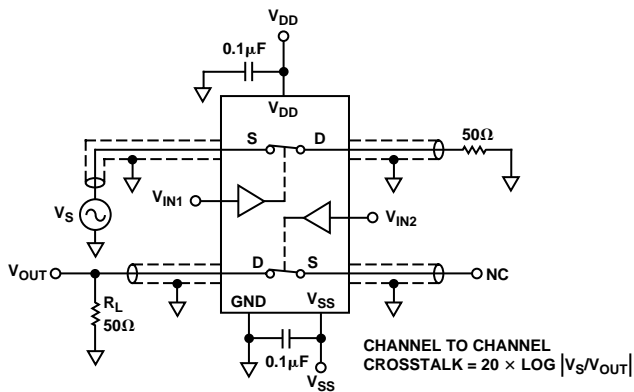


6. Charge Injection

Test Circuits (Continued)



7. Off Isolation



8. Channel-to-Channel Crosstalk

CHANNEL TO CHANNEL CROSSTALK =  $20 \times \text{LOG} |V_S/V_{OUT}|$

APPLICATION

Figure 9 illustrates a precise, sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an OP07. During the track mode, SW1 is closed and the output  $V_{OUT}$  follows the input signal  $V_{IN}$ . In the hold mode, SW1 is opened and the signal is held by the hold capacitor  $C_H$ .

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG661/ADG662/ADG663 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a poly-styrene hold capacitor. The droop rate for the circuit shown is typically  $15 \mu\text{V}/\mu\text{s}$ .

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp OP07 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network  $R_C$  and  $C_C$ . This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the  $\pm 3 \text{ V}$  input range. The acquisition time is 2.5 ms while the settling time is  $1.85 \mu\text{s}$ .

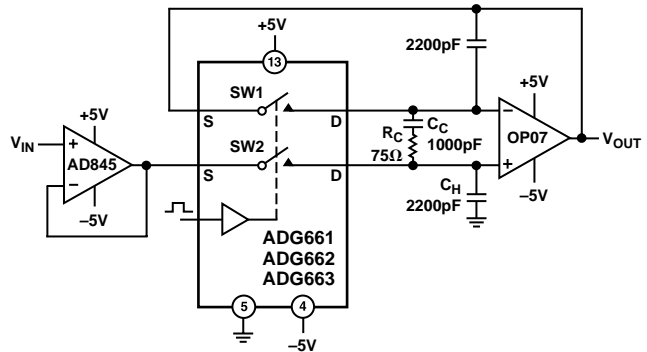
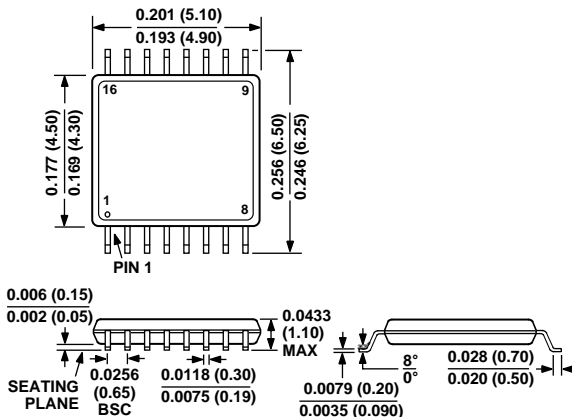


Figure 9. Accurate Sample-and-Hold

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP (RU-16)



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