



**THE DATASHEET OF  
9ZX21201AKLF**



# 12-OUTPUT DIFFERENTIAL Z-BUFFER FOR PCIe GEN2/3 AND QPI 9ZX21201

## General Description

The IDT9ZX21201 is a 12-output DB1200Z suitable for PCI-Express Gen3 or QPI applications. The part is backwards compatible to PCIe Gen1 and Gen2. A fixed external feedback maintains low drift for critical QPI applications. In bypass mode, the IDT9ZX21201 can provide outputs up to 150MHz.

## Recommended Application

12-output PCIe Gen3/ QPI differential buffer for Romley and newer platforms

## Key Specifications

- Cycle-to-cycle jitter <50ps
- Output-to-output skew < 65 ps
- Input-to-output delay variation <50ps
- PCIe Gen3 phase jitter < 1.0ps RMS
- QPI 9.6GT/s-12UI phase jitter < 0.2ps RMS

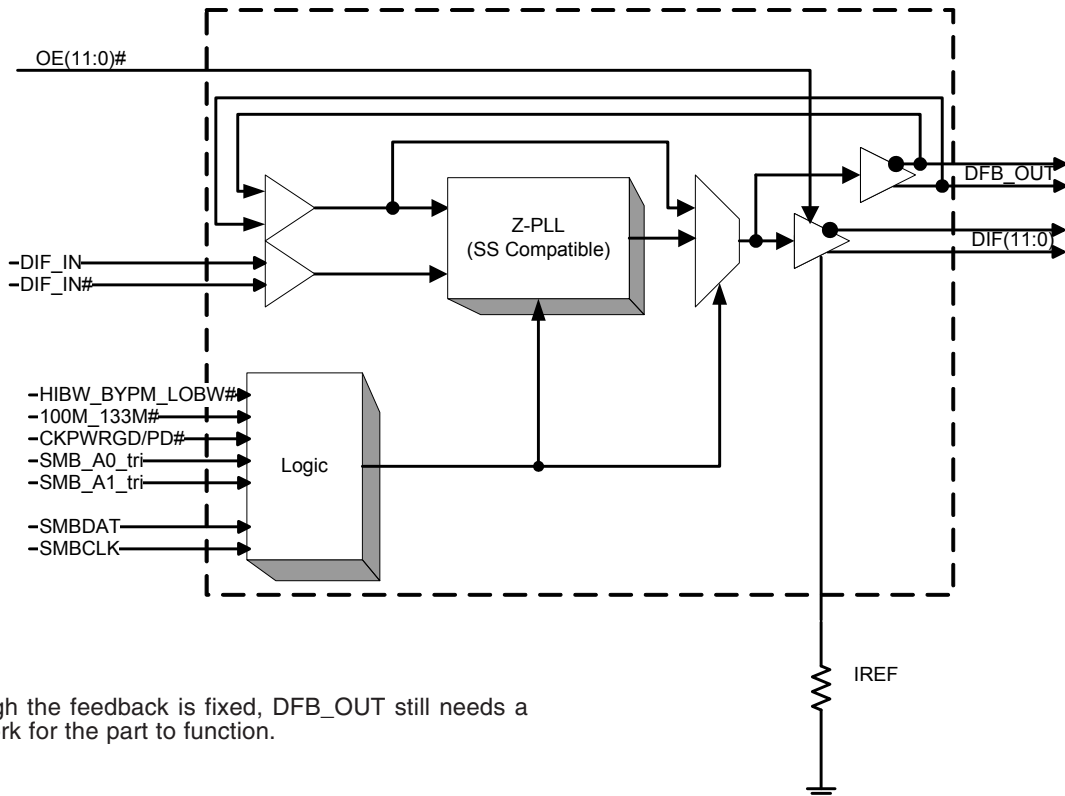
## Features/Benefits

- Space-saving 64-pin packages
- Fixed feedback path/ 0ps input-to-output delay
- 9 Selectable SMBus Addresses/Multiple devices can share the same SMBus Segment
- 12 OE# pins/Hardware control of each output
- PLL or bypass mode/PLL can dejitter incoming clock
- 100MHz or 133MHz PLL mode operation/supports PCIe and QPI applications
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- Software control of PLL Bandwidth and Bypass Settings/ PLL can dejitter incoming clock (B Rev only)

## Output Features

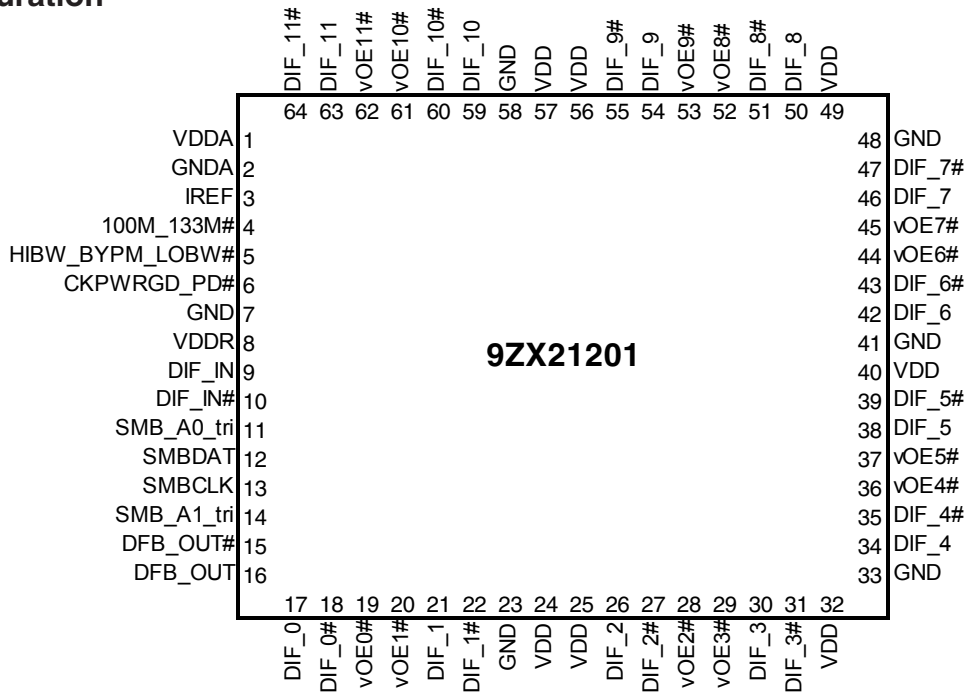
- 12 - 0.7V differential HCSL output pairs

## Functional Block Diagram



**Note:** Even though the feedback is fixed, DFB\_OUT still needs a termination network for the part to function.

## Pin Configuration



Notes: Pins with ^ prefix have internal ~100K pullup  
Pins with v prefix have internal ~100K pulldown.

### Tri-level Input Thresholds

| Level | Voltage      |
|-------|--------------|
| Low   | <0.8V        |
| Mid   | 1.2<Vin<1.8V |
| High  | Vin > 2.2V   |

### Functionality at Power Up (PLL Mode)

| 100M_133M# | DIF_IN (MHz) | DIF    |
|------------|--------------|--------|
| 1          | 100.00       | DIF_IN |
| 0          | 133.33       | DIF_IN |

### PLL Operating Mode Readback Table

| HiBW_BypM_LoBW# | Byte0, bit 7 | Byte 0, bit 6 |
|-----------------|--------------|---------------|
| Low (Low BW)    | 0            | 0             |
| Mid (Bypass)    | 0            | 1             |
| High (High BW)  | 1            | 1             |

### PLL Operating Mode

| HiBW_BypM_LoBW# | MODE      |
|-----------------|-----------|
| Low             | PLL Lo BW |
| Mid             | Bypass    |
| High            | PLL Hi BW |

**NOTE: PLL is OFF in Bypass Mode**

### MLF Power Connections

| Pin Number |             |                | Description  |
|------------|-------------|----------------|--------------|
| VDD        | VDD         | GND            |              |
| 1          |             | 2              | Analog PLL   |
| 8          |             | 7              | Analog Input |
| 24,40,57   | 25,32,49,56 | 23,33,41,48,58 | DIF clocks   |

### 9ZX21201 SMBus Addressing

| Pin        |            | SMBus Address (Rd/Wrt bit = 0) |
|------------|------------|--------------------------------|
| SMB_A1_tri | SMB_A0_tri |                                |
| 0          | 0          | D8                             |
| 0          | M          | DA                             |
| 0          | 1          | DE                             |
| M          | 0          | C2                             |
| M          | M          | C4                             |
| M          | 1          | C6                             |
| 1          | 0          | CA                             |
| 1          | M          | CC                             |
| 1          | 1          | CE                             |

## Pin Description

| PIN # | PIN NAME        | TYPE | DESCRIPTION   |
|-------|-----------------|------|---|
| 1     | VDDA            | PWR  | 3.3V power for the PLL core.  |
| 2     | GNDA            | PWR  | Ground pin for the PLL core.  |
| 3     | IREF            | OUT  | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 4     | 100M_133M#      | IN   | 3.3V Input to select operating frequency<br>See Functionality Table for Definition  |
| 5     | HIBW_BYPM_LOBW# | IN   | Trilevel input to select High BW, Bypass or Low BW mode.<br>See PLL Operating Mode Table for Details.   |
| 6     | CKPWRGD_PD#     | IN   | Notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.  |
| 7     | GND             | PWR  | Ground pin.   |
| 8     | VDDR            | PWR  | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.  |
| 9     | DIF_IN          | IN   | 0.7 V Differential TRUE input   |
| 10    | DIF_IN#         | IN   | 0.7 V Differential Complementary Input  |
| 11    | SMB_A0_tri      | IN   | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses.  |
| 12    | SMBDAT          | I/O  | Data pin of SMBUS circuitry, 5V tolerant  |
| 13    | SMBCLK          | IN   | Clock pin of SMBUS circuitry, 5V tolerant   |
| 14    | SMB_A1_tri      | IN   | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses.  |
| 15    | DFB_OUT#        | OUT  | Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error.  |
| 16    | DFB_OUT         | OUT  | True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error.   |
| 17    | DIF_0           | OUT  | 0.7V differential true clock output   |
| 18    | DIF_0#          | OUT  | 0.7V differential Complementary clock output  |
| 19    | vOE0#           | IN   | Active low input for enabling DIF pair 0.<br>1 =disable outputs, 0 = enable outputs   |
| 20    | vOE1#           | IN   | Active low input for enabling DIF pair 1.<br>1 =disable outputs, 0 = enable outputs   |
| 21    | DIF_1           | OUT  | 0.7V differential true clock output   |
| 22    | DIF_1#          | OUT  | 0.7V differential Complementary clock output  |
| 23    | GND             | PWR  | Ground pin.   |
| 24    | VDD             | PWR  | Power supply, nominal 3.3V  |
| 25    | VDD             | PWR  | Power supply, nominal 3.3V  |
| 26    | DIF_2           | OUT  | 0.7V differential true clock output   |
| 27    | DIF_2#          | OUT  | 0.7V differential Complementary clock output  |
| 28    | vOE2#           | IN   | Active low input for enabling DIF pair 2.<br>1 =disable outputs, 0 = enable outputs   |
| 29    | vOE3#           | IN   | Active low input for enabling DIF pair 3.<br>1 =disable outputs, 0 = enable outputs   |
| 30    | DIF_3           | OUT  | 0.7V differential true clock output   |
| 31    | DIF_3#          | OUT  | 0.7V differential Complementary clock output  |
| 32    | VDD             | PWR  | Power supply, nominal 3.3V  |

## Pin Description (continued)

|    |         |     |   |
|----|---------|-----|---|
| 33 | GND     | PWR | Ground pin.   |
| 34 | DIF_4   | OUT | 0.7V differential true clock output   |
| 35 | DIF_4#  | OUT | 0.7V differential Complementary clock output  |
| 36 | vOE4#   | IN  | Active low input for enabling DIF pair 4<br>1 =disable outputs, 0 = enable outputs                                      |
| 37 | vOE5#   | IN  | Active low input for enabling DIF pair 5. This pin has an internal pull-down<br>1 =disable outputs, 0 = enable outputs  |
| 38 | DIF_5   | OUT | 0.7V differential true clock output   |
| 39 | DIF_5#  | OUT | 0.7V differential Complementary clock output  |
| 40 | VDD     | PWR | Power supply, nominal 3.3V  |
| 41 | GND     | PWR | Ground pin.   |
| 42 | DIF_6   | OUT | 0.7V differential true clock output   |
| 43 | DIF_6#  | OUT | 0.7V differential Complementary clock output  |
| 44 | vOE6#   | IN  | Active low input for enabling DIF pair 6. This pin has an internal pull-down<br>1 =disable outputs, 0 = enable outputs  |
| 45 | vOE7#   | IN  | Active low input for enabling DIF pair 7. This pin has an internal pull-down<br>1 =disable outputs, 0 = enable outputs  |
| 46 | DIF_7   | OUT | 0.7V differential true clock output   |
| 47 | DIF_7#  | OUT | 0.7V differential Complementary clock output  |
| 48 | GND     | PWR | Ground pin.   |
| 49 | VDD     | PWR | Power supply, nominal 3.3V  |
| 50 | DIF_8   | OUT | 0.7V differential true clock output   |
| 51 | DIF_8#  | OUT | 0.7V differential Complementary clock output  |
| 52 | vOE8#   | IN  | Active low input for enabling DIF pair 8. This pin has an internal pull-down<br>1 =disable outputs, 0 = enable outputs  |
| 53 | vOE9#   | IN  | Active low input for enabling DIF pair 9. This pin has an internal pull-down<br>1 =disable outputs, 0 = enable outputs  |
| 54 | DIF_9   | OUT | 0.7V differential true clock output   |
| 55 | DIF_9#  | OUT | 0.7V differential Complementary clock output  |
| 56 | VDD     | PWR | Power supply, nominal 3.3V  |
| 57 | VDD     | PWR | Power supply, nominal 3.3V  |
| 58 | GND     | PWR | Ground pin.   |
| 59 | DIF_10  | OUT | 0.7V differential true clock output   |
| 60 | DIF_10# | OUT | 0.7V differential Complementary clock output  |
| 61 | vOE10#  | IN  | Active low input for enabling DIF pair 10. This pin has an internal pull-down<br>1 =disable outputs, 0 = enable outputs |
| 62 | vOE11#  | IN  | Active low input for enabling DIF pair 11. This pin has an internal pull-down<br>1 =disable outputs, 0 = enable outputs |
| 63 | DIF_11  | OUT | 0.7V differential true clock output   |
| 64 | DIF_11# | OUT | 0.7V differential Complementary clock output  |

**Electrical Characteristics - Absolute Maximum Ratings**

| PARAMETER                | SYMBOL             | CONDITIONS                 | MIN     | TYP | MAX                   | UNITS | NOTES |
|--------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDD, VDDA          | VDD for core logic and PLL |         |     | 4.6                   | V     | 1,2   |
| Input Low Voltage        | V <sub>IL</sub>    |                            | GND-0.5 |     |                       | V     | 1     |
| Input High Voltage       | V <sub>IH</sub>    | Except for SMBus interface |         |     | V <sub>DD</sub> +0.5V | V     | 1     |
| Input High Voltage       | V <sub>IHSMB</sub> | SMBus clock and data pins  |         |     | 5.5V                  | V     | 1     |
| Storage Temperature      | T <sub>s</sub>     |                            | -65     |     | 150                   | °C    | 1     |
| Junction Temperature     | T <sub>j</sub>     |                            |         |     | 125                   | °C    | 1     |
| Input ESD protection     | ESD prot           | Human Body Model           | 2000    |     |                       | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

**Electrical Characteristics - Input/Supply/Common Parameters**

T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V +/-5%

| PARAMETER                     | SYMBOL                | CONDITIONS  | MIN       | TYP    | MAX                   | UNITS  | NOTES |
|-------------------------------|-----------------------|---|-----------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature | T <sub>COM</sub>      | Commercial range  | 0         |        | 70                    | °C     | 1     |
| Input High Voltage            | V <sub>IH</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | 2         |        | V <sub>DD</sub> + 0.3 | V      | 1     |
| Input Low Voltage             | V <sub>IL</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | GND - 0.3 |        | 0.8                   | V      | 1     |
| Input Current                 | I <sub>IN</sub>       | Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD   | -5        |        | 5                     | uA     | 1     |
|                               | I <sub>INP</sub>      | Single-ended inputs<br>V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors<br>V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors | -200      |        | 200                   | uA     | 1     |
| Input Frequency               | F <sub>IBYP</sub>     | V <sub>DD</sub> = 3.3 V, Bypass mode  | 33        |        | 150                   | MHz    | 2     |
|                               | F <sub>IPLL</sub>     | V <sub>DD</sub> = 3.3 V, 100MHz PLL mode  | 90        | 100.00 | 110                   | MHz    | 2     |
|                               | F <sub>IPLL</sub>     | V <sub>DD</sub> = 3.3 V, 133.33MHz PLL mode   | 120       | 133.33 | 147                   | MHz    | 2     |
| Pin Inductance                | L <sub>pin</sub>      |   |           |        | 7                     | nH     | 1     |
| Capacitance                   | C <sub>IN</sub>       | Logic Inputs, except DIF_IN   | 1.5       |        | 5                     | pF     | 1     |
|                               | C <sub>INDIF_IN</sub> | DIF_IN differential clock inputs  | 1.5       |        | 2.7                   | pF     | 1,4   |
|                               | C <sub>OUT</sub>      | Output pin capacitance  |           |        | 6                     | pF     | 1     |
| Clk Stabilization             | T <sub>STAB</sub>     | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock   |           | 0.300  | 1                     | ms     | 1,2   |
| Input SS Modulation Frequency | f <sub>MODIN</sub>    | Allowable Frequency (Triangular Modulation)   | 30        |        | 33                    | kHz    | 1     |
| OE# Latency                   | t <sub>LATOE#</sub>   | DIF start after OE# assertion<br>DIF stop after OE# deassertion   | 4         | 6      | 12                    | clocks | 1     |
| Tdrive_PD#                    | t <sub>DRVPD</sub>    | DIF output enable after PD# de-assertion  |           | 16     | 300                   | us     | 1,3   |
| Tfall                         | t <sub>F</sub>        | Fall time of control inputs   |           |        | 10                    | ns     | 1,2   |
| Trise                         | t <sub>R</sub>        | Rise time of control inputs   |           |        | 10                    | ns     | 1,2   |
| SMBus Input Low Voltage       | V <sub>ILSMB</sub>    |   |           |        | 0.8                   | V      | 1     |
| SMBus Input High Voltage      | V <sub>IHSMB</sub>    |   | 2.1       |        | V <sub>DD</sub> SMB   | V      | 1     |
| SMBus Output Low Voltage      | V <sub>OLSMB</sub>    | @ I <sub>PULLUP</sub>   |           |        | 0.4                   | V      | 1     |
| SMBus Sink Current            | I <sub>PULLUP</sub>   | @ V <sub>OL</sub>   | 4         |        |                       | mA     | 1     |
| Nominal Bus Voltage           | V <sub>DD</sub> SMB   | 3V to 5V +/- 10%  | 2.7       |        | 5.5                   | V      | 1     |
| SCLK/SDATA Rise Time          | t <sub>RSMB</sub>     | (Max V <sub>IL</sub> - 0.15) to (Min V <sub>IH</sub> + 0.15)  |           |        | 1000                  | ns     | 1     |
| SCLK/SDATA Fall Time          | t <sub>FSMB</sub>     | (Min V <sub>IH</sub> + 0.15) to (Max V <sub>IL</sub> - 0.15)  |           |        | 300                   | ns     | 1     |
| SMBus Operating Frequency     | f <sub>MAXSMB</sub>   | Maximum SMBus operating frequency   |           |        | 100                   | kHz    | 1,5   |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active

**Electrical Characteristics - DIF\_IN Clock Input Parameters**

T<sub>AMB</sub>=T<sub>COM</sub> unless otherwise indicated, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER                        | SYMBOL             | CONDITIONS  | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|--------------------|---|-----|-----|-----|-------|-------|
| Input Crossover Voltage - DIF_IN | V <sub>CROSS</sub> | Cross Over Voltage  | 150 |     | 900 | mV    | 1     |
| Input Swing - DIF_IN             | V <sub>SWING</sub> | Differential value  | 300 |     |     | mV    | 1     |
| Input Slew Rate - DIF_IN         | dv/dt              | Measured differentially                                   | 0.4 |     | 8   | V/ns  | 1,2   |
| Input Leakage Current            | I <sub>IN</sub>    | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND | -5  |     | 5   | uA    |       |
| Input Duty Cycle                 | d <sub>in</sub>    | Measurement from differential waveform                    | 45  |     | 55  | %     | 1     |
| Input Jitter - Cycle to Cycle    | J <sub>DIFin</sub> | Differential Measurement                                  | 0   |     | 125 | ps    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Slew rate measured through +/-75mV window centered around differential zero

**Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs**

T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V +/-5%

| PARAMETER              | SYMBOL     | CONDITIONS  | MIN  | TYP  | MAX  | UNITS | NOTES   |
|------------------------|------------|---|------|------|------|-------|---------|
| Slew rate              | Trf        | Scope averaging on  | 1    | 2    | 4    | V/ns  | 1, 2, 3 |
| Slew rate matching     | ΔTrf       | Slew rate matching, Scope averaging on  |      | 8    | 20   | %     | 1, 2, 4 |
| Voltage High           | VHigh      | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660  | 705  | 850  | mV    | 1       |
| Voltage Low            | VLow       |   | -150 | 1    | 150  |       | 1       |
| Max Voltage            | Vmax       | Measurement on single ended signal using absolute value. (Scope averaging off)                        |      | 725  | 1150 | mV    | 1       |
| Min Voltage            | Vmin       |   | -300 | -22  |      |       | 1       |
| Vswing                 | Vswing     | Scope averaging off   | 300  | 1407 |      | mV    | 1, 2    |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off   | 250  | 309  | 550  | mV    | 1, 5    |
| Crossing Voltage (var) | ΔVcross    | Scope averaging off   |      | 22   | 140  | mV    | 1, 6    |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production. I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 412Ω (1%), I<sub>REF</sub> = 2.7mA.

I<sub>OH</sub> = 6.4 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub>=85Ω differential impedance.

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

<sup>5</sup> Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all Vcross measurements in any particular system. Note that this is a subset of V<sub>cross\_min</sub>/max (V<sub>cross</sub> absolute) allowed. The intent is to limit Vcross induced modulation by setting V<sub>cross\_delta</sub> to be smaller than V<sub>cross</sub> absolute.

**Electrical Characteristics - Current Consumption**

T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V +/-5%

| PARAMETER         | SYMBOL                | CONDITIONS  | MIN | TYP | MAX | UNITS | NOTES |
|-------------------|-----------------------|---|-----|-----|-----|-------|-------|
| Operating Current | I <sub>DDVDD</sub>    | 133MHz, C <sub>L</sub> = Full load; VDD rail, Z <sub>O</sub> =85Ω |     | 260 | 275 | mA    | 1     |
|                   | I <sub>DDVDDA</sub>   | 133MHz, C <sub>L</sub> = Full load; VDD rail, Z <sub>O</sub> =85Ω |     | 13  | 20  | mA    | 1     |
| Powerdown Current | I <sub>DDVDDPD</sub>  | Power Down, VDD rail, Z <sub>O</sub> =85Ω                         |     | 2   | 6   | mA    | 1     |
|                   | I <sub>DDVDDAPD</sub> | Power Down, VDD rail, Z <sub>O</sub> =85Ω                         |     | 1.3 | 2   | mA    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

**Electrical Characteristics - Skew and Differential Jitter Parameters**T<sub>A</sub> = T<sub>COMI</sub>; Supply Voltage V<sub>DD</sub>/V<sub>DPA</sub> = 3.3 V +/-5%

| PARAMETER              | SYMBOL                 | CONDITIONS  | MIN  | TYP  | MAX | UNITS       | NOTES     |
|------------------------|------------------------|---|------|------|-----|-------------|-----------|
| CLK_IN, DIF[x:0]       | t <sub>SPO_PLL</sub>   | Input-to-Output Skew in PLL mode<br>nominal value @ 25°C, 3.3V                              | -100 | 29   | 100 | ps          | 1,2,4,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>PD_BYP</sub>    | Input-to-Output Skew in Bypass mode<br>nominal value @ 25°C, 3.3V                           | 2.5  | 3.7  | 4.5 | ns          | 1,2,3,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>DSPO_PLL</sub>  | Input-to-Output Skew Variation in PLL mode<br>across voltage and temperature                | -50  |      | 50  | ps          | 1,2,3,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>DSPO_BYP</sub>  | Input-to-Output Skew Variation in Bypass mode<br>across voltage and temperature             | -250 |      | 250 | ps          | 1,2,3,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>DTE</sub>       | Random Differential Tracking error between two<br>9ZX devices in Hi BW Mode                 |      | 2.9  | 5   | ps<br>(rms) | 1,2,3,5,8 |
| CLK_IN, DIF[x:0]       | t <sub>DSSTE</sub>     | Random Differential Spread Spectrum Tracking<br>error between two 9ZX devices in Hi BW Mode |      | 14   | 75  | ps          | 1,2,3,5,8 |
| DIF[x:0]               | t <sub>SKREW_ALL</sub> | Output-to-Output Skew across all outputs<br>(Common to Bypass and PLL mode)                 |      | 32   | 65  | ps          | 1,2,3,8   |
| PLL Jitter Peaking     | j <sub>peak-hibw</sub> | LOBW#_BYPASS_HIBW = 1   | 0    | 1.8  | 2.5 | dB          | 7,8       |
| PLL Jitter Peaking     | j <sub>peak-lobw</sub> | LOBW#_BYPASS_HIBW = 0   | 0    | 0.7  | 2   | dB          | 7,8       |
| PLL Bandwidth          | p <sub>ll_HIBW</sub>   | LOBW#_BYPASS_HIBW = 1   | 2    | 3.1  | 4   | MHz         | 8,9       |
| PLL Bandwidth          | p <sub>ll_LOBW</sub>   | LOBW#_BYPASS_HIBW = 0   | 0.7  | 1.1  | 1.4 | MHz         | 8,9       |
| Duty Cycle             | t <sub>DC</sub>        | Measured differentially, PLL Mode   | 45   | 49.6 | 55  | %           | 1         |
| Duty Cycle Distortion  | t <sub>DCD</sub>       | Measured differentially, Bypass Mode<br>@100MHz   | -2   | -0.2 | 2   | %           | 1,10      |
| Jitter, Cycle to cycle | t <sub>jyc-cyc</sub>   | PLL mode  |      | 15.7 | 50  | ps          | 1,11      |
|                        |                        | Additive Jitter in Bypass Mode  |      | 0.1  | 50  | ps          | 1,11      |

**Notes for preceding table:**

- <sup>1</sup> Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
- <sup>2</sup> Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.
- <sup>3</sup> All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
- <sup>4</sup> This parameter is deterministic for a given device
- <sup>5</sup> Measured with scope averaging on to find mean value.
- <sup>6</sup> t is the period of the input clock
- <sup>7</sup> Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
- <sup>8</sup> Guaranteed by design and characterization, not 100% tested in production.
- <sup>9</sup> Measured at 3 db down or half power point.
- <sup>10</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
- <sup>11</sup> Measured from differential waveform

### Electrical Characteristics - Phase Jitter Parameters

T<sub>A</sub> = T<sub>COM</sub>; Supply Voltage V<sub>DD</sub>/V<sub>DDA</sub> = 3.3 V +/-5%

| PARAMETER                             | SYMBOL                 | CONDITIONS   | MIN  | TYP  | MAX      | UNITS    | Notes   |
|---------------------------------------|------------------------|--|------|------|----------|----------|---------|
| Phase Jitter, PLL Mode                | t <sub>phPCIeG1</sub>  | PCIe Gen 1   |      | 32   | 86       | ps (p-p) | 1,2,3   |
|                                       | t <sub>phPCIeG2</sub>  | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz               |      | 0.8  | 3        | ps (rms) | 1,2     |
|                                       |                        | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)   |      | 1.9  | 3.1      | ps (rms) | 1,2     |
|                                       | t <sub>phPCIeG3</sub>  | PCIe Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)          |      | 0.45 | 1        | ps (rms) | 1,2,4   |
|                                       | t <sub>phQPI_SMI</sub> | QPI & SMI<br>(100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) |      | 0.20 | 0.5      | ps (rms) | 1,5     |
|                                       |                        | QPI & SMI<br>(100MHz, 8.0Gb/s, 12UI)                   |      | 0.14 | 0.3      | ps (rms) | 1,5     |
| QPI & SMI<br>(100MHz, 9.6Gb/s, 12UI)  |                        |  | 0.12 | 0.2  | ps (rms) | 1,5      |         |
| Additive Phase Jitter,<br>Bypass mode | t <sub>phPCIeG1</sub>  | PCIe Gen 1   |      | 0.10 | 10       | ps (p-p) | 1,2,3   |
|                                       | t <sub>phPCIeG2</sub>  | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz               |      | 0.13 | 0.3      | ps (rms) | 1,2,6   |
|                                       |                        | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz)   |      | 0.10 | 0.7      | ps (rms) | 1,2,6   |
|                                       | t <sub>phPCIeG3</sub>  | PCIe Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)          |      | 0.10 | 0.3      | ps (rms) | 1,2,4,6 |
|                                       | t <sub>phQPI_SMI</sub> | QPI & SMI<br>(100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) |      | 0.09 | 0.3      | ps (rms) | 1,5,6   |
|                                       |                        | QPI & SMI<br>(100MHz, 8.0Gb/s, 12UI)                   |      | 0.09 | 0.1      | ps (rms) | 1,5,6   |
| QPI & SMI<br>(100MHz, 9.6Gb/s, 12UI)  |                        |  | 0.09 | 0.1  | ps (rms) | 1,5,6    |         |

<sup>1</sup> Applies to all outputs.

<sup>2</sup> See <http://www.pcisig.com> for complete specs

<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup> Subject to final radification by PCI SIG.

<sup>5</sup> Calculated from Intel-supplied Clock Jitter Tool v 1.6.4

<sup>6</sup> For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)<sup>2</sup> = (total jitter)<sup>2</sup> - (input jitter)<sup>2</sup>

### Power Management Table

| Inputs       |                    | Control Bits/Pins |         |                          | Outputs              | PLL State |
|--------------|--------------------|-------------------|---------|--------------------------|----------------------|-----------|
| CKPWRGD•/PD# | DIF_IN/<br>DIF_IN# | SMBus<br>EN bit   | OE# Pin | DIF(11:0)/<br>DIF(11:0)# | DFB_OUT/<br>DFB_OUT# |           |
| 0            | X                  | X                 | X       | Hi-Z <sup>1</sup>        | Hi-Z <sup>1</sup>    | OFF       |
| 1            | Running            | 0                 | X       | Hi-Z <sup>1</sup>        | Running              | ON        |
|              |                    | 1                 | 0       | Running                  | Running              | ON        |
|              |                    | 1                 | 1       | Hi-Z <sup>1</sup>        | Running              | ON        |

#### NOTE:

1. Due to external pull down resistors, HI-Z results in Low/Low on the True/Complement outputs

**Clock Periods - Differential Outputs with Spread Spectrum Disabled**

| SSC OFF | Center Freq. MHz | Measurement Window     |                             |                             |                      |                             |                             |                        | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
|         |                  | 1 Clock                | 1us                         | 0.1s                        | 0.1s                 | 0.1s                        | 1us                         | 1 Clock                |       |       |
|         |                  | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max |       |       |
| DIF     | 100.00           | 9.94900                |                             | 9.99900                     | 10.00000             | 10.00100                    |                             | 10.05100               | ns    | 1,2,3 |
|         | 133.33           | 7.44925                |                             | 7.49925                     | 7.50000              | 7.50075                     |                             | 7.55075                | ns    | 1,2,4 |

**Clock Periods - Differential Outputs with Spread Spectrum Enabled**

| SSC ON | Center Freq. MHz | Measurement Window     |                             |                             |                      |                             |                             |                        | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
|        |                  | 1 Clock                | 1us                         | 0.1s                        | 0.1s                 | 0.1s                        | 1us                         | 1 Clock                |       |       |
|        |                  | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max |       |       |
| DIF    | 99.75            | 9.94906                | 9.99906                     | 10.02406                    | 10.02506             | 10.02607                    | 10.05107                    | 10.10107               | ns    | 1,2,3 |
|        | 133.00           | 7.44930                | 7.49930                     | 7.51805                     | 7.51880              | 7.51955                     | 7.53830                     | 7.58830                | ns    | 1,2,4 |

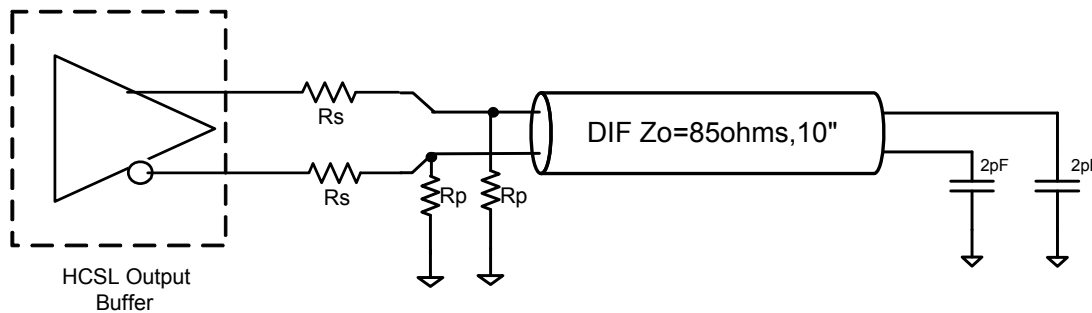
**Notes:**

- <sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.
- <sup>2</sup>All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZX21201 itself does not contribute to ppm error.
- <sup>3</sup> Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode
- <sup>4</sup> Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

**Differential Output Termination Table**

| DIF Zo (Ω) | Iref (Ω) | Rs (Ω) | Rp (Ω)       |
|------------|----------|--------|--------------|
| 100        | 475      | 33     | 50           |
| 85         | 412      | 27     | 42.2 or 43.2 |

**9ZX21201 Differential Test Loads**



## General SMBus serial interface information for the 9ZX21201

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $XX_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the data byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $XX_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $YY_{(H)}$
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends **Byte N + X - 1**
- IDT clock sends **Byte 0 through byte X (if  $X_{(H)}$  was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation |           |                      |
|-----------------------------|-----------|----------------------|
| Controller (Host)           |           | IDT (Slave/Receiver) |
| T                           | starT bit |                      |
| Slave Address $XX_{(H)}$    |           |                      |
| WR                          | WRite     |                      |
|                             |           | ACK                  |
| Beginning Byte = N          |           |                      |
|                             |           | ACK                  |
| Data Byte Count = X         |           |                      |
|                             |           | ACK                  |
| Beginning Byte N            | X Byte    |                      |
| ◇                           |           | ACK                  |
| ◇                           |           | ◇                    |
| ◇                           |           | ◇                    |
| Byte N + X - 1              |           | ◇                    |
|                             |           | ACK                  |
| P                           | stoP bit  |                      |

Note:  $XX_{(H)}$  is defined by SMBus address select pins.

| Index Block Read Operation |                 |                      |
|----------------------------|-----------------|----------------------|
| Controller (Host)          |                 | IDT (Slave/Receiver) |
| T                          | starT bit       |                      |
| Slave Address $XX_{(H)}$   |                 |                      |
| WR                         | WRite           |                      |
|                            |                 | ACK                  |
| Beginning Byte = N         |                 |                      |
|                            |                 | ACK                  |
| RT                         | Repeat starT    |                      |
| Slave Address $YY_{(H)}$   |                 |                      |
| RD                         | ReaD            |                      |
|                            |                 | ACK                  |
|                            |                 | Data Byte Count = X  |
| ACK                        |                 |                      |
|                            |                 | Beginning Byte N     |
| ACK                        |                 |                      |
| ◇                          |                 | X Byte               |
| ◇                          |                 |                      |
| ◇                          |                 |                      |
| ◇                          |                 |                      |
|                            |                 | Byte N + X - 1       |
| N                          | Not acknowledge |                      |
| P                          | stoP bit        |                      |

SMBusTable: PLL Mode, and Frequency Select Register

| Byte 0 | Pin #                               | Name       | Control Function             | Type | 0                                     | 1           | Default |
|--------|-------------------------------------|------------|------------------------------|------|---------------------------------------|-------------|---------|
| Bit 7  | 5                                   | PLL Mode 1 | PLL Operating Mode Rd back 1 | R    | See PLL Operating Mode Readback Table |             | Latch   |
| Bit 6  | 5                                   | PLL Mode 0 | PLL Operating Mode Rd back 0 | R    |                                       |             | Latch   |
| Bit 5  |                                     |            | Reserved                     |      |                                       |             | 0       |
| Bit 4  |                                     |            | Reserved                     |      |                                       |             | 0       |
| Bit 3  | These bits available in B rev only. | PLL_SW_EN  | Enable S/W control of PLL BW | RW   | HW Latch                              | S/W Control | 0       |
| Bit 2  |                                     | PLL Mode 1 | PLL Operating Mode 1         | RW   | See PLL Operating Mode Readback Table |             | 1       |
| Bit 1  |                                     | PLL Mode 0 | PLL Operating Mode 1         | RW   |                                       |             | 1       |
| Bit 0  | 4                                   | 100M 133M# | Frequency Select Readback    | R    | 133MHz                                | 100MHz      | Latch   |

SMBusTable: Output Control Register

| Byte 1 | Pin # | Name     | Control Function                       | Type | 0       | 1      | Default |
|--------|-------|----------|--|------|---------|--------|---------|
| Bit 7  | 47/46 | DIF 7 En | Output Control - '0' overrides OE# pin | RW   | Low/Low | Enable | 1       |
| Bit 6  | 43/42 | DIF 6 En | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |
| Bit 5  | 39/38 | DIF 5 En | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |
| Bit 4  | 35/34 | DIF 4 En | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |
| Bit 3  | 30/31 | DIF 3 En | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |
| Bit 2  | 26/27 | DIF 2 En | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |
| Bit 1  | 21/22 | DIF 1 En | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |
| Bit 0  | 17/18 | DIF 0 En | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |

SMBusTable: Output Control Register

| Byte 2 | Pin # | Name      | Control Function                       | Type | 0       | 1      | Default |
|--------|-------|-----------|--|------|---------|--------|---------|
| Bit 7  |       |           | Reserved                               |      |         |        | 0       |
| Bit 6  |       |           | Reserved                               |      |         |        | 0       |
| Bit 5  |       |           | Reserved                               |      |         |        | 0       |
| Bit 4  |       |           | Reserved                               |      |         |        | 0       |
| Bit 3  | 64/63 | DIF 11 En | Output Control - '0' overrides OE# pin | RW   | Low/Low | Enable | 1       |
| Bit 2  | 59/60 | DIF 10 En | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |
| Bit 1  | 54/55 | DIF 9 En  | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |
| Bit 0  | 50/51 | DIF 8 En  | Output Control - '0' overrides OE# pin | RW   |         |        | 1       |

SMBusTable: Reserved Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | 0       |
| Bit 6  |       |      | Reserved         |      |   |   | 0       |
| Bit 5  |       |      | Reserved         |      |   |   | 0       |
| Bit 4  |       |      | Reserved         |      |   |   | 0       |
| Bit 3  |       |      | Reserved         |      |   |   | 0       |
| Bit 2  |       |      | Reserved         |      |   |   | 0       |
| Bit 1  |       |      | Reserved         |      |   |   | 0       |
| Bit 0  |       |      | Reserved         |      |   |   | 0       |

SMBusTable: Reserved Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | 0       |
| Bit 6  |       |      | Reserved         |      |   |   | 0       |
| Bit 5  |       |      | Reserved         |      |   |   | 0       |
| Bit 4  |       |      | Reserved         |      |   |   | 0       |
| Bit 3  |       |      | Reserved         |      |   |   | 0       |
| Bit 2  |       |      | Reserved         |      |   |   | 0       |
| Bit 1  |       |      | Reserved         |      |   |   | 0       |
| Bit 0  |       |      | Reserved         |      |   |   | 0       |

SMBusTable: Vendor &amp; Revision ID Register

| Byte 5 | Pin # | Name | Control Function | Type | 0                            | 1 | Default |
|--------|-------|------|------------------|------|------------------------------|---|---------|
| Bit 7  | -     | RID3 | REVISION ID      | R    | A rev = 0000<br>B rev = 0001 |   | X       |
| Bit 6  | -     | RID2 |                  | R    |                              |   | X       |
| Bit 5  | -     | RID1 |                  | R    |                              |   | X       |
| Bit 4  | -     | RID0 |                  | R    |                              |   | X       |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | 0001 for IDT/ICS             |   | 0       |
| Bit 2  | -     | VID2 |                  | R    |                              |   | 0       |
| Bit 1  | -     | VID1 |                  | R    |                              |   | 0       |
| Bit 0  | -     | VID0 |                  | R    |                              |   | 1       |

SMBusTable: DEVICE ID

| Byte 6 | Pin # | Name | Control Function  | Type | 0                             | 1 | Default |
|--------|-------|------|-------------------|------|-------------------------------|---|---------|
| Bit 7  | -     |      | Device ID 7 (MSB) | R    | 1201 is 201 decimal or C9 hex |   | 1       |
| Bit 6  | -     |      | Device ID 6       | R    |                               |   | 1       |
| Bit 5  | -     |      | Device ID 5       | R    |                               |   | 0       |
| Bit 4  | -     |      | Device ID 4       | R    |                               |   | 0       |
| Bit 3  | -     |      | Device ID 3       | R    |                               |   | 1       |
| Bit 2  | -     |      | Device ID 2       | R    |                               |   | 0       |
| Bit 1  | -     |      | Device ID 1       | R    |                               |   | 0       |
| Bit 0  | -     |      | Device ID 0       | R    |                               |   | 1       |

SMBusTable: Byte Count Register

| Byte 7 | Pin # | Name | Control Function  | Type | 0   | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7  |       |      | Reserved  |      |   |   | 0       |
| Bit 6  |       |      | Reserved  |      |   |   | 0       |
| Bit 5  |       |      | Reserved  |      |   |   | 0       |
| Bit 4  | -     | BC4  | Writing to this register configures how many bytes will be read back. | RW   | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. |   | 0       |
| Bit 3  | -     | BC3  |   | RW   |   |   | 1       |
| Bit 2  | -     | BC2  |   | RW   |   |   | 0       |
| Bit 1  | -     | BC1  |   | RW   |   |   | 0       |
| Bit 0  | -     | BC0  |   | RW   |   |   | 0       |

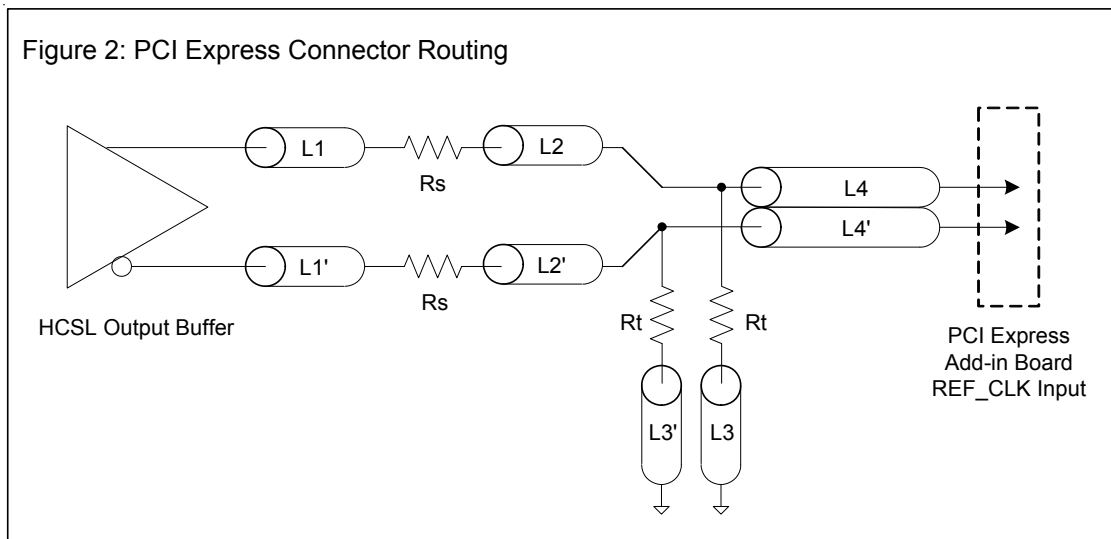
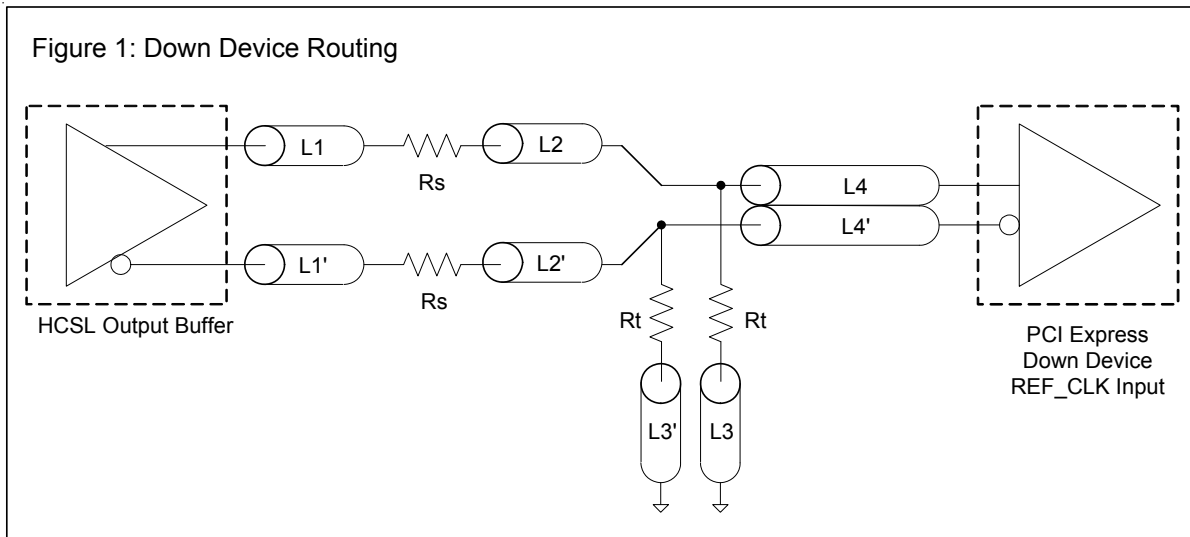
SMBusTable: Reserved Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | 0       |
| Bit 6  |       |      | Reserved         |      |   |   | 0       |
| Bit 5  |       |      | Reserved         |      |   |   | 0       |
| Bit 4  |       |      | Reserved         |      |   |   | 0       |
| Bit 3  |       |      | Reserved         |      |   |   | 0       |
| Bit 2  |       |      | Reserved         |      |   |   | 0       |
| Bit 1  |       |      | Reserved         |      |   |   | 0       |
| Bit 0  |       |      | Reserved         |      |   |   | 0       |

| DIF Reference Clock                             |                    |      |        |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace     | 0.5 max            | inch | 1      |
| L2 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| L3 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| $R_s$   | 33                 | ohm  | 1      |
| $R_t$   | 49.9               | ohm  | 1      |

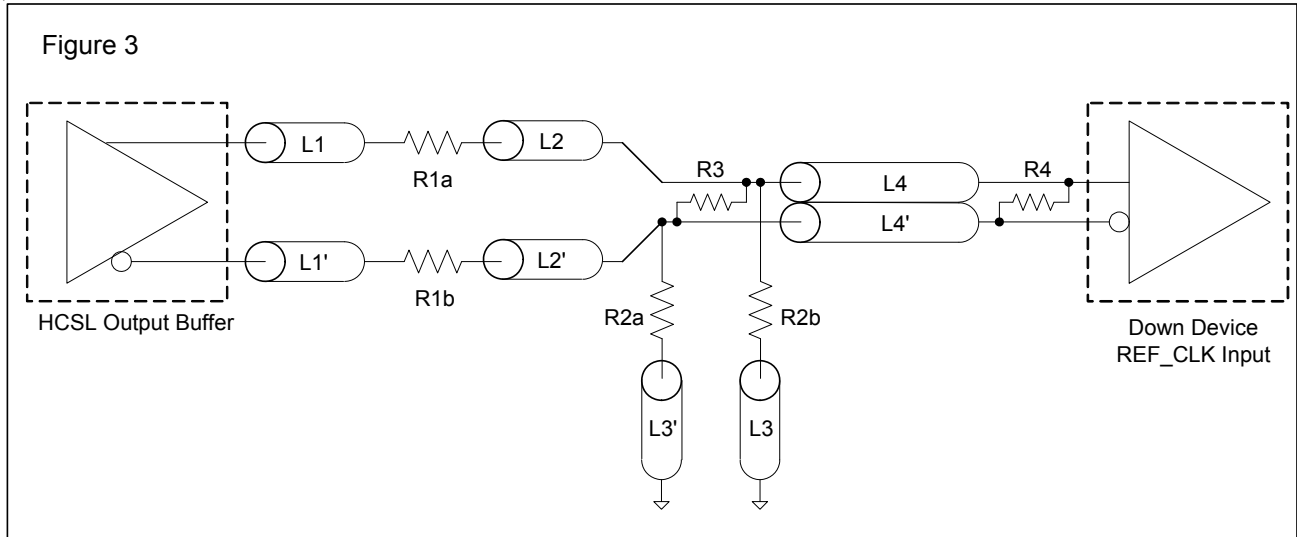
| Down Device Differential Routing                                 |                     |      |   |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max     | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace  | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector                    |                       |      |   |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max        | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace  | 0.225 min to 12.6 max | inch | 2 |

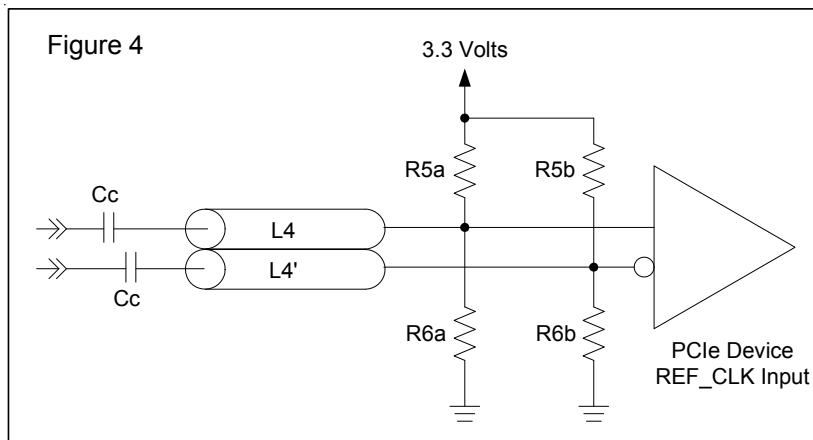


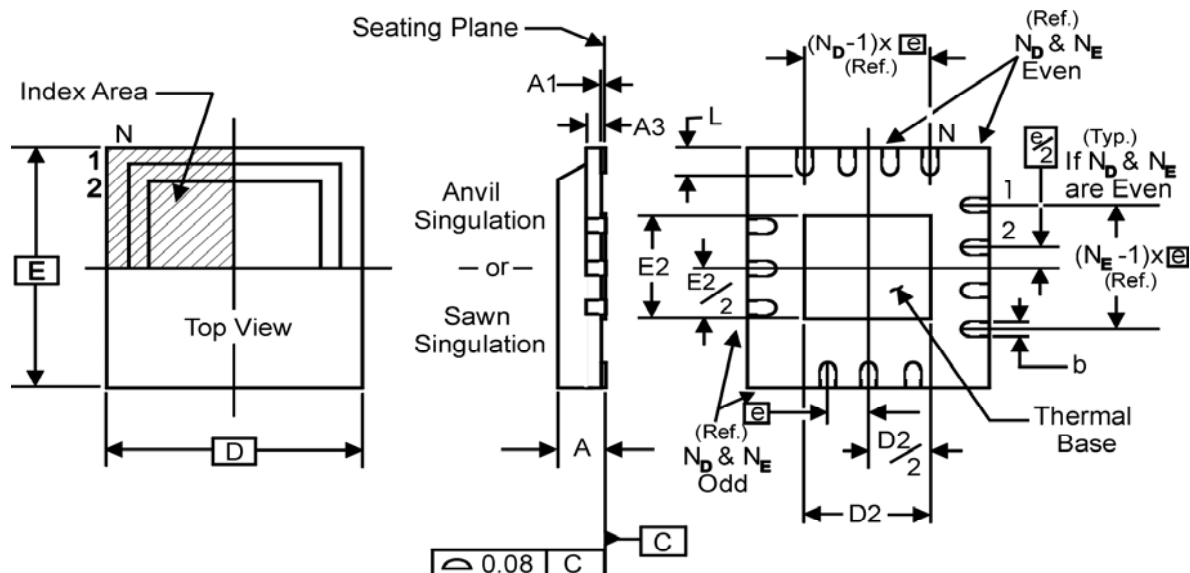
| Alternative Termination for LVDS and other Common Differential Signals (figure 3) |                  |                 |    |      |      |     |                                |
|---|------------------|-----------------|----|------|------|-----|--------------------------------|
| V <sub>diff</sub>   | V <sub>p-p</sub> | V <sub>cm</sub> | R1 | R2   | R3   | R4  | Note                           |
| 0.45v   | 0.22v            | 1.08            | 33 | 150  | 100  | 100 |                                |
| 0.58  | 0.28             | 0.6             | 33 | 78.7 | 137  | 100 |                                |
| 0.80  | 0.40             | 0.6             | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60  | 0.3              | 1.2             | 33 | 174  | 140  | 100 | Standard LVDS                  |

R1a = R1b = R1  
R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) |             |      |
|---|-------------|------|
| Component   | Value       | Note |
| R5a, R5b  | 8.2K 5%     |      |
| R6a, R6b  | 1K 5%       |      |
| Cc  | 0.1 μF      |      |
| V <sub>cm</sub>                                   | 0.350 volts |      |





**THERMALLY ENHANCED, VERY THIN, FINE PITCH  
QUAD FLAT / NO LEAD PLASTIC PACKAGE**

**DIMENSIONS**

| SYMBOL | 64L |
|--------|-----|
| N      | 64  |
| $N_D$  | 16  |
| $N_E$  | 16  |

**DIMENSIONS (mm)**

| SYMBOL         | MIN.           | MAX. |
|----------------|----------------|------|
| A              | 0.8            | 1.0  |
| A1             | 0              | 0.05 |
| A3             | 0.25 Reference |      |
| b              | 0.18           | 0.3  |
| e              | 0.50 BASIC     |      |
| D x E BASIC    | 9.00 x 9.00    |      |
| D2 MIN. / MAX. | 6.00           | 6.25 |
| E2 MIN. / MAX. | 6.00           | 6.25 |
| L MIN. / MAX.  | 0.30           | 0.50 |

## Ordering Information

| Part / Order Number | Shipping Package | Package    | Temperature | Difference                   |
|---------------------|------------------|------------|-------------|------------------------------|
| 9ZX21201AKLF        | Trays            | 64-pin MLF | 0 to +70°C  | W/O Byte 0 PLL Control       |
| 9ZX21201AKLFT       | Tape and Reel    | 64-pin MLF | 0 to +70°C  |                              |
| 9ZX21201BKLF        | Trays            | 64-pin MLF | 0 to +70°C  | With Byte 0 PLL Mode Control |
| 9ZX21201BKLFT       | Tape and Reel    | 64-pin MLF | 0 to +70°C  |                              |

"LF" designates PB-free configuration, RoHS compliant.

"A and B" are the device revision designators (will not correlate with the datasheet revision).

**Revision History**

| <b>Rev.</b> | <b>Issuer</b> | <b>Issue Date</b> | <b>Description</b>   | <b>Page #</b> |
|-------------|---------------|-------------------|--|---------------|
| A           | RDW           | 9/13/2011         | 1. Updated electrical tables with char data<br>2. Fixed minor typographical errors<br>3. Moved to final  | Various       |
| B           | RDW           | 12/8/2011         | 1. Added B rev functionality description to Features, Benefits<br>2. Updated tDSPO_BYP parameter from +/-350ps to +/-250ps<br>3. Updated SMBus Byte 0 with B rev functionality<br>4. Updated ordering information to include B rev | 1,7,11,15     |
| C           | RDW           | 4/18/20112        | 1. Updated Power connections table to be consistent with 9ZXL1231.<br>2. Updated Rp value for 85 ohm differential Zo from 43.2ohms to 42.2 OR 43.2 ohms to be consistent with Intel recommendations.                               | 2,9           |
| D           | RDW           | 5/5/2014          | 1. Fixed error in feedback path on block diagram   | 1             |
| E           | RDW           | 11/19/2015        | 1. Updated the DIF_IN Input clock specification to align with the PCIe SIG specification.  | 6             |

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