



**THE DATASHEET OF
9112AG-27LFT**





Low Skew Output Buffer

General Description

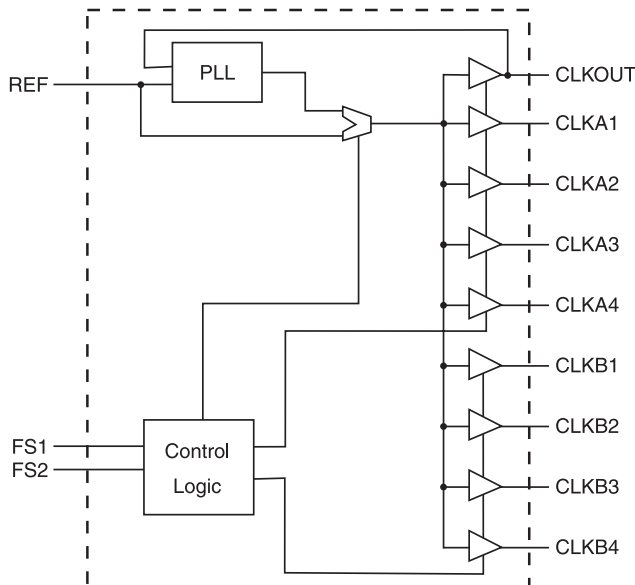
The **ICS9112-17** is a high performance, low skew, low jitter zero delay buffer. It uses a phase lock loop (PLL) technology to align, in both phase and frequency, the REF input with the CLKOUT signal. It is designed to distribute high speed clocks in PC systems operating at speeds from 25 to 133 MHz.

ICS9112-17 is a zero delay buffer that provides synchronization between the input and output. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than +/- 350 pS, the part acts as a zero delay buffer.

The **ICS9112-17** has two banks of four outputs controlled by two address lines. Depending on the selected address line, bank B or both banks can be put in a tri-state mode. In this mode, the PLL is still running and only the output buffers are put in a high impedance mode. The test mode shuts off the PLL and connects the input directly to the output buffers (see table below for functionality).

The **ICS9112-17** comes in a sixteen pin 150 mil SOIC or 16 pin SSOP package. In the absence of REF input, will be in the power down mode. In this mode, the PLL is turned off and the output buffers are pulled low. Power down mode provides the lowest power consumption for a standby condition.

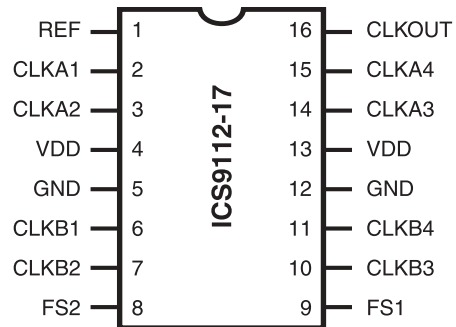
Block Diagram



Features

- Zero input - output delay
- Frequency range 25 - 133 MHz (3.3V)
- High loop filter bandwidth ideal for Spread Spectrum applications.
- Less than 200 ps cycle to cycle Jitter
- Skew controlled outputs
- Skew less than 250 ps between outputs
- Available in 16 pin, 150 mil SSOP & SOIC package

Pin Configuration



16 pin SSOP & SOIC

Functionality

| FS2 | FS1 | CLKA (1, 4) | CLKB (1, 4) | CLKOUT | Output Source | PLL Shutdown |
|-----|-----|-----------------|-----------------|-----------------|---------------|--------------|
| 0 | 0 | Tristate | Tristate | Driven | PLL | N |
| 0 | 1 | Driven | Tristate | Driven | PLL | N |
| 1 | 0 | PLL Bypass Mode | PLL Bypass Mode | PLL Bypass Mode | REF | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |



Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|------------|---------------------|------|------------------------------------------------------|
| 1 | REF ² | IN | Input reference frequency. |
| 2 | CLKA1 ³ | OUT | Buffered clock output, Bank A |
| 3 | CLKA2 ³ | OUT | Buffered clock output, Bank A |
| 4, 13 | VDD | PWR | Power Supply (3.3V) |
| 5, 12 | GND | PWR | Ground |
| 6 | CLKB1 ³ | OUT | Buffered clock output. Bank B |
| 7 | CLKB2 ³ | OUT | Buffered clock output. Bank B |
| 8 | FS2 ⁴ | IN | Select input, bit 2 |
| 9 | FS1 ⁴ | IN | Select input, bit 1 |
| 10 | CLKB3 ³ | OUT | Buffered clock output. Bank B |
| 11 | CLKB4 ³ | OUT | Buffered clock output. Bank B |
| 14 | CLKA3 ³ | OUT | Buffered clock output, Bank A |
| 15 | CLKA4 ³ | OUT | Buffered clock output, Bank A |
| 16 | CLKOUT ³ | OUT | Buffered clock output, internal feedback on this pin |

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. Weak pull-down
3. Weak pull-down on all outputs
4. Weak pull-ups on these inputs



Absolute Maximum Ratings

- Supply Voltage 7.0 V
- Logic Inputs GND -0.5 V to V_{DD} +0.5 V
- Ambient Operating Temperature 0°C to +70°C
- Storage Temperature -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input & Supply

T_A = 0 - 70C; Supply Voltage V_{DD} = 5.0 V +/-10% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|------------------------------|----------------------------------------------|----------|-----|----------------------|-------|
| Input High Voltage | V _{IH} | | 2.0 | 2.5 | V _{DD} +0.5 | V |
| Input Low Voltage | V _{IL} | | GND -0.5 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 100 | uA |
| Input Low Current | I _{IL} | V _{IN} = 0 V; | | 19 | 50 | uA |
| Operating current | I _{DD1} | C _L = 0 pF; F _{IN} @ 66M | | 45 | 65 | mA |
| Input frequency | F _i ¹ | V _{DD} = 3.3 V; All Outputs Loaded | 25 | | 133 | MHz |
| Input Capacitance | C _{IN} ¹ | Logic Inputs | | | 5 | pF |

¹ Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input & Supply

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-10% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|------------------------------|----------------------------------------------|---------|-----|----------------------|-------|
| Input High Voltage | V _{IH} | | 2.0 | 2.0 | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | GND-0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 100 | uA |
| Input Low Current | I _{IL} | V _{IN} = 0 V; | | 19 | 50 | uA |
| Operating current | I _{DD1} | C _L = 0 pF; F _{IN} @ 66M | | 30 | 45 | mA |
| Input frequency | F _i ¹ | V _{DD} = 3.3 V; All Outputs Loaded | 25 | | 133 | MHz |
| Input Capacitance | C _{IN} ¹ | Logic Inputs | | | 5.0 | pF |

¹Guarenteed by design, not 100% tested in production.



Electrical Characteristics - OUTPUT

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 5.0 \text{ V} \pm 10\%$; $C_L = 20 - 30 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|-----------|-------------------------------------------------------|------|------|-----|----------|
| Output Impedance | R_{DSP} | $V_O = V_{DD}^*(0.5)$ | 10 | | 24 | Ω |
| Output Impedance | R_{DSN} | $V_O = V_{DD}^*(0.5)$ | 10 | | 24 | Ω |
| Output High Voltage | V_{OH} | $I_{OH} = -8 \text{ mA}$ | 2.4 | 2.9 | 5.0 | V |
| Output Low Voltage | V_{OL} | $I_{OL} = 8 \text{ mA}$ | | 0.25 | 0.4 | V |
| Rise Time ¹ | T_r | $V_{OL} = 0.8 \text{ V}, V_{OH} = 2.0 \text{ V}$ | | 0.8 | 1.5 | ns |
| Fall Time ¹ | T_f | $V_{OH} = 2.0 \text{ V}, V_{OL} = 0.8 \text{ V}$ | | 1.0 | 1.5 | ns |
| PLL Lock Time ¹ | tLOCK | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |
| Duty Cycle ¹ | D_t | $V_T = 1.4\text{V}; C_l=30\text{pF}$ | 40 | 50 | 60 | % |
| Cycle to Cycle jitter ¹ | Tcyc-cyc | at 66MHz , Loaded Outputs | | | 250 | ps |
| | Tcyc-cyc | >66MHz , Loaded Outputs | | | 200 | ps |
| Absolute Jitter ¹ | Tjabs | 10000 cycles; $C_l=30\text{pF}$ | -100 | 60 | 100 | ps |
| Jitter; 1-Sigma ¹ | Tj1s | 10000 cycles; $C_l=30\text{pF}$ | | 14 | 30 | ps |
| Skew ¹ | T_{sk} | $V_T = 1.4 \text{ V}$ (Window) Output to Output | | | 250 | ps |
| Device to Device Skew ¹ | Tdsk-Tdsk | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | | 0 | 700 | ps |
| Delay Input-Output ¹ | D_{R1} | $V_T = 1.4 \text{ V}$ | | 0 | 700 | ps |

¹ Guaranteed by design, not 100% tested in production.

Electrical Characteristics - OUTPUT

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 10\%$; $C_L = 20 - 30 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|-----------|-------------------------------------------------------|------|------|-----|----------|
| Output Impedance | R_{DSP} | $V_O = V_{DD}^*(0.5)$ | 10 | | 24 | Ω |
| Output Impedance | R_{DSN} | $V_O = V_{DD}^*(0.5)$ | 10 | | 24 | Ω |
| Output High Voltage | V_{OH} | $I_{OH} = -8 \text{ mA}$ | 2.4 | 2.9 | 3.3 | V |
| Output Low Voltage | V_{OL} | $I_{OL} = 8 \text{ mA}$ | | 0.25 | 0.4 | V |
| Rise Time ¹ | T_r | $V_{OL} = 0.8 \text{ V}, V_{OH} = 2.0 \text{ V}$ | | 1.2 | 2.0 | ns |
| Fall Time ¹ | T_f | $V_{OH} = 2.0 \text{ V}, V_{OL} = 0.8 \text{ V}$ | | 1.2 | 2.0 | ns |
| PLL Lock Time ¹ | tLOCK | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |
| Duty Cycle ¹ | D_t | $V_T = 1.4\text{V}; C_l=30\text{pF}$ | 40 | 50 | 60 | % |
| | D_t | $V_T = V_{DD}/2; F_{out} < 66.6\text{MHz}$ | 45 | 50 | 55 | % |
| Cycle to Cycle jitter ¹ | Tcyc-cyc | at 66MHz , Loaded Outputs | | | 250 | ps |
| | Tcyc-cyc | >66MHz , Loaded Outputs | | | 200 | ps |
| Absolute Jitter ¹ | Tjabs | 10000 cycles; $C_l=30\text{pF}$ | -100 | 70 | 100 | ps |
| Jitter; 1-Sigma ¹ | Tj1s | 10000 cycles; $C_l=30\text{pF}$ | | 14 | 30 | ps |
| Skew ¹ | T_{sk} | $V_T = 1.4 \text{ V}$ (Window) Output to Output | | | 250 | ps |
| Device to Device Skew ¹ | Tdsk-Tdsk | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | | 0 | 700 | ps |
| Delay Input-Output ¹ | D_{R1} | $V_T = 1.4 \text{ V}$ | | 0 | 700 | ps |

¹ Guaranteed by design, not 100% tested in production.



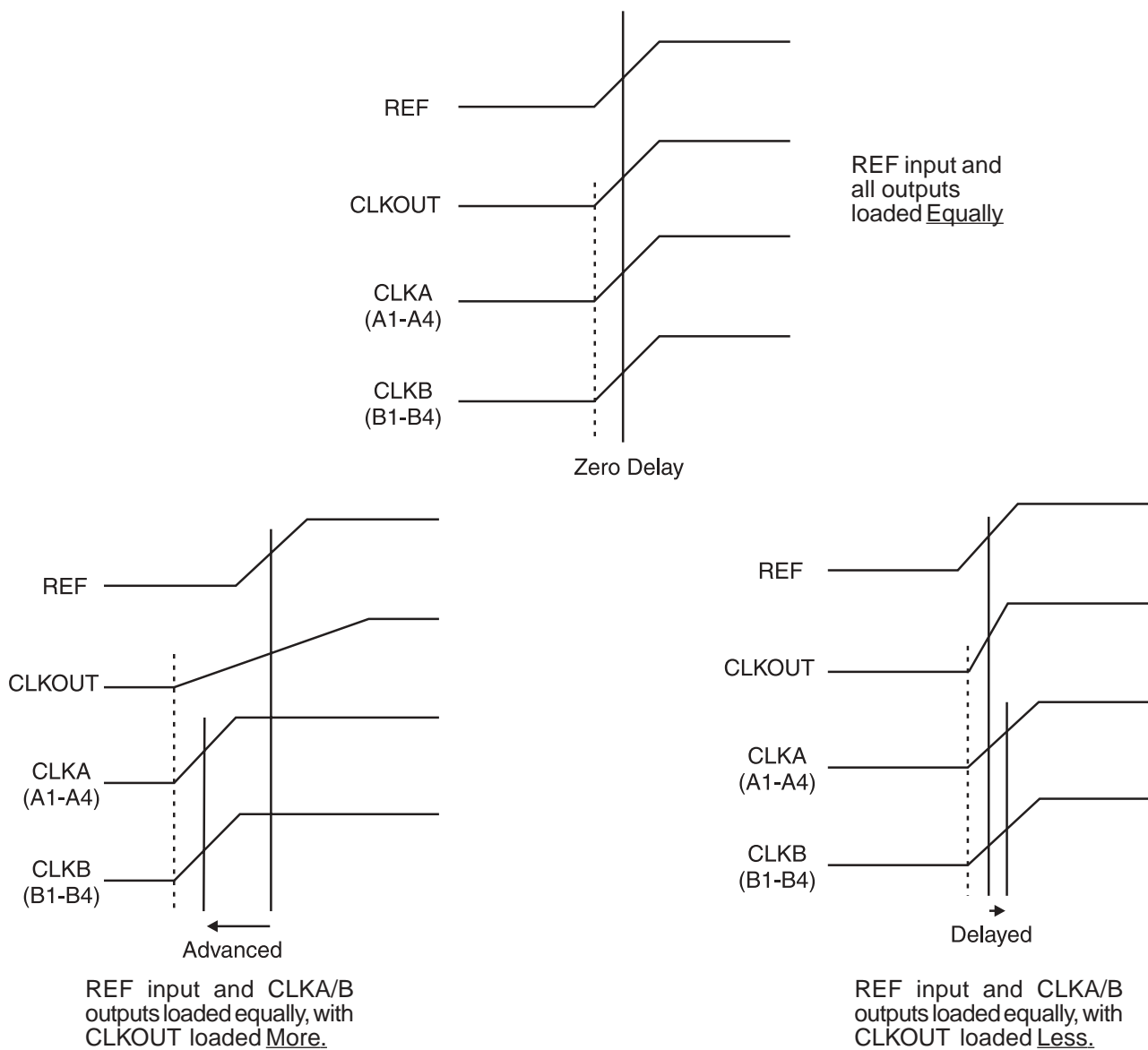
Output to Output Skew

The skew between CLKOUT and the CLKA/B outputs is not dynamically adjusted by the PLL. Since CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF to CLKOUT. If all outputs are equally loaded, zero phase difference will be maintained from REF to all outputs.

If applications requiring zero output-to-output skew, all the outputs must be equally loaded.

If the CLKA/B outputs are less loaded than CLKOUT, CLKA/B outputs will lead it; and if the CLKA/B is more loaded than CLKOUT, CLKA/B will lag the CLKOUT.

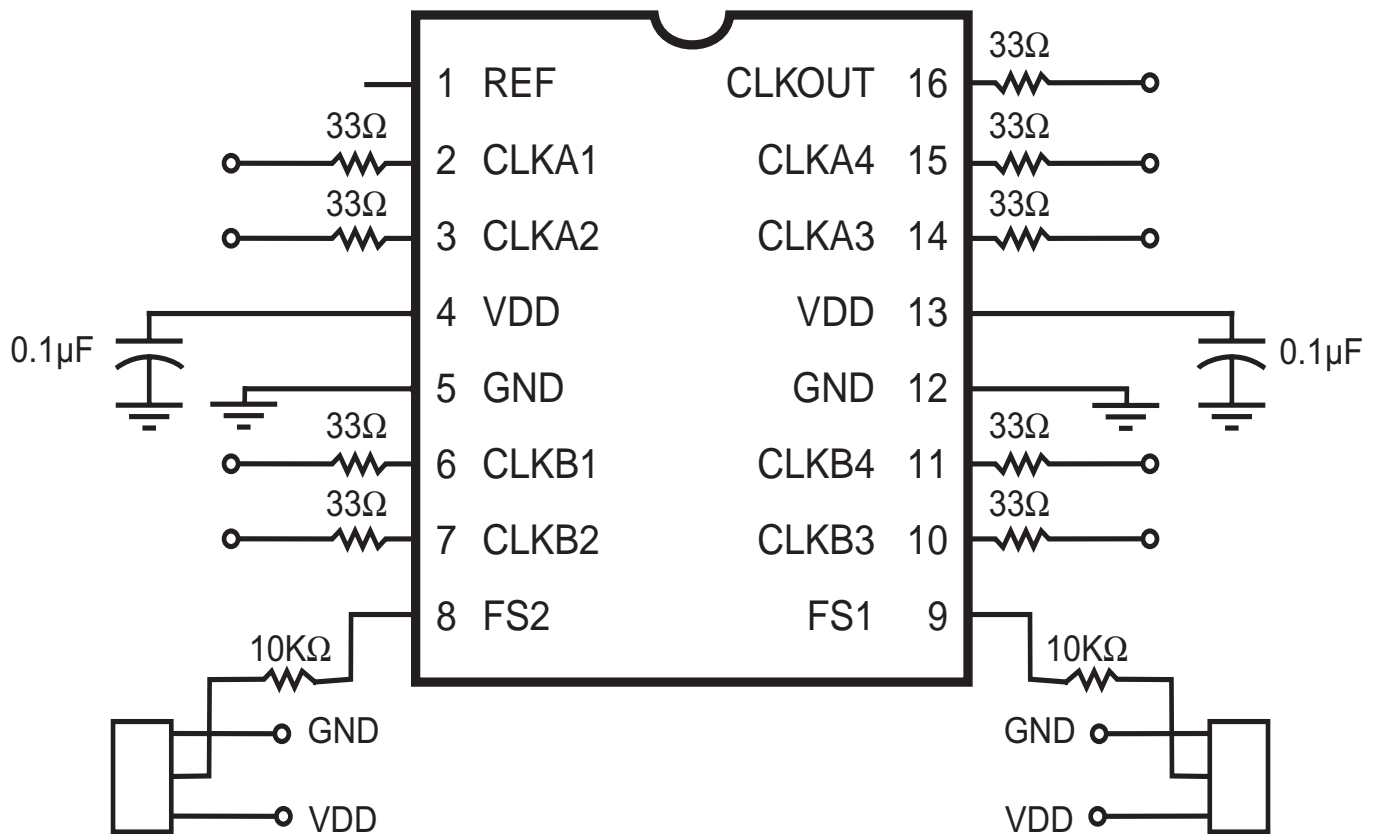
Since the CLKOUT and the CLKA/B outputs are identical, they all start at the same time, but different loads cause them to have different rise times and different times crossing the measurement thresholds.

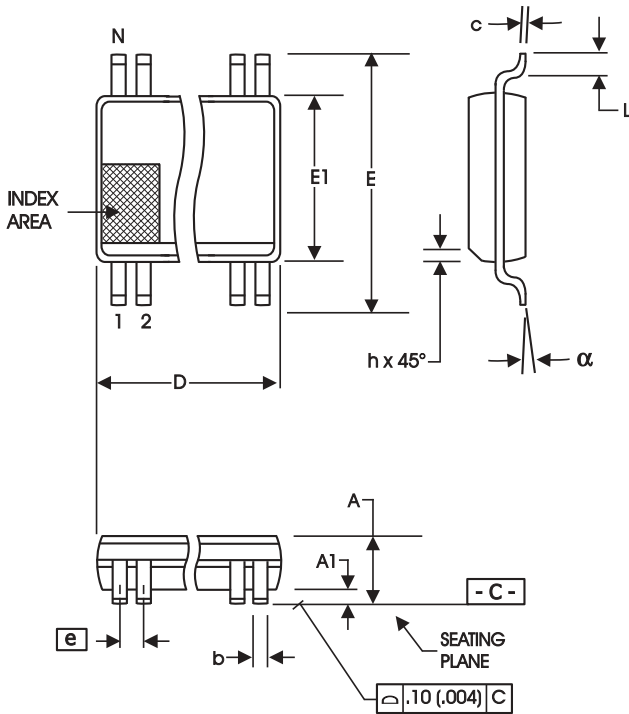




Application Suggestion:

ICS9112-17 is a mixed analog/digital product. The analog portion of the PLL is very sensitive to any random noise generated by charging or discharging of internal or external capacitor on the power supply pins. This type of noise will cause excess jitter to the outputs of ICS9112-17. Below is a recommended lay out to alleviate any addition noise. For additional information on FT. layout, please refer to our AN07. The 0.1 uF capacitors should be connected as close as possible to power pins (4 & 13). An Isolated power plane with a 2.2 uF capacitor to ground will enhance the power line stability.





150 mil SSOP (QSOP)

| SYMBOL | In Millimeters | | In Inches | |
|----------|-------------------|------|-------------------|------|
| | COMMON DIMENSIONS | | COMMON DIMENSIONS | |
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | .053 | .069 |
| A1 | 0.10 | 0.25 | .004 | .010 |
| A2 | -- | 1.50 | -- | .059 |
| b | 0.20 | 0.30 | .008 | .012 |
| c | 0.18 | 0.25 | .007 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 5.80 | 6.20 | .228 | .244 |
| E1 | 3.80 | 4.00 | .150 | .157 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| L | 0.40 | 1.27 | .016 | .050 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| ZD | SEE VARIATIONS | | SEE VARIATIONS | |

VARIATIONS

| N | D mm. | | ZD (Ref) | D (inch) | | ZD (Ref) |
|----|-------|------|-------------|----------|------|-------------|
| | MIN | MAX | | MIN | MAX | |
| 16 | 4.80 | 5.00 | 0.23 | .189 | .197 | .009 |

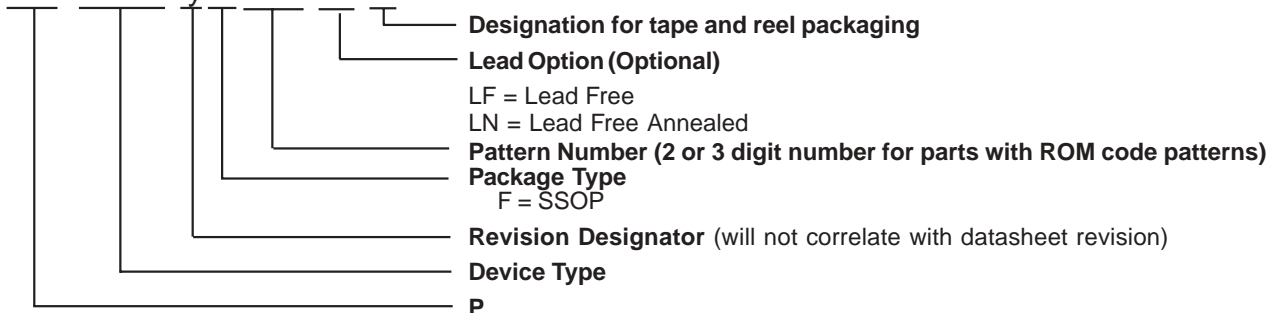
Reference Doc.: JEDEC Publication 95, MO-137
10-0032

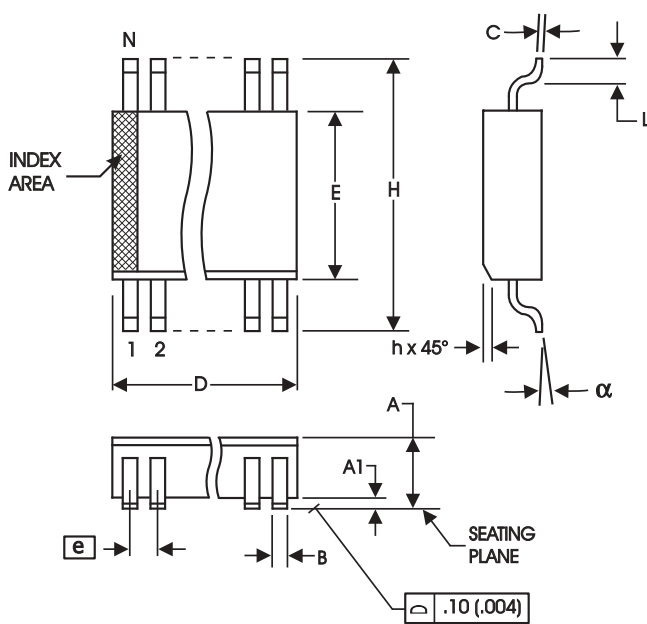
Ordering Information

9112yF-17LF-T

Example:

XXXX y F PPP Lx-T





150 mil (Narrow Body) SOIC

| SYMBOL | In Millimeters | | In Inches | |
|----------|-------------------|-------------------|-------------------|-------------------|
| | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS |
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

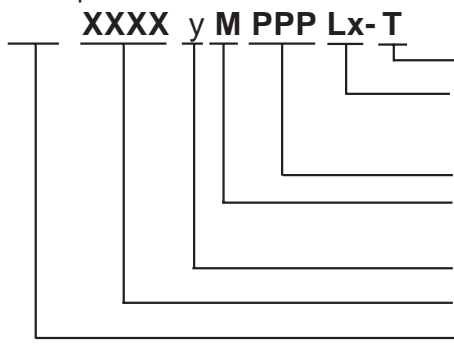
| N | D mm. | | D (inch) | |
|----|-------|-------|----------|-------|
| | MIN | MAX | MIN | MAX |
| 16 | 9.80 | 10.00 | .3859 | .3937 |

Reference Doc.: JEDEC Publication 95, MS-012
10-0030

Ordering Information

9112yM-17LF-T

Example:



Designation for tape and reel packaging

Lead Option (Optional)

LF = Lead Free

LN = Lead Free Annealed

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

M = SOIC

Revision Designator (will not correlate with datasheet revision)

Device Type

P

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-  Excess Inventory Management