



**THE DATASHEET OF  
74AUP2G80GT,115**



# 74AUP2G80

Low-power dual D-type flip-flop; positive-edge trigger

Rev. 12 — 21 July 2023

Product data sheet

## 1. General description

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The 74AUP2G80 provides the dual positive-edge triggered D-type flip-flop. Information on the data input is transferred to the  $\bar{Q}$  output on the LOW-to-HIGH transition of the clock pulse. The input pin D must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire  $V_{CC}$  range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

## 2. Features and benefits

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- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Low static power consumption;  $I_{CC} = 0.9 \mu\text{A}$  (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of  $V_{CC}$
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74AUP2G80DC</a>	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<a href="#">SOT765-1</a>
<a href="#">74AUP2G80GT</a>	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	<a href="#">SOT833-1</a>
<a href="#">74AUP2G80GN</a>	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	<a href="#">SOT1116</a>
<a href="#">74AUP2G80GS</a>	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	<a href="#">SOT1203</a>

### 4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AUP2G80DC	p80
74AUP2G80GT	p80
74AUP2G80GN	pT
74AUP2G80GS	pT

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

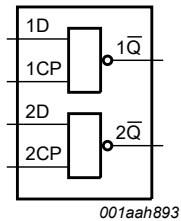


Fig. 1. Logic symbol

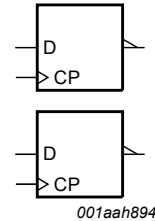


Fig. 2. IEC logic symbol

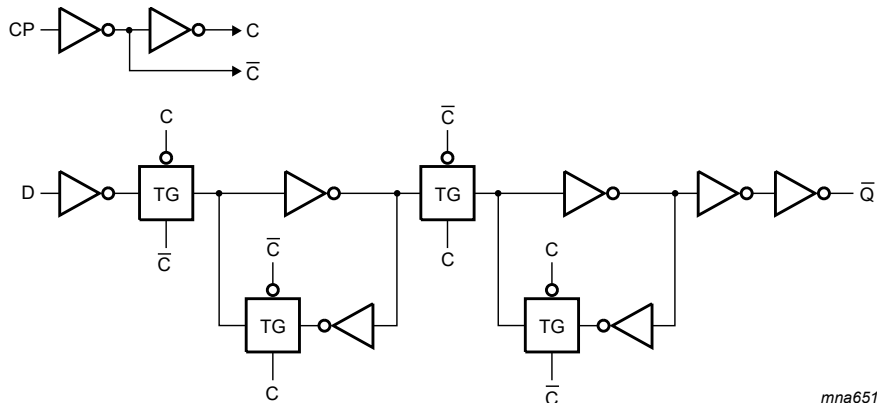
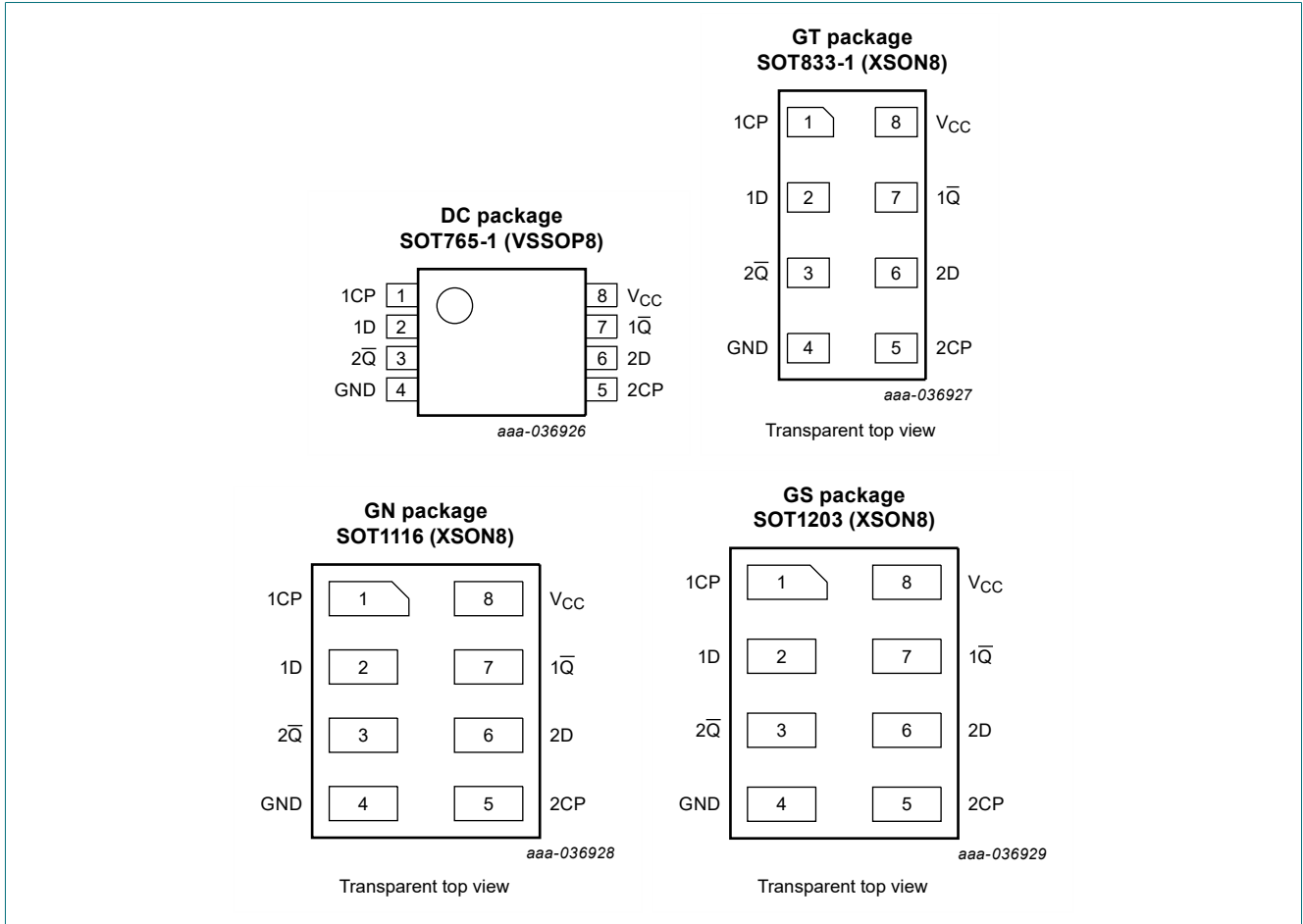


Fig. 3. Logic diagram (one flip-flop)

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 5	clock input
1D, 2D	2, 6	data input
GND	4	ground (0 V)
1Q̄, 2Q̄	7, 3	data output
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition; X = don't care;*

*q̄ = lower case letter indicates the state of referenced input, one setup time prior to the LOW-to-HIGH CP transition.*

Input		Output
nCP	nD	nQ̄
↑	L	H
↑	H	L
L	X	q̄

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$V_O$	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±20	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99 °C.  
 For SOT833-1 (XSON8) package:  $P_{tot}$  derates linearly with 3.1 mW/K above 68 °C.  
 For SOT1116 (XSON8) package:  $P_{tot}$  derates linearly with 4.2 mW/K above 90 °C.  
 For SOT1203 (XSON8) package:  $P_{tot}$  derates linearly with 3.6 mW/K above 81 °C.

## 9. Recommended operating conditions

**Table 6. Operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		0.8	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	-	200	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	0.70 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	0.30 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -1.1 mA; V <sub>CC</sub> = 1.1 V	0.75 × V <sub>CC</sub>	-	-	V
		I <sub>O</sub> = -1.7 mA; V <sub>CC</sub> = 1.4 V	1.11	-	-	V
		I <sub>O</sub> = -1.9 mA; V <sub>CC</sub> = 1.65 V	1.32	-	-	V
		I <sub>O</sub> = -2.3 mA; V <sub>CC</sub> = 2.3 V	2.05	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.9	-	-	V
		I <sub>O</sub> = -2.7 mA; V <sub>CC</sub> = 3.0 V	2.72	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.1	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.30 × V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.31	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.31	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.31	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.44	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.31	V
	I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.44	V	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.1	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.2	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.2	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.3 V [1]	-	-	40	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.6	-	pF
C <sub>O</sub>	output capacitance	V <sub>O</sub> = GND; V <sub>CC</sub> = 0 V	-	1.3	-	pF

## Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	0.70 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	0.30 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -1.1 mA; V <sub>CC</sub> = 1.1 V	0.70 × V <sub>CC</sub>	-	-	V
		I <sub>O</sub> = -1.7 mA; V <sub>CC</sub> = 1.4 V	1.03	-	-	V
		I <sub>O</sub> = -1.9 mA; V <sub>CC</sub> = 1.65 V	1.30	-	-	V
		I <sub>O</sub> = -2.3 mA; V <sub>CC</sub> = 2.3 V	1.97	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.85	-	-	V
		I <sub>O</sub> = -2.7 mA; V <sub>CC</sub> = 3.0 V	2.67	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.1	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.30 × V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.37	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.35	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.33	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.33	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.5	μA
		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.5	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.5	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.6	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.9	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.3 V [1]	-	-	50	μA

## Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	0.75 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	0.70 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	0.25 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.30 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	V <sub>CC</sub> - 0.11	-	-	V
		I <sub>O</sub> = -1.1 mA; V <sub>CC</sub> = 1.1 V	0.60 × V <sub>CC</sub>	-	-	V
		I <sub>O</sub> = -1.7 mA; V <sub>CC</sub> = 1.4 V	0.93	-	-	V
		I <sub>O</sub> = -1.9 mA; V <sub>CC</sub> = 1.65 V	1.17	-	-	V
		I <sub>O</sub> = -2.3 mA; V <sub>CC</sub> = 2.3 V	1.77	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.67	-	-	V
		I <sub>O</sub> = -2.7 mA; V <sub>CC</sub> = 3.0 V	2.40	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.11	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.33 × V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.41	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.39	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.36	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.50	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.75	μA
		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.75	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.75	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.75	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.3 V [1]	-	-	75	μA

[1] One input at V<sub>CC</sub> - 0.6 V, other input at V<sub>CC</sub> or GND.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>C<sub>L</sub> = 5 pF</b>										
t <sub>pd</sub>	propagation delay	nCP to nQ̄; see Fig. 4 [2]								
		V <sub>CC</sub> = 0.8 V	-	20.9	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.9	6.0	12.9	2.6	14.3	2.6	15.7	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	1.9	4.2	7.6	2.0	8.9	2.0	9.8	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.7	3.4	5.9	1.6	7.0	1.6	7.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.4	2.6	4.3	1.2	5.6	1.2	6.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.2	2.2	3.6	1.0	4.4	1.0	4.8	ns
f <sub>max</sub>	maximum frequency	nCP; see Fig. 5								
		V <sub>CC</sub> = 0.8 V	-	53	-	-	-	-	-	MHz
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	203	-	170	-	170	-	MHz
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	347	-	310	-	300	-	MHz
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	435	-	400	-	390	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	550	-	490	-	480	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	619	-	550	-	510	-	MHz
<b>C<sub>L</sub> = 10 pF</b>										
t <sub>pd</sub>	propagation delay	nCP to nQ̄; see Fig. 4 [2]								
		V <sub>CC</sub> = 0.8 V	-	24.6	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.3	6.9	14.9	3.0	16.5	3.0	18.2	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.6	4.8	8.8	2.3	10.3	2.3	11.3	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.3	3.9	6.8	2.0	8.1	2.0	8.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.9	3.1	5.1	1.7	6.3	1.7	6.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.8	2.7	4.4	1.4	4.9	1.4	5.4	ns
f <sub>max</sub>	maximum frequency	nCP; see Fig. 5								
		V <sub>CC</sub> = 0.8 V	-	52	-	-	-	-	-	MHz
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	192	-	150	-	150	-	MHz
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	324	-	280	-	230	-	MHz
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	421	-	310	-	250	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	486	-	370	-	360	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	550	-	410	-	360	-	MHz

Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>C<sub>L</sub> = 15 pF</b>										
t <sub>pd</sub>	propagation delay	nCP to nQ̄; see Fig. 4 [2]								
		V <sub>CC</sub> = 0.8 V	-	28.2	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.0	7.6	16.7	3.4	18.6	3.4	20.5	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	3.0	5.3	9.8	2.6	11.5	2.6	12.7	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.6	4.4	7.6	2.3	9.1	2.3	10.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.2	3.5	5.7	2.0	6.9	2.0	7.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.9	3.1	5.0	1.8	5.5	1.8	6.1	ns
f <sub>max</sub>	maximum frequency	nCP; see Fig. 5								
		V <sub>CC</sub> = 0.8 V	-	50	-	-	-	-	-	MHz
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz
<b>C<sub>L</sub> = 30 pF</b>										
t <sub>pd</sub>	propagation delay	nCP to nQ̄; see Fig. 4 [2]								
		V <sub>CC</sub> = 0.8 V	-	38.8	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	4.9	9.8	20.7	4.4	24.7	4.4	27.2	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	4.0	6.8	12.7	3.5	15.0	3.5	16.5	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.5	5.6	9.9	2.2	11.9	2.2	13.1	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.1	4.5	7.5	2.8	9.3	2.8	10.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.9	4.1	6.4	2.7	7.5	2.7	8.3	ns
f <sub>max</sub>	maximum frequency	nCP; see Fig. 5								
		V <sub>CC</sub> = 0.8 V	-	28	-	-	-	-	-	MHz
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	128	-	70	-	70	-	MHz
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	206	-	120	-	110	-	MHz
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	262	-	150	-	120	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	269	-	190	-	170	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	309	-	200	-	190	-	MHz

Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>C<sub>L</sub> = 5 pF, 10 pF, 15 pF and 30 pF</b>										
t <sub>su(H)</sub>	set-up time HIGH	nD to nCP; see Fig. 5								
		V <sub>CC</sub> = 0.8 V	-	2.5	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	0.5	-	2.3	-	2.3	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	0.3	-	1.2	-	1.2	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.3	-	0.8	-	0.8	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	0.2	-	0.6	-	0.6	-	ns
t <sub>su(L)</sub>	set-up time LOW	nD to nCP; see Fig. 5								
		V <sub>CC</sub> = 0.8 V	-	1.7	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	0.3	-	1.9	-	1.9	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	0.2	-	1.3	-	1.3	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.2	-	1.1	-	1.1	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	0.3	-	0.8	-	0.8	-	ns
t <sub>h</sub>	hold time	nD to nCP; see Fig. 5								
		V <sub>CC</sub> = 0.8 V	-	-2.1	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	-0.4	-	0.1	-	0.1	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	-0.3	-	0	-	0	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-0.2	-	0	-	0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-0.2	-	0	-	0	-	ns
t <sub>w</sub>	pulse width	nCP HIGH or LOW; see Fig. 5								
		V <sub>CC</sub> = 0.8 V	-	5.2	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	1.0	-	3.0	-	3.0	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	0.8	-	2.0	-	2.0	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.6	-	2.0	-	2.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	0.5	-	2.0	-	2.0	-	ns
C <sub>PD</sub>	power dissipation capacitance	f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [3]								
		V <sub>CC</sub> = 0.8 V	-	1.8	-	-	-	-	-	pF
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	1.8	-	-	-	-	-	pF
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	1.9	-	-	-	-	-	pF
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	2.0	-	-	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	2.4	-	-	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	2.9	-	-	-	-	pF	

[1] All typical values are measured at nominal V<sub>CC</sub>.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz; C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V; N = number of inputs switching; Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

11.1. Waveforms and test circuit

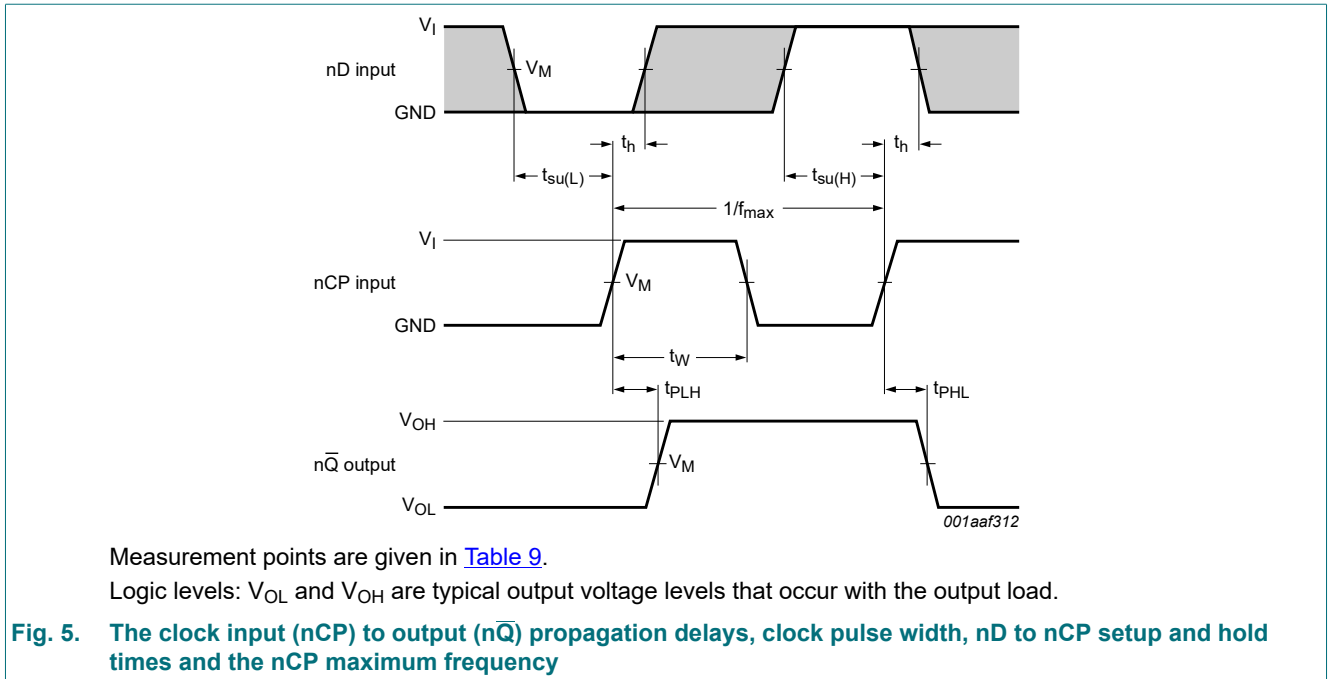
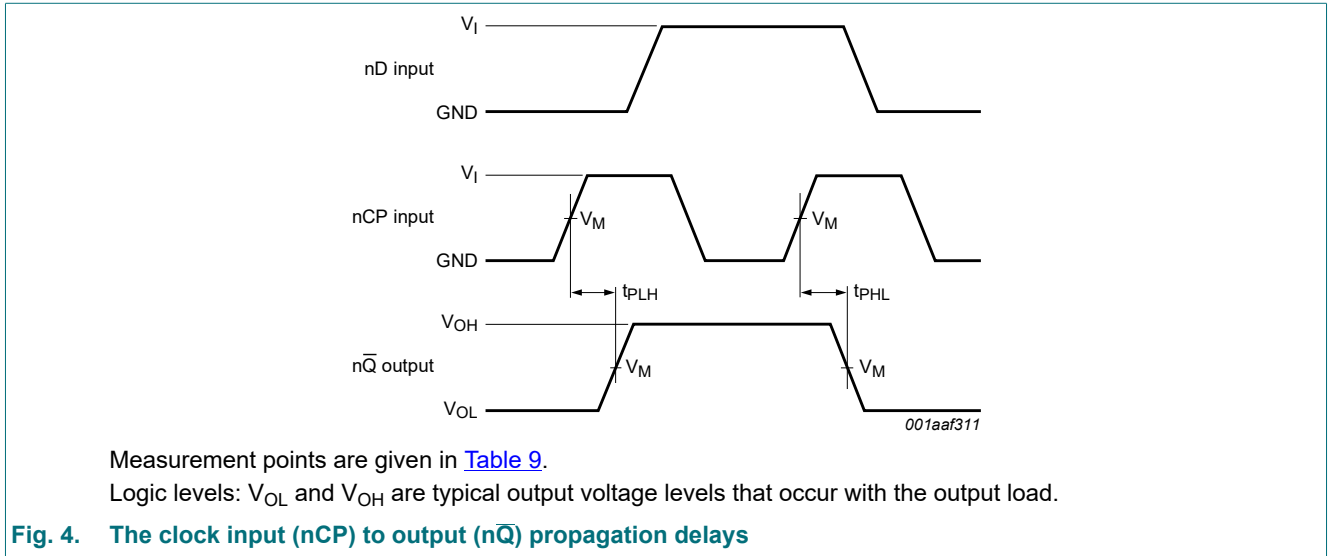
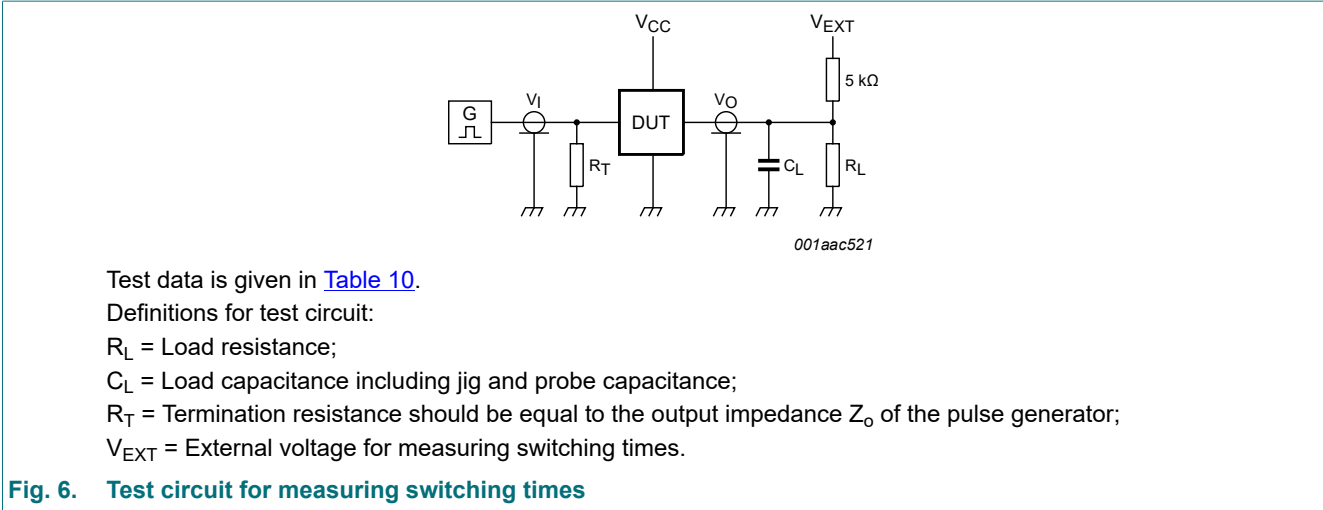


Table 9. Measurement points

Supply voltage	Output	Input		
$V_{CC}$	$V_M$	$V_M$	$V_I$	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 3.0$ ns



**Fig. 6. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage		Load		$V_{EXT}$		
$V_{CC}$	$C_L$	$R_L$ [1]	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$	
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$	

[1] For measuring enable and disable times  $R_L = 5 \text{ k}\Omega$   
 For measuring propagation delays, setup and hold times and pulse width  $R_L = 1 \text{ M}\Omega$ .

## 12. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

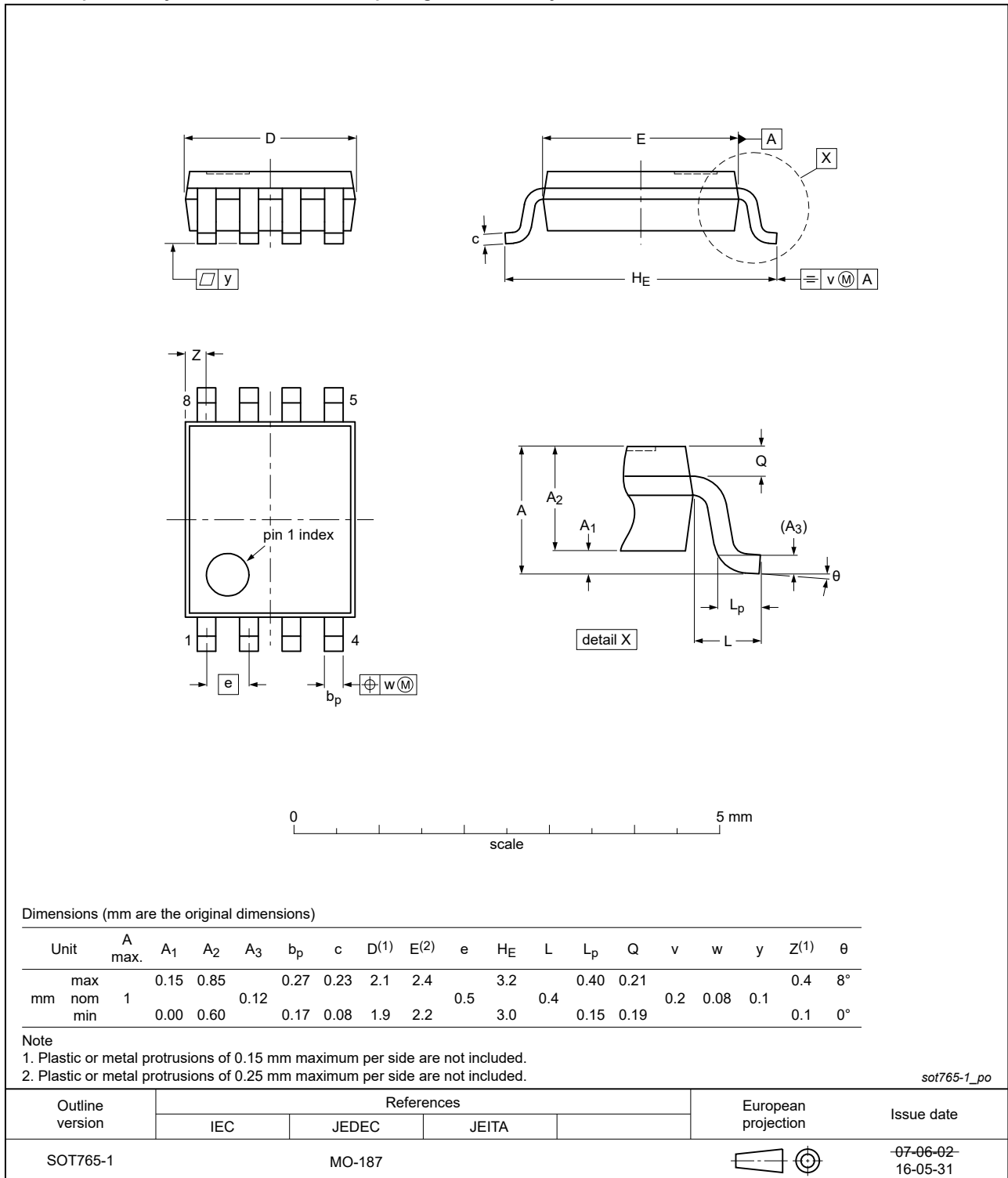


Fig. 7. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

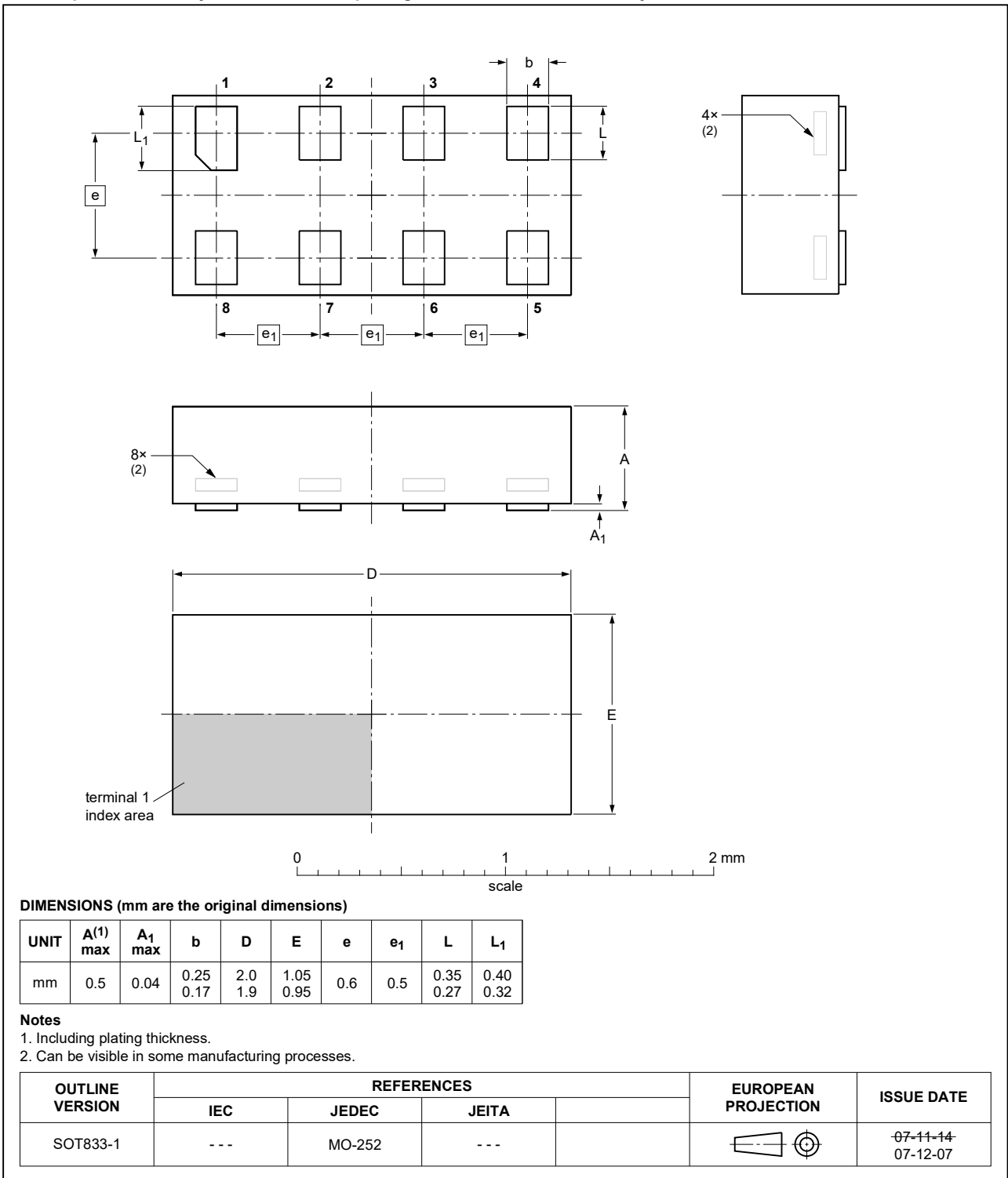


Fig. 8. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

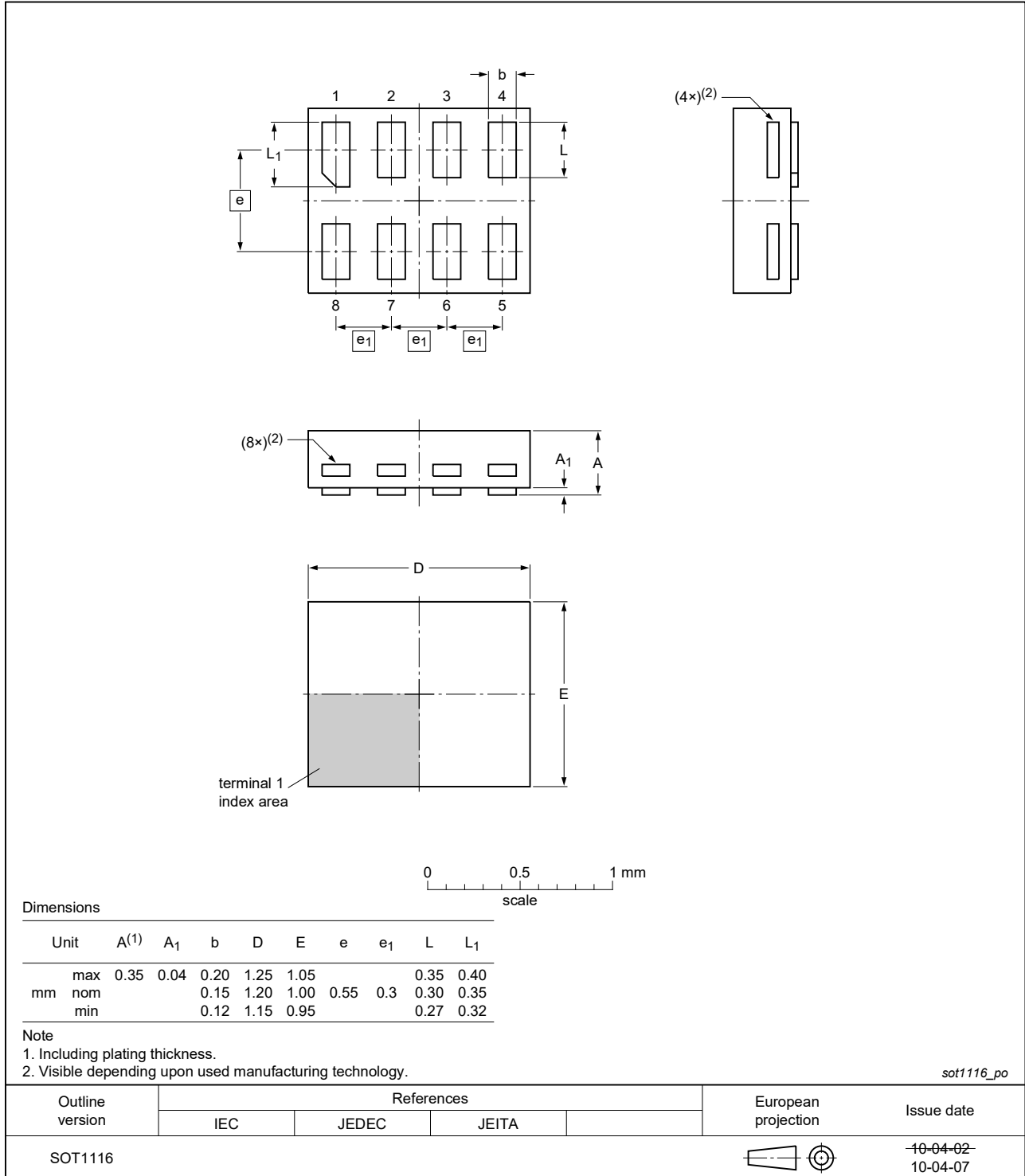


Fig. 9. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

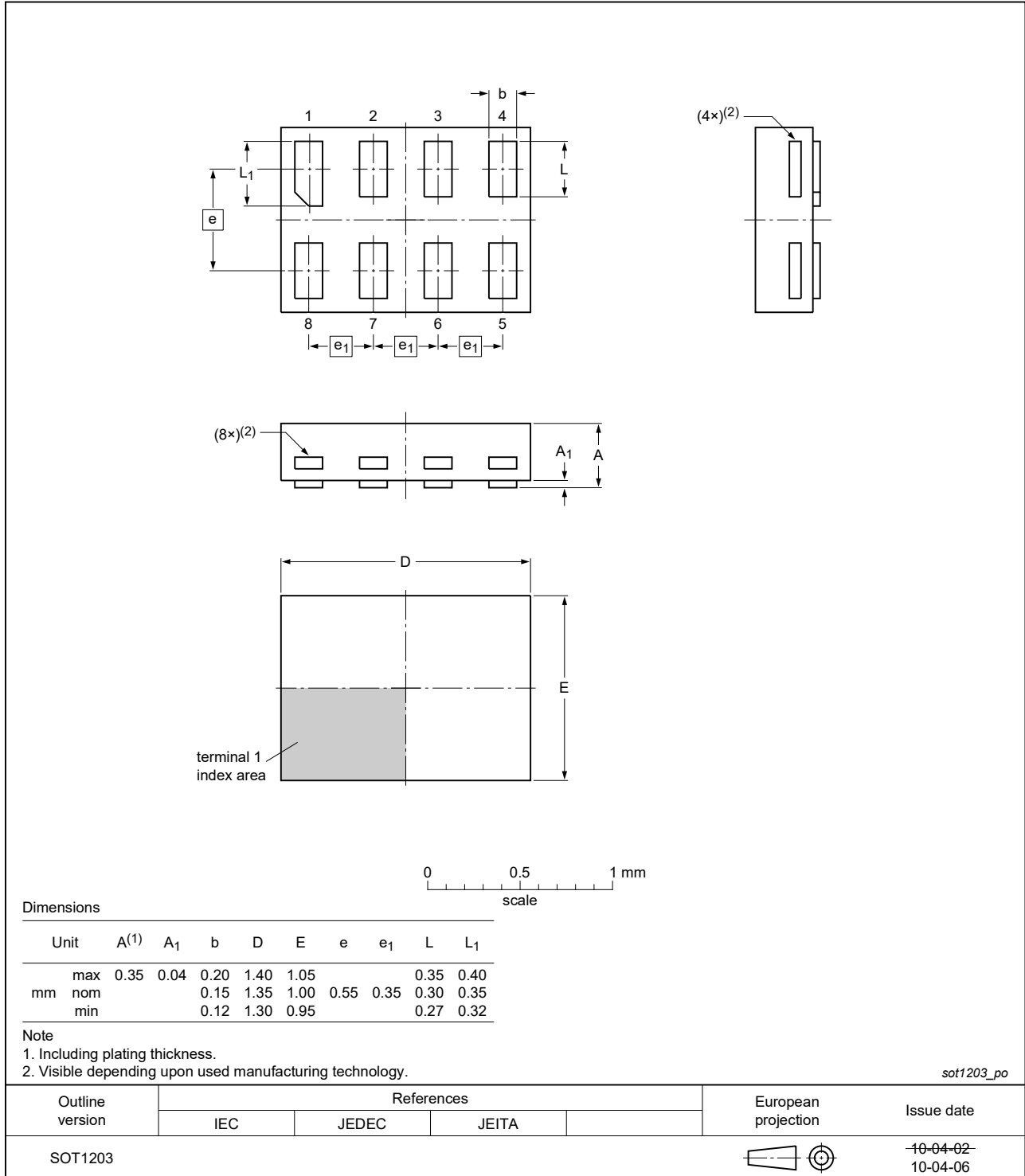


Fig. 10. Package outline SOT1203 (XSON8)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G80 v.12	20230721	Product data sheet	-	74AUP2G80 v.11
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74AUP2G80 v.11	20201207	Product data sheet	-	74AUP2G80 v.10
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> <li>Type numbers 74AUP2G80GF (SOT1089/XSON8) and 74AUP2G80GM (SOT902-1/XQFN8) removed.</li> </ul>			
74AUP2G80 v.10	20181119	Product data sheet	-	74AUP2G80 v.9
Modifications:	<ul style="list-style-type: none"> <li>Type number 74AUP2G80GD (SOT996-2/XSON8) removed.</li> </ul>			
74AUP2G80 v.9	20170818	Product data sheet	-	74AUP2G80 v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74AUP2G80 v.8	20130121	Product data sheet	-	74AUP2G80 v.7
Modifications:	<ul style="list-style-type: none"> <li>For type number 74AUP2G80GD XSON8U has changed to XSON8.</li> </ul>			
74AUP2G80 v.7	20120614	Product data sheet	-	74AUP2G80 v.6
74AUP2G80 v.6	20111207	Product data sheet	-	74AUP2G80 v.5
74AUP2G80 v.5	20101005	Product data sheet	-	74AUP2G80 v.4
74AUP2G80 v.4	20080602	Product data sheet	-	74AUP2G80 v.3
74AUP2G80 v.3	20080328	Product data sheet	-	74AUP2G80 v.2
74AUP2G80 v.2	20070801	Product data sheet	-	74AUP2G80 v.1
74AUP2G80 v.1	20060825	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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