



**THE DATASHEET OF
PTN36043ABXY**



1. General description

PTN36043A is a very small, low power 2 differential channel 2-to-1 active multiplex/demultiplexer switch with integrated SuperSpeed USB 3.1 Gen 1 (also known as USB 3.0) redriver IC that can switch two differential signals to one of two locations. The active switch has optimized performance with minimized crosstalk, as required by the high-speed serial interface for USB Type-C connector. PTN36043A allows expansion of existing high-speed ports for very low power consumption.

With integrated USB 3.1 Gen 1 redriver, signal quality is enhanced by performing receive equalization on the deteriorated input signal followed by transmit de-emphasis maximizing system link performance. With its superior differential signal conditioning and enhancement capability, the device delivers significant flexibility and performance scaling for various systems with different PCB characteristics and cable channel conditions and still benefit from optimum power consumption.

PTN36043A has built-in advanced power management capability that enables significant power savings under various different USB 3.1 Gen 1 Low-power modes (U2/U3). It can detect link electrical conditions and can dynamically activate/deactivate internal circuitry and logic. The device performs these actions without host software intervention and conserves power.

PTN36043A is powered from a 1.8 V supply and is available in a small DHX2QFN18 package (2.4 mm × 2.0 mm × 0.35 mm) with 0.4 mm pitch.

2. Features and benefits

- 2 bidirectional differential channel, 2 : 1 multiplex/demultiplexer switch, supports USB 3.1 Gen 1 specification (SuperSpeed only)
- Compliant to SuperSpeed USB 3.1 Gen 1 standard
- Pin out data flow matches USB Type-C connector pin assignments
- Two control pins for each channel to select optimized signal conditions
 - ◆ Receive equalization on each channel to recover from InterSymbol Interference (ISI) and high-frequency losses, with provision to choose equalization gain settings per channel
 - ◆ Transmit de-emphasis on each channel delivers pre-compensation suited to channel conditions
 - ◆ Output swing adjustment
- Integrated termination resistors provide impedance matching on both transmit and receive sides
- Automatic receiver termination detection
- Low active power: 203 mW/113 mA (typical) for VDD = 1.8 V



- Power-saving states:
 - ◆ 1.35 mW/0.75 mA (typical) when in U2/U3 states
 - ◆ 0.81 mW/0.45 mA (typical) when no connection detected
- Excellent differential and common return loss performance
 - ◆ 14 dB differential and 15 dB common-mode return loss for 10 MHz to 1250 MHz
- Flow-through pinout to ease PCB layout and minimize crosstalk effects
- Power supply: VDD = 1.8 V (typical)
- Compliant with JESD 78 Class II latch up test standard
- Very thin DHX2QFN18 package: 2.4 mm x 2.0 mm x 0.35 mm, 0.4 mm pitch
- ESD protection exceeds 7000 V HBM per JDS-001-2012 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating temperature range: -40°C to +85°C

3. Applications

- USB 3.1 Gen 1 application for USB Type-C connectors
- Smart Phones, Tablets/Mobile Devices
- Desktop/Notebook Computers
- Docking Stations
- USB 3.1 Gen 1 Peripherals such as flat panel display, consumer/storage devices, printers or USB 3.1 Gen 1 capable hubs/repeaters

4. Ordering information

Table 1. Ordering information

| Type number | Topside marking | Package | | |
|-------------|-----------------|-----------|---|-----------|
| | | Name | Description | Version |
| PTN36043ABX | 3A | DHX2QFN18 | plastic dual in-line compatible thermal enhanced extremely thin quad flat package; no leads; 18 terminals; body 2.4 mm × 2.0 mm × 0.35 mm | SOT1442-1 |

4.1 Ordering options

Table 2. Ordering options

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature |
|-------------|-----------------------|-----------|--------------------------------------|------------------------|-------------------------------------|
| PTN36043ABX | PTN36043ABXY | DHX2QFN18 | REEL 13" Q1/T1 *STANDARD MARK SMD DP | 10000 | T _{amb} = -40 °C to +85 °C |

5. Block diagram

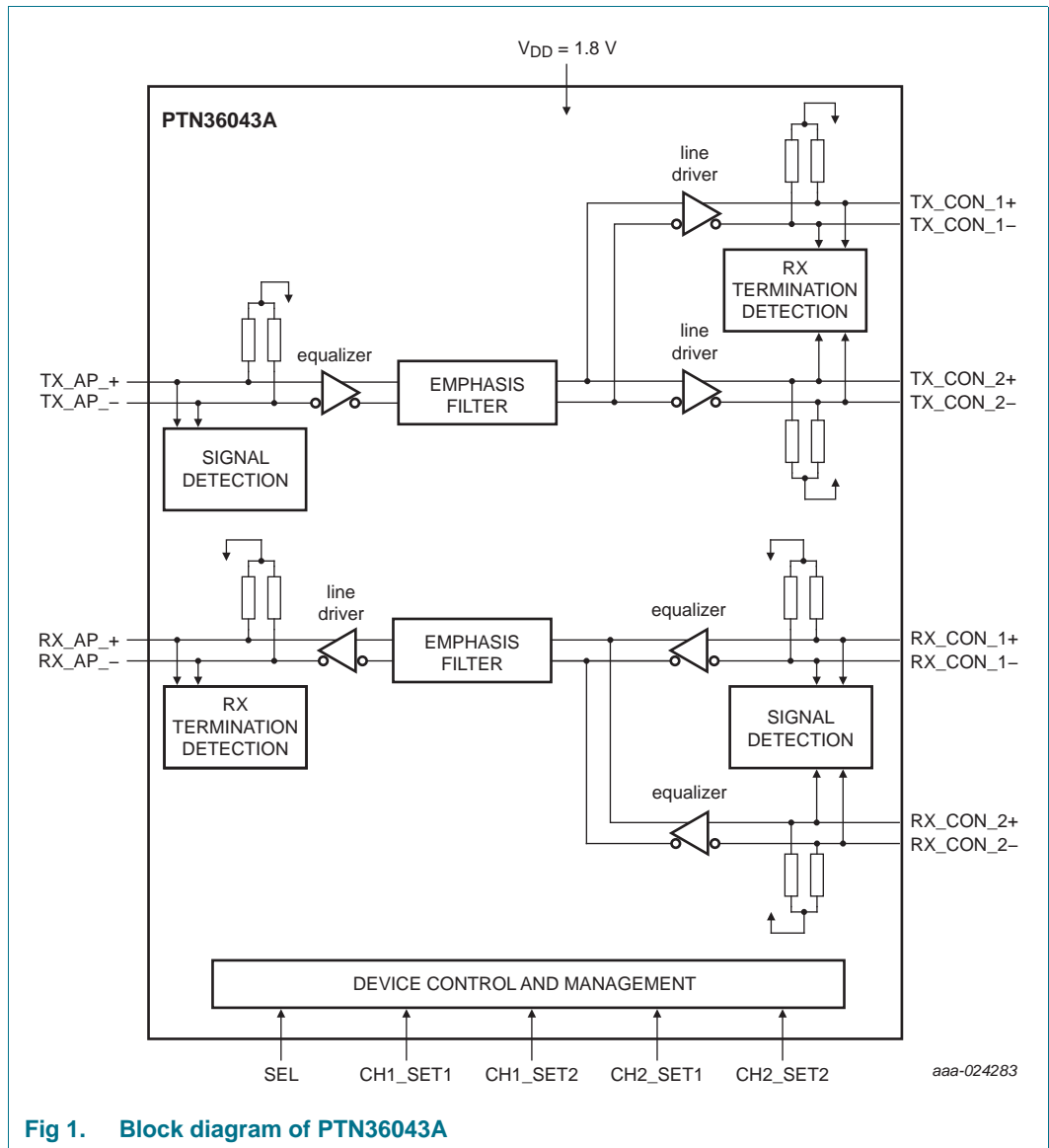


Fig 1. Block diagram of PTN36043A

6. Pinning information

6.1 Pinning

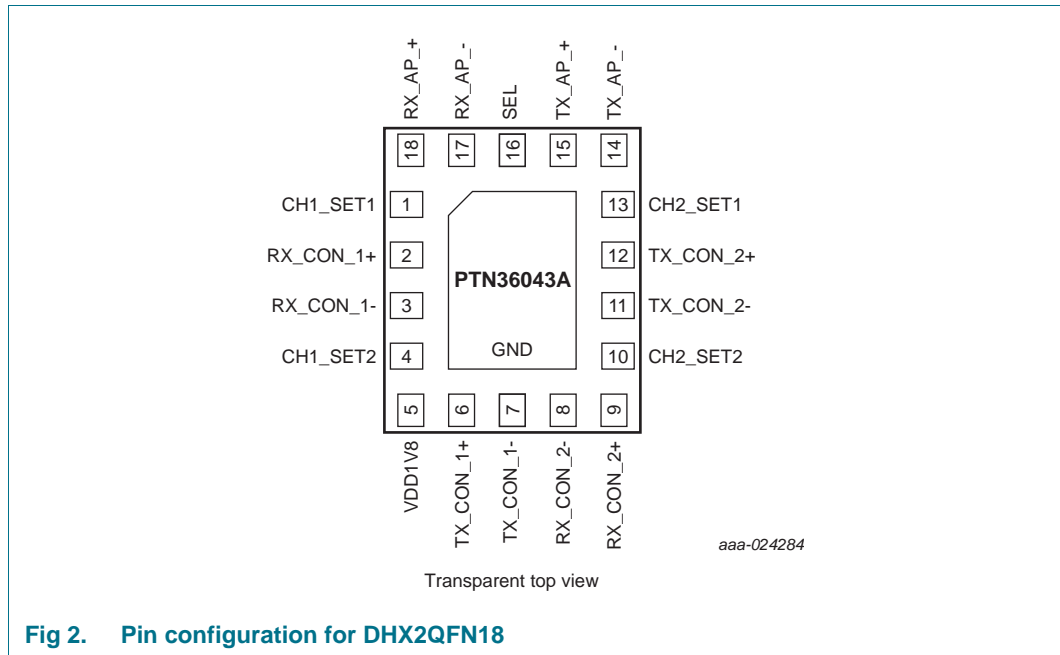


Fig 2. Pin configuration for DHX2QFN18

6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Type | Description |
|-----------|-----|--------|--|
| RX_AP_+ | 18 | Output | USB 3.1 Gen 1 differential output signals of the RX path to application processor |
| RX_AP_- | 17 | | |
| TX_AP_+ | 15 | Input | USB 3.1 Gen 1 differential input signals of the TX path from application processor |
| TX_AP_- | 14 | | |
| TX_CON_1+ | 6 | Output | USB 3.1 Gen 1 differential output signals of the TX path to connector side port 1 |
| TX_CON_1- | 7 | | |
| RX_CON_1+ | 2 | Input | USB 3.1 Gen 1 differential input signals of the RX path from connector side port 1 |
| RX_CON_1- | 3 | | |
| TX_CON_2+ | 12 | Output | USB 3.1 Gen 1 differential output signals of the TX path to connector side port 2 |
| TX_CON_2- | 11 | | |
| RX_CON_2+ | 9 | Input | USB 3.1 Gen 1 differential input signals of the RX path from connector side port 2 |
| RX_CON_2- | 8 | | |

Table 3. Pin description ...continued

| Symbol | Pin | Type | Description |
|----------|------------|---------------|--|
| SEL | 16 | input | Output selection control When SEL=0, RX_AP_±/TX_AP_± are connected to RX_CON_2±/TX_CON_2±, and RX_CON_1±/TX_CON_1± are in high impedance state. When SEL=1, RX_AP_±/TX_AP_± are connected to RX_CON_1±/TX_CON_1±, and RX_CON_2±/TX_CON_2± are in high impedance state. |
| CH1_SET1 | 1 | Ternary input | OS/DE/EQ control pins for channel facing the application processor side |
| CH1_SET2 | 4 | | |
| CH2_SET1 | 13 | Ternary input | OS/DE/EQ control pins for channel facing the connector side |
| CH2_SET2 | 10 | | |
| VDD1V8 | 5 | Power | Power supply (1.8 V typical) |
| GND | Center Pad | Power | Ground. Center pad must be connected to GND plane for both electrical grounding and thermal relief purposes. |

7. Functional description

Refer to [Figure 1 “Block diagram of PTN36043A”](#).

PTN36043A is a high speed 2 to 1 active switch with integrated SuperSpeed USB 3.1 Gen 1 redriver meant to be used for signal integrity enhancement on various platforms - smart phone, tablet, notebook, hub, A/V display and peripheral devices, for example. With its high fidelity differential signal conditioning capability and wide configurability, this device is flexible and versatile enough for use under a variety of system environments.

The following sections describe the individual block functions and capabilities of the device in more detail.

7.1 Receive equalization, transmitter de-emphasis and output swing level controls

On the high-speed signal path, the device performs receive equalization (EQ) and transmitter de-emphasis (DE) and output swing control (OS). In addition, the device provides flat frequency gain by boosting output signal. Both flat and frequency selective gains prepare the system to cover up to losses further down the link.

[Table 4](#) lists DE/OS/EQ configuration options of the channel toward application processor side.

Table 4. Application Processor side DE/OS/EQ configuration options

| CH1_SET1 | CH1_SET2 | RX_AP_± De-emphasis | RX_AP_± Output Swing | TX_AP_± Equalizer |
|----------|----------|------------------------|-------------------------|----------------------|
| LOW | LOW | -3.9 dB | 1100 mV | 3.0 dB |
| | OPEN | -3.5 dB | 900 mV | 3.0 dB |
| | HIGH | 0 dB | 1100 mV | 3.0 dB |
| OPEN | LOW | 0 dB | 900 mV | 3.0 dB |
| | OPEN | -3.9 dB | 1100 mV | 0 dB |
| | HIGH | -3.5 dB | 900 mV | 0 dB |
| HIGH | LOW | 0 dB | 1100 mV | 0 dB |
| | OPEN | 0 dB | 900 mV | 0 dB |
| | HIGH | -5.3 dB | 1100 mV | 6.0 dB |

[Table 5](#) lists DE/OS/EQ configuration options of the channel toward connector side.

Table 5. Connector side DE/OS/EQ configuration options

| CH2_SET1 | CH2_SET2 | TX_CON_1± TX_CON_2± De-emphasis | TX_CON_1± TX_CON_2± Output Swing | RX_CON_1± RX_CON_2± Equalizer |
|----------|----------|---------------------------------------|--|-------------------------------------|
| LOW | LOW | -5.3 dB | 1100 mV | 0 dB |
| | OPEN | -3.9 dB | 1100 mV | 0 dB |
| | HIGH | -3.5 dB | 900 mV | 0 dB |
| OPEN | LOW | -5.1 dB | 900 mV | 0 dB |
| | OPEN | -3.9 dB | 1100 mV | 6.0 dB |
| | HIGH | -3.5 dB | 900 mV | 6.0 dB |
| HIGH | LOW | -5.3 dB | 1100 mV | 6.0 dB |
| | OPEN | -5.1 dB | 900 mV | 6.0 dB |
| | HIGH | -5.3 dB | 1100 mV | 9.0 dB |

7.2 Device states and power management

PTN36043A has implemented an advanced power management scheme that operates in tune with USB 3.1 Gen 1 bus electrical condition. Although the device does not decode USB power management commands (related to USB 3.1 Gen 1 U1/U2/U3 transitions) exchanged between USB 3.1 Gen 1 host and peripheral/device, it relies on bus electrical conditions and SEL pin setting to decide to be in one of the following states:

- **Active state** wherein device is fully operational, USB data is transported on either port 1 or port 2 in Figure 1. In this state, USB connection exists and the Receive Termination indication remains active. But there is no need for Receive Termination detection.
- **Power-saving state** wherein either port 1 or port 2 is kept enabled. In this state, squelching, detection and/or Receive termination detection circuitry are active. Based on USB connection, there are two possibilities:
 - No USB connection.
 - A USB connection exists and the link is in USB 3.1 Gen 1 U2/U3 mode.
- **Off state** when PTN36043A is not being powered (i.e., VDD1V8 = 0 V), special steps should be done to prevent back-current issues on control pins such SEL or CH1/2_SET1/2 pins when these pins' states are not low. These pins can be controlled through two different ways.
 - pull-up/pull-down resistors - make sure these pull-up resistors' VDD is the same power source as to power PTN36043A. When power to PTN36043A is off, power to these pull-up resistors will be off as well.
 - external processor's GPIO - if PTN36043A is turned off when the external processor's power stays on, processor should configure these GPIOs connected to these control pins as output low (< 0.4 V) or tri-state mode (configure GPIOs as input mode). This will make sure no current will be flowing into PTN36043A through these control pins.

7.3 SEL input pin

PTN36043A is designed with 1:2 high speed de-multiplexer configuration. TX_AP_± and RX_AP_± can be connected to either TX_CON_1± and RX_CON_1±, or TX_CON_2± and RX_CON_2± by changing the SEL input state.

Table 6. SEL input setting

| SEL | Function |
|-----|--|
| 0 | TX_CON_2± and RX_CON_2± are connected to TX_AP_± and RX_AP_± TX_CON_1± and RX_CON_1± are in high impedance state. |
| 1 | TX_CON_1± and RX_CON_1± are connected to TX_AP_± and RX_AP_± TX_CON_2± and RX_CON_2± are in high impedance state. |

8. Application guideline for Control of CHx_SETx and SEL input pins

PTN36043A implements ternary control IO logic on CHx_SETx and SEL control pins to detect HIGH (connected to VDD), LOW (connected to GND) or left unconnected condition (OPEN).

For all control pins except SEL, all 3 pin conditions are applicable. If the SEL pin is left unconnected (OPEN), the internal logic treats it as LOW.

To minimize the current consumption of IO circuitry on SEL pin, it is recommended this pin be driven from 1.8 V capable push-pull IO. If 1.8 V push-pull IO is not available in the application, the SEL pin can be driven from an open drain grounded NMOS GPIO with external pull-up resistor to the 1.8 V supply of PTN36043A. The recommended value of the external pull-up resistor is 30 kΩ.

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------|---------------------------------|------------|----------|------|------|
| $V_{DD(1V8)}$ | supply voltage (1.8 V) | | [1] -0.3 | +2.2 | V |
| V_I | input voltage | | [1] -0.3 | +2.2 | V |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| V_{ESD} | electrostatic discharge voltage | HBM | [2] - | 7000 | V |
| | | CDM | [3] - | 1000 | V |

[1] All voltage values (except differential voltages) are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

10. Recommended operating conditions

Table 8. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|------------------------|-----------------------|------|---------------|------|------|
| $V_{DD(1V8)}$ | supply voltage (1.8 V) | 1.8 V supply option | 1.7 | 1.8 | 1.9 | V |
| V_I | input voltage | CMOS inputs | -0.3 | $V_{DD(1V8)}$ | +2.2 | V |
| | | differential pairs | -0.3 | - | +2.2 | V |
| T_{amb} | ambient temperature | operating in free air | -40 | - | +85 | °C |

11. Characteristics

11.1 Device characteristics

Table 9. Device characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|---|---|------|------|-----|----------------------|
| t_{startup} | start-up time | between supply voltage within operating range (90 % of V_{DD}) until automatic receiver termination detection | - | - | 6 | ms |
| t_{rcfg1} | setting reconfiguration time | any configuration pin change (from one setting to another setting) to specified operating characteristics; device is supplied with valid supply voltage | - | - | 3 | ms |
| t_{rcfg2} | port reconfiguration time | Switching from one port to the other port (i.e., Port 1 to Port 2 or vice versa) until automatic receiver detection; device is supplied with valid supply voltage | - | - | 7 | ms |
| $t_{\text{PD(dif)}}$ | differential propagation delay | between 50 % level at input and output; see Figure 3 | - | - | 0.5 | ns |
| t_{idle} | idle time | default wait time to wait before getting into Power-saving state | - | 300 | 400 | ms |
| $t_{\text{d(pwrsave-act)}}$ | delay time from power-save to active | time for exiting from Power-saving state and get into Active state; see Figure 5 | - | - | 115 | μs |
| $t_{\text{d(act-idle)}}$ | delay time from active to idle | reaction time for squelch detection circuit; see Figure 4 | - | 9 | 14 | ns |
| $t_{\text{d(idle-act)}}$ | delay time from idle to active | reaction time for squelch detection circuit; see Figure 4 | - | 5 | 11 | ns |
| DDNEXT | Differential near-end crosstalk between TX and RX signal pairs within the same port | $f < 2.5 \text{ GHz}$ | - | -50 | - | dB |
| $R_{\text{th(j-a)}}$ | thermal resistance from junction to ambient | JEDEC still air test environment; value is based on simulation under JEDEC still air test environment with 2S2P(4L) JEDEC PCB | - | 96 | - | $^{\circ}\text{C/W}$ |
| Ψ_{jt} | junction to top of case thermal characterization parameter | to case top; at ambient temperature of 85 $^{\circ}\text{C}$; value is based on simulation under JEDEC still air test environment with 2S2P(4L) JEDEC PCB | - | 1.0 | - | $^{\circ}\text{C/W}$ |
| I_{DD} | supply current | Active state | | | | |
| | | OS = 1100 mV/DE = -3.9 dB for both AP side and CON side | - | 113 | - | mA |
| | | OS = 900 mV/DE = -3.5 dB for AP side, OS = 1100 mV/DE = -3.9 dB for CON side | - | 108 | - | mA |
| | | OS = 900 mV/DE = 0 dB for AP side, OS = 1100 mV/DE = -3.9 dB for CON side | - | 103 | - | mA |
| | | U2/U3 Power-saving state | - | 0.75 | - | mA |
| | no USB connection state | - | 0.45 | - | mA | |

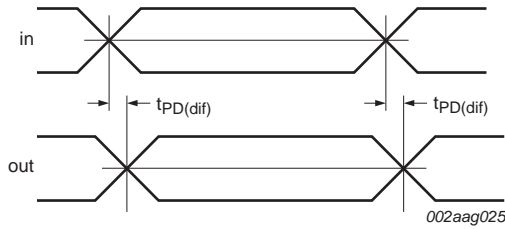


Fig 3. Propagation delay

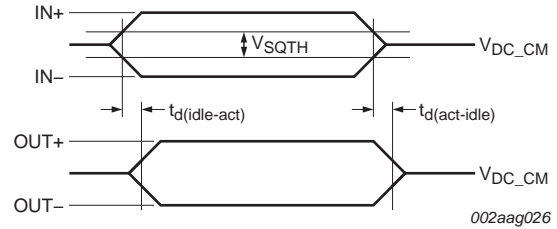


Fig 4. LFPS electrical idle transitions in U0/U1 modes

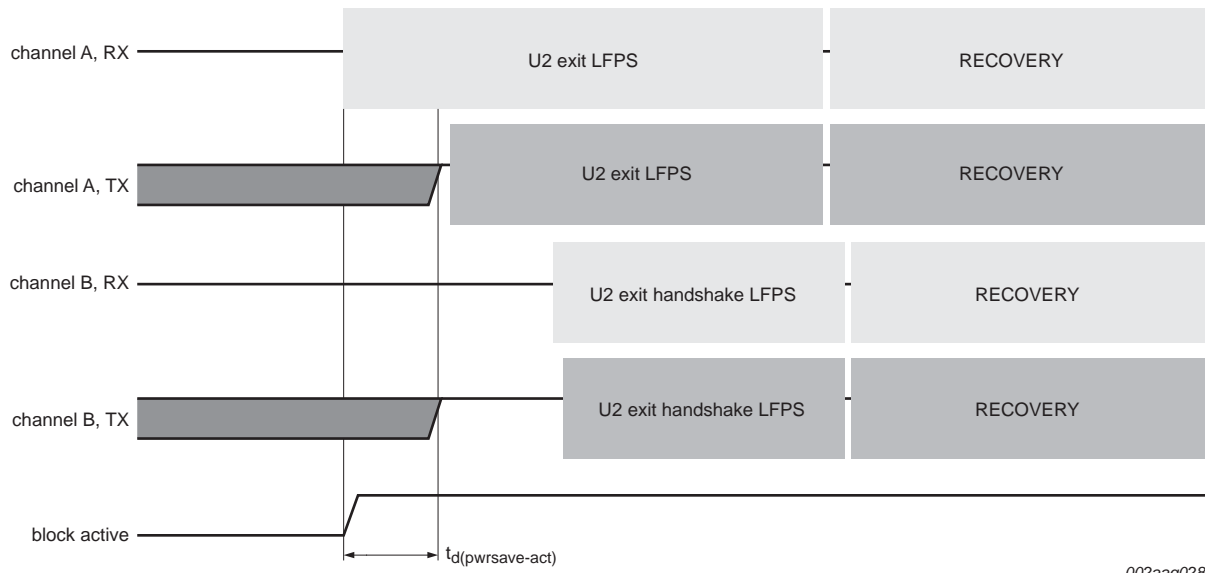


Fig 5. U2/U3 exit behavior

11.2 Receiver AC/DC characteristics

Table 10. Receiver AC/DC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|--|-----|-----|------|-----------|
| Z_{RX_DC} | receiver DC common-mode impedance | | 18 | - | 30 | Ω |
| $Z_{RX_DIFF_DC}$ | DC differential impedance | RX pair | 72 | - | 120 | Ω |
| $Z_{RX_HIGH_IMP}$ | common-mode input impedance | DC common-mode input impedance when output of redriver is not terminated | 25 | - | - | $k\Omega$ |
| $V_{RX(diff)(p-p)}$ | peak-to-peak differential receiver voltage | | 100 | - | 1200 | mV |
| $V_{RX_DC_CM}$ | RX DC common mode voltage | | - | 1.8 | - | V |
| $V_{RX_CM_AC_P}$ | RX AC common-mode voltage | peak | - | - | 150 | mV |
| $V_{th(i)}$ | signal detector input threshold voltage | differential peak-to-peak value | 75 | - | 150 | mV |
| $RL_{DD11,RX}$ | RX differential mode return loss | 10 MHz to 1250 MHz | 12 | 14 | - | dB |
| | | 1250 MHz to 2500 MHz | 7 | 8.5 | - | dB |
| | | 2500 MHz to 3000 MHz | 6 | 7.5 | - | dB |
| $RL_{CC11,RX}$ | RX common mode return loss | 10 MHz to 1250 MHz | 12 | 15 | - | dB |
| | | 1250 MHz to 2500 MHz | 8 | 10 | - | dB |
| | | 2500 MHz to 3000 MHz | 7 | 9 | - | dB |

11.3 Transmitter AC/DC characteristics

Table 11. Transmitter AC/DC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|--|------|-------------------------------|----------------------|------|
| Z _{TX_DC} | transmitter DC common-mode impedance | | 18 | - | 30 | Ω |
| Z _{TX_DIFF_DC} | DC differential impedance | | 72 | - | 120 | Ω |
| V _{TX_DIFFp-p} | differential peak-to-peak output voltage | R _L = 100 Ω | | | | |
| | | OS = 900 mV | 800 | 900 | 1000 | mV |
| | | OS = 1100 mV | 1000 | 1100 | 1200 | mV |
| V _{TX_DC_CM} | transmitter DC common-mode voltage | | - | 1.3 | V _{DD(1V8)} | V |
| V _{TX_CM_ACpp_ACTIV} | TX AC common-mode peak-to-peak output voltage (active state) | device input fed with differential signal | - | - | 100 | mV |
| V _{TX_IDL_DIFF_ACpp} | electrical idle differential peak-to-peak output voltage | when link is in electrical idle | - | - | 10 | mV |
| t _{W(deemp)TX} | transmitter de-emphasis pulse width | | 160 | 180 | 200 | ps |
| V _{TX_RCV_DETECT} | voltage change allowed during receiver detection | positive voltage swing to sense the receiver termination detection | - | 0.5 × V _{TX_DIFFp-p} | 600 | mV |
| R _{TX_RCV_DETECT} | TX receiver termination detect charging resistance | output resistor of the transmitter when it does RX detection | - | 3.1 | - | kΩ |
| t _{r(tx)} | transmit rise time | measured using 20 % and 80 % levels; see Figure 6 | 40 | 55 | 75 | ps |
| t _{f(tx)} | transmit fall time | measured using 20 % and 80 % levels; see Figure 6 | 40 | 55 | 75 | ps |
| t _{(r-f)tx} | difference between transmit rise and fall time | measured using 20 % and 80 % levels | - | - | 20 | ps |
| RL _{DD11,TX} | TX differential mode return loss | 10 MHz to 1250 MHz | 12 | 13.5 | - | dB |
| | | 1250 MHz to 2500 MHz | 6.5 | 8 | - | dB |
| | | 2500 MHz to 3000 MHz | 5 | 6.5 | - | dB |
| RL _{CC11,TX} | TX common mode return loss | 10 MHz to 1250 MHz | 12 | 14 | - | dB |
| | | 1250 MHz to 2500 MHz | 8 | 10 | - | dB |
| | | 2500 MHz to 3000 MHz | 9 | 10 | - | dB |

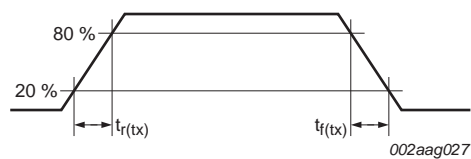


Fig 6. Output rise and fall times

11.4 Ternary control inputs

Table 12. Ternary control inputs CHx_SETx characteristics^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------|-------------------------------|--|------------------------|-----------------|------------------------|------|
| V _{IH} | HIGH-level input voltage | Trigger level of the Schmitt Trigger buffer when input is going from LOW to HIGH | 0.70 × V _{DD} | V _{DD} | V _{DD} + 0.3 | V |
| V _{IL} | LOW-level input voltage | Trigger level of the Schmitt Trigger buffer when input is going from HIGH to LOW | -0.3 | 0 | 0.30 × V _{DD} | V |
| R _{pu(ext)} | external pull-up resistor | connected between VDD1V8 and setting pin; for detection of HIGH condition | 0 | - | 30 | kΩ |
| R _{pd(ext)} | external pull-down resistor | connected between setting pin and GND; for detection of LOW condition | 0 | - | 30 | kΩ |
| Z _{ext(OPEN)} | external impedance | for detection of OPEN condition | 250 | - | - | kΩ |
| I _{IL} | LOW-level input current | setting pin is driven LOW by external GPIO | -45 | - | - | μA |
| I _{IH} | HIGH-level input current | setting pin is driven HIGH (to 1.8 V) by external GPIO | - | - | +45 | μA |
| I _{Lext(OPEN)} | external leakage current | of external GPIO; for reliable detection of OPEN condition | -6 | - | +6 | μA |
| C _{L(ext)} | external load capacitance | on setting pin; for reliable detection of OPEN condition | - | - | 150 | pF |
| R _{pu(int)} | internal pull-up resistance | for detection of Ternary setting | - | 50 | - | kΩ |
| R _{pd(int)} | internal pull-down resistance | for detection of Ternary setting | - | 50 | - | kΩ |

[1] See [Section 8](#) for application guidelines for the Ternary control pins.

Table 13. Ternary control input SEL characteristics^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|-----------------------------|--|------------------------|-----------------|------------------------|------|
| V _{IH} | HIGH-level input voltage | Trigger level of the Schmitt Trigger buffer when input is going from LOW to HIGH | 0.70 × V _{DD} | V _{DD} | V _{DD} + 0.3 | V |
| V _{IL} | LOW-level input voltage | Trigger level of the Schmitt Trigger buffer when input is going from HIGH to LOW | -0.3 | 0 | 0.30 × V _{DD} | V |
| R _{pu(ext)} | external pull-up resistor | connected between VDD1V8 and setting pin; for detection of HIGH condition | 0 | - | 30 | kΩ |
| R _{pd(ext)} | external pull-down resistor | connected between setting pin and GND; for detection of LOW condition | 0 | - | 30 | kΩ |
| Z _{ext(OPEN)} | external impedance | for detection of OPEN condition and will be interpreted as LOW condition | 250 | - | - | kΩ |
| I _{IL} | LOW-level input current | setting pin is driven LOW by external GPIO | -45 | - | - | μA |

Table 13. Ternary control input SEL characteristics^[1] ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|-------------------------------|--|-----|-----|-----|------------------|
| I_{IH} | HIGH-level input current | setting pin is driven HIGH (to 1.8 V) by external GPIO | - | - | +45 | μA |
| $C_{L(\text{ext})}$ | external load capacitance | on setting pin; for reliable detection of OPEN condition | - | - | 150 | pF |
| $R_{pu(\text{int})}$ | internal pull-up resistance | for detection of Ternary setting | - | 50 | - | $\text{k}\Omega$ |
| $R_{pd(\text{int})}$ | internal pull-down resistance | for detection of Ternary setting | - | 50 | - | $\text{k}\Omega$ |

[1] See [Section 8](#) for application guidelines for the Ternary control pins.

12. Package outline

DHX2QFN18: plastic dual in-line compatible thermal enhanced super-thin quad flat package; no leads; 18 terminals; body 2.4 x 2.0 x 0.35 mm

SOT1442-1

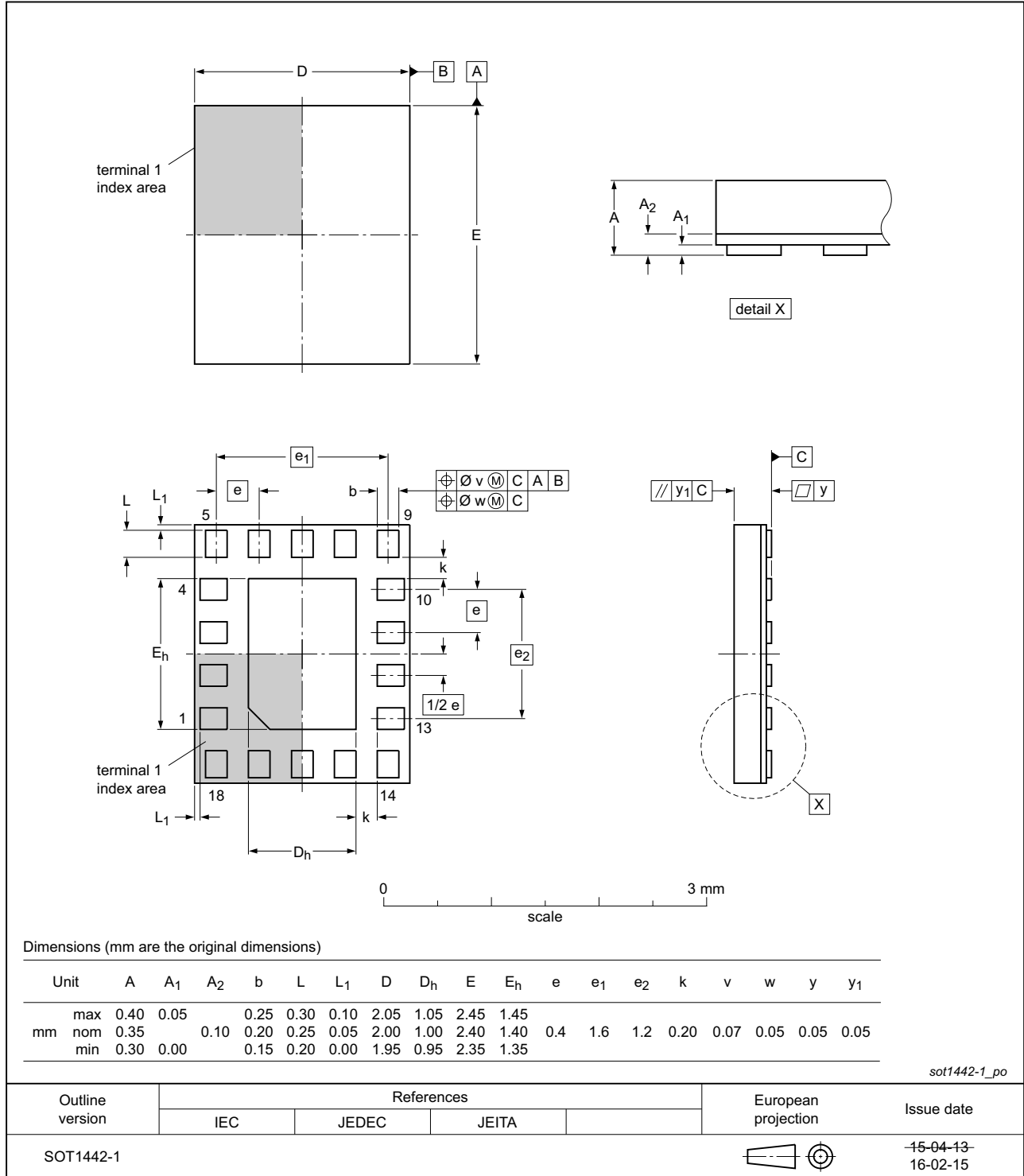


Fig 7. Package outline SOT1442-1 (DHX2QFN18)

13. Packing information

13.1 SOT1442-1 (DHXQFN18); Reel dry pack, SMD, 13" Q1/T1 standard product orientation; Orderable part number ending ,518 or Y; Ordering code (12NC) ending 518

13.1.1 Packing method

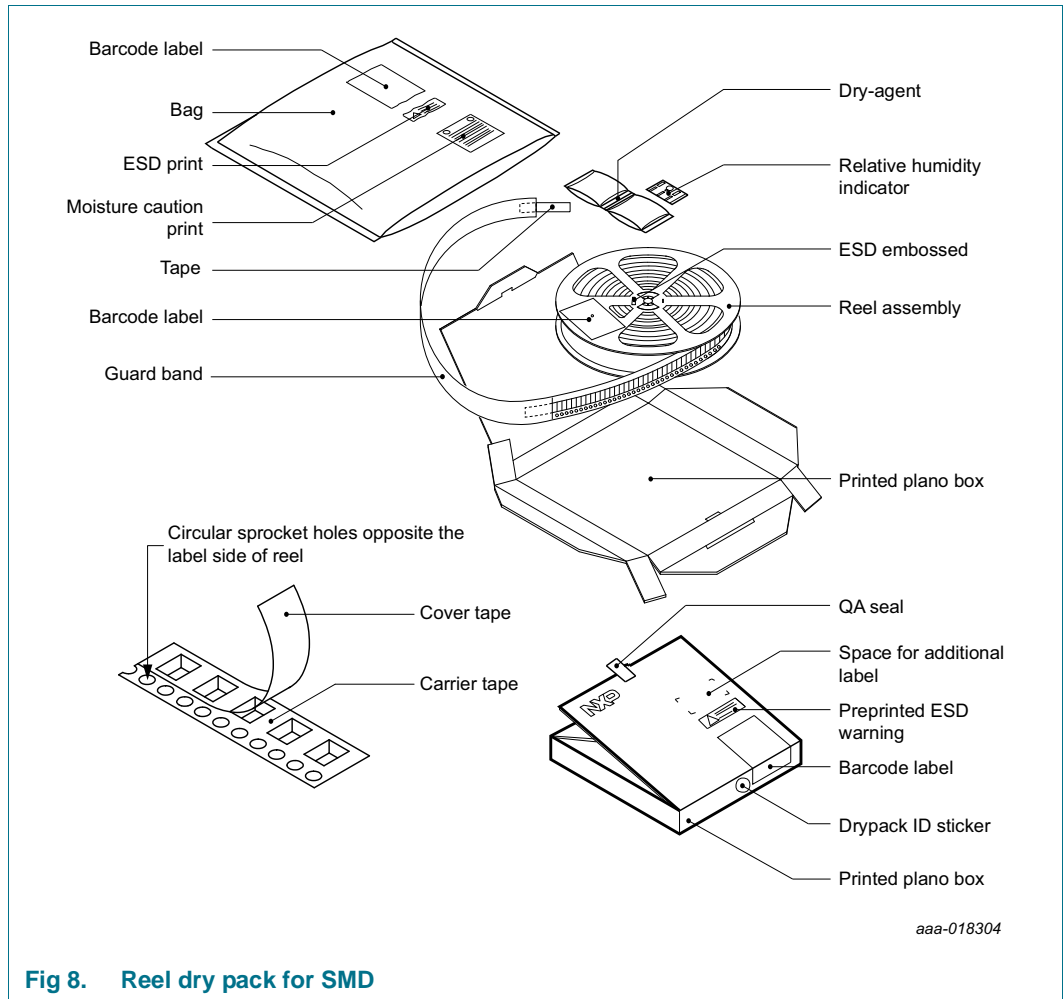


Table 14. Dimensions and quantities

| Reel dimensions d × w (mm) [1] | SPQ/PQ (pcs) [2] | Reels per box | Outer box dimensions l × w × h (mm) |
|-----------------------------------|---------------------|------------------|--|
| 330 × 8 | 10000 | 1 | 342 × 338 × 39 |

[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.

View ordering and availability details at [NXP order portal](#), or contact your local NXP representative.

13.1.1.1 Product orientation

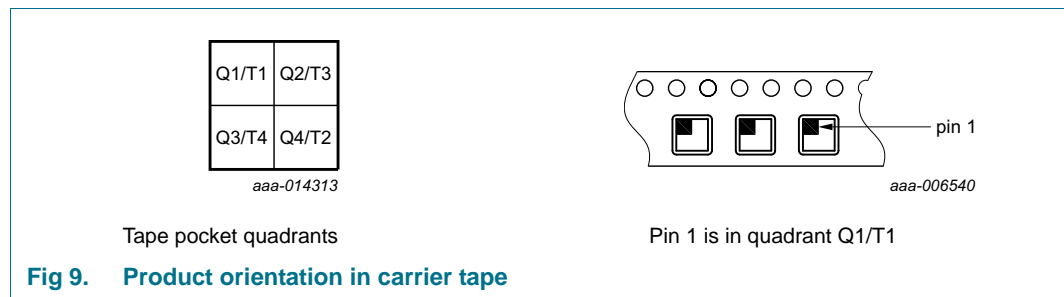


Fig 9. Product orientation in carrier tape

13.1.1.2 Carrier tape dimensions

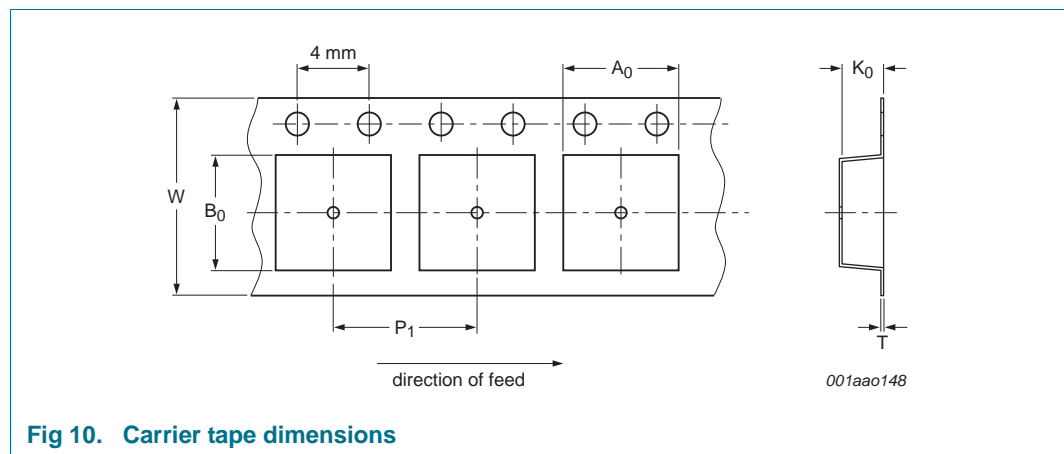


Fig 10. Carrier tape dimensions

Table 15. Carrier tape dimensions

In accordance with IEC 60286-3.

| A ₀ (mm) | B ₀ (mm) | K ₀ (mm) | T (mm) | P ₁ (mm) | W (mm) |
|---------------------|---------------------|---------------------|-------------|---------------------|-------------------|
| 2.25 ± 0.1 | 2.65 ± 0.1 | 0.53 ± 0.05 | 0.25 ± 0.03 | 4.0 ± 0.1 | 8.0 + 0.3 / - 0.1 |

13.1.1.3 Reel dimensions

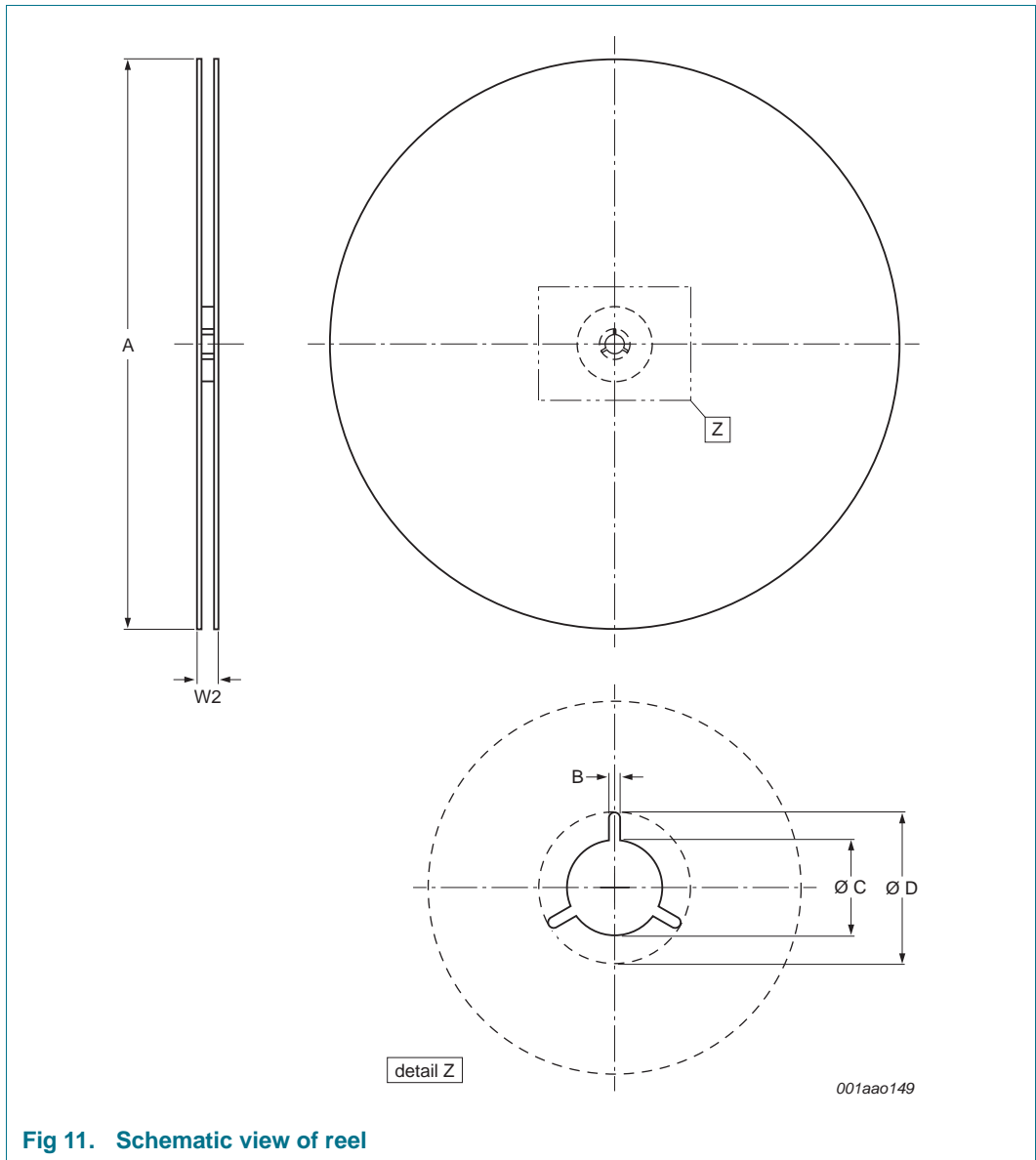


Fig 11. Schematic view of reel

Table 16. Reel dimensions
In accordance with IEC 60286-3.

| A [nom] (mm) | W2 [max] (mm) | B [min] (mm) | C [min] (mm) | D [min] (mm) |
|--------------|---------------|--------------|--------------|--------------|
| 330 | 14.4 | 1.5 | 12.8 | 20.2 |

13.1.1.4 Barcode label

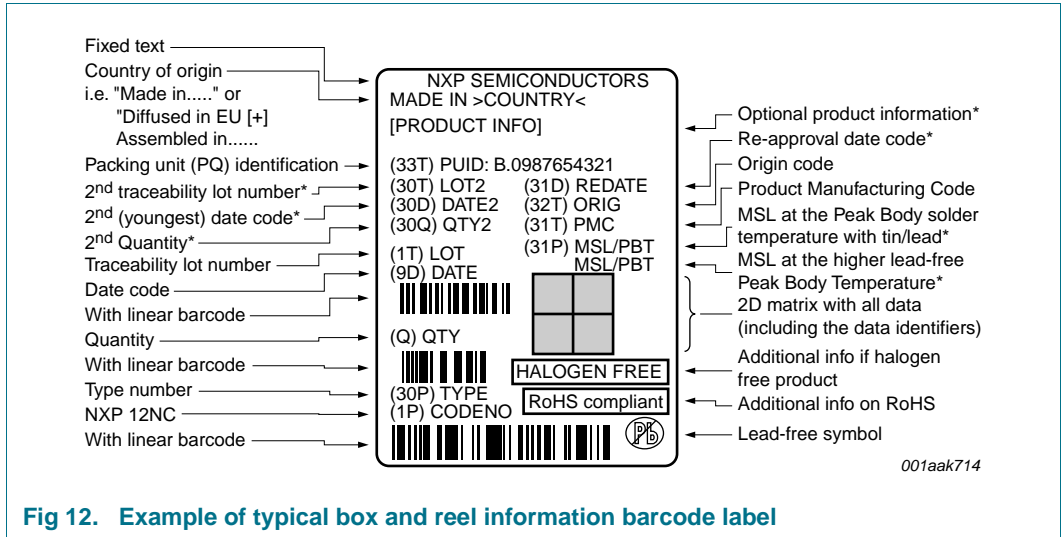


Fig 12. Example of typical box and reel information barcode label

Table 17. Barcode label dimensions

| Box barcode label l × w (mm) | Reel barcode label l × w (mm) |
|---------------------------------|----------------------------------|
| 100 × 75 | 100 × 75 |

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 13](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 18](#) and [19](#)

Table 18. SnPb eutectic process (from J-STD-020D)

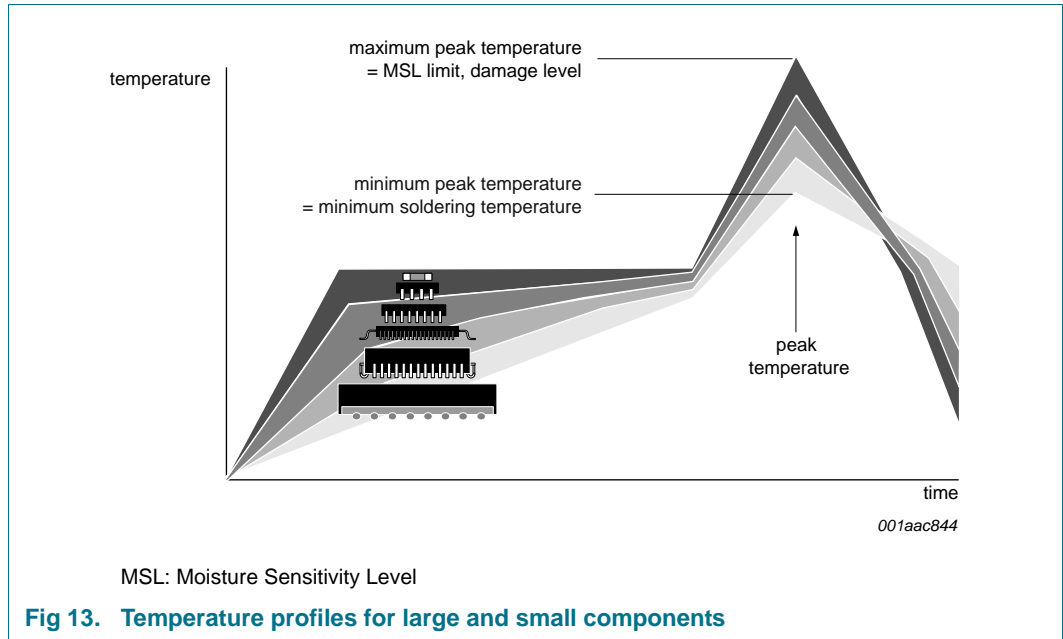
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 19. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

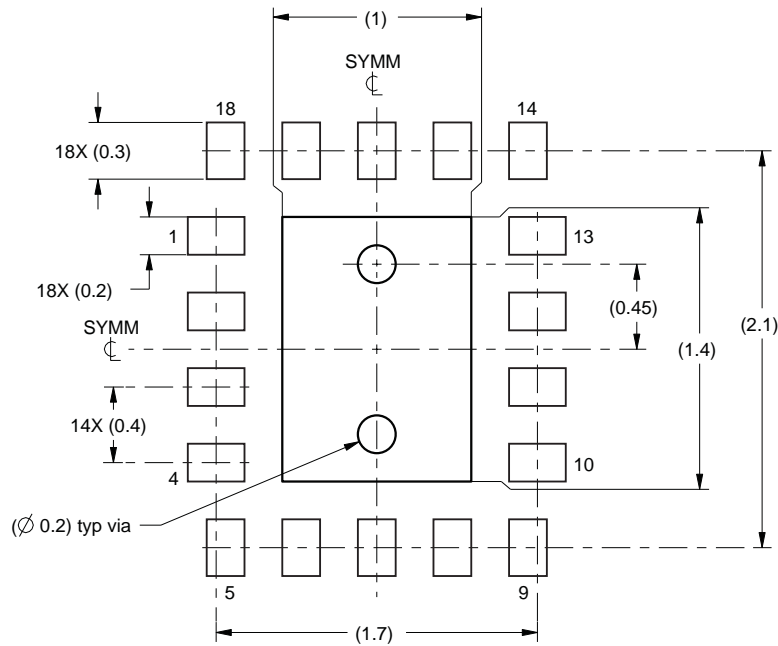
Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 13](#).

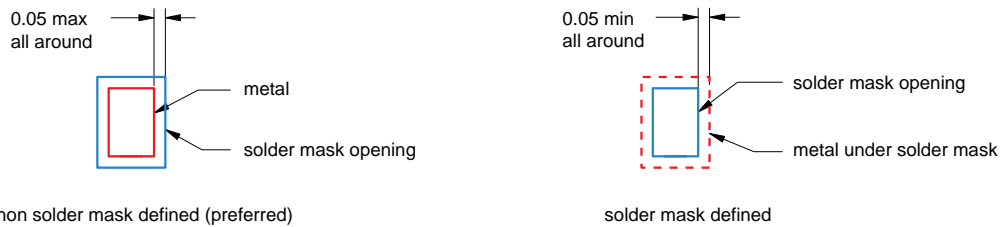


For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

15. Soldering

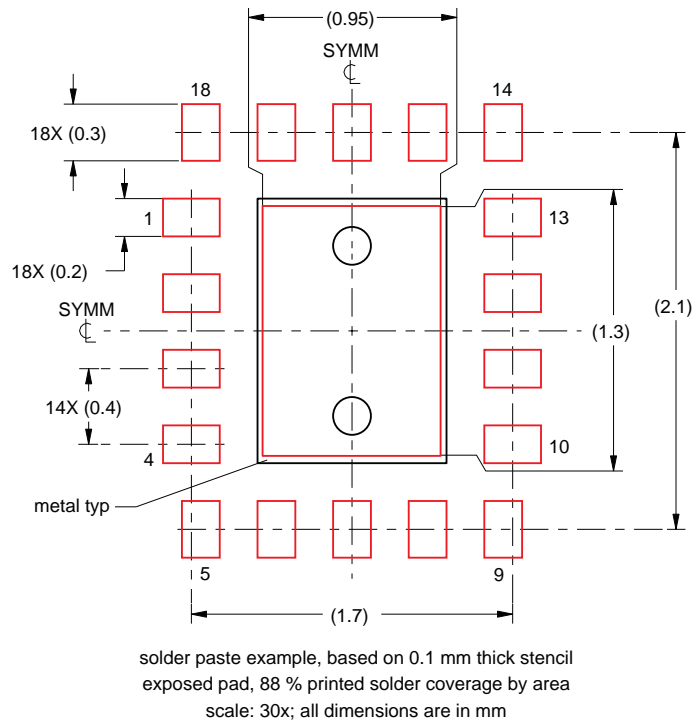


land pattern example
scale: 25x; all dimensions are in mm



aaa-021290

Fig 14. PCB footprint for SOT1442-1 (DHX2QFN18); reflow soldering



aaa-021333

Fig 15. Solder paste example

16. Abbreviations

Table 20. Abbreviations

| Acronym | Description |
|----------------------|---|
| A/V | Audio/Video device |
| AIO | All In One computer platform |
| CDM | Charged-Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| I ² C-bus | Inter-Integrated Circuit bus |
| I/O | Input/Output |
| IC | Integrated Circuit |
| ISI | InterSymbol Interference |
| LFPS | Low Frequency Periodic Signaling |
| PCB | Printed-Circuit Board |
| RX | Receive (or Receiver) |
| SI | Signal Integrity |
| TX | Transmit (or Transmitter) |
| USB | Universal Serial Bus |

17. Revision history

Table 21. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| PTN36043A v.1 | 20180219 | Product data sheet | - | - |

18. Legal information

18.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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20. Contents

| | | | | | |
|-----------|--|-----------|-----------|--------------------------------------|-----------|
| 1 | General description | 1 | 18.2 | Definitions | 27 |
| 2 | Features and benefits | 1 | 18.3 | Disclaimers | 27 |
| 3 | Applications | 2 | 18.4 | Trademarks | 28 |
| 4 | Ordering information | 2 | 19 | Contact information | 28 |
| 4.1 | Ordering options | 2 | 20 | Contents | 29 |
| 5 | Block diagram | 3 | | | |
| 6 | Pinning information | 4 | | | |
| 6.1 | Pinning | 4 | | | |
| 6.2 | Pin description | 4 | | | |
| 7 | Functional description | 6 | | | |
| 7.1 | Receive equalization, transmitter de-emphasis and output swing level controls | 6 | | | |
| 7.2 | Device states and power management | 7 | | | |
| 7.3 | SEL input pin | 8 | | | |
| 8 | Application guideline for Control of CHx_SETx and SEL input pins | 8 | | | |
| 9 | Limiting values | 9 | | | |
| 10 | Recommended operating conditions | 9 | | | |
| 11 | Characteristics | 10 | | | |
| 11.1 | Device characteristics | 10 | | | |
| 11.2 | Receiver AC/DC characteristics | 12 | | | |
| 11.3 | Transmitter AC/DC characteristics | 13 | | | |
| 11.4 | Ternary control inputs | 14 | | | |
| 12 | Package outline | 16 | | | |
| 13 | Packing information | 17 | | | |
| 13.1 | SOT1442-1 (DHXQFN18); Reel dry pack, SMD, 13" Q1/T1 standard product orientation; Orderable part number ending ,518 or Y; Ordering code (12NC) ending 518 | 17 | | | |
| 13.1.1 | Packing method | 17 | | | |
| 13.1.1.1 | Product orientation | 18 | | | |
| 13.1.1.2 | Carrier tape dimensions | 18 | | | |
| 13.1.1.3 | Reel dimensions | 19 | | | |
| 13.1.1.4 | Barcode label | 20 | | | |
| 14 | Soldering of SMD packages | 21 | | | |
| 14.1 | Introduction to soldering | 21 | | | |
| 14.2 | Wave and reflow soldering | 21 | | | |
| 14.3 | Wave soldering | 21 | | | |
| 14.4 | Reflow soldering | 22 | | | |
| 15 | Soldering | 24 | | | |
| 16 | Abbreviations | 26 | | | |
| 17 | Revision history | 26 | | | |
| 18 | Legal information | 27 | | | |
| 18.1 | Data sheet status | 27 | | | |

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