



**THE DATASHEET OF  
NX20P0407UKAZ**



# NX20P0407

## USB Type-C CC and SBU Protection IC

Rev. 1.3 — 22 August 2019

Product data sheet

## 1 General description

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The NX20P0407 is a single-chip USB Type-C port protection device that provides 28V short-to-VBUS overvoltage protection to CC1/CC2 and SBU1/SBU2 pins.

USB Type-C allows VBUS voltage to increase up to 20V through Power delivery protocol. CC1/2 and SBU1/2 pins can be shorted to VBUS due to mechanical twisting and sliding of the connector since Type-C connector contact pins are 25% closer to each other than a micro USB connector. Moisture or fine dust may also cause the 20V VBUS pin to be shorted to adjacent pins.

NX20P0407 enables CC and SBU pins to be more robust in even abnormal conditions. NX20P0407 is 28V DC tolerant on CON\_CC1, CON\_CC2, CON\_SBU1 and CON\_SBU2 pins in connector side and quickly disconnects switches if the voltage is above overvoltage threshold, protecting CC1, CC2, SBU1 and SBU2 in system side from high voltage.

NX20P0407 integrates IEC 61000-4-2 ESD protection on CON\_CC1 and CON\_CC2, +15KV air discharge and +8KV contact discharge, which helps to reduce external BOM cost. NX20P0407 CON\_CC1/2 pins are designed to be protected from surges up to +/- 35V.

## 2 Features and benefits

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- USB Type C CC1/2 and SBU1/2 short protection to VBUS
  - CON\_CC1 / CON\_CC2 : 28V<sub>DC</sub>
  - CON\_SBU1 / CON\_SBU2 : 28V<sub>DC</sub>
- Rd circuit in CON\_CC1/CON\_CC2 in dead battery
- Low R<sub>DSon</sub> switch
  - CC switch : 160mΩ
  - SBU switch : 3.6Ω
- Robust ESD immunity for CON\_CC1/2
  - IEC 61000-4-2 Contact discharge: 8KV
  - IEC 61000-4-2 Air discharge: 15KV
- +/- 35V surge protection on CON\_CC1/2
- Low SYS leakage current : 32μA
- CC1/2 leakage current : < 1μA
- Fast OVP turn off time : 60ns



### 3 Applications

- Smartphone
- Tablet
- Laptop

### 4 Ordering information

Table 1. Ordering information

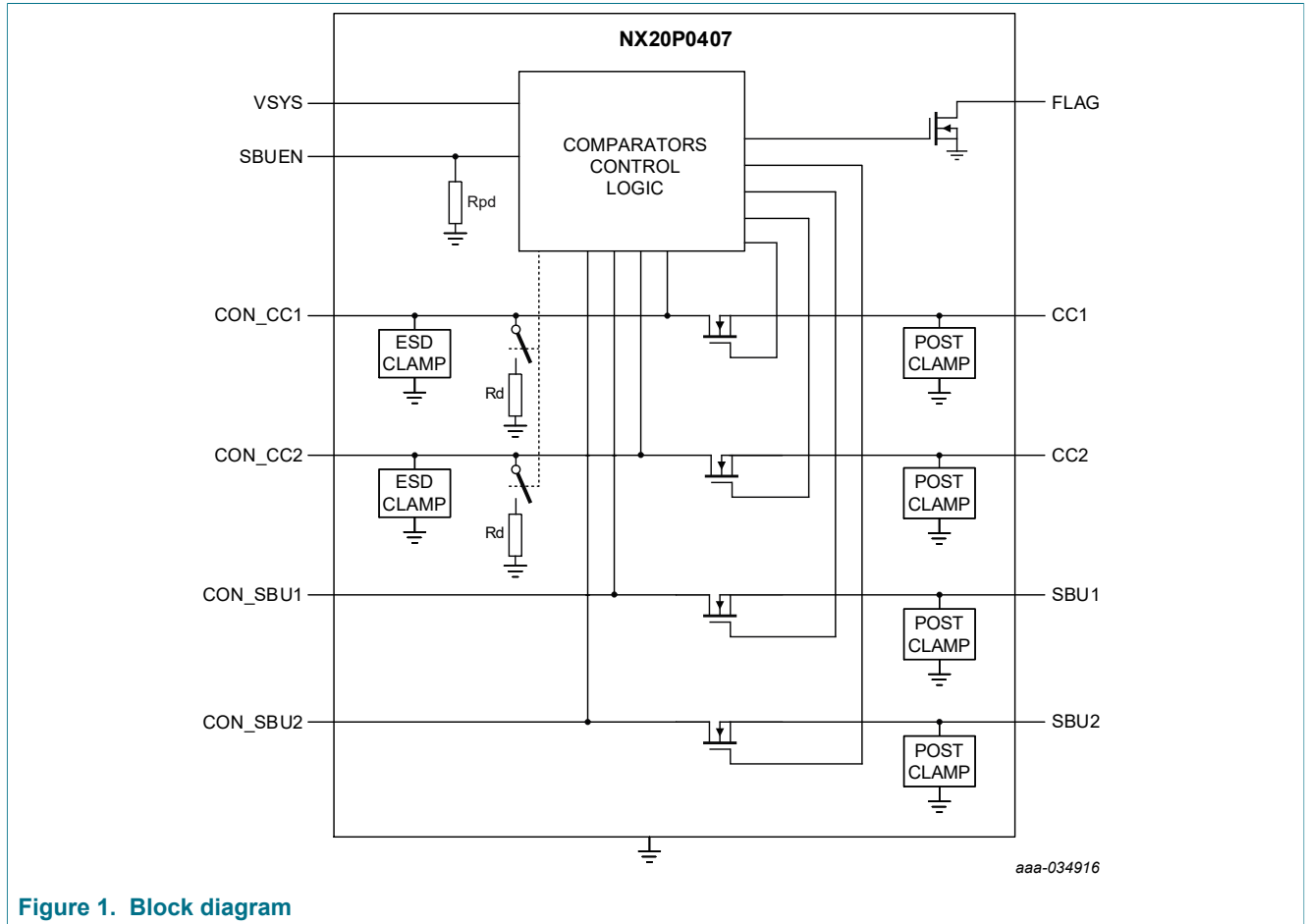
Type number	Topside marking	Package		
		Name	Description	Version
NX20P0407UK	N07	WLCSP12	Wafer level chip-scale package, 12 bumps; 1.67 mm x 1.27 mm x 0.525 mm body (backside coating included)	SOT1390-7

#### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX20P0407UK	NX20P0407UKAZ	WLCSP12	REEL 7" Q1/T1 DP CHIPS	4000	T <sub>amb</sub> = -40 °C to +85 °C
	NX20P0407UKZ	WLCSP12	REEL 13" Q1/T1 DP CHIPS	15000	T <sub>amb</sub> = -40 °C to +85 °C

**5 Functional diagram**



**Figure 1. Block diagram**

## 6 Pinning information

### 6.1 Pinning

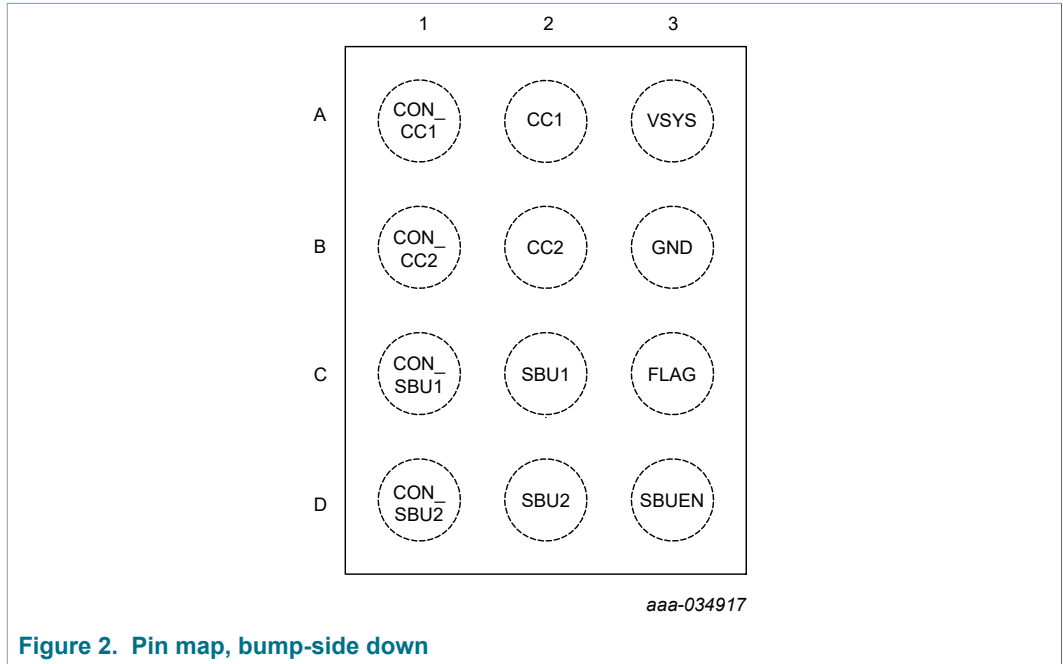


Figure 2. Pin map, bump-side down

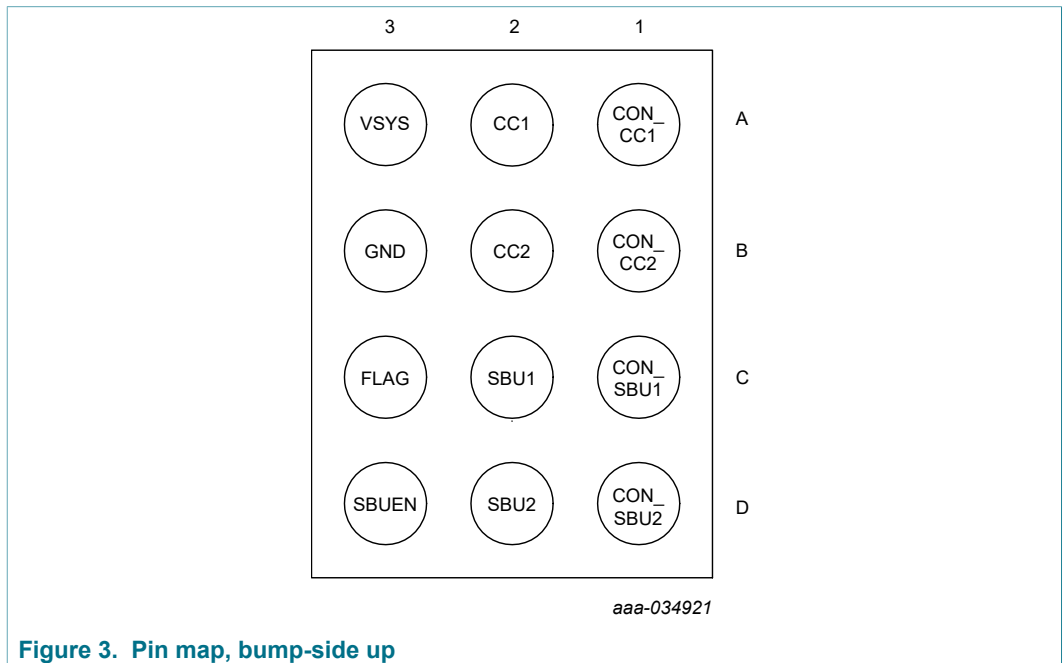


Figure 3. Pin map, bump-side up

## 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
CON_CC1	A1	P/AIO	Type-C connector side CC1. Connect CC1 of Type-C USB connector.
CON_CC2	B1	P/AIO	Type-C connector side CC2. Connect CC2 of Type-C USB connector.
CON_SBU1	C1	DIO	Type-C connector side SBU1. Connect SBU1 of Type-C USB connector.
CON_SBU2	D1	DIO	Type-C connector side SBU2. Connect SBU2 of Type-C USB connector.
CC1	A2	P/AIO	System side CC1. Connect CC1 of USB CC/PD controller.
CC2	B2	P/AIO	System side CC2. Connect CC2 of USB CC/PD controller.
SBU1	C2	DIO	System side SBU1.
SBU2	D2	DIO	System side SBU2.
SBUEN	D3	DI	SBU switch enable/disable control pin. SBUEN is driven high to enable SBU switch. There is a 460kΩ Internal pull-down resistor.
VSYS	A3	P	Power supply input; connect System voltage and bypass 1μF capacitor to GND.
FLAG	C3	DO	Open-drain output indicating fault condition. Low when Fault condition happens, external pull-up resistor is required.
GND	B3	P	Ground

## 7 Functional description

NX20P0407 is placed in front of Type-C connector and protects CC and SBU pins in System side from 20V VBUS short, ESD and surge.

NX20P0407 has Rd clamp circuit on both CON\_CC1 and CON\_CC2 when VSYS is below UVLO threshold, i.e., dead battery condition. It allows Type-C adapter to detect sink through CC and start providing 5V VBUS. Main charger regulates system voltage from the VBUS. Once VSYS comes up, NX20P0407 enables switches and disconnects the Rd clamp circuit from CON\_CC1 and CON\_CC2.

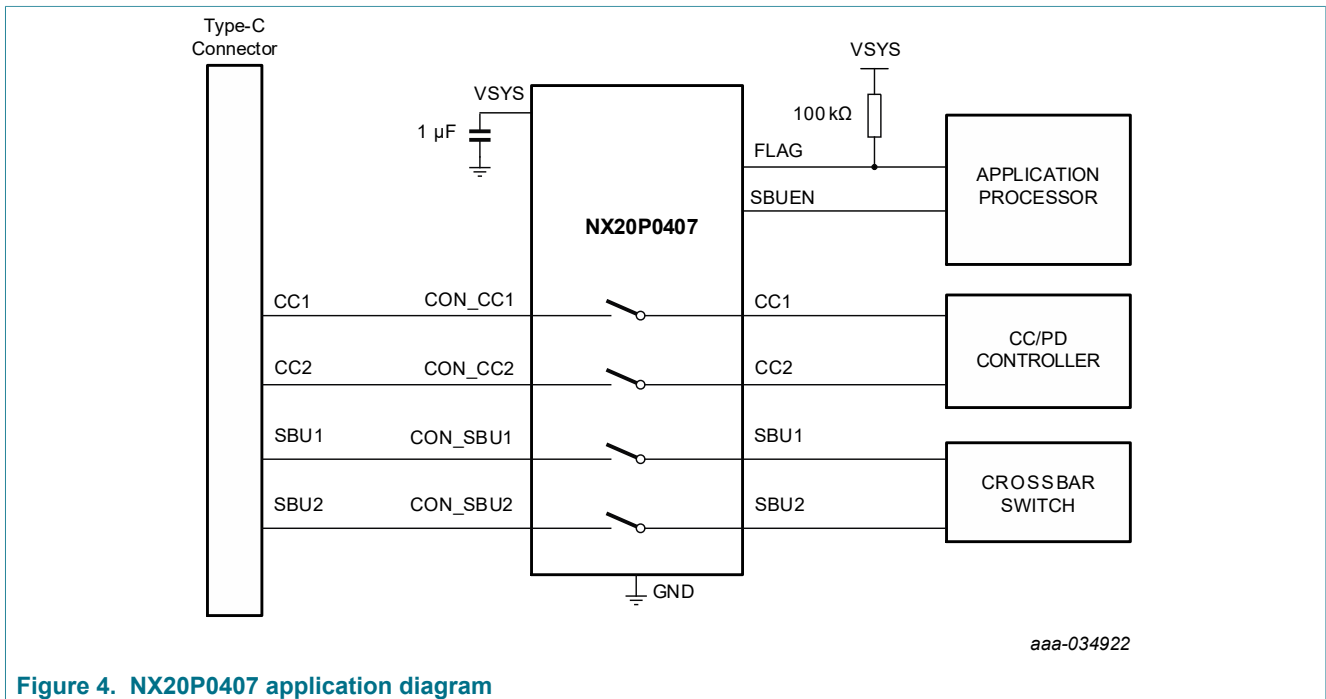


Figure 4. NX20P0407 application diagram

### 7.1 Power status

When VSYS is below  $V_{SYSUVLO}$ , NX20P0407 stays in shutdown mode. Bias circuit, switches and all comparators are disabled, but Rd clamp circuits on CON\_CC1 and CON\_CC2 are enabled. It allows the Type-C adapter to detect Rd and to supply 5V through VBUS pin in dead battery condition.

NX20P0407 enters standby mode when VSYS exceeds  $V_{SYSUVLO}$ . CC switch turns on automatically and SBU switch is controlled by SBUEN. After CC switch is fully turned ON, the Rd clamp circuit is disabled.

5V VCONN power supply on CC1 or CC2 should be supplied after VSYS is valid.

Table 4. Power states

Power states	VSYS	Flag	SBUEN	Rd circuit	CC Switch	SBU Switch
Dead battery	$< V_{SYSUVLO}$	Hi-Z	x	ON	OFF	OFF
Power ON_A	$> V_{SYSUVLO}$	Hi-Z	Low	OFF	ON	OFF
Power ON_B	$> V_{SYSUVLO}$	Hi-Z	High	OFF	ON	ON

### 7.2 Overvoltage protection

NX20P0407 has short circuit protection of CON\_CC1/2 and CON\_SBU1/2 up to 28V. CC switch overvoltage threshold is  $V_{OVP_{CC}}$  to guarantee VCONN power supply passes to VCONN load, which is maximum 5.5V by USB Type-C spec. SBU switch overvoltage threshold is  $V_{OVP_{SBU}}$  to securely turn the switch off and prevent high voltage to SBU in system side.

Once overvoltage on any channel is detected, the switch is quickly turned off within  $t_{OVP_{RES}}$ , to prevent overvoltage to system side. FLAG pin goes low in  $t_{FLAG_{RES}}$  to inform system of the fault condition. If the voltage of the channel triggered OVP comes down below overvoltage threshold for  $t_{OVP_{DEB}}$ , the switch is turned back on and FLAG pin gets Hi-Z.

Each of the four switches for CC1/2 and SBU1/2 has its own OVP comparator and is controlled by its comparator independently. If CC1 voltage exceeds OVP threshold, the CC1 switch is turned off, but the other switches stay ON.

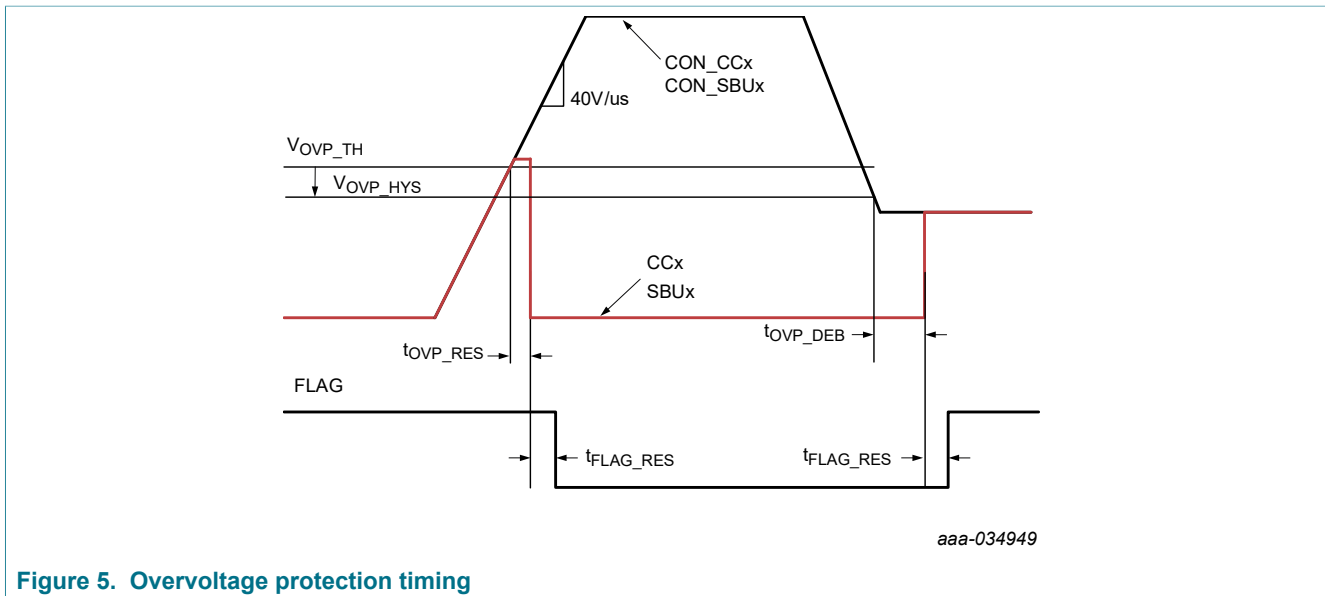
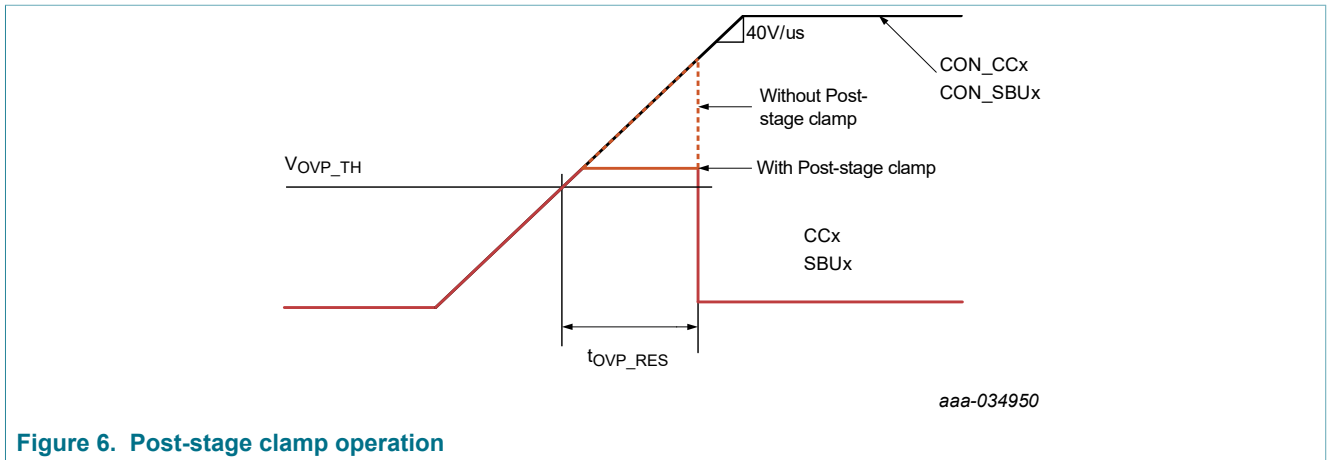


Figure 5. Overvoltage protection timing

### 7.3 Post-stage clamp circuit

NX20P0407 has a post-stage clamp circuit to clamp extra voltage on CC1, CC2, SBU1 and SBU2 in system side. When shorting with VBUS, the voltage on CON\_CCx and SBU\_CCx is rapidly increased. Even though NX20P0407 features super fast response time for overvoltage condition, the overvoltage may pass through to CCx / SBUx for the response time,  $t_{OVP_{RES}}$ . NX20P0407 post-stage clamp circuit provides secondary protection to clamp the voltage on CCx/ SBUx in system side, to prevent exceeding 7V Clamping voltage.



### 7.4 Flag

Flag pin is an open drain output to indicate device fault condition to application processor. If Fault condition is detected, Flag output is latched to low until the fault condition is cleared.

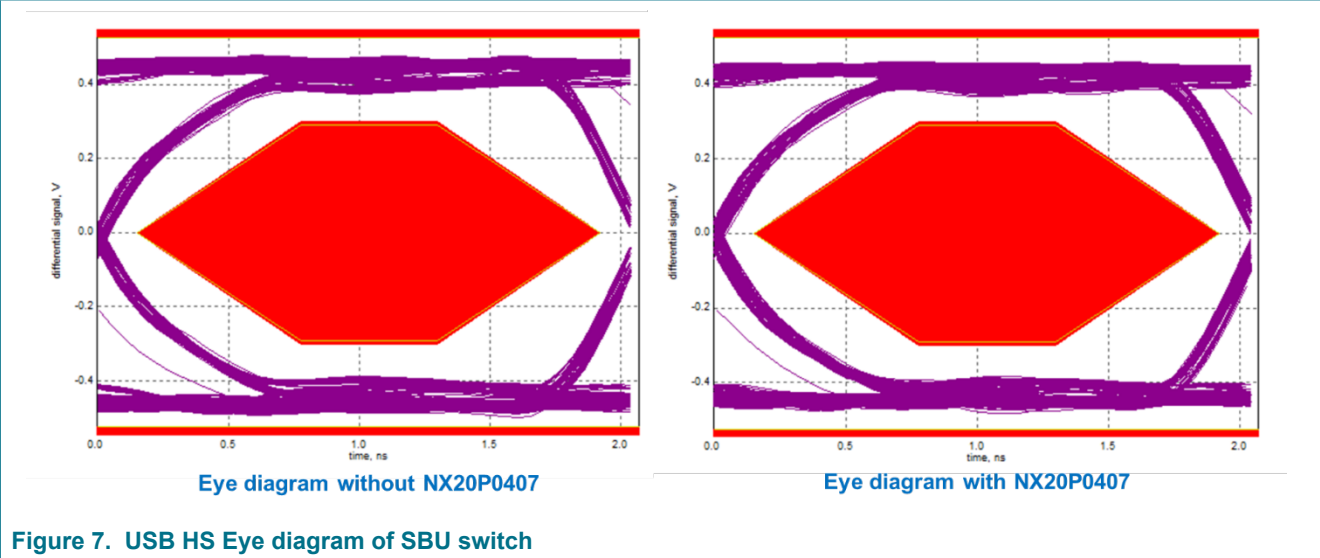
Table 5 shows NX20P0407 fault conditions and its behavior.

Table 5. Fault conditions and behavior

Fault	Condition	SBUEN	Flag	CC Switch	SBU Switch
Thermal Protection	$T_j > T_{OTP}$	Low	Low	ON	OFF
Thermal Protection	$T_j > T_{OTP}$	High	Low	ON	ON
CC OVP	$V_{CON\_CCx} > V_{OVPC}$	Low	Low	OFF	OFF
CC OVP	$V_{CON\_CCx} > V_{OVPC}$	High	Low	OFF	ON
SBU OVP	$V_{CON\_SBUx} > V_{OVPSBU}$	Low	Hi-Z	ON	OFF
SBU OVP	$V_{CON\_SBUx} > V_{OVPSBU}$	High	Low	ON	OFF

### 7.5 CC and SBU Switch

NX20P0407 has two pairs of switches: CC switches and SBU switches. CC switches are always ON when SYS power is valid and there is no fault condition. The switches are capable of +/- 1.2A current with  $R_{ON\_CC}$  switch resistance. SBU switches are controlled by SBUEN when SYS power is valid. The switch bandwidth is 1.5GHz so that it can be used to protect USB D+/D- from overvoltage if SBU is not used.



## 8 Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>IO</sub>	input/output voltage	CON_CC1, CON_CC2, CON_SBU1, CON_SBU2	-0.5	28	V
		CC1, CC2, SBU1, SBU2	-0.5	6	V
V <sub>I</sub>	input voltage	SBUEN, VSYS	-0.5	6	V
V <sub>O</sub>	output voltage	FLAG	-0.5	6	V
I <sub>O</sub>	output current	CON_CC1, CON_CC2, CC1, CC2; T <sub>j</sub> < 105°C	-1.25	1.25	A
		CON_SBU1, CON_SBU2, SBU1, SBU2	-100	100	mA
T <sub>j</sub>	junction temperature		-40	135	°C
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2 Contact discharge; CON_CC1, CON_CC2	-8	+8	kV
		IEC 61000-4-2 Air discharge; CON_CC1, CON_CC2	+15	+15	kV
		HBM (JESD22-001); all other pins	-2	+2	kV
		CDM (JESD22-C101E); all other pins	-500	+500	V

## 9 Recommended operating conditions

**Table 7. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>IO</sub>	input/output voltage	CC1, CC2, CON_CC1, CON_CC	0	5.5	V
		SBU1, SBU2, CON_SBU1, CON_SBU2	0	4.5	V
V <sub>I</sub>	input voltage	SBUEN	0	5.5	V
		VSYS	2.5	5.5	V
V <sub>O</sub>	output voltage	FLAG	0	5.5	V
I <sub>IO(CC)</sub>	CC input/output current	CON_CC1, CON_CC2, CC1, CC2; V <sub>CC</sub> - V <sub>CON_CC</sub> ≤ 300mV	-1.2	+1.2	A
T <sub>amb</sub>	ambient temperature		-40	85	°C

## 10 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1] [2] 110	°C/W

- [1] The overall  $R_{th(j-a)}$  can vary depending on the board layout. To minimize the effective  $R_{th(j-a)}$ , all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.
- [2] This  $R_{th(j-a)}$  is calculated based on JEDEX2S2P board. The actual  $R_{th(j-a)}$  value may vary in applications using different layer stacks and layouts.

## 11 Electrical characteristics

### 11.1 Static characteristics

Table 9. Static characteristics

At recommended input voltages and  $T_{amb} = -40\text{ °C}$  to  $+85\text{ °C}$ ; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply current / Leakage current</b>						
$V_{SYSUVLO}$	VSYS Under Voltage Lockout	Falling, 100mV hysteresis	2.14	2.27	2.40	V
$I_{SYS}$	Standby current	$V_{SYS} = 3.6V$ , $SBUEN = 0V$ $CCx = 5.1k\Omega$		32	55.5	$\mu A$
		$V_{SYS} = 3.6V$ , $SBUEN = 3.6V$ $CCx = 5.1k\Omega$		107	170	$\mu A$
$I_{CC\_Leak}$	Leakage current for CC pins	$V_{SYS} = 3.6V$ , $V_{CCx} = 3.0V$ , CON_CCx floating, $V_{SYS} > V_{CCx} + 0.6V$			1	$\mu A$
	Leakage current for CC pins	$V_{SYS} = 3.6V$ , $V_{CCx} = 3.6V$ , CON_CCx floating, $V_{SYS} < V_{CCx} + 0.6V$			5	$\mu A$
$I_{SBU\_Leak}$	Leakage current for SBU pins	$V_{SYS} = 3.6V$ , $V_{SBUx} = 3.6V$ , CON_SBUx floating			1	$\mu A$
<b>CC switcher</b>						
$R_{on\_CC}$	On resistance	$V_{SYS} = 3.6V$ , $V_{CCx} = 5.5V$	-	160	250	m $\Omega$
$R_{on\_CC\_Flat}$	On resistance flatness	Sweep CCx voltage between 0V and 3.6V		2	10	m $\Omega$
$V_{CLAMPH}$	CON_CCx clamping voltage	External 330 $\mu A$	0.9		2.13	V
$V_{CLAMPM}$	CON_CCx clamping voltage	External 180 $\mu A$	0.5		1.2	V
$V_{CLAMPD}$	CON_CCx clamping voltage	External 80 $\mu A$	0.3		1.2	V
$V_{OVPC}$	OVP threshold on CON_CCx	$V_{SYS} = 3.6V$ , rising	5.6	5.8	6.0	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OVPC\_hys}$	OVP threshold hysteresis			100		mV
$C_{on\_cc}$	Equivalent on capacitance	Capacitance between CCx/CON_CCx and GND when Powered up. $V_{CCx} = 0V$ to $1.2V$ , $f = 240MHz$		25		pF
$BW_{CC}$	3dB Bandwidth	Single ended, $50\Omega$ termination, $V_{CCx} = 0.1V$ to $1.2V$		250		MHz
$V_{CLAMP}$	Clamp voltage on system side	Hot plug voltage CON_CCx = $22V$ . load $150nF$ cap and $40\Omega$ in series to GND on CCx $40V/us$		7		V
<b>SBU switcher</b>						
$R_{on\_SBU}$	On resistance	$V_{SYS} = 3.6V$ , SBUEN = High, $SBUx = 3.6V$	-	3.6	5.4	$\Omega$
$R_{on\_SBU\_Flat}$	On resistance flatness	Sweep SBUx voltage between $0V$ and $3.6V$		30	150	m $\Omega$
$V_{OVPSBU}$	OVP threshold on CON_SBUx	$V_{SYS} = 3.6V$ , SBUEN = High, rising	4.6	4.8	5.0	V
$V_{OVPSBU\_hys}$	OVP threshold hysteresis			100		mV
$C_{on\_SBU}$	Equivalent on capacitance	Capacitance between SBUx/CON_SBUx and GND when Powered up. $V_{SBUx} = 0V$ to $1.2V$ , $f = 240MHz$		4.5		pF
$BW_{SBU}$	3dB Bandwidth	Single ended, $50\Omega$ termination, $V_{SBUx} = 0.1V$ to $1.2V$		1500		MHz
XTALK	Crosstalk	Swing $1V_{pp}$ at $10MHz$ , measure the other channels with $50m\Omega$ termination		-84		dB
$V_{CLAMP}$	Clamp voltage on system side	Hot plug voltage CON_SBUx = $22V$ . load $150nF$ cap and $40\Omega$ in series to GND on SBUx		7		V
<b>FLAG</b>						
$V_{OL}$	Output low voltage	$I_{OL} = 5mA$			0.3	V
$I_{OH}$	High level leakage current	$V_{FLAG} = 5.5V$			1	$\mu A$
<b>SBUEN</b>						
$V_{IH}$	Valid input high		1.5			V
$V_{IL}$	Valid input low				0.4	V
$R_{PD}$	Pull down resistor		350	450	600	k $\Omega$
<b>Over Temperature flag</b>						
$T_{OTP}$	Over temperature Flag			125		$^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T <sub>OTP_hys</sub>	Over temperature Flag hysteresis		-	10	-	°C

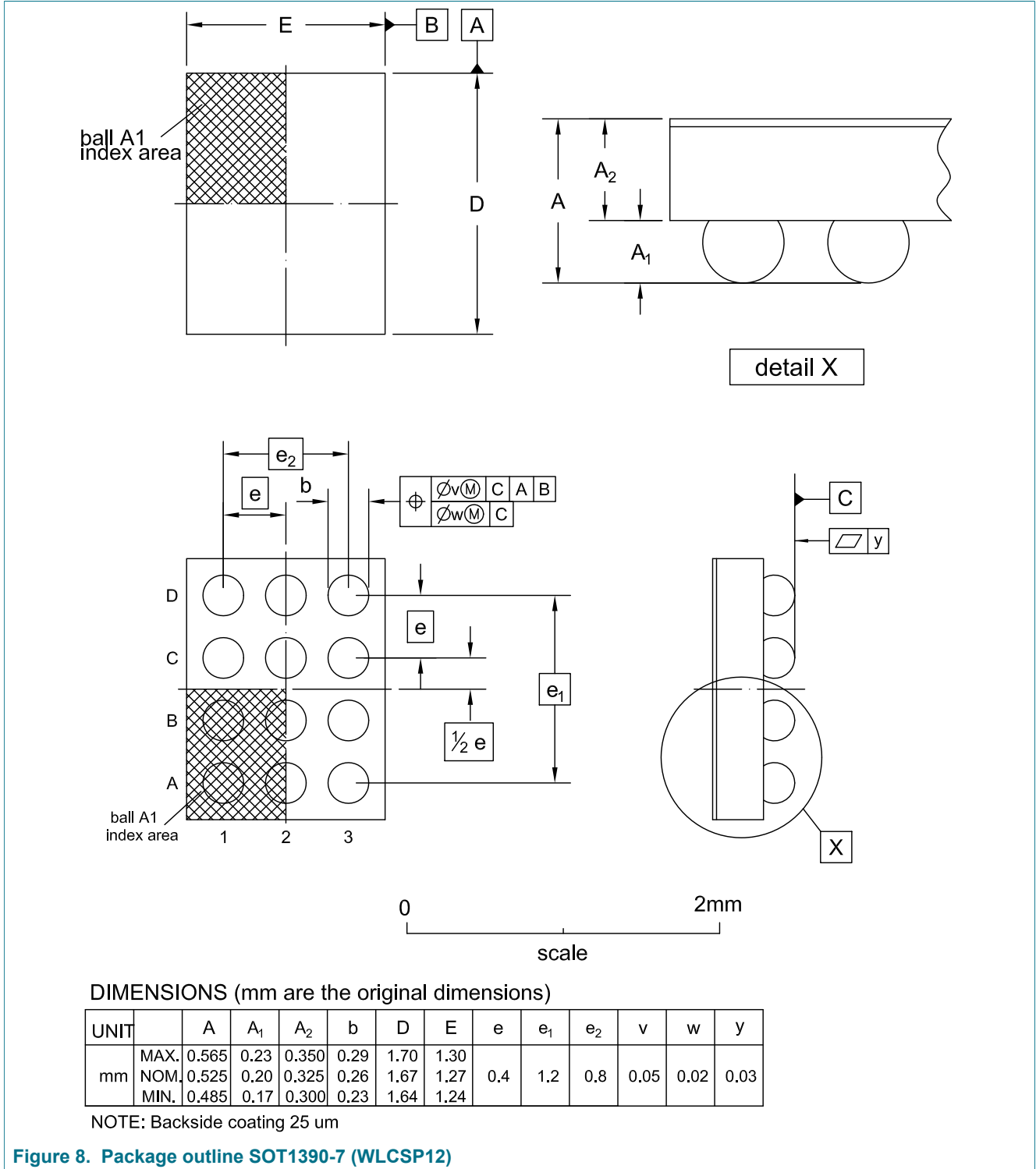
## 11.2 Dynamic characteristics

Table 10. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Switch Dynamic Characteristics</b>						
t <sub>pwrap</sub>	Power up time from Valid power source of VSYS			2.5	5	ms
t <sub>OVP_res_CC</sub>	OVP response time	Time from OVP trip voltage asserted to OVP FET turn-off	-	60		ns
t <sub>OVP_res_SBU</sub>	OVP response time	Time from OVP trip voltage asserted to OVP FET turn-off	-	60		ns
t <sub>OVP_deb</sub>	Minimum time to exit OVP shutdown, CON_CCx or CON_SBUx voltage should be lower than OVP voltage for this time		-	20		ms
t <sub>SBU_ON</sub>	SBU switch enable time from SBUEN to high			40	80	us
t <sub>OTP_deb</sub>	Minimum time to exit over temperature flag	[1]	-	20		ms
t <sub>FLAG_RES</sub>	Time to FLAG assertion from OVP detected.			5		us
t <sub>OTP_flag</sub>	Time to Flag from over temperature	[1]		20		us

[1] Guaranteed by Design

12 Package outline



## 13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX20P0407 v.1.3	20190822	Product data sheet	-	NX20P0407 v.1.2

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management