THE DATASHEET OF

AOD661

ALPHA & OMEGA SEMICONDUCTOR

AOD661

30V Dual Complementary MOSFET

General Description

- Trench Power MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Excellent Thermal Performance
- RoHS and Halogen-Free Compliant

Applications

- Pch+Nch Complementary MOSFET for DC-FAN

Product Summary

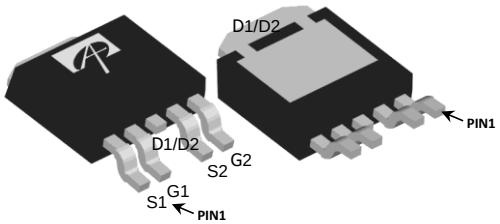
	Q1	Q2
V_{DS}	30V	-30V
I_D (at V_{GS}=10V)	12A	-12A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 16.5mΩ	< 22.5mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 21mΩ	< 36mΩ

100% UIS Tested
100% Rg Tested

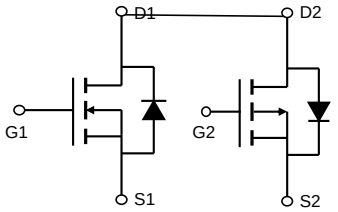
Green Product

TO252-4L
DPAK

Top View



Bottom View



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD661	TO-252-4L	Tape & Reel	2500

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	12	-12	A
	T_C=100°C		12	-9.4	
Pulsed Drain Current [C]		I_{DM}	50	-50	
Continuous Drain Current [G]	T_A=25°C	I_{DSM}	12	12	A
	T_A=70°C		11	10.5	
Avalanche Current [C]		I_{AS}	22	-27	A
Avalanche energy	L=0.1mH [C]	E_{AS}	24	36	mJ
V_{DS} Spike	10µs	V_{SPIKE}	36	-36	V
Power Dissipation [B]	T_C=25°C	P_D	15.6	31.0	W
	T_C=100°C		6.2	12.5	
Power Dissipation [A]	T_A=25°C	P_{DSM}	4.4	6.2	W
	T_A=70°C		2.8	4	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	20	15	28	20	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		45	35	60	45	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	6	3	8	4	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	ID=250µA, VGS=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1.5	1.9	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A		13	16.5	mΩ
		T_J=125°C		19	24	
		V_{GS}=4.5V, I_D=10A		16	21	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=12A		43		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				10	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		760		pF
C_{oss}	Output Capacitance			125		pF
C_{rss}	Reverse Transfer Capacitance			70		pF
R_g	Gate resistance	f=1MHz	0.8	1.6	2.4	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=12A		14	20	nC
Q_g(4.5V)	Total Gate Charge			6.6	10	nC
Q_{gs}	Gate Source Charge			2.4		nC
Q_{gd}	Gate Drain Charge			3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.25Ω, R_{GEN}=3Ω		4.4		ns
t_r	Turn-On Rise Time			9		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, di/dt=500A/µs		7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, di/dt=500A/µs		8		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

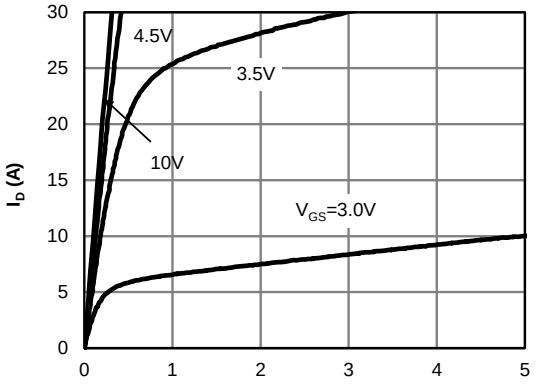


Figure 1: On-Region Characteristics (Note E)

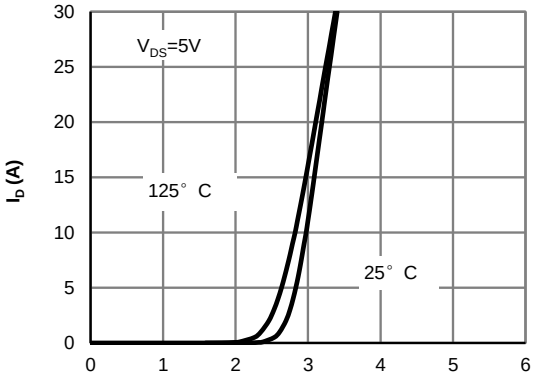


Figure 2: Transfer Characteristics (Note E)

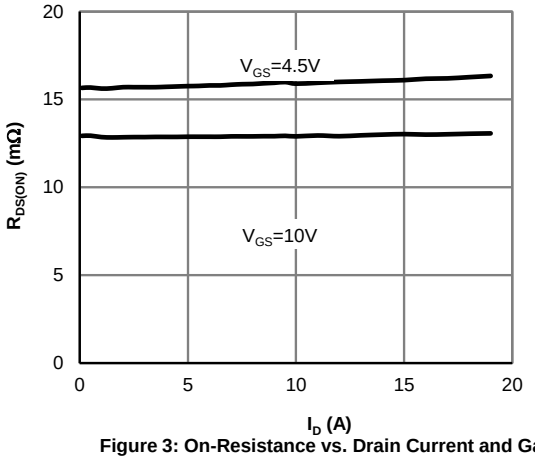


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

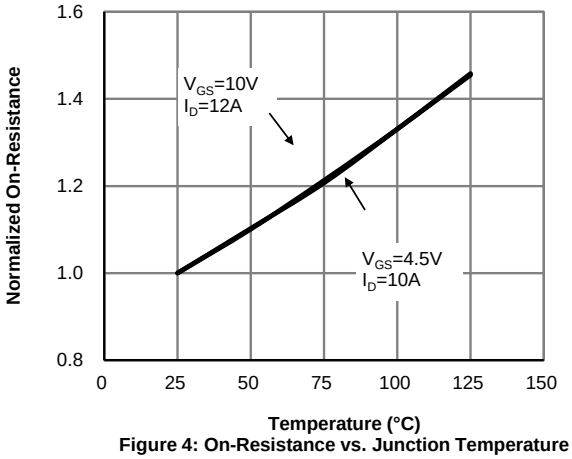


Figure 4: On-Resistance vs. Junction Temperature (Note E)

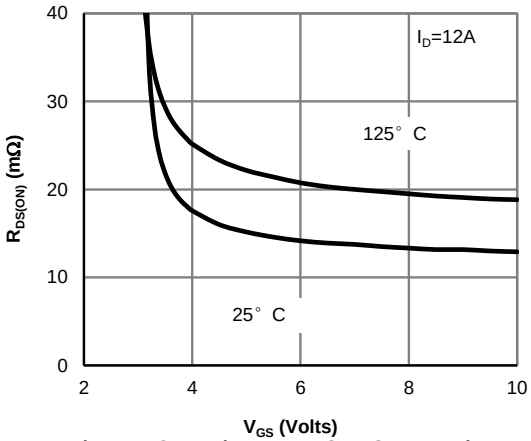


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

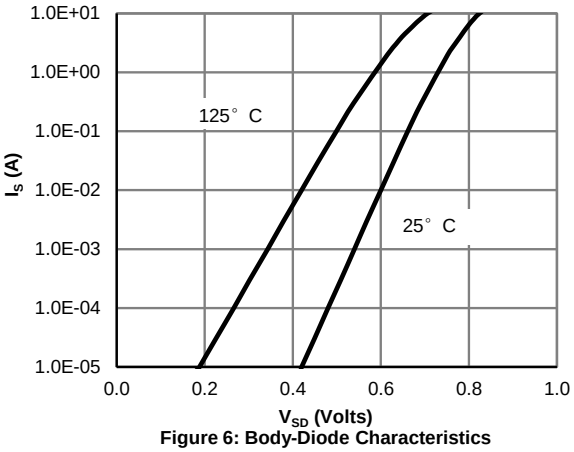


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

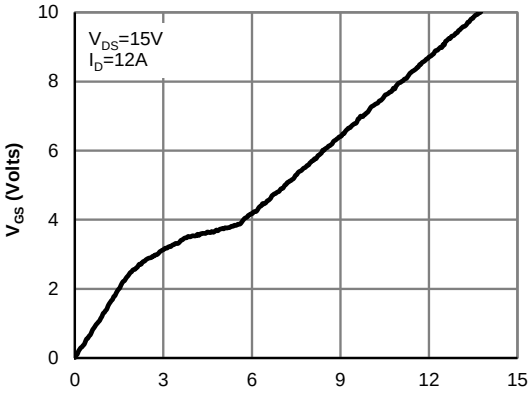


Figure 7: Gate-Charge Characteristics

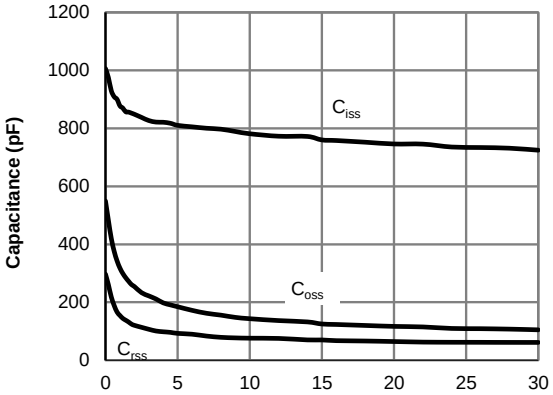
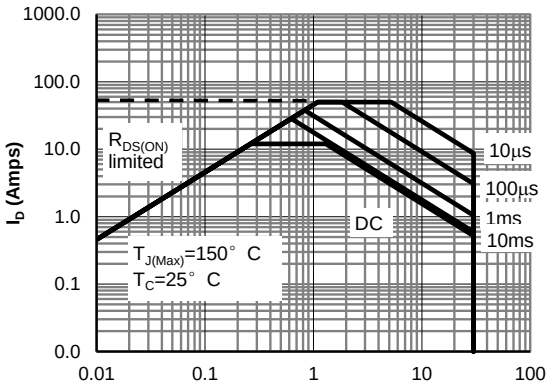


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

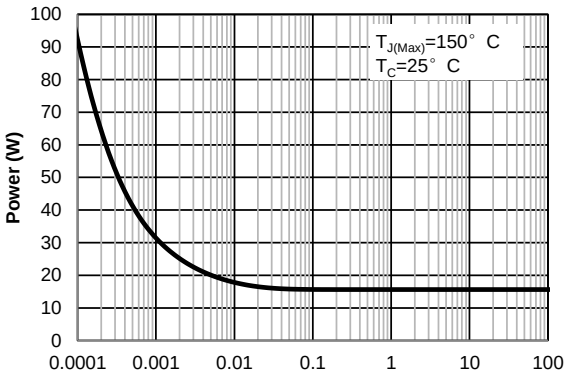


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

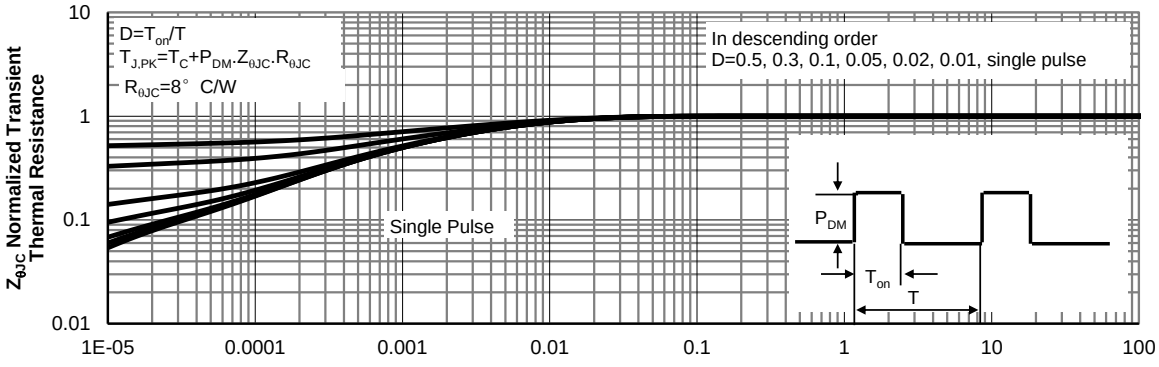


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

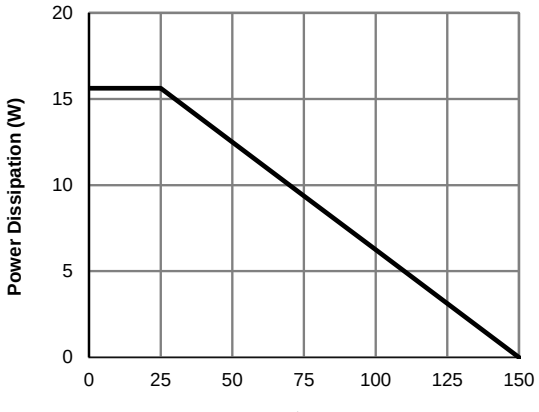


Figure 12: Power De-rating (Note F)

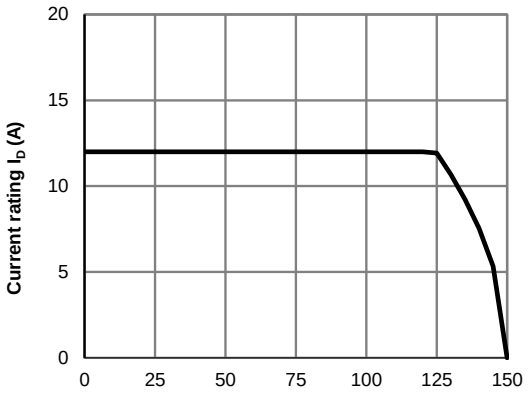


Figure 13: Current De-rating (Note F)

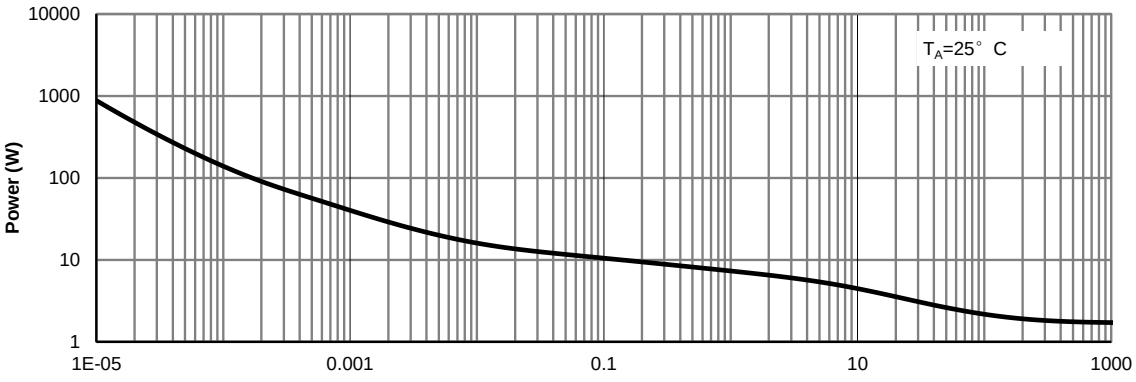


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

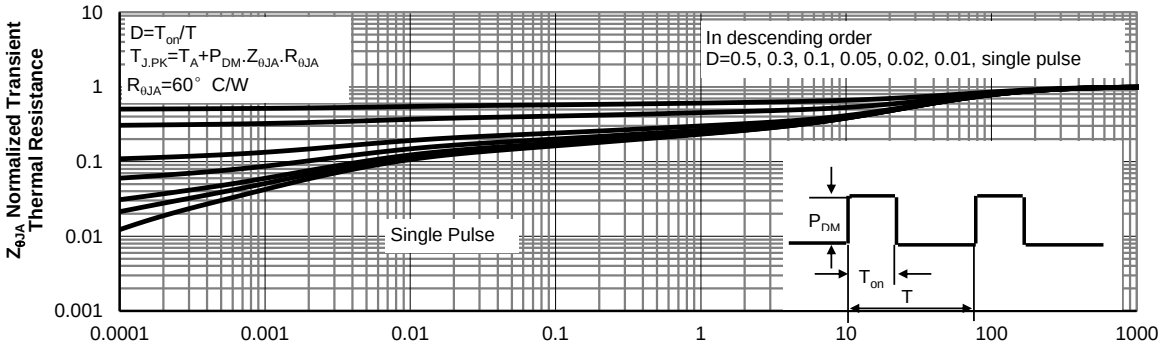


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V		-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V				-1	µA
			T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=-250µA		-1.5	-2.0	-2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-9.7A			17	22.5	mΩ
			T_J=125°C		24	32	
		V_{GS}=-4.5V, I_D=-7A			26.5	36	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-9.7A			27		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V			-0.75	-1	V
I_S	Maximum Body-Diode Continuous Current [G]					-12	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz			1040		pF
C_{oss}	Output Capacitance				180		pF
C_{rss}	Reverse Transfer Capacitance				125		pF
R_g	Gate resistance	f=1MHz		2	4	6	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-9.7A			19	30	nC
Q_g(4.5V)	Total Gate Charge				9.6	15	nC
Q_{gs}	Gate Source Charge				3.6		nC
Q_{gd}	Gate Drain Charge				4.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=1.5Ω, R_{GEN}=3Ω			10		ns
t_r	Turn-On Rise Time				5.5		ns
$t_{D(off)}$	Turn-Off DelayTime				26.0		ns
t_f	Turn-Off Fall Time				9		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-9.7A, dI/dt=500A/µs			11.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-9.7A, dI/dt=500A/µs			25		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

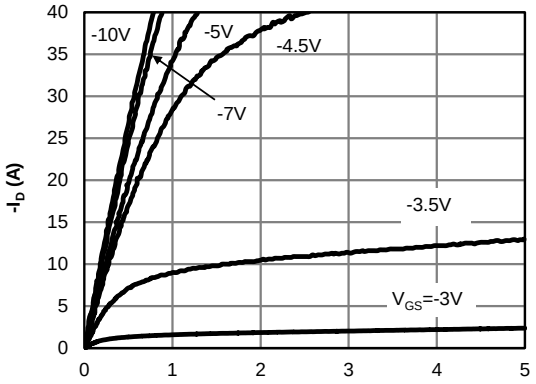


Figure 1: On-Region Characteristics (Note E)

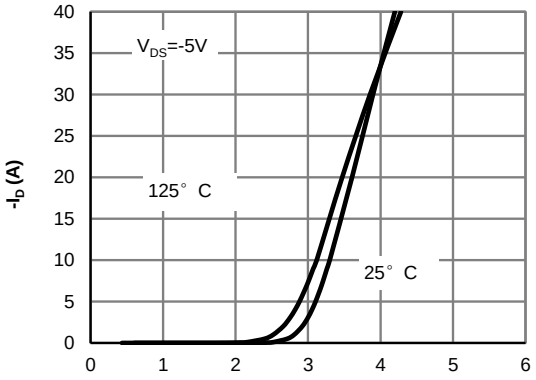


Figure 2: Transfer Characteristics (Note E)

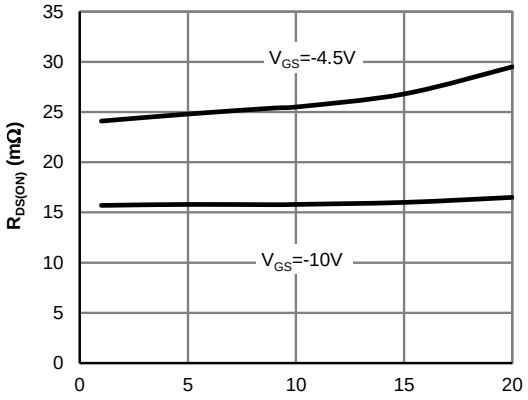


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

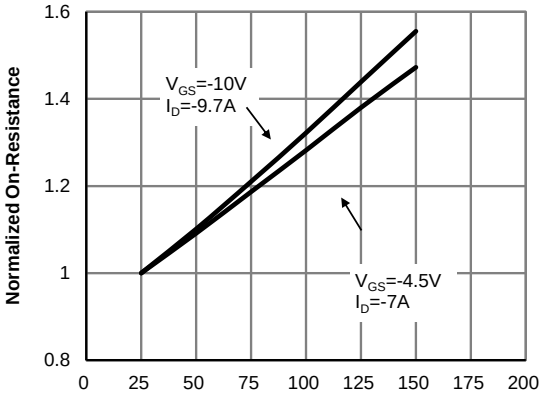


Figure 4: On-Resistance vs. Junction Temperature (Note E)

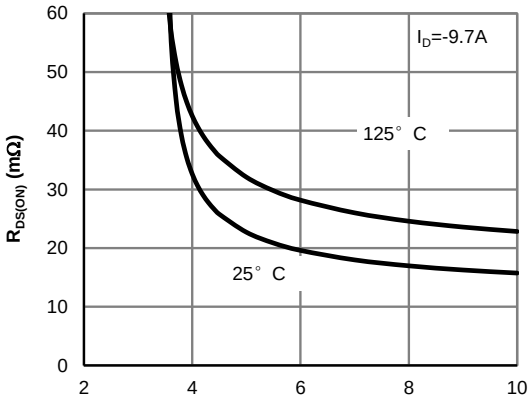


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

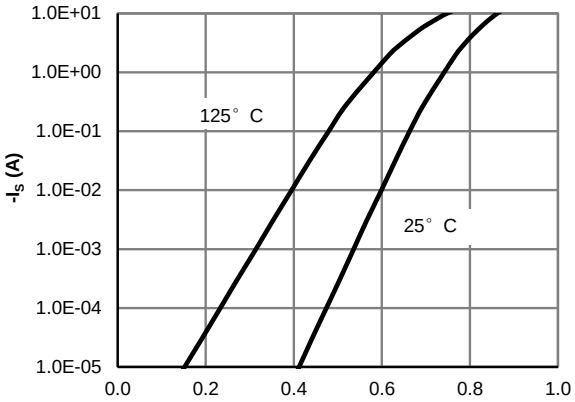


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

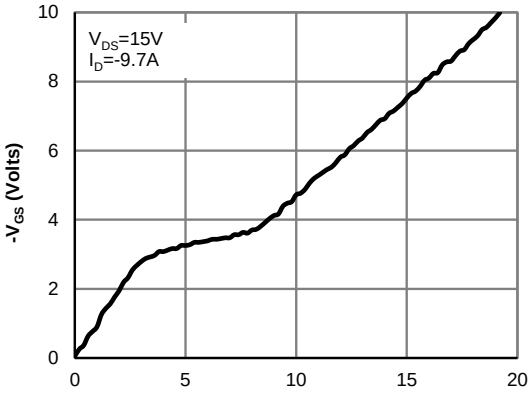


Figure 7: Gate-Charge Characteristics

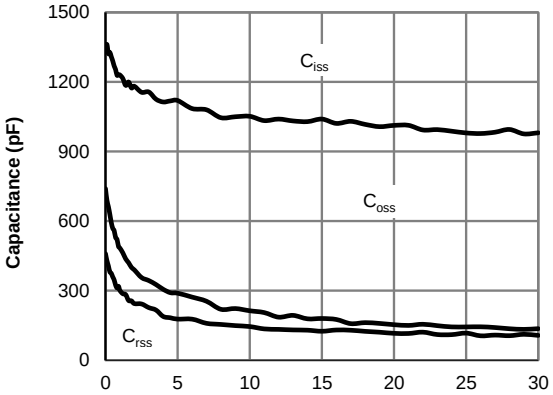
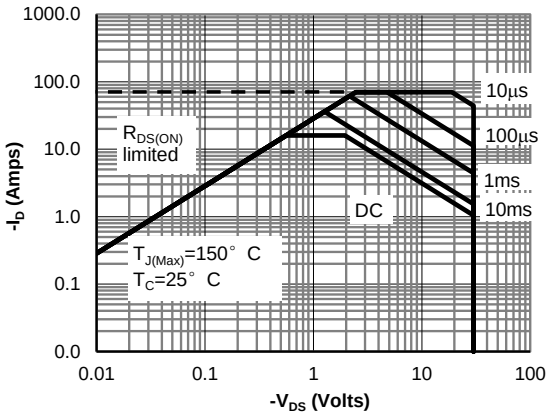


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

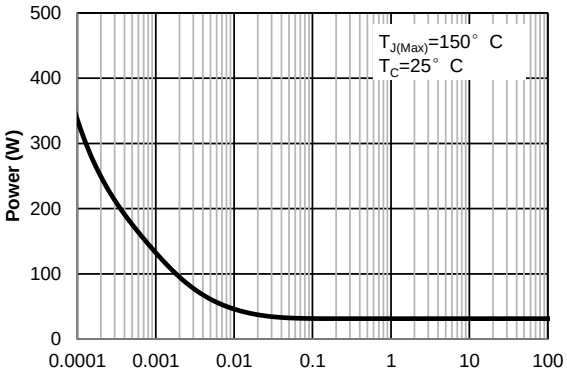


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

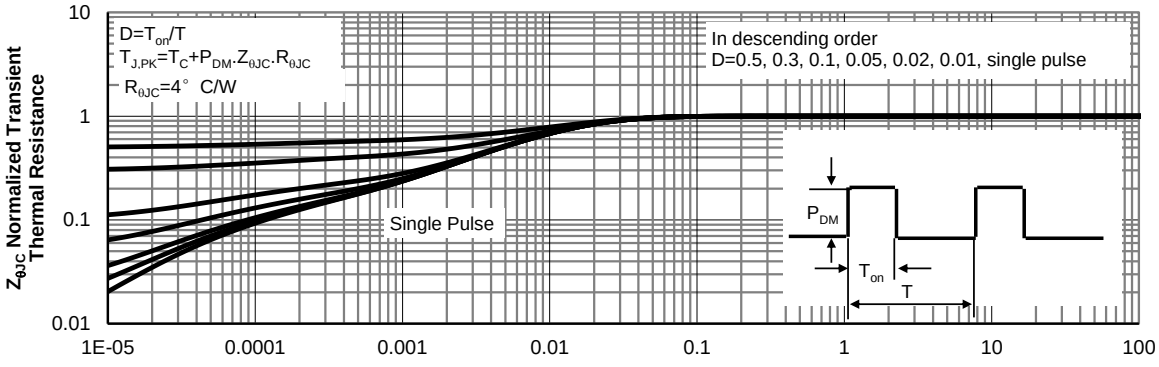


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

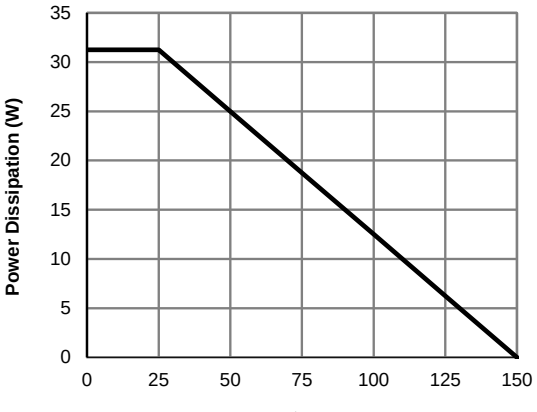


Figure 12: Power De-rating (Note F)

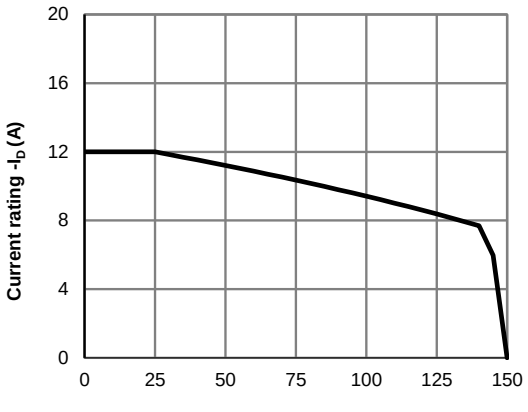


Figure 13: Current De-rating (Note F)

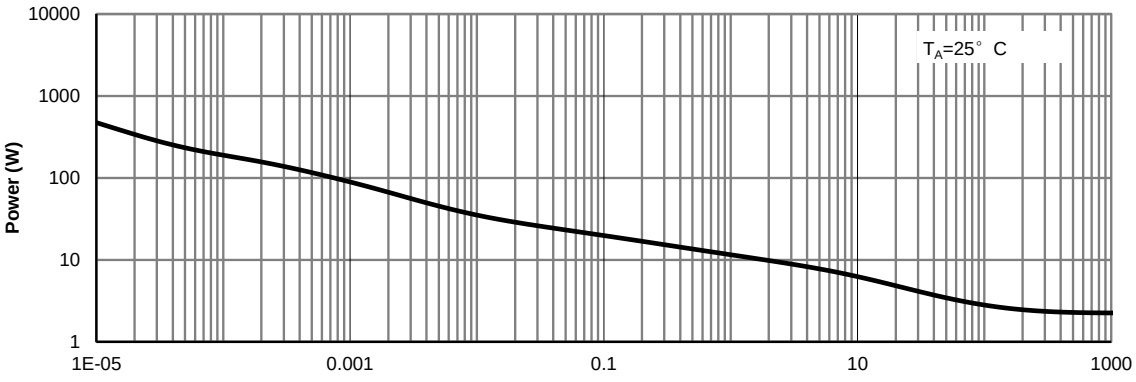


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

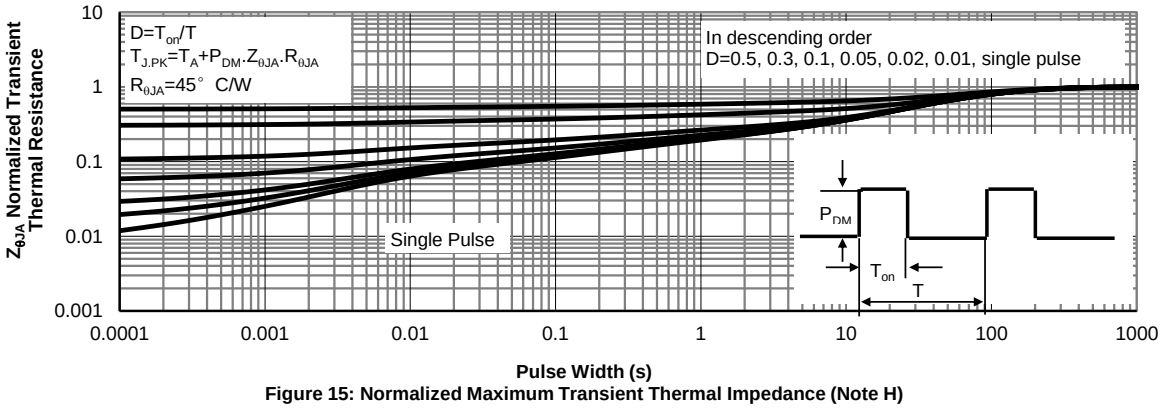


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

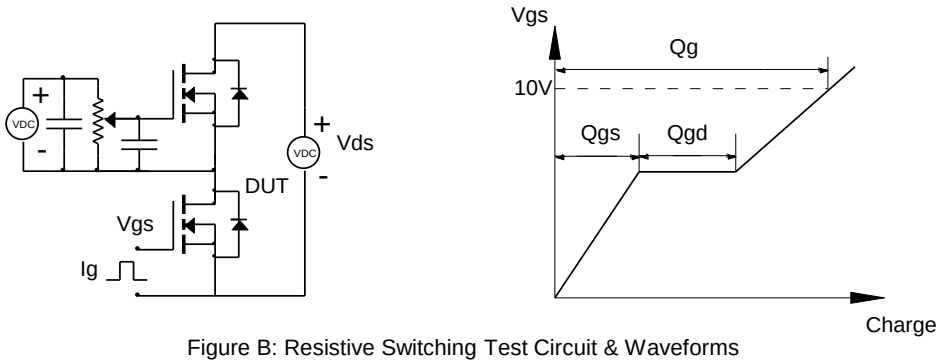


Figure B: Resistive Switching Test Circuit & Waveforms

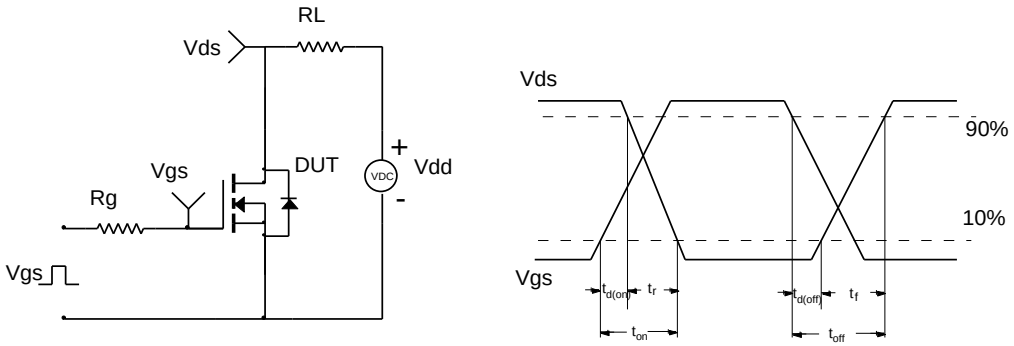


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

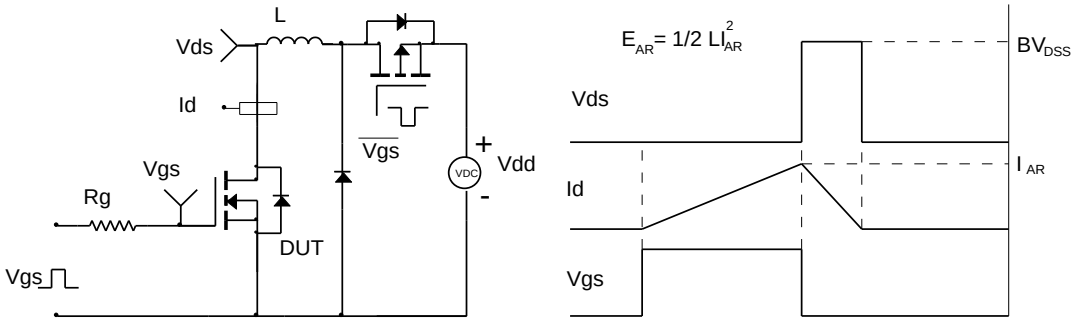
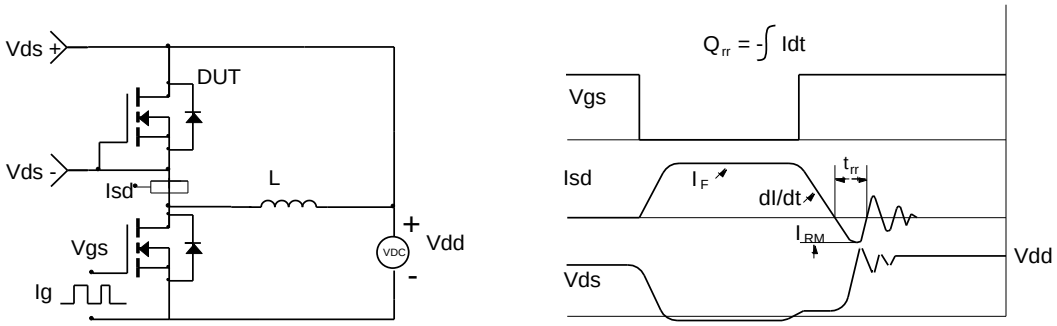
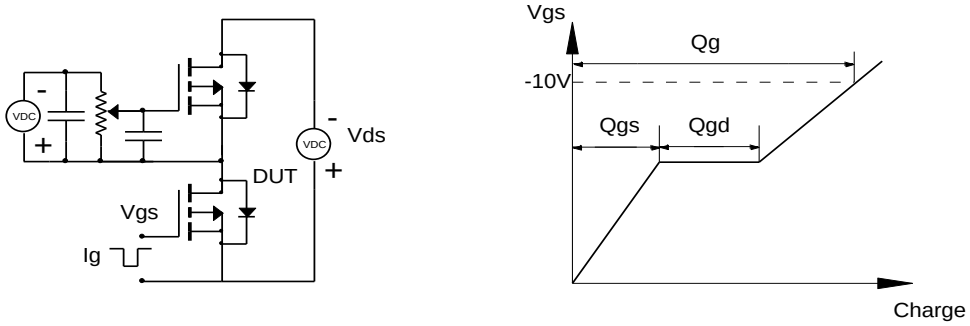


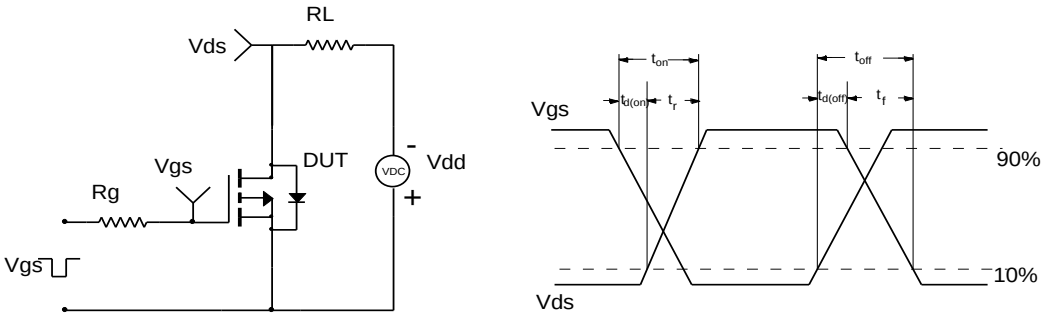
Figure D: Diode Recovery Test Circuit & Waveforms



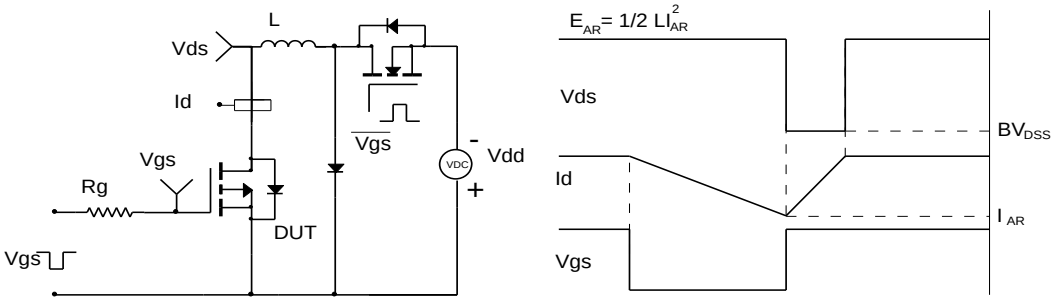
Gate Charge Test Circuit & Waveform



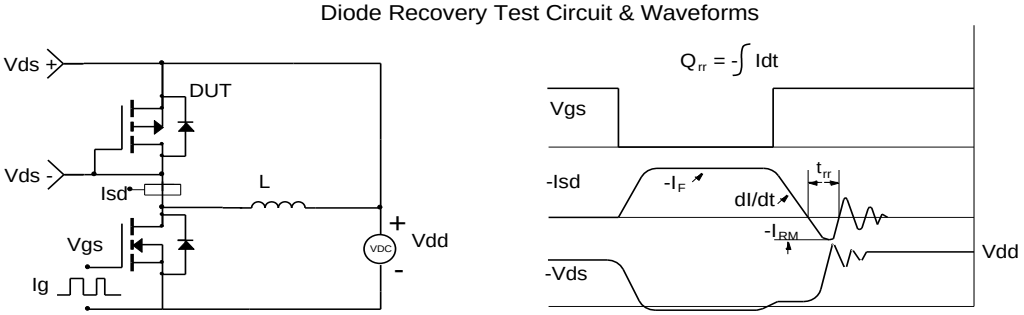
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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