



**THE DATASHEET OF
EFM32TG842F32-QFP64**



EFM32 Gecko Family

EFM32TG Data Sheet



The EFM32 Gecko MCUs are the world's most energy-friendly microcontrollers.

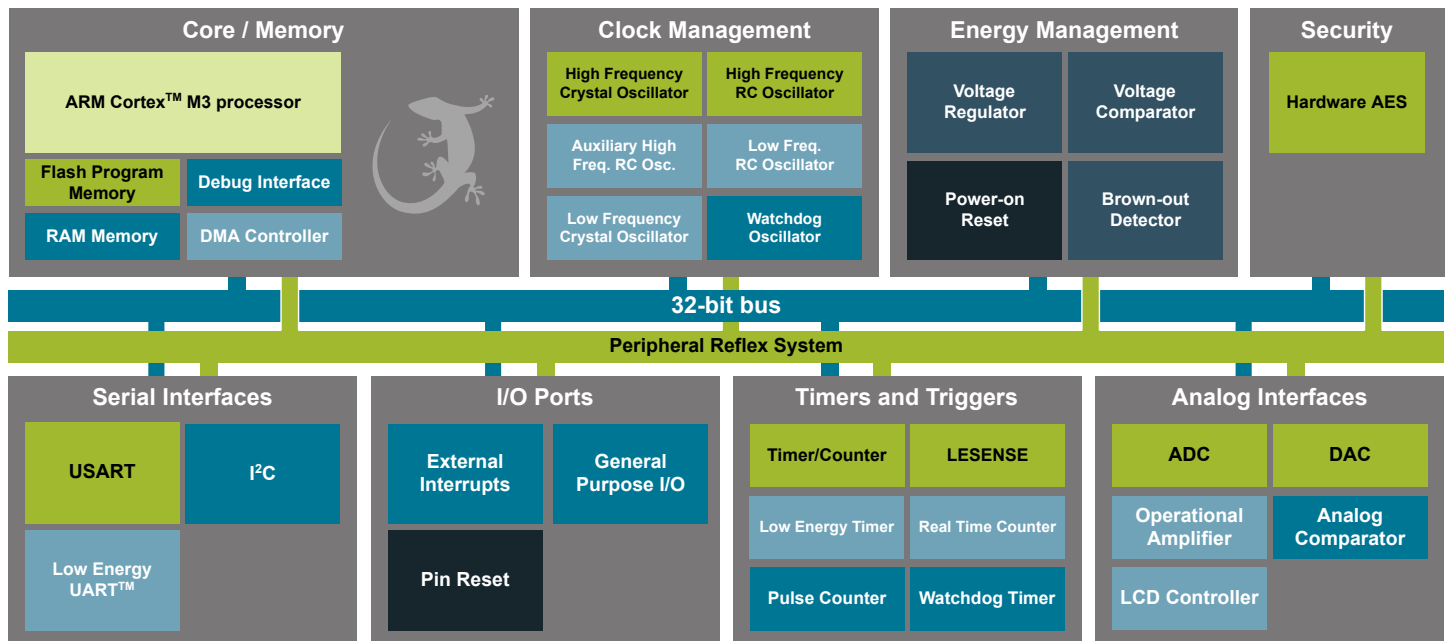
The EFM32TG offers unmatched performance and ultra low power consumption in both active and sleep modes. EFM32TG devices consume as little as 0.6 μA in Stop mode and 150 $\mu\text{A}/\text{MHz}$ in Run mode. It also features autonomous peripherals, high overall chip and analog integration, and the performance of the industry standard 32-bit ARM Cortex-M3 processor, making it perfect for battery-powered systems and systems with high-performance, low-energy requirements.

EFM32TG applications include the following:

- Smart metering
- Water metering
- Gas metering
- Industrial and home automation
- Alarm and security systems
- Health and fitness applications

KEY FEATURES

- ARM Cortex-M3 at 32 MHz
- Ultra low power operation
 - 0.6 μA current in Stop (EM3), with brown-out detection and RAM retention
 - 51 $\mu\text{A}/\text{MHz}$ in EM1
 - 150 $\mu\text{A}/\text{MHz}$ in Run mode (EM0)
- Fast wake-up time of 2 μs
- Hardware cryptography (AES)
- Up to 32 kB of Flash and 4 kB of RAM



Lowest power mode with peripheral operational:



1. Feature List

- ARM Cortex-M3 CPU platform
 - High Performance 32-bit processor @ up to 32 MHz
 - Wake-up Interrupt Controller
 - SysTick System Timer
- Flexible Energy Management System
 - 20 nA @ 3 V Shutoff Mode
 - 0.6 μ A @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
 - 1.0 μ A @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
 - 51 μ A/MHz @ 3 V Sleep Mode
 - 150 μ A/MHz @ 3 V Run Mode, with code executed from flash
- 32/16/8 KB Flash
- 4/2 KB RAM
- Up to 56 General Purpose I/O pins
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - 16 asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- 8 Channel DMA Controller
- 8 Channel Peripheral Reflex System (PRS) for autonomous inter- peripheral signaling
- Hardware AES with 128/256-bit keys in 54/75 cycles
- Timers/Counters
 - 2 \times 16-bit Timer/Counter
 - 2 \times 3 Compare/Capture/PWM channels
 - 16-bit Low Energy Timer
 - 1 \times 24-bit Real-Time Counter
 - 1 \times 16-bit Pulse Counter
 - Watchdog Timer with dedicated RC oscillator @ 50 nA
- Integrated LCD Controller for up to 8 \times 20 segments
 - Voltage boost, adjustable contrast and autonomous animation
- Communication interfaces
 - Up to 2 \times Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
 - Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - I²C Interface with SMBus support
 - Address recognition in Stop Mode
- Ultra low power precision analog peripherals
 - 12-bit 1 Msamples/s Analog to Digital Converter
 - 8 single ended channels/4 differential channels
 - On-chip temperature sensor
 - 12-bit 500 ksamples/s Digital to Analog Converter
 - Up to 2 \times Analog Comparator
 - Capacitive sensing with up to 8 inputs
 - 3 \times Operational Amplifier
 - 6.1 MHz GBW, Rail-to-rail, Programmable Gain
 - Supply Voltage Comparator
- Low Energy Sensor Interface (LESENSE)
 - Autonomous sensor monitoring in Deep Sleep Mode
 - Wide range of sensors supported, including LC sensors and capacitive buttons
- Ultra efficient Power-on Reset and Brown-Out Detector

- 2-pin Serial Wire Debug interface
 - 1-pin Serial Wire Viewer
- Pre-Programmed UART Bootloader
- Temperature range -40 to 85 °C
- Single power supply 1.98 to 3.8 V
- Packages:
 - BGA48
 - QFN24
 - QFN32
 - QFN64
 - TQFP48
 - TQFP64

2. Ordering Information

The following table shows the available EFM32TG devices.

Table 2.1. Ordering Information

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (°C) | Package |
|-----------------------|------------|----------|-----------------|--------------------|------------------|---------|
| EFM32TG108F4-D-QFN24 | 4 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32TG108F8-D-QFN24 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32TG108F16-D-QFN24 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32TG108F32-D-QFN24 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32TG110F4-D-QFN24 | 4 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32TG110F8-D-QFN24 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32TG110F16-D-QFN24 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32TG110F32-D-QFN24 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN24 |
| EFM32TG210F8-D-QFN32 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32TG210F16-D-QFN32 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32TG210F32-D-QFN32 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN32 |
| EFM32TG222F8-D-QFP48 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32TG222F16-D-QFP48 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32TG222F32-D-QFP48 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32TG225F8-D-BGA48 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | BGA48 |
| EFM32TG225F16-D-BGA48 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | BGA48 |
| EFM32TG225F32-D-BGA48 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | BGA48 |
| EFM32TG230F8-D-QFN64 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32TG230F16-D-QFN64 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32TG230F32-D-QFN64 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32TG232F8-D-QFP64 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32TG232F16-D-QFP64 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32TG232F32-D-QFP64 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32TG822F8-D-QFP48 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32TG822F16-D-QFP48 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32TG822F32-D-QFP48 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP48 |
| EFM32TG825F8-D-BGA48 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | BGA48 |
| EFM32TG825F16-D-BGA48 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | BGA48 |
| EFM32TG825F32-D-BGA48 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | BGA48 |
| EFM32TG840F8-D-QFN64 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32TG840F16-D-QFN64 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |
| EFM32TG840F32-D-QFN64 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | QFN64 |

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (°C) | Package |
|-----------------------|------------|----------|-----------------|--------------------|------------------|---------|
| EFM32TG842F8-D-QFP64 | 8 | 2 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32TG842F16-D-QFP64 | 16 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |
| EFM32TG842F32-D-QFP64 | 32 | 4 | 32 | 1.98 - 3.8 | -40 - 85 | TQFP64 |

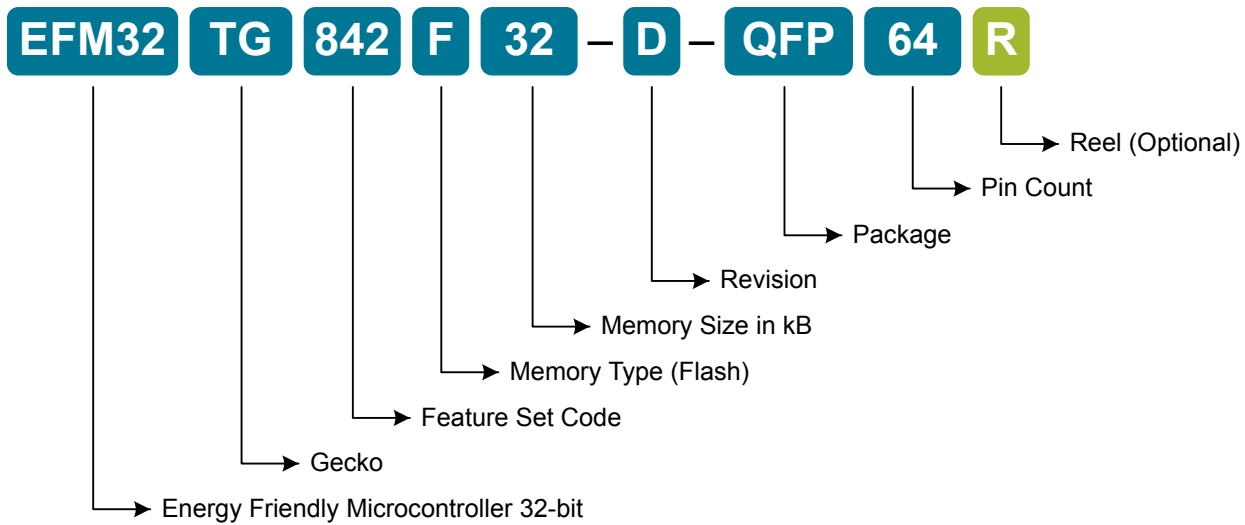


Figure 2.1. Ordering Code Decoder

Adding the suffix 'R' to the part number (e.g. EFM32TG842F32-D-QFP64R) denotes reel.

Visit <http://www.silabs.com> for information on global distributors and representatives.

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3. System Summary

3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32TG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32TG devices. For a complete feature set and in-depth information on the modules, refer to the [EFM32TG Reference Manual](#).

A block diagram of the EFM32TG is shown in the following figure.

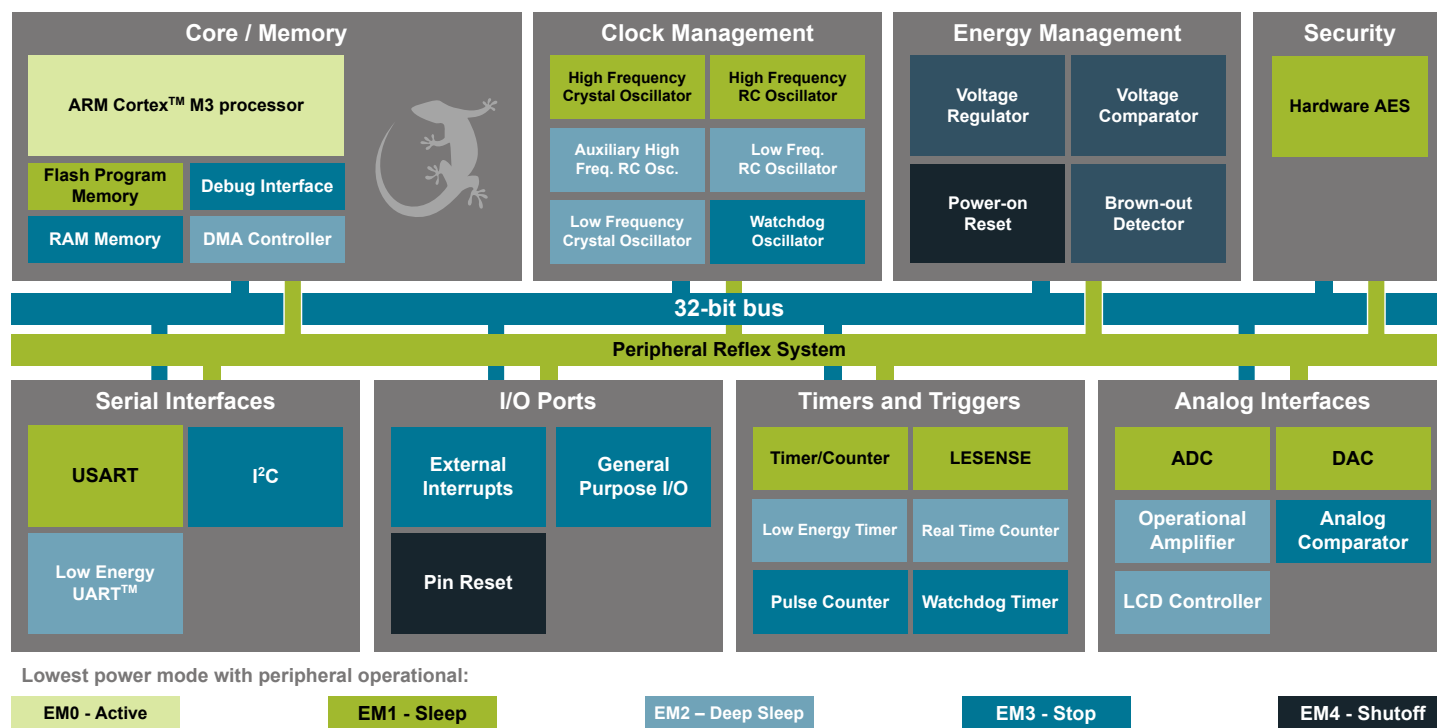


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32TG Reference Manual.

3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32TG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

3.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32TG.

3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32TG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32TG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

3.1.10 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 Smart-Cards, IrDA, and I2S devices.

3.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

3.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/ s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse- Width Modulation (PWM) output.

3.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.16 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

3.1.17 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACTK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.1.18 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.19 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

3.1.21 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single-ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

3.1.22 Operational Amplifier (OPAMP)

The EFM32TG features up to three Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single-ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

3.1.23 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE™), is a highly configurable sensor interface with support for up to 8 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.1.24 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

3.1.25 General Purpose Input/Output (GPIO)

In the EFM32TG, there are up to 56 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

3.1.26 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x20 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.2 Configuration Summary

3.2.1 EFM32TG108

The features of the EFM32TG108 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.1. EFM32TG108 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[1:0], ACMP1_O |
| VCMP | Full configuration | NA |
| GPIO | 17 pins | Available pins are shown in 5.1.3 GPIO Pinout Overview |

3.2.2 EFM32TG110

The features of the EFM32TG110 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.2. EFM32TG110 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[1:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:6] |
| DAC0 | Full configuration | DAC0_OUT[0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUT0, OPAMP_OUT0ALT, OPAMP_OUT1ALT, Inputs: OPAMP_P1, OPAMP_N1 |
| AES | Full configuration | NA |
| GPIO | 17 pins | Available pins are shown in 5.2.3 GPIO Pinout Overview |

3.2.3 EFM32TG210

The features of the EFM32TG210 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.3. EFM32TG210 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:5], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUT0, OPAMP_OUT0ALT, OPAMP_OUT1ALT, OPAMP_OUT2, Inputs: OPAMP_P1, OPAMP_N1, OPAMP_P2 |
| AES | Full configuration | NA |
| GPIO | 24 pins | Available pins are shown in 5.3.3 GPIO Pinout Overview |

3.2.4 EFM32TG222

The features of the EFM32TG222 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.4. EFM32TG222 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[1], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUT0, OPAMP_OUT0ALT, OPAMP_OUT1ALT, OPAMP_OUT2, Inputs: OPAMP_P0, OPAMP_P1, OPAMP_N1, OPAMP_P2 |
| AES | Full configuration | NA |
| GPIO | 37 pins | Available pins are shown in 5.4.3 GPIO Pinout Overview |

3.2.5 EFM32TG225

The features of the EFM32TG225 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.5. EFM32TG225 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[3:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUT0, OPAMP_OUT0ALT, OPAMP_OUT1ALT, OPAMP_OUT2, Inputs: OPAMP_P0, OPAMP_P1, OPAMP_N1, OPAMP_P2 |
| AES | Full configuration | NA |
| GPIO | 37 pins | Available pins are shown in 5.5.3 GPIO Pinout Overview |

3.2.6 EFM32TG230

The features of the EFM32TG230 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.6. EFM32TG230 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 56 pins | Available pins are shown in 5.6.3 GPIO Pinout Overview |

3.2.7 EFM32TG232

The features of the EFM32TG232 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.7. EFM32TG232 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 53 pins | Available pins are shown in 5.7.3 GPIO Pinout Overview |

3.2.8 EFM32TG822

The features of the EFM32TG822 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.8. EFM32TG822 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:5], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUT0, OPAMP_OUT1ALT, OPAMP_OUT2, Inputs: OPAMP_P0, OPAMP_P1, OPAMP_N1, OPAMP_P2 |
| AES | Full configuration | NA |
| GPIO | 37 pins | Available pins are shown in 5.8.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[10:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

3.2.9 EFM32TG825

The features of the EFM32TG825 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.9. EFM32TG825 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|--|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:5], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:4] |
| DAC0 | Full configuration | DAC0_OUT[0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUT0, OPAMP_OUT1ALT, OPAMP_OUT2, Inputs: OPAMP_P0, OPAMP_P1, OPAMP_N1, OPAMP_P2 |
| AES | Full configuration | NA |
| GPIO | 37 pins | Available pins are shown in 5.9.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[10:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

3.2.10 EFM32TG840

The features of the EFM32TG840 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.10. EFM32TG840 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:4], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUT0, OPAMP_OUT0ALT, OPAMP_OUT1ALT, OPAMP_OUT2, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 56 pins | Available pins are shown in 5.10.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[19:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

3.2.11 EFM32TG842

The features of the EFM32TG842 is a subset of the feature set described in the EFM32TG Reference Manual. The following table describes device specific implementation of the features.

Table 3.11. EFM32TG842 Configuration Summary

| Module | Configuration | Pin Connections |
|-----------|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:4], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:4], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUT0, OPAMP_OUT0ALT, OPAMP_OUT1ALT, OPAMP_OUT2, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 53 pins | Available pins are shown in 5.11.3 GPIO Pinout Overview |
| LCD | Full configuration | LCD_SEG[17:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT |

3.3 Memory Map

The EFM32TG memory map is shown in the following figure, with RAM and Flash sizes for the largest memory configuration.

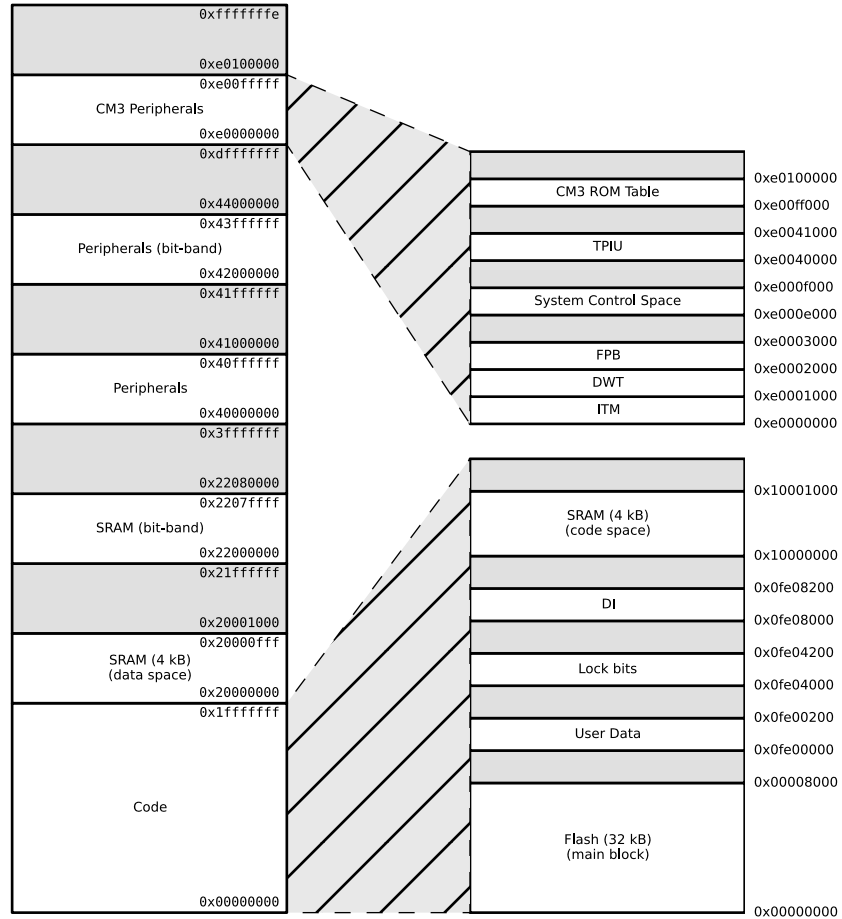


Figure 3.2. System Address Space with Core and Code Space Listing

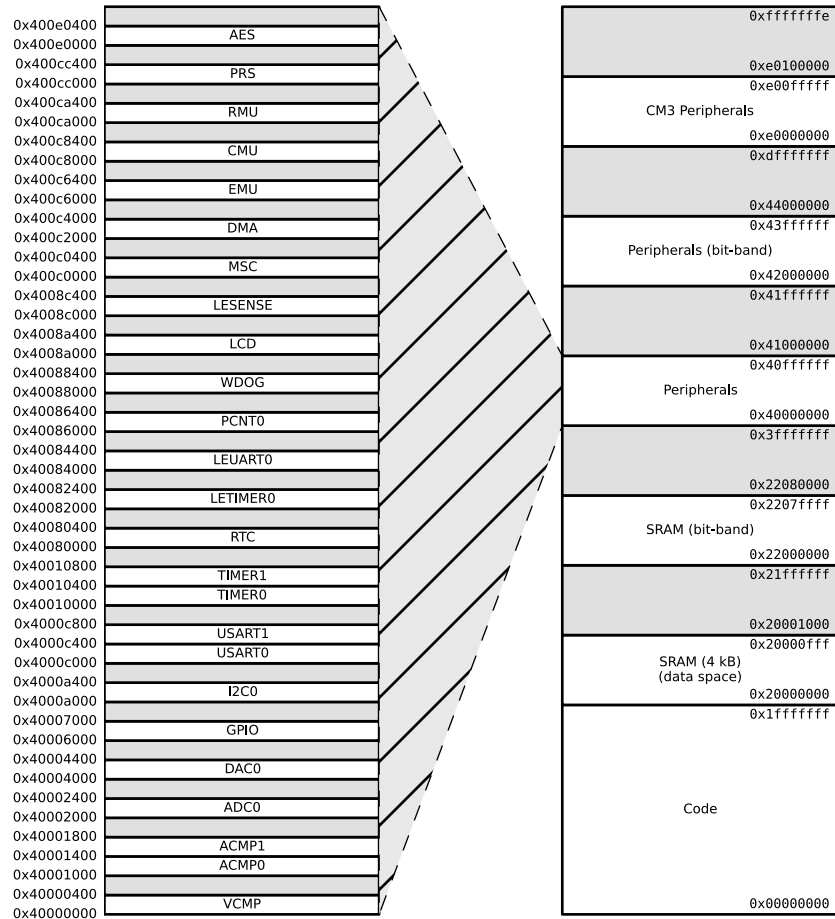


Figure 3.3. System Address Space with Peripheral Listing

4. Electrical Characteristics

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in 4.3 General Operating Conditions, unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in 4.3 General Operating Conditions, unless otherwise specified.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the following table may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in 4.3 General Operating Conditions.

Table 4.1. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|---------------------|-------------------------------------|------|-----|--------------|--------------------|
| Storage temperature range | T_{STG} | | -40 | — | 150 | $^{\circ}\text{C}$ |
| Maximum soldering temperature | T_S | Latest IPC/JEDEC J-STD-020 Standard | — | — | 260 | $^{\circ}\text{C}$ |
| External main supply voltage | V_{DDMAX} | | 0 | — | 3.8 | V |
| Voltage on any I/O pin | V_{IOPIN} | | -0.3 | — | $V_{DD}+0.3$ | V |
| Current per I/O pin (sink) | I_{IOMAX_SINK} | | — | — | 100 | mA |
| Current per I/O pin (source) | I_{IOMAX_SOURCE} | | — | — | -100 | mA |

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------|------------|------|-----|-----|--------------------|
| Ambient temperature range | T_{AMB} | -40 | — | 85 | $^{\circ}\text{C}$ |
| Operating supply voltage | V_{DDOP} | 1.98 | — | 3.8 | V |
| Internal APB clock frequency | f_{APB} | — | — | 32 | MHz |
| Internal AHB clock frequency | f_{AHB} | — | — | 32 | MHz |

4.4 Current Consumption

Table 4.3. Current Consumption

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------|---|-----|------|-------|--------------------------|
| EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz) | I_{EM0} | 32 MHz HFXO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 157 | — | $\mu\text{A}/\text{MHz}$ |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 150 | 170 | $\mu\text{A}/\text{MHz}$ |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 153 | 172 | $\mu\text{A}/\text{MHz}$ |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 155 | 175 | $\mu\text{A}/\text{MHz}$ |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 157 | 178 | $\mu\text{A}/\text{MHz}$ |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 162 | 183 | $\mu\text{A}/\text{MHz}$ |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 200 | 240 | $\mu\text{A}/\text{MHz}$ |
| EM1 current (Production test condition = 14 MHz) | I_{EM1} | 32 MHz HFXO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 53 | — | $\mu\text{A}/\text{MHz}$ |
| | | 28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 51 | 57 | $\mu\text{A}/\text{MHz}$ |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 55 | 59 | $\mu\text{A}/\text{MHz}$ |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 56 | 61 | $\mu\text{A}/\text{MHz}$ |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 58 | 63 | $\mu\text{A}/\text{MHz}$ |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 63 | 68 | $\mu\text{A}/\text{MHz}$ |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}= 3.0\text{ V}$ | — | 100 | 122 | $\mu\text{A}/\text{MHz}$ |
| EM2 current | I_{EM2} | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}= 3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$ | — | 1.0 | 1.2 | μA |
| | | EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, $V_{DD}= 3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$ | — | 2.4 | 5.0 | μA |
| EM3 current | I_{EM3} | $V_{DD}= 3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$ | — | 0.59 | 1.0 | μA |
| | | $V_{DD}= 3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$ | — | 2.0 | 4.5 | μA |
| EM4 current | I_{EM4} | $V_{DD}= 3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$ | — | 0.02 | 0.055 | μA |
| | | $V_{DD}= 3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$ | — | 0.25 | 0.70 | μA |

4.4.1 EM2 Current Consumption

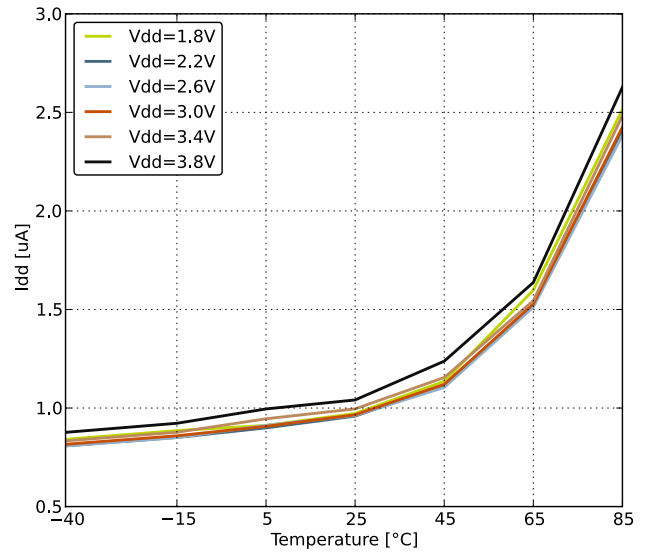
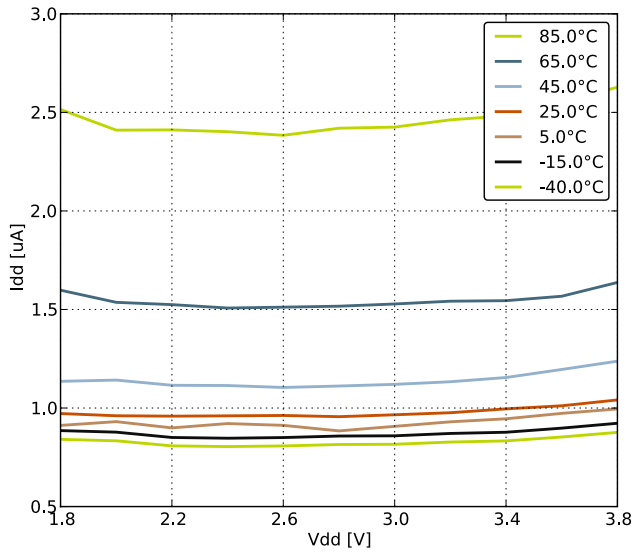


Figure 4.1. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO

4.4.2 EM3 Current Consumption

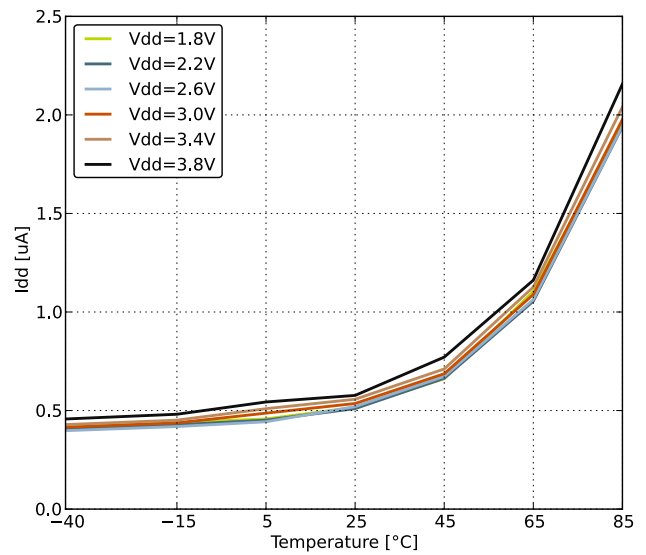
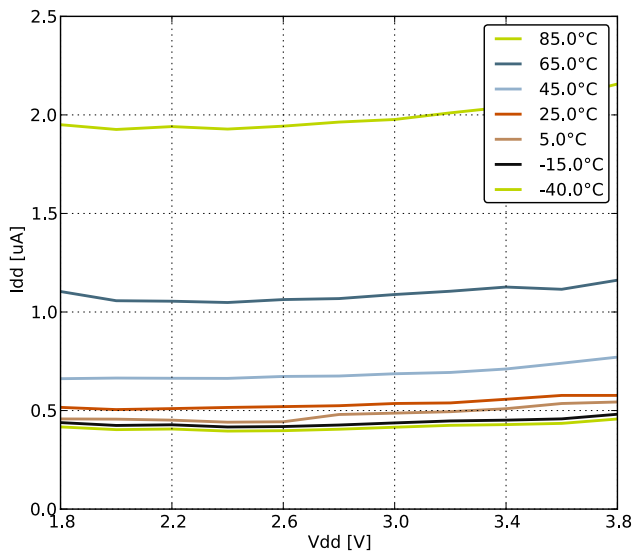


Figure 4.2. EM3 Current Consumption

4.4.3 EM4 Current Consumption

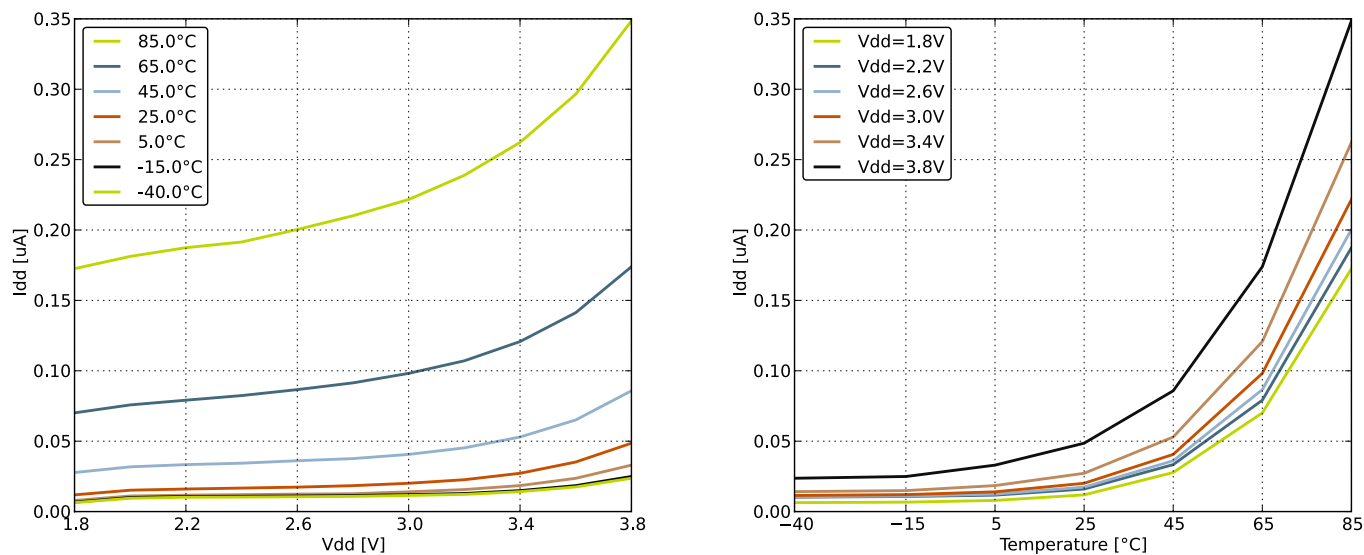


Figure 4.3. EM4 Current Consumption

4.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.4. Energy Modes Transitions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------|------------|-----|-----|-----|------------------|
| Transition time from EM1 to EM0 | t_{EM10} | — | 0 | — | HFCORECLK cycles |
| Transition time from EM2 to EM0 | t_{EM20} | — | 2 | — | μs |
| Transition time from EM3 to EM0 | t_{EM30} | — | 2 | — | μs |
| Transition time from EM4 to EM0 | t_{EM40} | — | 163 | — | μs |

4.6 Power Management

The EFM32TG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, *AN0002 EFM32 Hardware Design Considerations*.

Table 4.5. Power Management

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------------|--|------|------|------|------|
| BOD threshold on falling external supply voltage | V _{BODextthr-} | | 1.74 | — | 1.96 | V |
| BOD threshold on rising external supply voltage | V _{BODextthr+} | | — | 1.85 | 1.98 | V |
| Power-on Reset (POR) threshold on rising external supply voltage | V _{PORthr+} | | — | — | 1.98 | V |
| Delay from reset is released until program execution starts | t _{RESET} | Applies to Power-on Reset, Brown-out Reset and pin reset. | — | 163 | — | μs |
| Voltage regulator decoupling capacitor. | C _{DECOUPLE} | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | — | 1 | — | μF |

4.7 Flash

Table 4.6. Flash

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------|-------------------------|-------|------|----------------|--------|
| Flash erase cycles before failure | EC _{FLASH} | | 20000 | — | — | cycles |
| Flash word write cycles between erase | WWC _{FLASH} | | — | — | 2 ¹ | cycles |
| Flash data retention | RET _{FLASH} | T _{AMB} <150°C | 10000 | — | — | h |
| | | T _{AMB} <85°C | 10 | — | — | years |
| | | T _{AMB} <70°C | 20 | — | — | years |
| Word (32-bit) programming time | t _{W_PROG} | | 20 | — | — | μs |
| Page erase time | t _{P_ERASE} | | 20 | 20.4 | 20.8 | ms |
| Device erase time | t _{D_ERASE} | | 40 | 40.8 | 41.6 | ms |
| Erase current | I _{ERASE} | | — | — | 7 ² | mA |
| Write current | I _{WRITE} | | — | — | 7 ² | mA |
| Supply voltage during flash erase and write | V _{FLASH} | | 1.98 | — | 3.8 | V |

Note:

1. There is a maximum of two writes to the same word between each erase due to a physical limitation of the flash. No bit should be written to '0' more than once between erases. To write a word twice between erases, any bit written to '0' by the first write should be written to '1' by the second write. This preserves the specified flash write/erase endurance and does not change the '0' written by the first write.
2. Measured at 25°C

4.8 General Purpose Input Output

Table 4.7. GPIO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|--|----------------------|----------------------|----------------------|------|
| Input low voltage | V_{IOIL} | | — | — | $0.30 \times V_{DD}$ | V |
| Input high voltage | V_{IOIH} | | $0.70 \times V_{DD}$ | — | — | V |
| Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | V_{IOOH} | Sourcing 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW-EST | — | $0.80 \times V_{DD}$ | — | V |
| | | Sourcing 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW-EST | — | $0.90 \times V_{DD}$ | — | V |
| | | Sourcing 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW | — | $0.85 \times V_{DD}$ | — | V |
| | | Sourcing 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW | — | $0.90 \times V_{DD}$ | — | V |
| | | Sourcing 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.75 \times V_{DD}$ | — | — | V |
| | | Sourcing 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.85 \times V_{DD}$ | — | — | V |
| | | Sourcing 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.60 \times V_{DD}$ | — | — | V |
| | | Sourcing 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.80 \times V_{DD}$ | — | — | V |
| Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | V_{IOOL} | Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW-EST | — | $0.20 \times V_{DD}$ | — | V |
| | | Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW-EST | — | $0.10 \times V_{DD}$ | — | V |
| | | Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW | — | $0.10 \times V_{DD}$ | — | V |
| | | Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW | — | $0.05 \times V_{DD}$ | — | V |
| | | Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD | — | — | $0.30 \times V_{DD}$ | V |
| | | Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD | — | — | $0.20 \times V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH | — | — | $0.35 \times V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH | — | — | $0.20 \times V_{DD}$ | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------------|--|---------------------|-----------|-----------|------------|
| Input leakage current | I_{IOLEAK} | High Impedance IO connected to GROUND or V_{DD} | — | ± 0.1 | ± 100 | nA |
| I/O pin pull-up resistor | R_{PU} | | — | 40 | — | k Ω |
| I/O pin pull-down resistor | R_{PD} | | — | 40 | — | k Ω |
| Internal ESD series resistor | R_{IOESD} | | — | 200 | — | Ω |
| Pulse width of pulses to be removed by the glitch suppression filter | $t_{IO-GLITCH}$ | | 10 | — | 50 | ns |
| Output fall time | t_{IOOF} | GPIO_Px_CTRL DRIVEMODE = LOW-EST and load capacitance $C_L=12.5-25\text{pF}$. | $20+0.1 \times C_L$ | — | 250 | ns |
| | | GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance $C_L=350-600\text{pF}$ | $20+0.1 \times C_L$ | — | 250 | ns |
| I/O pin hysteresis ($V_{IOTHR+} - V_{IOTHR-}$) | V_{IOHYST} | $V_{DD} = 1.98 - 3.8 \text{ V}$ | $0.1 \times V_{DD}$ | — | — | V |

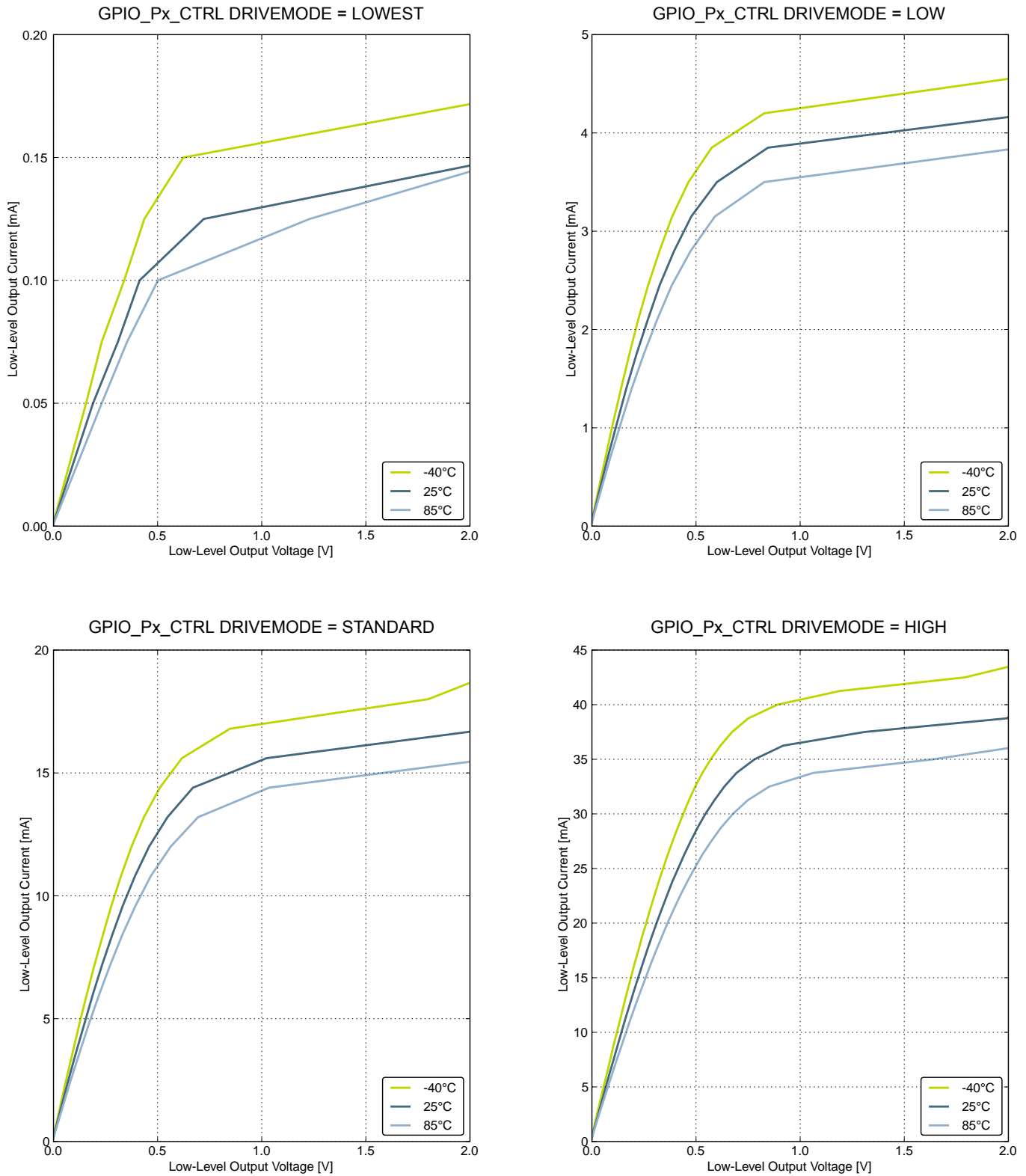


Figure 4.4. Typical Low-Level Output Current, 2V Supply Voltage

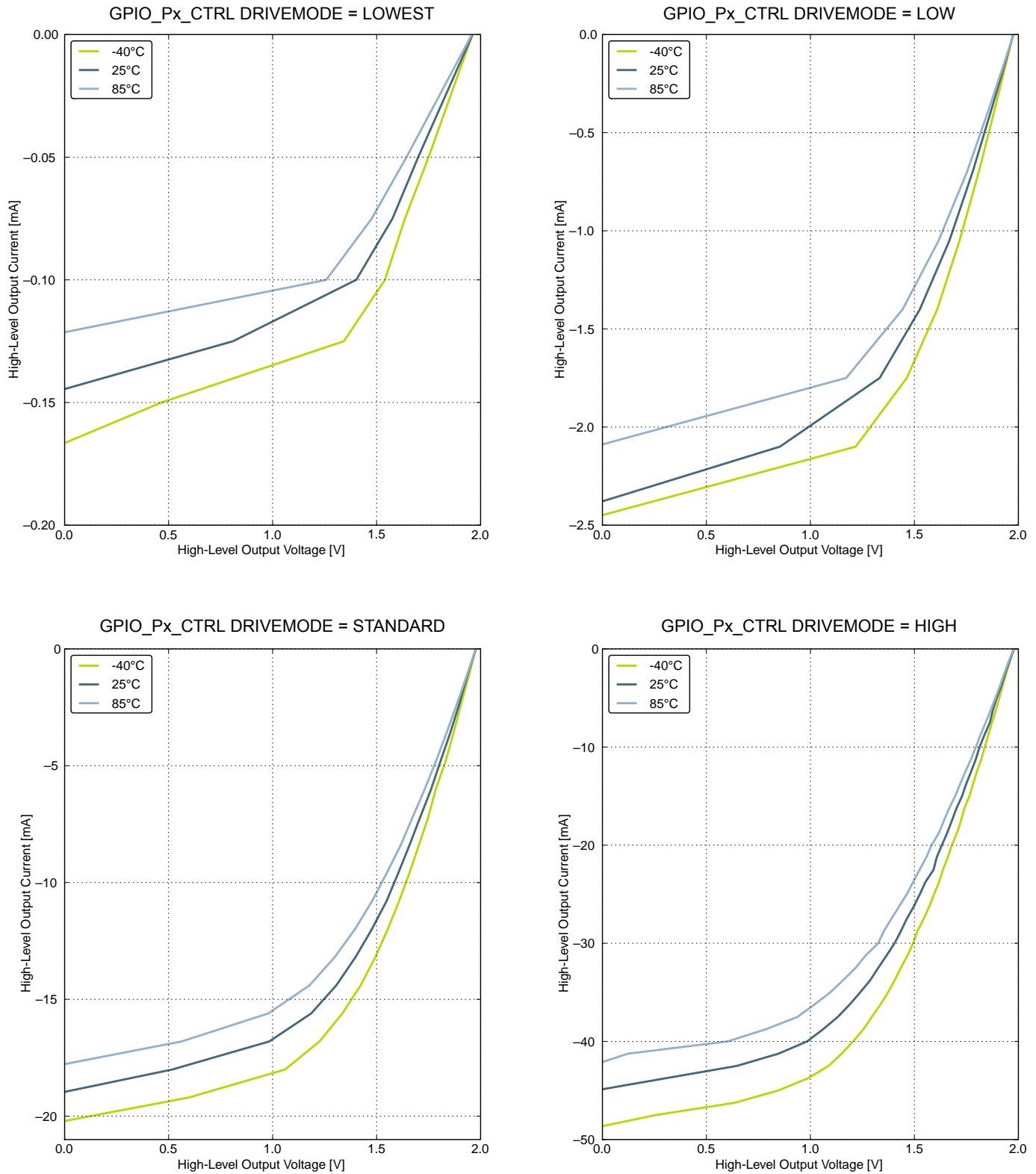


Figure 4.5. Typical High-Level Output Current, 2 V Supply Voltage

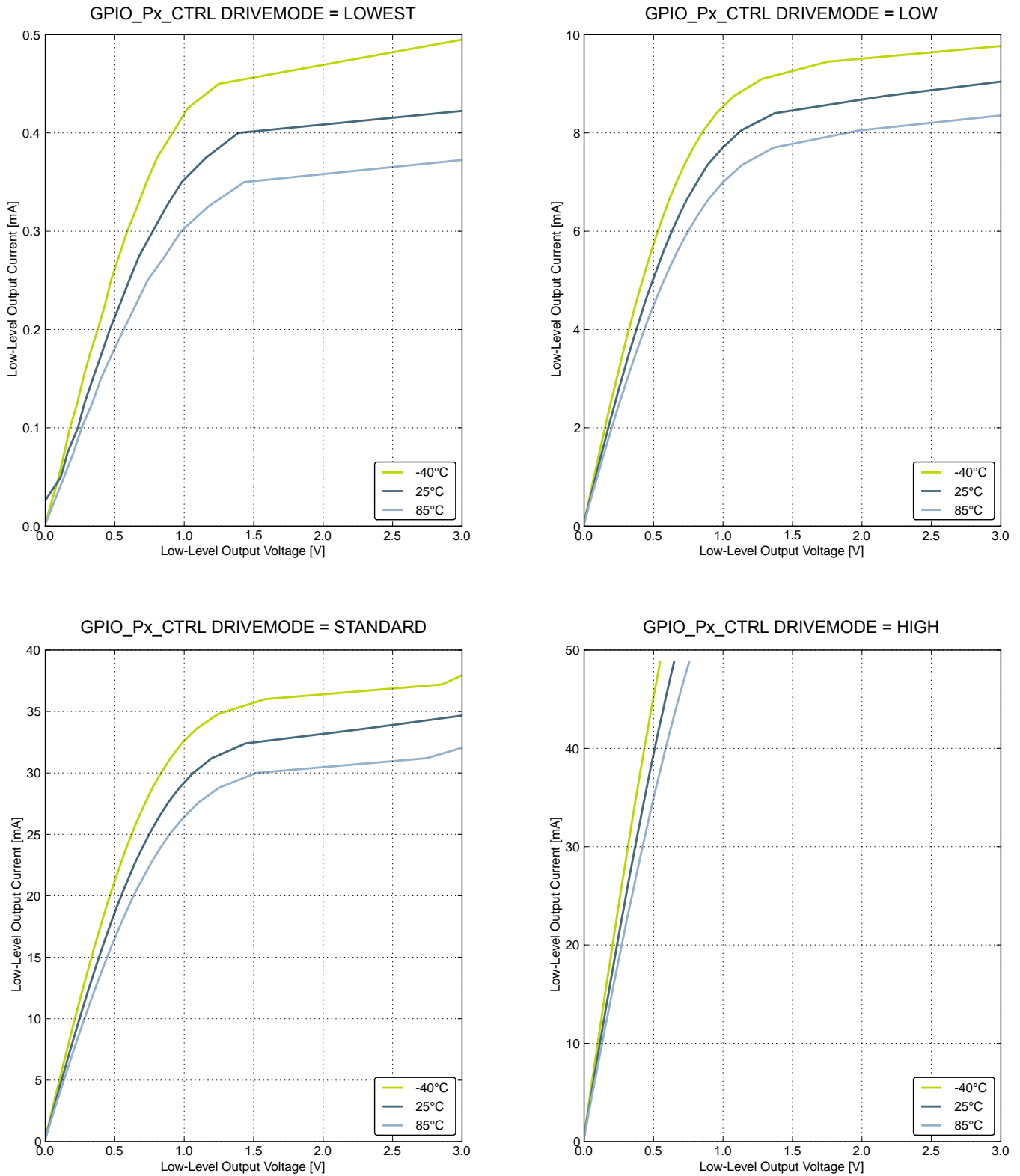


Figure 4.6. Typical Low-Level Output Current, 3 V Supply Voltage

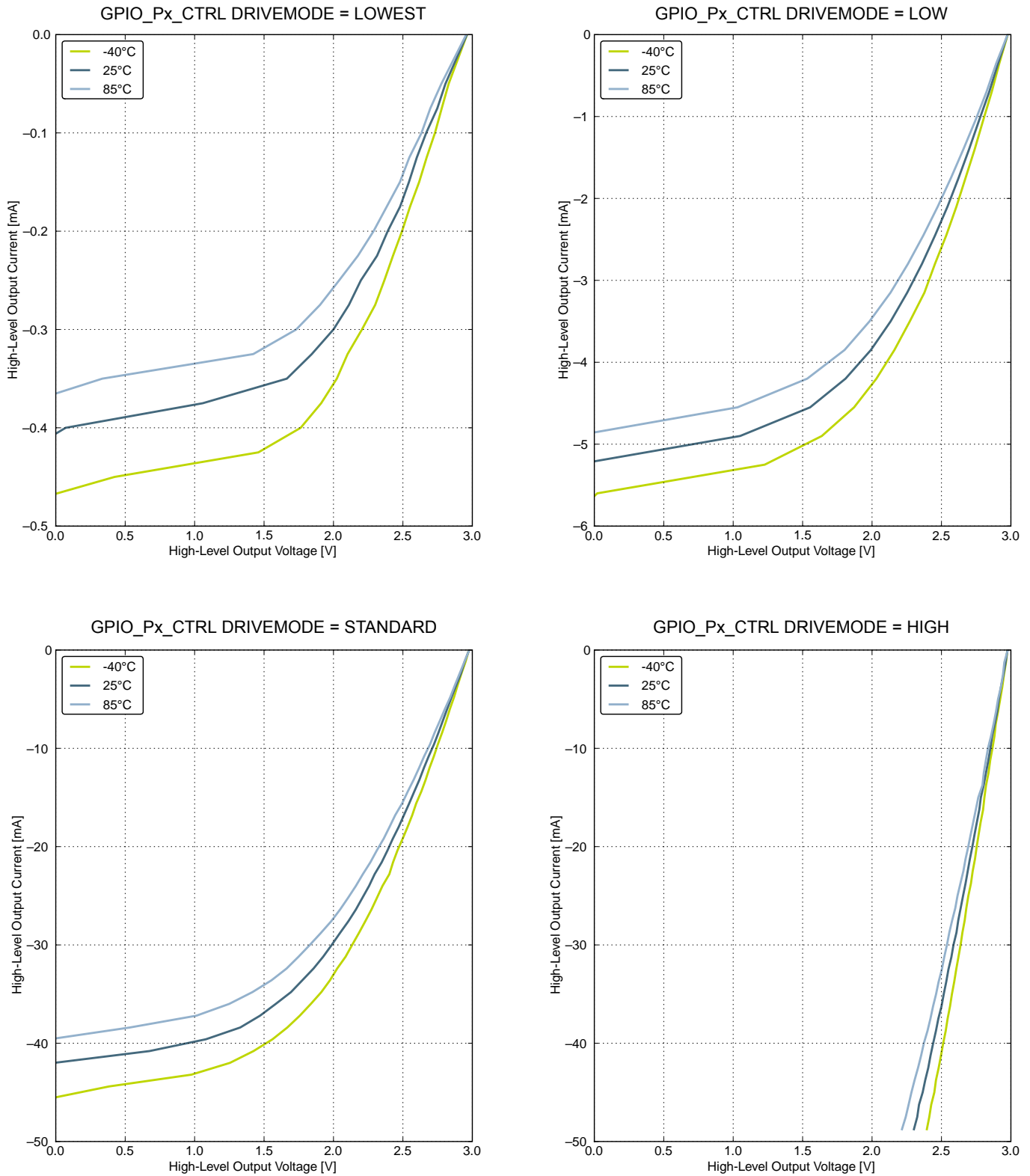


Figure 4.7. Typical High-Level Output Current, 3 V Supply Voltage

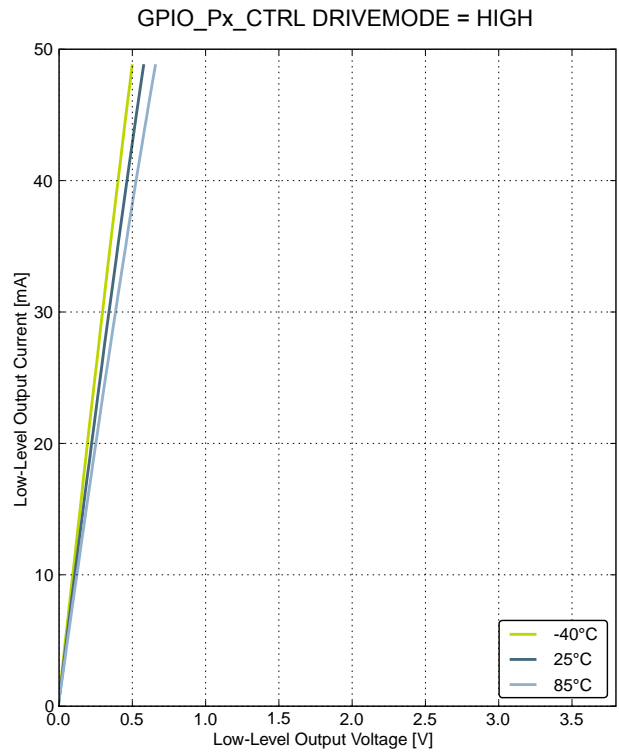
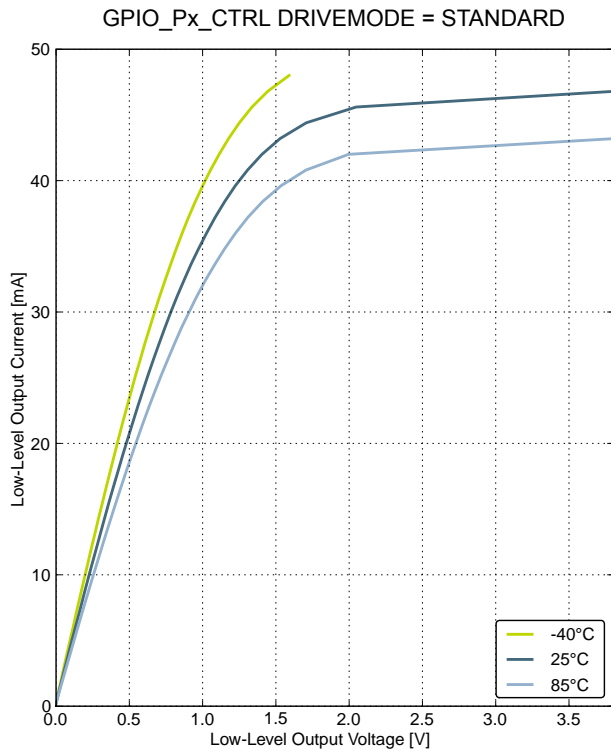
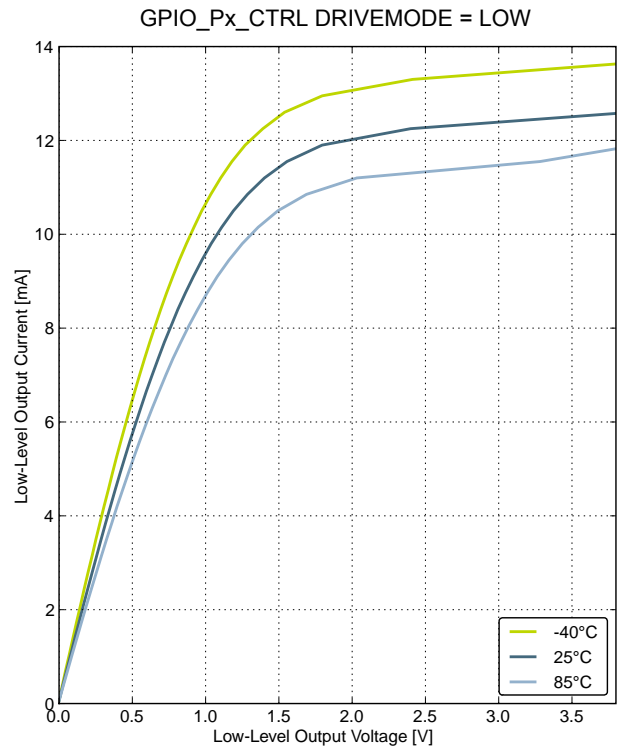
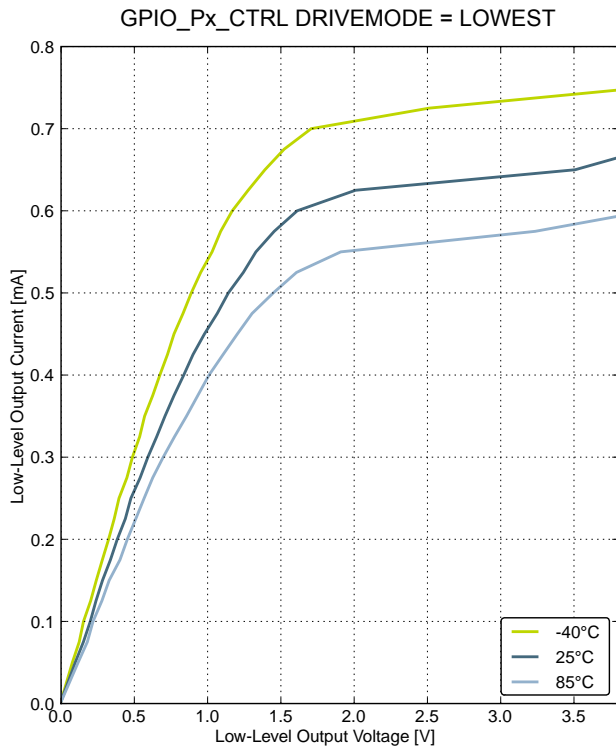


Figure 4.8. Typical Low-Level Output Current, 3.8 V Supply Voltage

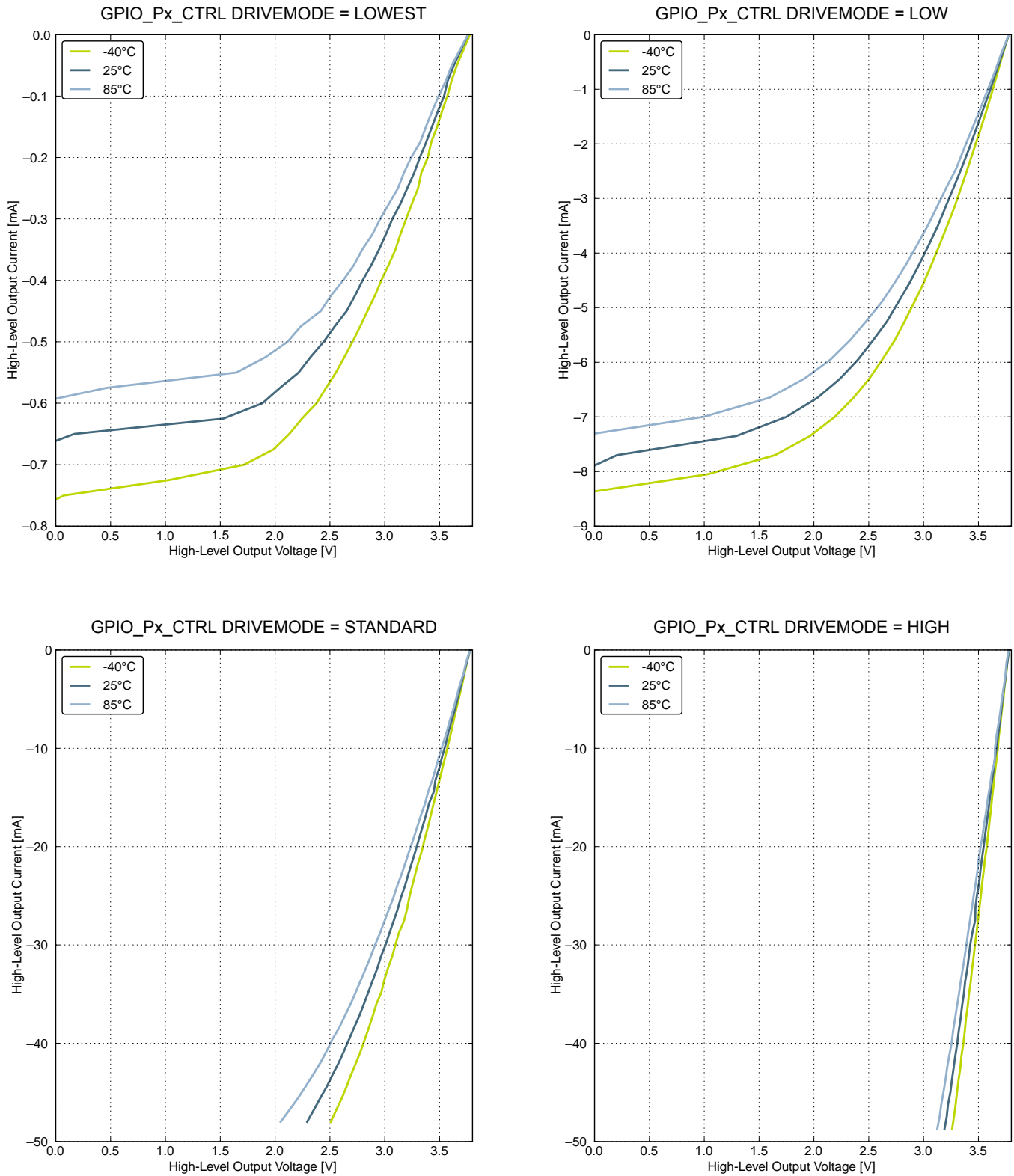


Figure 4.9. Typical High-Level Output Current, 3.8 V Supply Voltage

4.9 Oscillators

4.9.1 LFXO

Table 4.8. LFXO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------|---|----------------|--------|-----|------------|
| Supported nominal crystal frequency | f_{LFXO} | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{LFXO} | | — | 30 | 120 | k Ω |
| Supported crystal external load range | C_{LFXOL} | | X ¹ | — | 25 | pF |
| Current consumption for core and buffer after startup. | I_{LFXO} | ESR=30 kOhm, C_L =10 pF, LFXO-BOOST in CMU_CTRL is 1 | — | 190 | — | nA |
| Start- up time. | t_{LFXO} | ESR=30 kOhm, C_L =10 pF, 40% - 60% duty cycle has been reached, LFXO-BOOST in CMU_CTRL is 1 | — | 400 | — | ms |
| Note: | | | | | | |
| 1. See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in Configurator in Simplicity Studio. | | | | | | |

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note *AN0016 EFM32 Oscillator Design Consideration*.

4.9.2 HFXO

Table 4.9. HFXO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------|---|-----|-----|------|----------|
| Supported nominal crystal Frequency | f_{HFXO} | | 4 | — | 32 | MHz |
| Supported crystal equivalent series resistance (ESR) | ESR_{HFXO} | Crystal frequency 32 MHz | — | 30 | 60 | Ω |
| | | Crystal frequency 4 MHz | — | 400 | 1500 | Ω |
| The transconductance of the HFXO input transistor at crystal startup | g_{mHFXO} | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | — | — | mS |
| Supported crystal external load range | C_{HFXOL} | | 5 | — | 25 | pF |
| Current consumption for HFXO after startup | g_{mHFXO} | 4 MHz: ESR=400 Ohm, C_L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 85 | — | μ A |
| | | 32 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 165 | — | μ A |
| Startup time | t_{HFXO} | 32 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | — | 400 | — | μ s |

4.9.3 LFRCO

Table 4.10. LFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|----------------|-------|--------|-------|---------------|
| Oscillation frequency, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$ | f_{LFRCO} | | 31.29 | 32.768 | 34.24 | kHz |
| Startup time not including software calibration | t_{LFRCO} | | — | 150 | — | μs |
| Current consumption | I_{LFRCO} | | — | 210 | 380 | nA |
| Frequency step for LSB change in TUNING value | $TUNESTEP_{LFRCO}$ | | — | 1.5 | — | % |

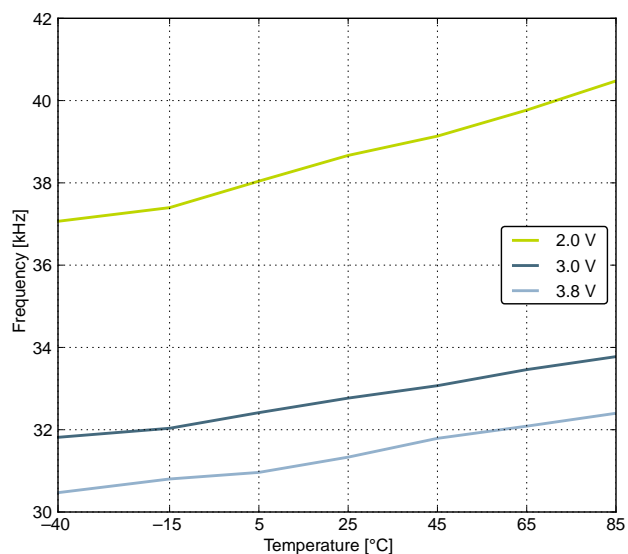
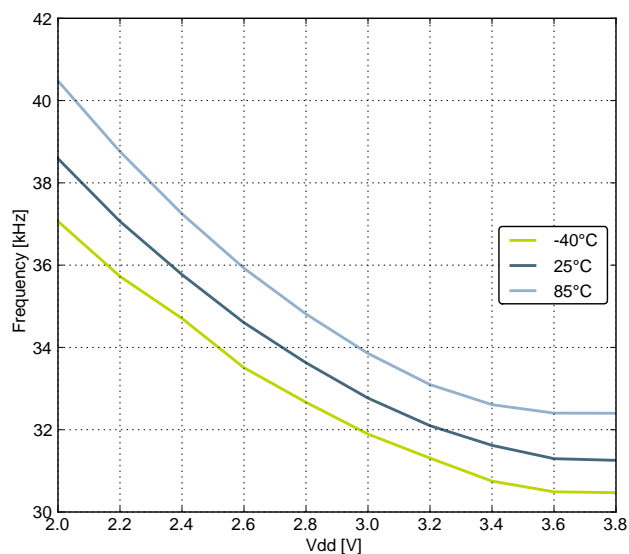


Figure 4.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

4.9.4 HFRCO

Table 4.11. HFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------------------------------|-------------------------------------|-------------------|-------------------|-------------------|---------------|
| Oscillation frequency, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$ | f_{HFRCO} | 28 MHz frequency band | 27.16 | 28.0 | 28.84 | MHz |
| | | 21 MHz frequency band | 20.37 | 21.0 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14.0 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11.0 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.40 ¹ | 6.60 ¹ | 6.80 ¹ | MHz |
| | | 1 MHz frequency band | 1.16 ² | 1.20 ² | 1.24 ² | MHz |
| Settling time after start-up | $t_{\text{HFRCO_settling}}$ | $f_{\text{HFRCO}} = 14\text{ MHz}$ | — | 0.6 | — | Cycles |
| Current consumption (Production test condition = 14 MHz) | I_{HFRCO} | $f_{\text{HFRCO}} = 28\text{ MHz}$ | — | 160 | 190 | μA |
| | | $f_{\text{HFRCO}} = 21\text{ MHz}$ | — | 125 | 155 | μA |
| | | $f_{\text{HFRCO}} = 14\text{ MHz}$ | — | 104 | 120 | μA |
| | | $f_{\text{HFRCO}} = 11\text{ MHz}$ | — | 94 | 110 | μA |
| | | $f_{\text{HFRCO}} = 6.6\text{ MHz}$ | — | 63 | 90 | μA |
| | | $f_{\text{HFRCO}} = 1.2\text{ MHz}$ | — | 22 | 32 | μA |
| Frequency step for LSB change in TUNING value | $\text{TUNESTEP}_{\text{HFRCO}}$ | | — | 0.3 ³ | — | % |

Note:

1. For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.
2. For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.
3. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

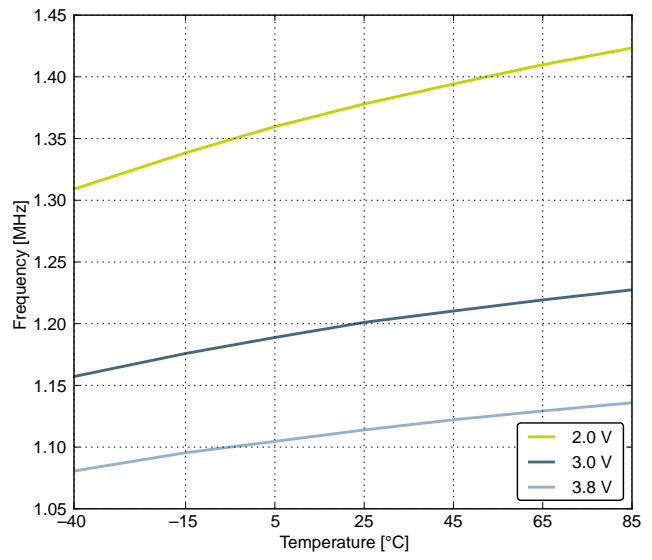
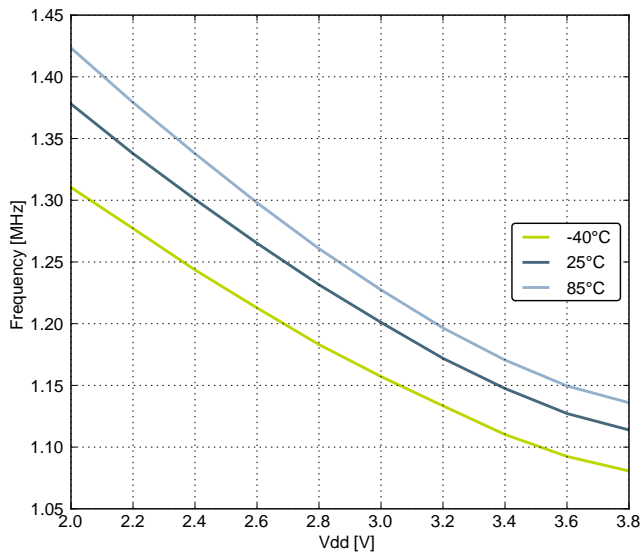


Figure 4.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

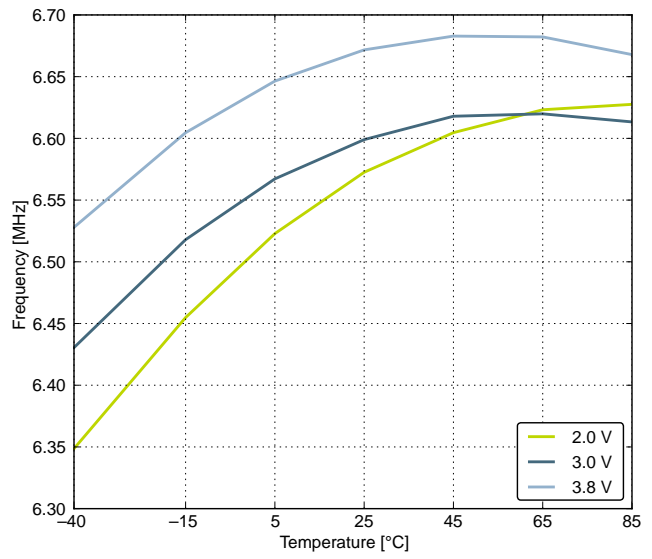
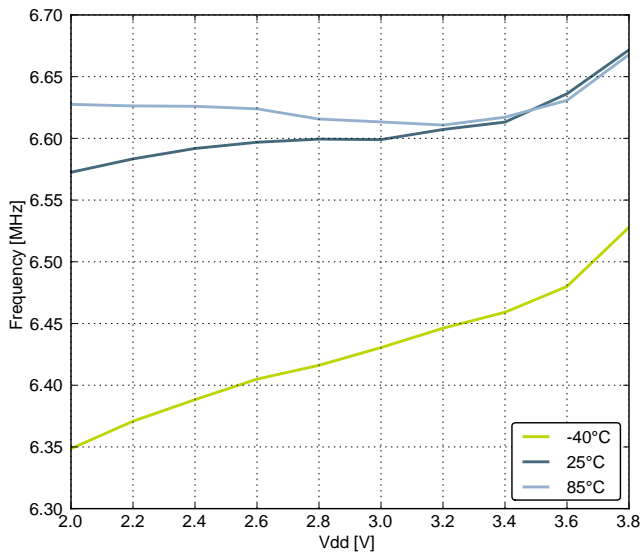


Figure 4.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

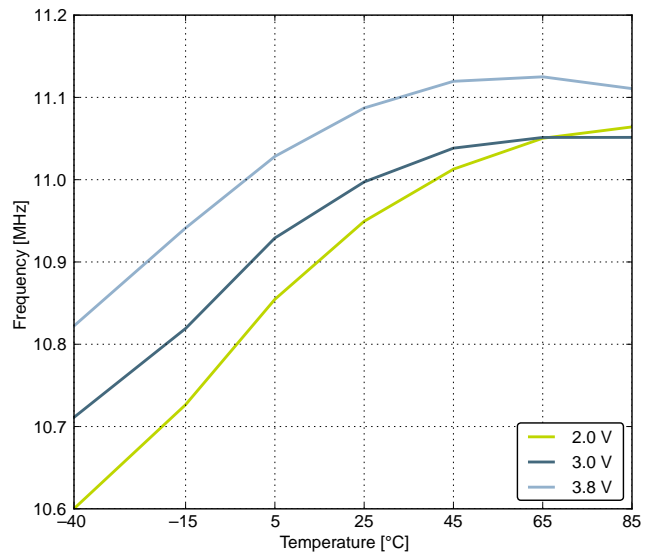
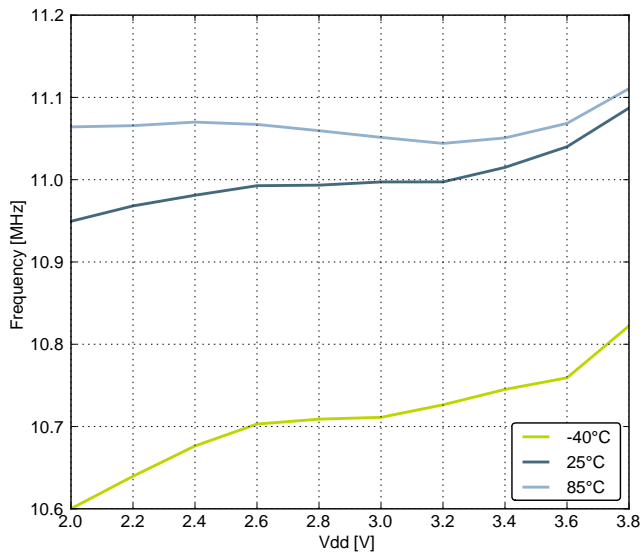


Figure 4.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

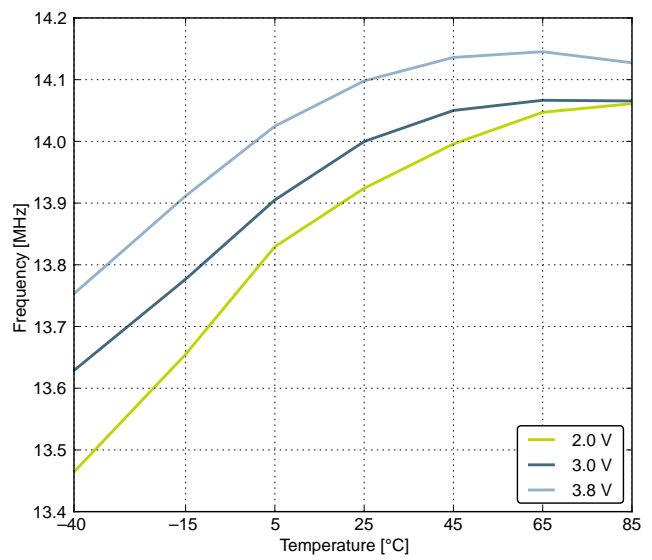
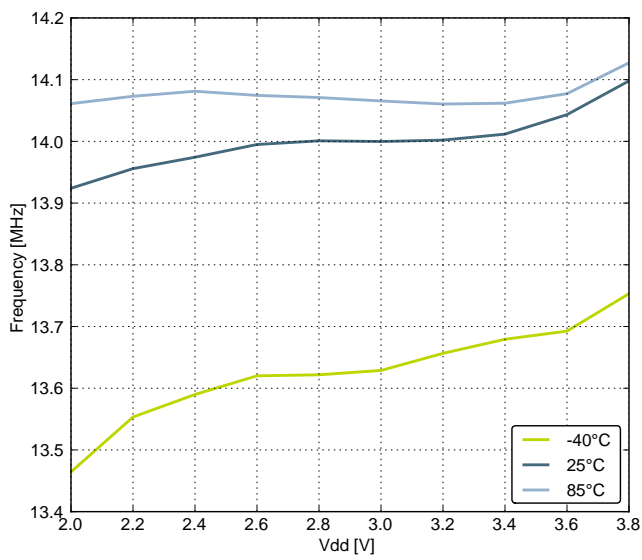


Figure 4.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

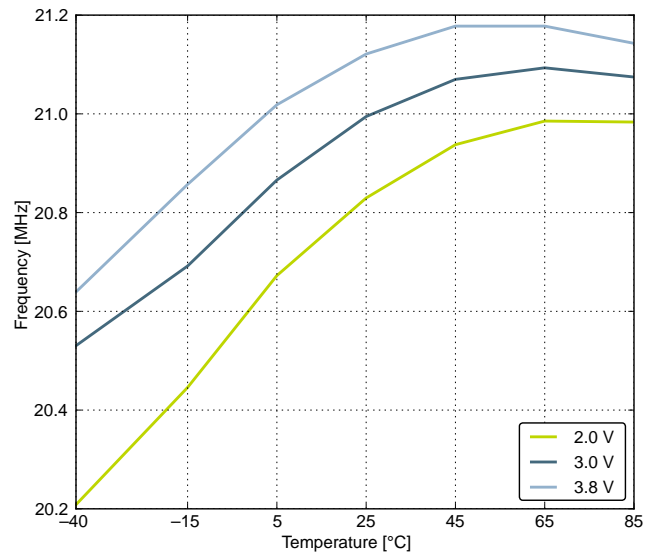
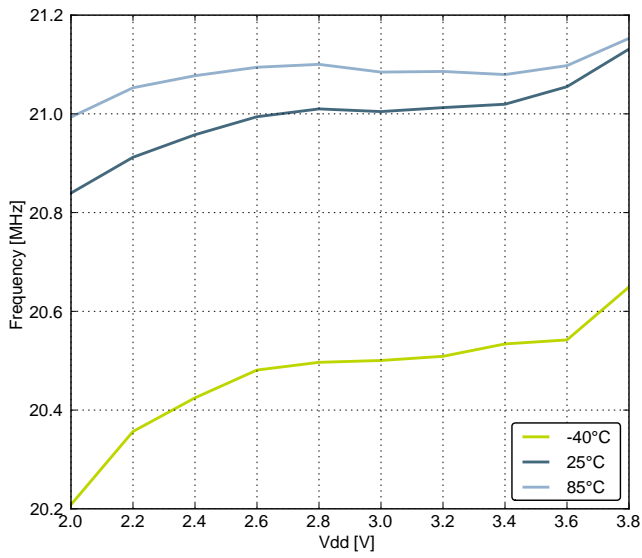


Figure 4.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

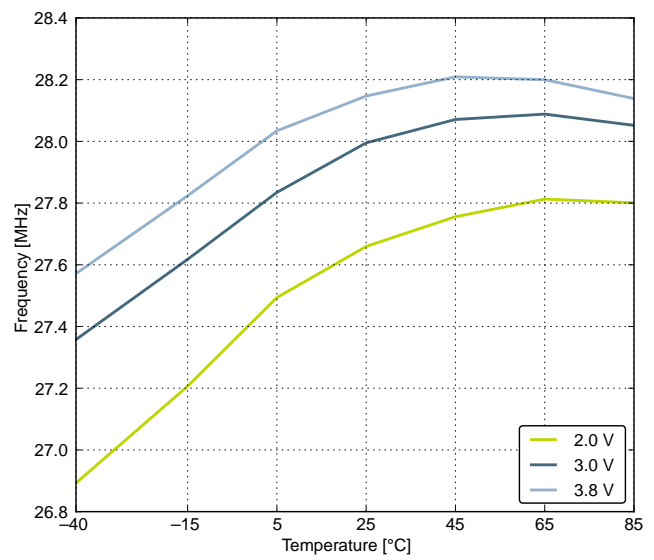
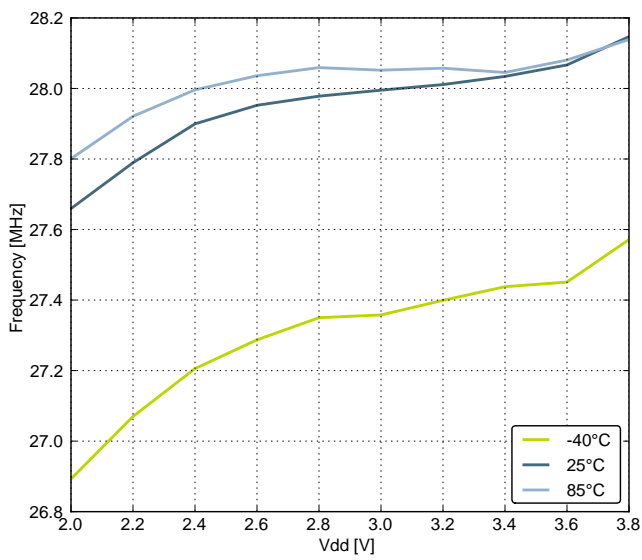


Figure 4.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature

4.9.5 AUXHFRCO

Table 4.12. AUXHFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------------|---------------------------------------|-------------------|-------------------|-------------------|--------|
| Oscillation frequency, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$ | f_{AUXHFRCO} | 28 MHz frequency band | 27.16 | 28.0 | 28.84 | MHz |
| | | 21 MHz frequency band | 20.37 | 21.0 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14.0 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11.0 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.40 ¹ | 6.60 ¹ | 6.80 ¹ | MHz |
| | | 1 MHz frequency band | 1.16 ² | 1.20 ² | 1.24 ² | MHz |
| Settling time after start-up | $t_{\text{AUXHFRCO_settling}}$ | $f_{\text{AUXHFRCO}} = 14\text{ MHz}$ | — | 0.6 | — | Cycles |
| Frequency step for LSB change in TUNING value | TUNE-STEP _{AUXHFRCO} | | — | 0.3 ³ | — | % |

Note:

- For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable
- For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.
- The TUNING field in the CMU_AUXHFRCCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

4.9.6 ULFRCO

Table 4.13. ULFRCO

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------|----------------------|----------------|-----|-------|------|------|
| Oscillation frequency | f_{ULFRCO} | 25°C, 3V | 0.7 | — | 1.75 | kHz |
| Temperature coefficient | TC_{ULFRCO} | | — | 0.05 | — | %/°C |
| Supply voltage coefficient | VC_{ULFRCO} | | — | -18.2 | — | %/V |

4.10 Analog Digital Converter (ADC)

Table 4.14. ADC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|---------------------|---|--------------|------|--------------|------------|
| Input voltage range | V_{ADCIN} | Single ended | 0 | — | V_{REF} | V |
| | | Differential | $-V_{REF}/2$ | — | $V_{REF}/2$ | V |
| Input range of external reference voltage, single ended and differential | $V_{ADCREFIN}$ | | 1.25 | — | V_{DD} | V |
| Input range of external negative reference voltage on channel 7 | $V_{ADCREFIN_CH7}$ | See $V_{ADCREFIN}$ | 0 | — | $V_{DD}-1.1$ | V |
| Input range of external positive reference voltage on channel 6 | $V_{ADCREFIN_CH6}$ | See $V_{ADCREFIN}$ | 0.625 | — | V_{DD} | V |
| Common mode input range | $V_{ADCCMIN}$ | | 0 | — | V_{DD} | V |
| Input current | I_{ADCIN} | 2pF sampling capacitors | — | <100 | — | nA |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | | — | 65 | — | dB |
| Average active current | I_{ADC} | 1 MSamples/s, 12 bit, external reference | — | 377 | — | μ A |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00 | — | 67 | — | μ A |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01 | — | 68 | — | μ A |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10 | — | 71 | — | μ A |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11 | — | 244 | — | μ A |
| Current consumption of internal voltage reference | I_{ADCREF} | Internal voltage reference | — | 65 | — | μ A |
| Input capacitance | C_{ADCIN} | | — | 2 | — | pF |
| Input ON resistance | R_{ADCIN} | | 300 | — | 800 | Ω |
| Input RC filter resistance | $R_{ADCFILT}$ | | — | 10 | — | k Ω |
| Input RC filter/decoupling capacitance | $C_{ADCFILT}$ | | — | 250 | — | fF |
| ADC Clock Frequency | f_{ADCCLK} | | — | — | 13 | MHz |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---------------------------|---|-----|-----|-----|---------------|
| Conversion time | $t_{ADCCONV}$ | 6 bit | 7 | — | — | ADCCLK Cycles |
| | | 8 bit | 11 | — | — | ADCCLK Cycles |
| | | 12 bit | 13 | — | — | ADCCLK Cycles |
| Acquisition time | t_{ADCACQ} | Programmable | 1 | — | 256 | ADCCLK Cycles |
| Required acquisition time for VDD/3 reference | $t_{ADCACQVDD3}$ | | 2 | — | — | μs |
| Startup time of reference generator and ADC core in NORMAL mode Startup time of reference generator and ADC core in KEEPADCWARM mode | $t_{ADCSTART}$ | | — | 5 | — | μs |
| | | | — | 1 | — | μs |
| Signal to Noise Ratio (SNR) | SNR_{ADC} | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | — | 59 | — | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | — | 63 | — | dB |
| | | 1 MSamples/s, 12 bit, single ended, V_{DD} reference | — | 65 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | — | 60 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | — | 65 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | — | 54 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, V_{DD} reference | — | 67 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{\text{DD}}$ reference | — | 69 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 62 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, V_{DD} reference | 63 | 67 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, V_{DD} reference | — | 69 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, $2xV_{\text{DD}}$ reference | — | 70 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------------|---|-----|-----|-----|------|
| Signal-to-Noise And Distortion-ratio (SINAD) | SINAD _{ADC} | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | — | 58 | — | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | — | 62 | — | dB |
| | | 1 MSamples/s, 12 bit, single ended, V _{DD} reference | — | 64 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | — | 60 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | — | 64 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | — | 54 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, V _{DD} reference | — | 66 | — | dB |
| | | 1 MSamples/s, 12 bit, differential, 2xV _{DD} reference | — | 68 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 61 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 65 | — | dB |
| | | 200 kSamples/s, 12 bit, single ended, V _{DD} reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 63 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | — | 66 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, V _{DD} reference | 62 | 68 | — | dB |
| | | 200 kSamples/s, 12 bit, differential, 2xV _{DD} reference | — | 69 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------------|---|---------------------|-------------------|--------------------|--------------|
| Spurious-Free Dynamic Range (SFDR) | SFDR _{ADC} | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | — | 64 | — | dBc |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, single ended, V _{DD} reference | — | 73 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | — | 66 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | — | 77 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, V _{DD} reference | — | 76 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, 2xV _{DD} reference | — | 75 | — | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | — | 69 | — | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 75 | — | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 75 | — | dBc |
| | | 200 kSamples/s, 12 bit, single ended, V _{DD} reference | 68 | 76 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | — | 78 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, V _{DD} reference | — | 79 | — | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2xV _{DD} reference | — | 79 | — | dBc |
| Offset voltage | V _{ADCOFFSET} | After calibration, single ended | -4 | 0.3 | 4 | mV |
| | | After calibration, differential | — | 0.3 | — | mV |
| Thermometer output gradient | TGRAD _{ADCTH} | | — | -1.92 | — | mV/°C |
| | | | — | -6.3 | — | ADC Codes/°C |
| Differential non-linearity (DNL) | DNL _{ADC} | V _{DD} = 3.0 V, external 2.5V reference | -1 | ±0.7 | 4 | LSB |
| Integral non-linearity (INL), End point method | INL _{ADC} | V _{DD} = 3.0 V, external 2.5V reference | — | ±1.2 | ±3 | LSB |
| No missing codes | MC _{ADC} | | 11.999 ¹ | 12 | — | bits |
| Gain error drift | GAIN _{ED} | 1.25V reference | — | 0.01 ² | 0.033 ³ | %/°C |
| | | 2.5V reference | — | 0.01 ² | 0.03 ³ | %/°C |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------|----------------------|-----------------|-----|------------------|-------------------|--------|
| Offset error drift | OFFSET _{ED} | 1.25V reference | — | 0.2 ² | 0.7 ³ | LSB/°C |
| | | 2.5V reference | — | 0.2 ² | 0.62 ³ | LSB/°C |

Note:

1. On the average every ADC will have one missing code, most likely to appear around $2048 \pm n \cdot 512$ where n can be a value in the set $\{-3, -2, -1, 1, 2, 3\}$. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.
2. Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.
3. Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

The integral non-linearity (INL) and differential non-linearity parameters are explained in the following two figures.

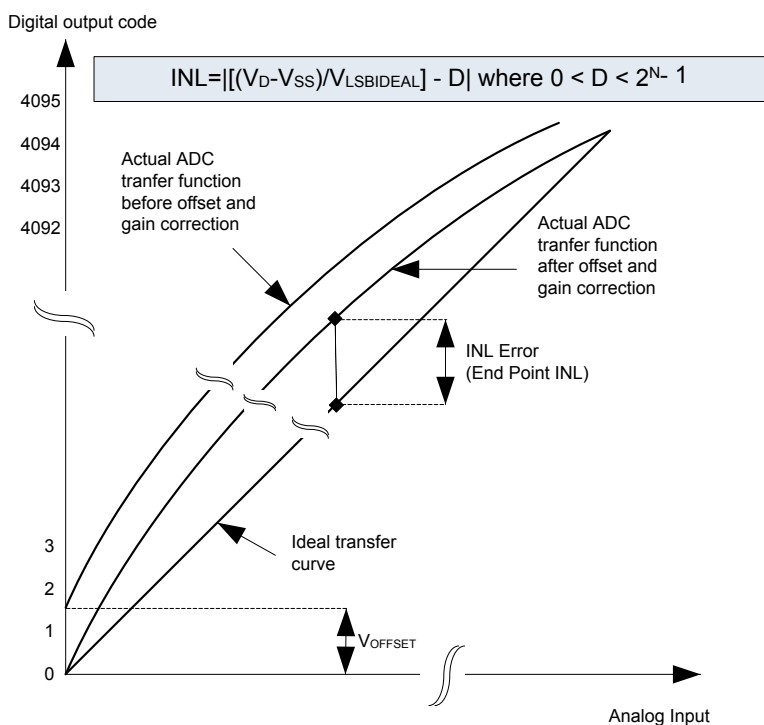


Figure 4.17. Integral Non-Linearity (INL)

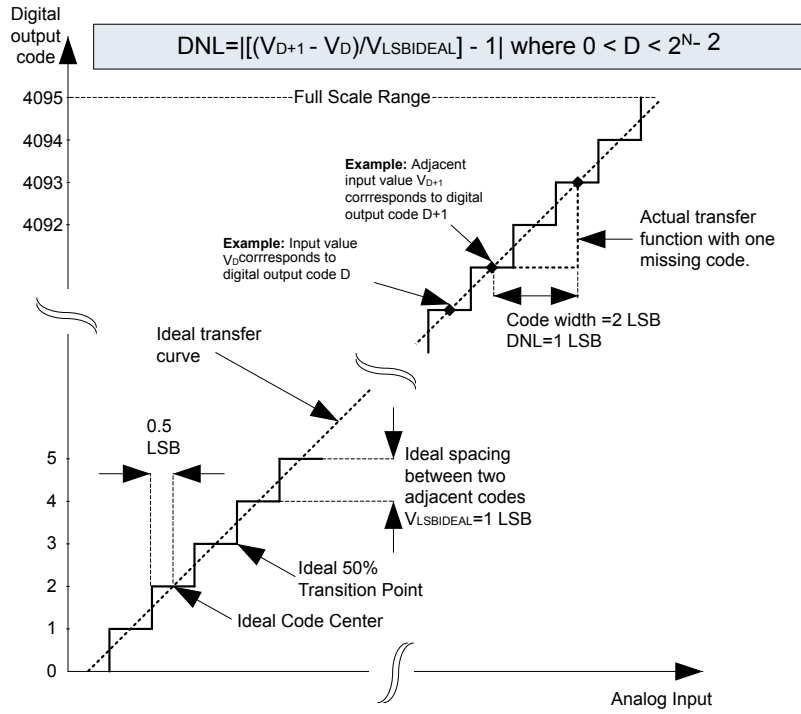


Figure 4.18. Differential Non-Linearity (DNL)

4.10.1 Typical Performance

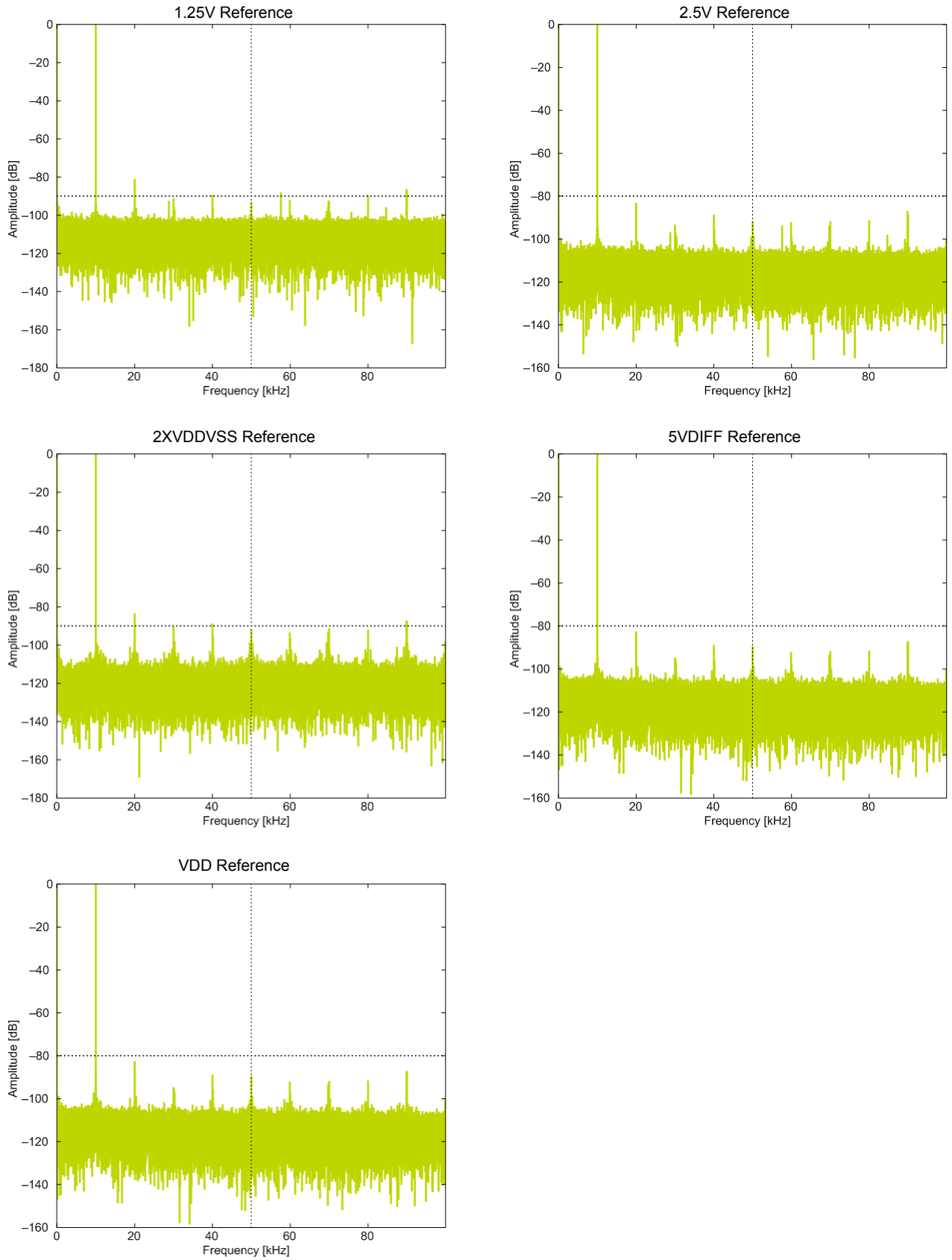


Figure 4.19. ADC Frequency Spectrum, VDD = 3 V, Temp = 25 °C

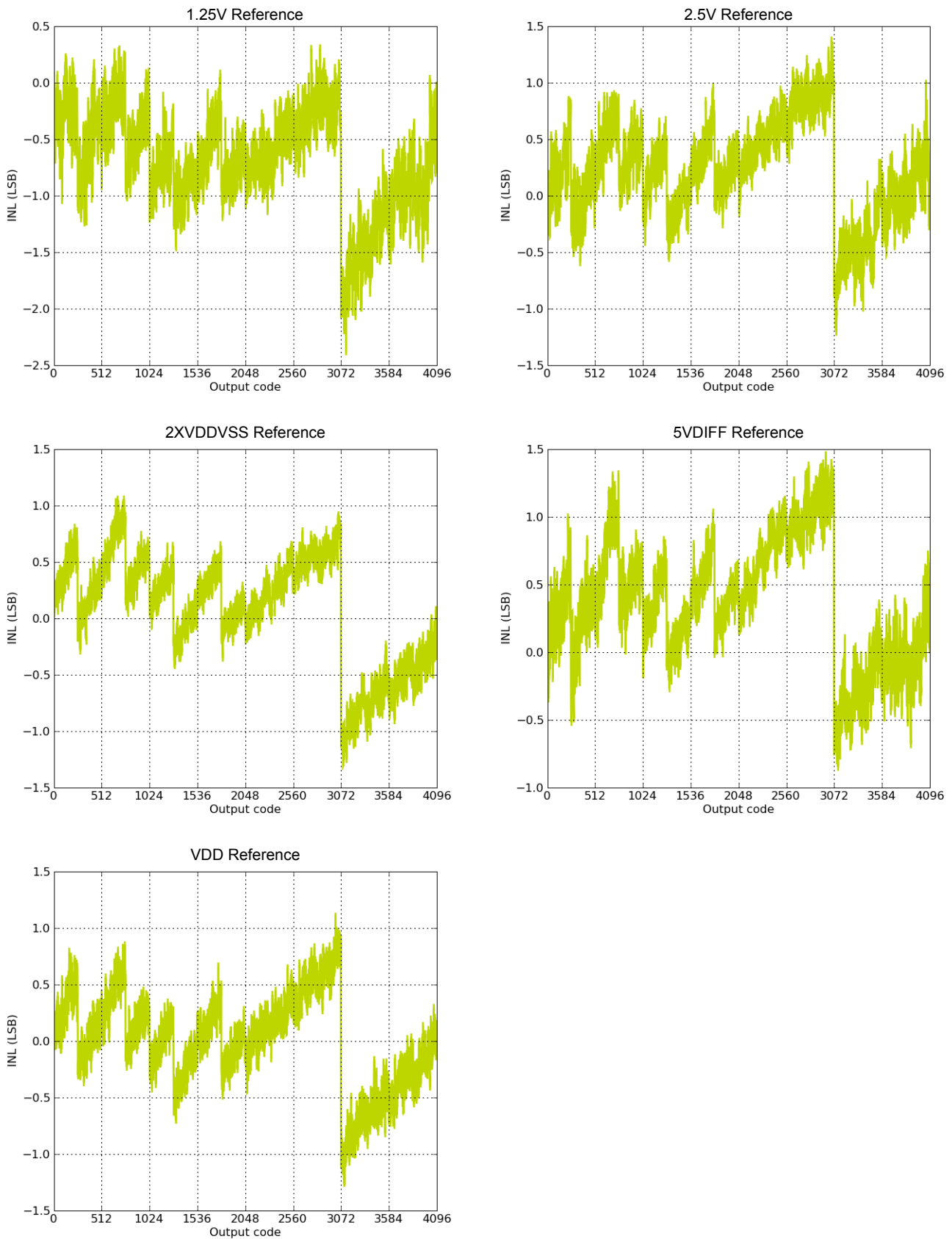


Figure 4.20. ADC Integral Linearity Error vs Code, VDD = 3 V, Temp = 25 °C

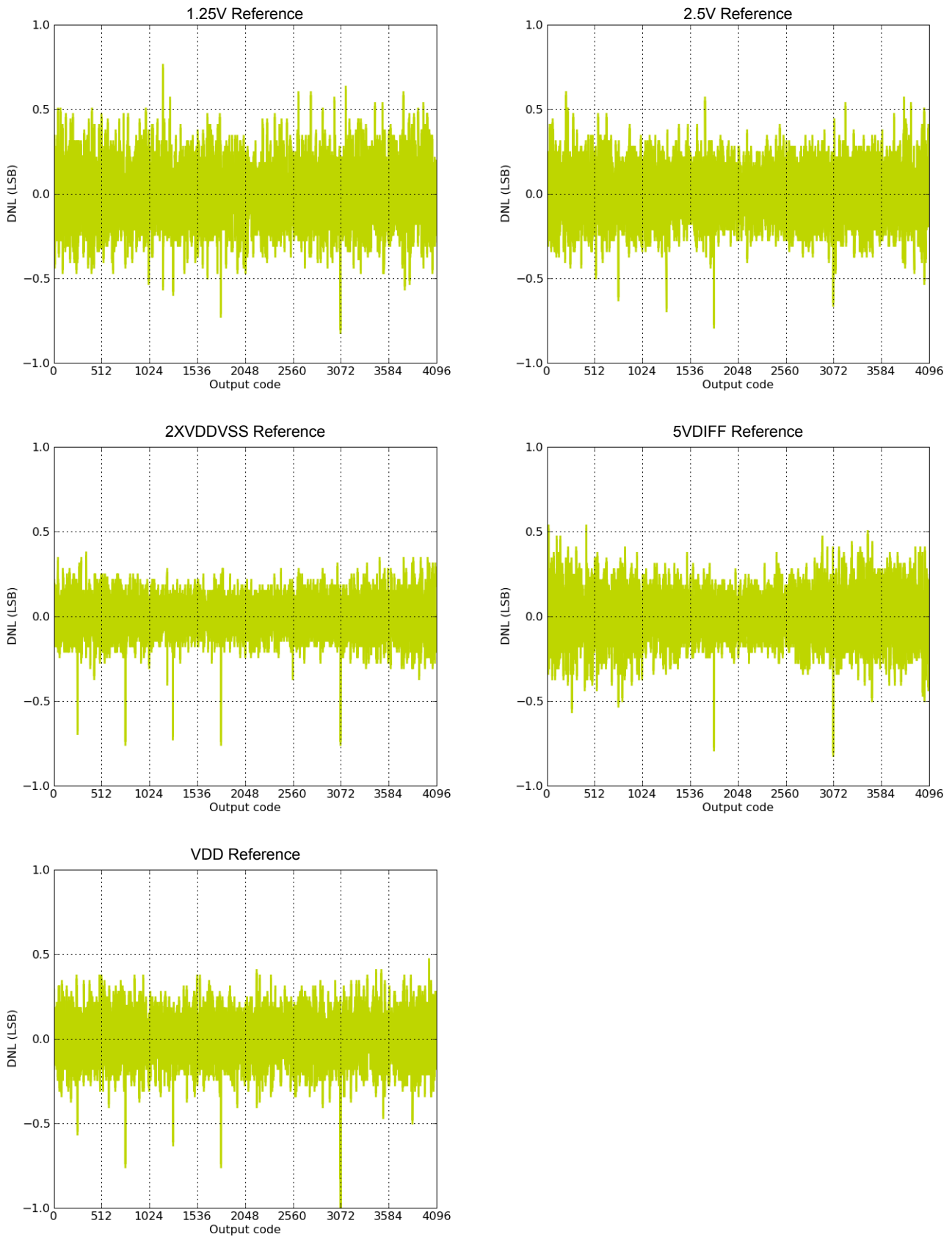


Figure 4.21. ADC Differential Linearity Error vs Code, VDD = 3 V, Temp = 25 °C

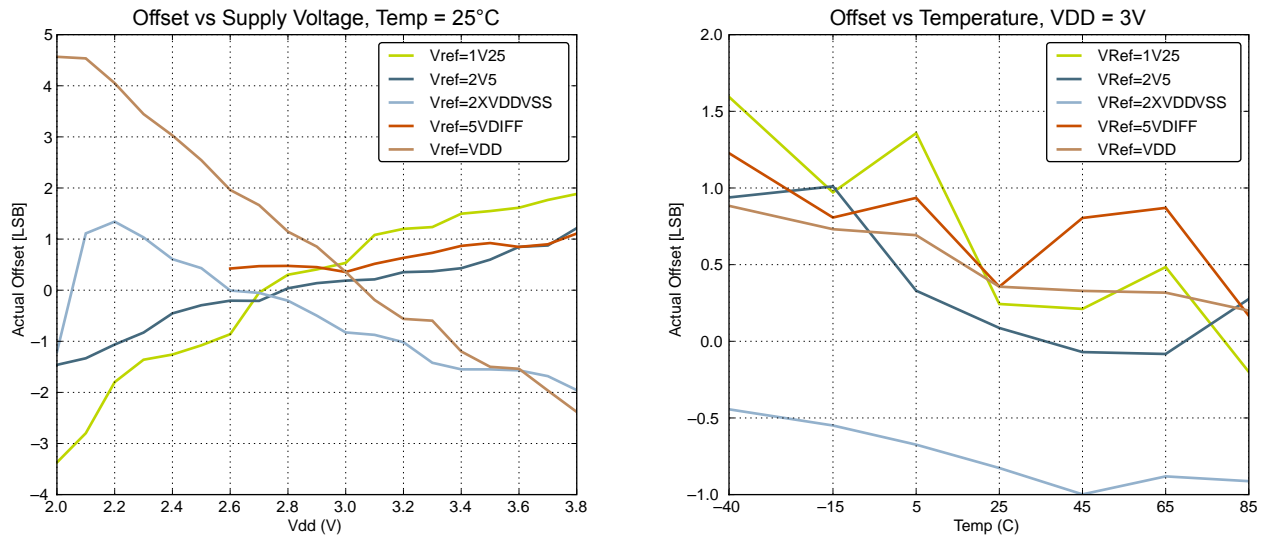


Figure 4.22. ADC Absolute Offset, Common Mode = VDD/2

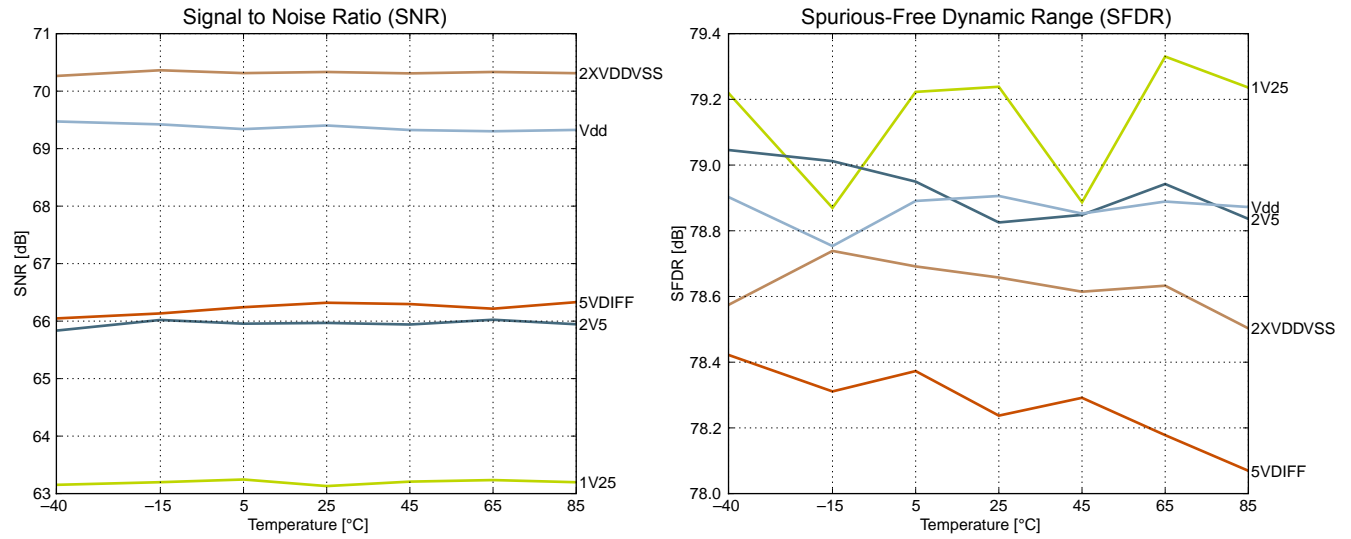


Figure 4.23. ADC Dynamic Performance vs Temperature for all ADC References, VDD = 3 V

4.11 Digital Analog Converter (DAC)

Table 4.15. DAC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------------|--|-----------|-----|----------|------------|
| Output voltage range | V_{DACOUT} | VDD voltage reference, single ended | 0 | — | V_{DD} | V |
| | | VDD voltage reference, differential | $-V_{DD}$ | — | V_{DD} | V |
| Output common mode voltage range | V_{DACCM} | | 0 | — | V_{DD} | V |
| Active current including references for 2 channels | I_{DAC} | 500 kSamples/s, 12bit | — | 400 | 650 | μ A |
| | | 100 kSamples/s, 12 bit | — | 200 | 250 | μ A |
| | | 1 kSamples/s 12 bit NORMAL | — | 17 | 25 | μ A |
| Sample rate | SR_{DAC} | | — | — | 500 | ksamples/s |
| DAC clock frequency | f_{DAC} | Continuous Mode | — | — | 1000 | kHz |
| | | Sample/Hold Mode | — | — | 250 | kHz |
| | | Sample/Off Mode | — | — | 250 | kHz |
| Clock cycles per conversion | $CYC_{DAC-CONV}$ | | — | 2 | — | cycles |
| Conversion time | $t_{DACCONV}$ | | 2 | — | — | μ s |
| Settling time | $t_{DACSETTLE}$ | | — | 5 | — | μ s |
| Signal to Noise Ratio (SNR) | SNR_{DAC} | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 59 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 58 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, V_{DD} reference | — | 59 | — | dB |
| Signal to Noise-pulse Distortion Ratio (SNDR) | $SNDR_{DAC}$ | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 57 | — | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 54 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 56 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 53 | — | dB |
| | | 500 kSamples/s, 12 bit, differential, V_{DD} reference | — | 55 | — | dB |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|-------------------------|---|-----|-----|-----|------|
| Spurious-Free Dynamic Range(SFDR) | SFDR _{DAC} | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | — | 62 | — | dBc |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | — | 56 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | — | 61 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | — | 55 | — | dBc |
| | | 500 kSamples/s, 12 bit, differential, V _{DD} reference | — | 60 | — | dBc |
| Offset voltage | V _{DACOFF-SET} | After calibration, single ended | — | 2 | — | mV |
| | | After calibration, differential | — | 2 | — | mV |
| Differential non-linearity | DNL _{DAC} | V _{DD} = 3.0 V, V _{DD} reference | — | ±1 | — | LSB |
| Integral non-linearity | INL _{DAC} | V _{DD} = 3.0 V, V _{DD} reference | — | ±5 | — | LSB |
| No missing codes | MC _{DAC} | | — | 12 | — | bits |
| Load current | I _{LOAD_DC} | | — | — | 11 | mA |

4.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 4.16. OPAMP

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|------------------------|----------------------|---|-----------------|-------|----------------------|------|
| Active Current | I _{OPAMP} | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain | — | 350 | 405 | μA |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain | — | 95 | 115 | μA |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain | — | 13 | 17 | μA |
| Open Loop Gain | G _{OL} | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | — | 101 | — | dB |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | — | 98 | — | dB |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | — | 91 | — | dB |
| Gain Bandwidth Product | GBW _{OPAMP} | OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0 | — | 16.36 | — | MHz |
| | | OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1 | — | 0.81 | — | MHz |
| | | OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1 | — | 0.11 | — | MHz |
| | | OPA2 BIASPROG=0xF, HALF- BIAS=0x0 | — | 2.11 | — | MHz |
| | | OPA2 BIASPROG=0x7, HALF- BIAS=0x1 | — | 0.72 | — | MHz |
| | | OPA2 BIASPROG=0x0, HALF- BIAS=0x1 | — | 0.09 | — | MHz |
| Phase Margin | PM _{OPAMP} | BIASPROG=0xF, HALFBIAS=0x0, CL=75 pF | — | 64 | — | ° |
| | | BIASPROG=0x7, HALFBIAS=0x1, CL=75 pF | — | 58 | — | ° |
| | | BIASPROG=0x0, HALFBIAS=0x1, CL=75 pF | — | 58 | — | ° |
| Input Resistance | R _{INPUT} | | — | 100 | — | MΩ |
| Load Resistance | R _{LOAD} | OPA0/OPA1 | 200 | — | — | Ω |
| | | OPA2 | 2000 | — | — | Ω |
| Load Current | I _{LOAD_DC} | OPA0/OPA1 | — | — | 11 | mA |
| | | OPA2 | — | — | 1.5 | mA |
| Input Voltage | V _{INPUT} | OPAxHCMDIS=0 | V _{SS} | — | V _{DD} | V |
| | | OPAxHCMDIS=1 | V _{SS} | — | V _{DD} -1.2 | V |
| Output Voltage | V _{OUTPUT} | | V _{SS} | — | V _{DD} | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------|---------------------------|--|-----|-------|------|-------------------|
| Input Offset Voltage | V _{OFFSET} | Unity Gain, V _{SS} <V _{in} <V _{DD} , OPAxHCMDIS=0 | — | 6 | — | mV |
| | | Unity Gain, V _{SS} <V _{in} <V _{DD} -1.2, OPAxHCMDIS=1 | — | 1 | — | mV |
| Input Offset Voltage Drift | V _{OFFSET_DRIFT} | | — | — | 0.02 | mV/°C |
| Slew Rate | SR _{OPAMP} | OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0 | — | 46.11 | — | V/μs |
| | | OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1 | — | 1.21 | — | V/μs |
| | | OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1 | — | 0.16 | — | V/μs |
| | | OPA2 BIASPROG=0xF, HALFBIAS=0x0 | — | 4.43 | — | V/μs |
| | | OPA2 BIASPROG=0x7, HALFBIAS=0x1 | — | 1.30 | — | V/μs |
| | | OPA2 BIASPROG=0x0, HALFBIAS=0x1 | — | 0.16 | — | V/μs |
| Power-up Time | PU _{OPAMP} | OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0 | — | 0.09 | — | μs |
| | | OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1 | — | 1.52 | — | μs |
| | | OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1 | — | 12.74 | — | μs |
| | | OPA2 BIASPROG=0xF, HALFBIAS=0x0 | — | 0.09 | — | μs |
| | | OPA2 BIASPROG=0x7, HALFBIAS=0x1 | — | 0.13 | — | μs |
| | | OPA2 BIASPROG=0x0, HALFBIAS=0x1 | — | 0.17 | — | μs |
| Voltage Noise | N _{OPAMP} | V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0 | — | 101 | — | μV _{RMS} |
| | | V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1 | — | 141 | — | μV _{RMS} |
| | | V _{out} =1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | — | 196 | — | μV _{RMS} |
| | | V _{out} =1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1 | — | 229 | — | μV _{RMS} |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0 | — | 1230 | — | μV _{RMS} |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1 | — | 2130 | — | μV _{RMS} |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | — | 1630 | — | μV _{RMS} |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1 | — | 2590 | — | μV _{RMS} |

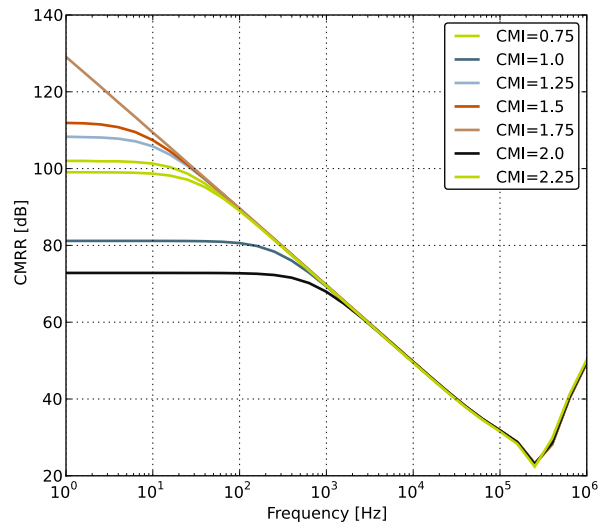


Figure 4.24. OPAMP Common Mode Rejection Ratio

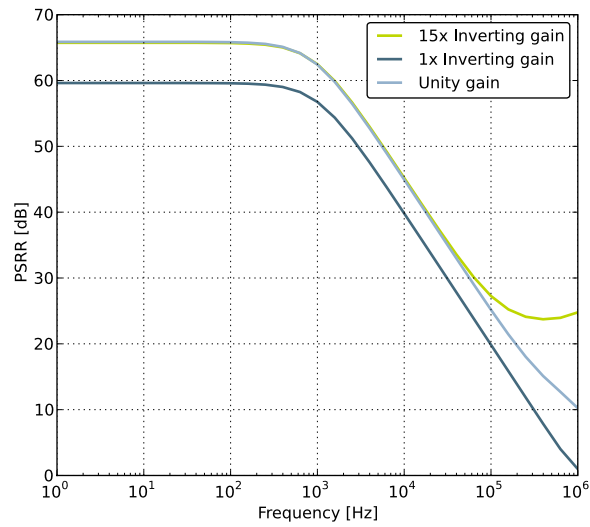


Figure 4.25. OPAMP Positive Power Supply Rejection Ratio

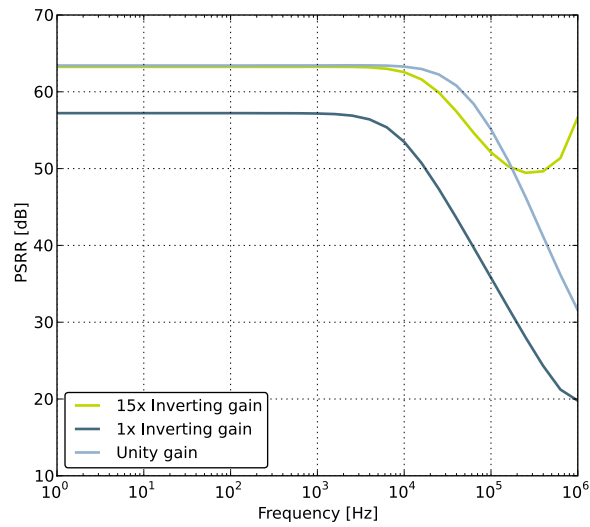


Figure 4.26. OPAMP Negative Power Supply Rejection Ratio

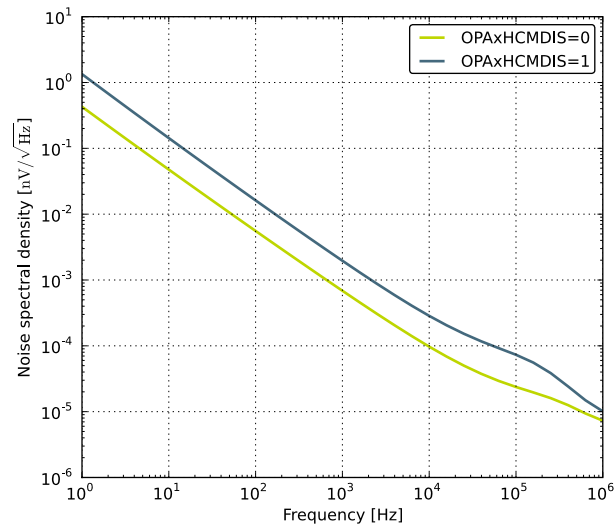


Figure 4.27. OPAMP Voltage Noise Spectral Density (Unity Gain) $V_{out}=1V$

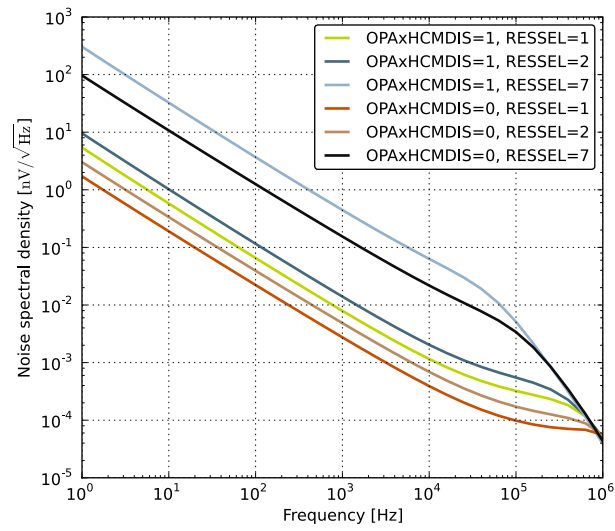


Figure 4.28. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)

4.13 Analog Comparator (ACMP)

Table 4.17. ACMP

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------------|---|-----|------|----------|------------|
| Input voltage range | V_{ACMPIN} | | 0 | — | V_{DD} | V |
| ACMP Common Mode voltage range | V_{ACMPCM} | | 0 | — | V_{DD} | V |
| Active current | I_{ACMP} | BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register | — | 0.1 | 0.6 | μA |
| | | BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | — | 2.87 | 12 | μA |
| | | BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register | — | 195 | 520 | μA |
| Current consumption of internal voltage reference | $I_{ACMPREF}$ | Internal voltage reference off. Using external voltage reference | — | 0.0 | 0.5 | μA |
| | | Internal voltage reference | — | 2.15 | 3.00 | μA |
| Offset voltage | $V_{ACMPOFFSET}$ | BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | -12 | 0 | 12 | mV |
| ACMP hysteresis | $V_{ACMPHYST}$ | Programmable | — | 17 | — | mV |
| Capacitive Sense Internal Resistance | R_{CSRES} | CSRESSEL=0b00 in ACMPn_INPUTSEL | — | 39 | — | k Ω |
| | | CSRESSEL=0b01 in ACMPn_INPUTSEL | — | 71 | — | k Ω |
| | | CSRESSEL=0b10 in ACMPn_INPUTSEL | — | 104 | — | k Ω |
| | | CSRESSEL=0b11 in ACMPn_INPUTSEL | — | 136 | — | k Ω |
| Startup time | $t_{ACMPSTART}$ | | — | — | 10 | μs |

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in the following equation. $I_{ACMPREF}$ is zero if an external voltage reference is used.

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

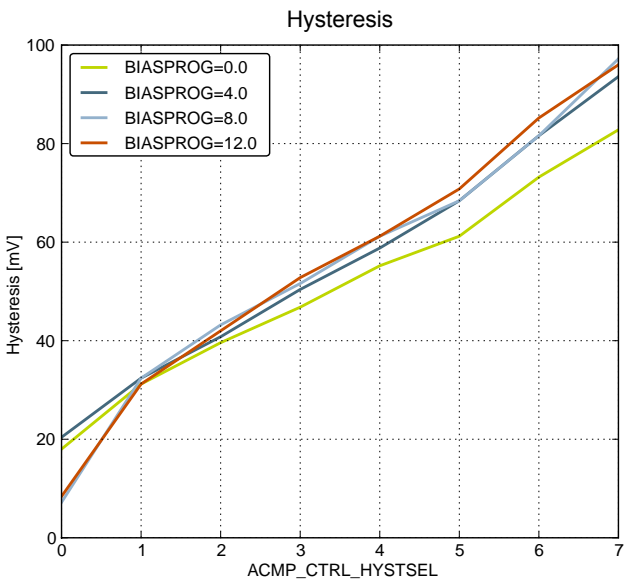
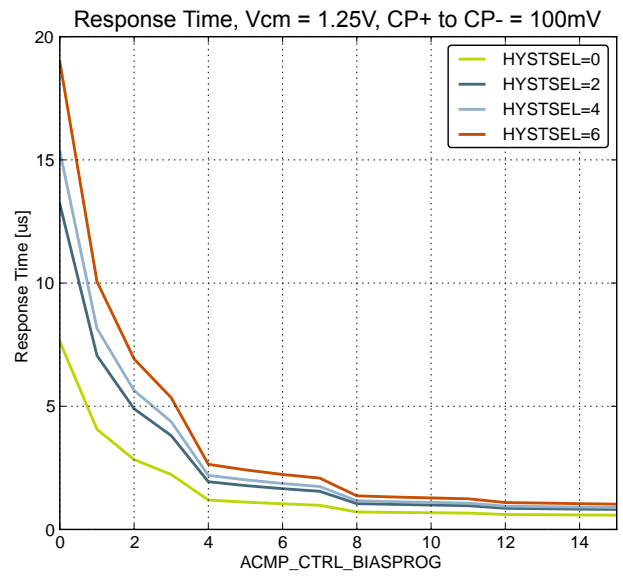
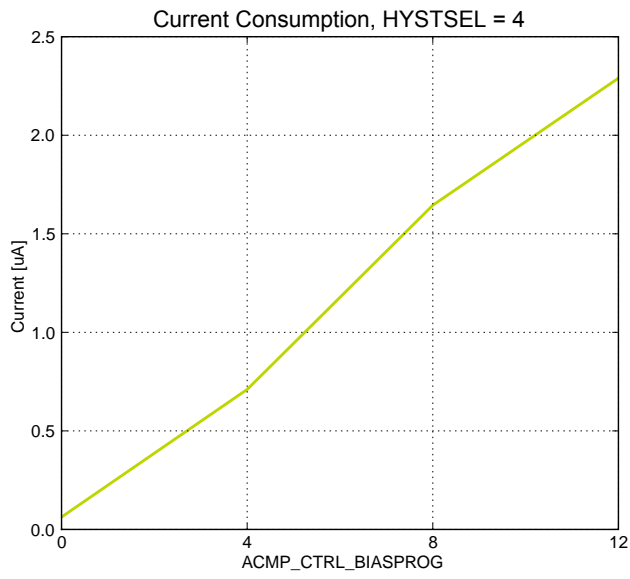


Figure 4.29. ACMP Characteristics, Vdd = 3 V, Temp = 25 °C, FULLBIAS = 0, HALFBIAS = 1

4.14 Voltage Comparator (VCMP)

Table 4.18. VCMP

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|------------------------------------|--|-----|-----------------|-----|------|
| Input voltage range | V _{VCMPIN} | | — | V _{DD} | — | V |
| VCMP Common Mode voltage range | V _{VCMP_{CM}} | | — | V _{DD} | — | V |
| Active current | I _{VCMP} | BIASPROG=0b0000 and HALF-BIAS=1 in VCMPn_CTRL register | — | 0.3 | 0.6 | μA |
| | | BIASPROG=0b1111 and HALF-BIAS=0 in VCMPn_CTRL register. LPREF=0. | — | 22 | 30 | μA |
| Startup time reference generator | t _{VCMPREF} | NORMAL | — | 10 | — | μs |
| Offset voltage | V _{VCMP_{OFFSET}} | Single ended | — | 10 | — | mV |
| | | Differential | — | 10 | — | mV |
| VCMP hysteresis | V _{VCMP_{HYST}} | | — | 17 | — | mV |
| Startup time | t _{VCMP_{START}} | | — | — | 10 | μs |

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{DD \text{ Trigger Level}} = 1.667V + 0.034 \times \text{TRIGLEVEL}$$

4.15 LCD

Table 4.19. LCD

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|--|-----|------|-----|------|
| Frame rate | f_{LCDFR} | | 30 | — | 200 | Hz |
| Number of segments supported | NUM _{SEG} | | — | 20×8 | — | seg |
| LCD supply voltage range | V_{LCD} | Internal boost circuit enabled | 2.0 | — | 3.8 | V |
| Steady state current consumption. | I_{LCD} | Display disconnected, static mode, framerate 32 Hz, all segments on. | — | 250 | — | nA |
| | | Display disconnected, quadruplex mode, framerate 32 Hz, all segments on, bias mode to ONETHIRD in LCD_DISPCTRL register. | — | 550 | — | nA |
| Steady state Current contribution of internal boost. | $I_{LCDBOOST}$ | Internal voltage boost off | — | 0 | — | μA |
| | | Internal voltage boost on, boosting from 2.2 V to 3.0 V. | — | 8.4 | — | μA |
| Boost Voltage | V_{BOOST} | VBLEV of LCD_DISPCTRL register to LEVEL0 | — | 3.0 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL1 | — | 3.08 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL2 | — | 3.17 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL3 | — | 3.26 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL4 | — | 3.34 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL5 | — | 3.43 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL6 | — | 3.52 | — | V |
| | | VBLEV of LCD_DISPCTRL register to LEVEL7 | — | 3.6 | — | V |

The total LCD current is given by the following equation. $I_{LCDBOOST}$ is zero if internal boost is off.

$$I_{LCDTOTAL} = I_{LCD} + I_{LCDBOOST}$$

4.16 I2C

Table 4.20. I2C Standard-mode (Sm)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------------|-----|-----|---------------------|---------|
| SCL clock frequency | f_{SCL} | 0 | — | 100 ¹ | kHz |
| SCL clock low time | t_{LOW} | 4.7 | — | — | μs |
| SCL clock high time | t_{HIGH} | 4.0 | — | — | μs |
| SDA set-up time | $t_{SU,DAT}$ | 250 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | 3450 ^{2,3} | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 4.7 | — | — | μs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 4.0 | — | — | μs |
| STOP condition set-up time | $t_{SU,STO}$ | 4.0 | — | — | μs |
| Bus free time between a STOP and a START condition | t_{BUF} | 4.7 | — | — | μs |

Note:

1. For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32TG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((3450 \cdot 10^{-9} [s] \cdot f_{HFPERCLK} [Hz]) - 4)$.

Table 4.21. I2C Fast-mode (Fm)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------------|-----|-----|--------------------|---------|
| SCL clock frequency | f_{SCL} | 0 | — | 400 ¹ | kHz |
| SCL clock low time | t_{LOW} | 1.3 | — | — | μs |
| SCL clock high time | t_{HIGH} | 0.6 | — | — | μs |
| SDA set-up time | $t_{SU,DAT}$ | 100 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | 900 ^{2,3} | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.6 | — | — | μs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.6 | — | — | μs |
| STOP condition set-up time | $t_{SU,STO}$ | 0.6 | — | — | μs |
| Bus free time between a STOP and a START condition | t_{BUF} | 1.3 | — | — | μs |

Note:

1. For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32TG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when $I2Cn_CLKDIV < ((900 \cdot 10^{-9} [s] \cdot f_{HFPERCLK} [Hz]) - 4)$.

Table 4.22. I2C Fast-mode Plus (Fm+)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|--------------|------|-----|-------------------|---------|
| SCL clock frequency | f_{SCL} | 0 | — | 1000 ¹ | kHz |
| SCL clock low time | t_{LOW} | 0.5 | — | — | μs |
| SCL clock high time | t_{HIGH} | 0.26 | — | — | μs |
| SDA set-up time | $t_{SU,DAT}$ | 50 | — | — | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | — | — | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.26 | — | — | μs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.26 | — | — | μs |
| STOP condition set-up time | $t_{SU,STO}$ | 0.26 | — | — | μs |
| Bus free time between a STOP and a START condition | t_{BUF} | 0.5 | — | — | μs |
| Note: | | | | | |
| 1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32TG Reference Manual. | | | | | |

4.17 Digital Peripherals

Table 4.23. Digital Peripherals

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------|---------------|-------------------------------------|-----|------|-----|-------------|
| USART current | I_{USART} | USART idle current, clock enabled | — | 7.5 | — | $\mu A/MHz$ |
| LEUART current | I_{LEUART} | LEUART idle current, clock enabled | — | 150 | — | nA |
| I2C current | I_{I2C} | I2C idle current, clock enabled | — | 6.25 | — | $\mu A/MHz$ |
| TIMER current | I_{TIMER} | TIMER_0 idle current, clock enabled | — | 8.75 | — | $\mu A/MHz$ |
| LETIMER current | $I_{LETIMER}$ | LETIMER idle current, clock enabled | — | 75 | — | nA |
| PCNT current | I_{PCNT} | PCNT idle current, clock enabled | — | 60 | — | nA |
| RTC current | I_{RTC} | RTC idle current, clock enabled | — | 40 | — | nA |
| LCD current | I_{LCD} | LCD idle current, clock enabled | — | 50 | — | nA |
| AES current | I_{AES} | AES idle current, clock enabled | — | 2.5 | — | $\mu A/MHz$ |
| GPIO current | I_{GPIO} | GPIO idle current, clock enabled | — | 5.31 | — | $\mu A/MHz$ |
| PRS current | I_{PRS} | PRS idle current | — | 2.81 | — | $\mu A/MHz$ |
| DMA current | I_{DMA} | Clock enable | — | 8.12 | — | $\mu A/MHz$ |

5. Pin Definitions

Note: Please refer to the application note *AN0002 EFM32 Hardware Design Considerations* for guidelines on designing Printed Circuit Boards (PCBs) for the EFM32TG.

5.1 EFM32TG108 (QFN24)

5.1.1 Pinout

The EFM32TG108 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

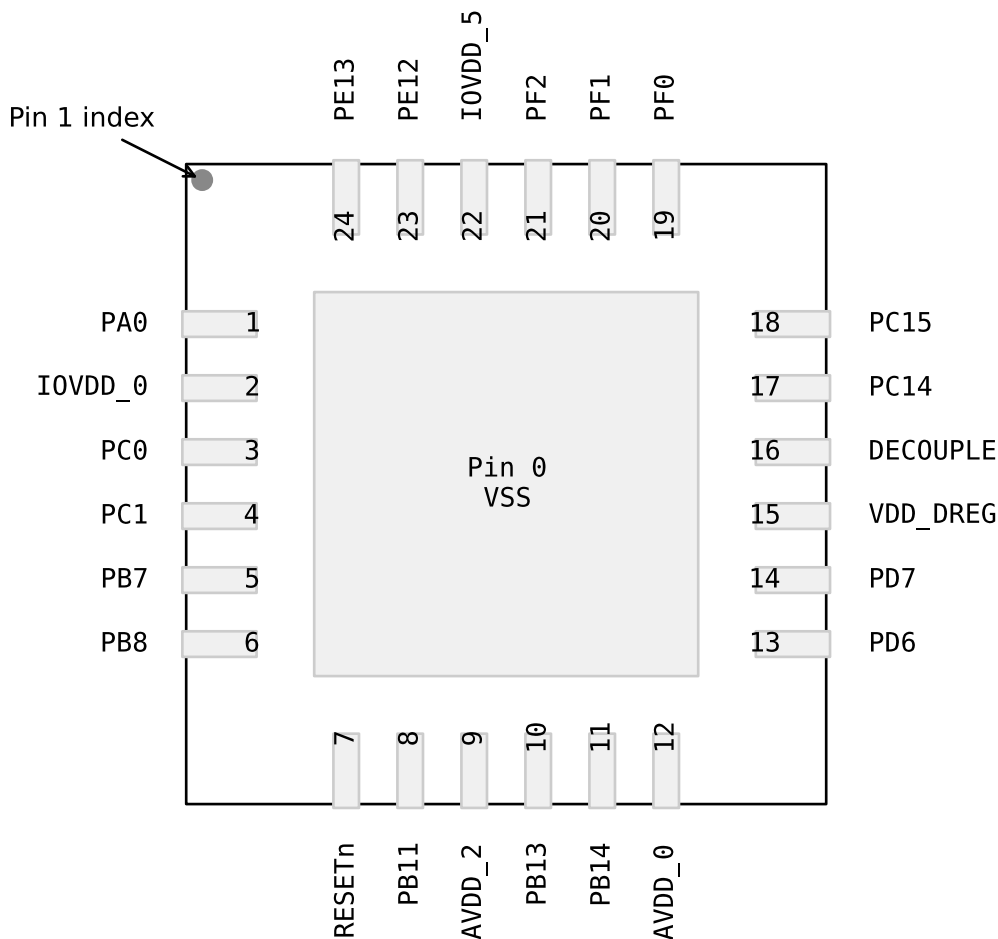


Figure 5.1. EFM32TG108 Pinout (top view, not to scale)

Table 5.1. Device Pinout

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | IOVDD_0 | Digital IO power supply 0. | | | |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PC0 | ACMP0_CH0 | TIM0_CC1 #4 PCNT0_S0IN #2 | US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 4 | PC1 | ACMP0_CH1 | TIM0_CC2 #4 PCNT0_S1IN #2 | US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 5 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US1_CLK #0 | |
| 6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US1_CS #0 | |
| 7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 8 | PB11 | | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| 9 | AVDD_2 | Analog power supply 2. | | | |
| 10 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 11 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 12 | AVDD_0 | Analog power supply 0. | | | |
| 13 | PD6 | | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 14 | PD7 | | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 15 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 16 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 17 | PC14 | ACMP1_CH6 | TIM1_CC1 #0 PCNT0_S1IN #0 | | LES_CH14 #0 |
| 18 | PC15 | ACMP1_CH7 | TIM1_CC2 #0 | | LES_CH15 #0 DBG_SWO #1 |
| 19 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 BOOT_TX |
| 20 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 BOOT_RX |
| 21 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------|---------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 22 | IOVDD_5 | Digital IO power supply 5. | | | |
| 23 | PE12 | | TIM1_CC2 #1 | I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 24 | PE13 | | | I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |

5.1.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.2. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|----------------------------|----------|------|------|---|-----|-----|------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | | | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFX TAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |

| Alternate | LOCATION | | | | | | | Description |
|-------------|----------|------|-----|------|-----|-----|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exit output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | | PB14 | | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH2 | PC0 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | | | | | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | | | | | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | | | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| US1_CLK | PB7 | | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.1.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG108 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.3. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | - | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | - | - | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

5.2 EFM32TG110 (QFN24)

5.2.1 Pinout

The EFM32TG110 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

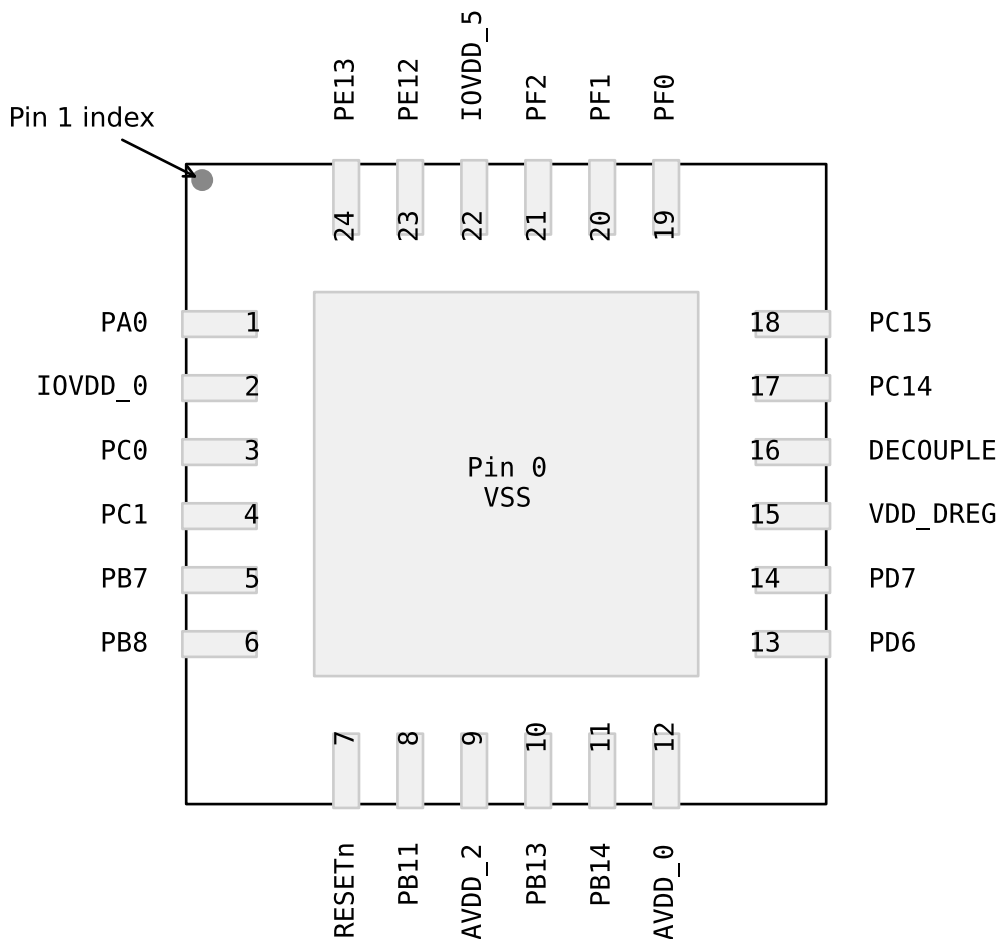


Figure 5.2. EFM32TG110 Pinout (top view, not to scale)

Table 5.4. Device Pinout

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | IOVDD_0 | Digital IO power supply 0. | | | |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---------------------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 4 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 5 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 7 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 8 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| 9 | AVDD_2 | Analog power supply 2. | | | |
| 10 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 11 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 12 | AVDD_0 | Analog power supply 0. | | | |
| 13 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 14 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 15 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 16 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 17 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 18 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 19 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 BOOT_TX |
| 20 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWCLK #0/1 GPIO_EM4WU3 BOOT_RX |
| 21 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 22 | IOVDD_5 | Digital IO power supply 5. | | | |
| 23 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 24 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |

5.2.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.5. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|--|----------|-----|------|------|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX. |
| BOOT_TX | PF0 | | | | | | | Bootloader TX. |
| CMU_CLK0 | | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | | | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0 ALT | PC0 | PC1 | | | | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT / OPAMP_OUT1 ALT | | | PC14 | PC15 | | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|------|-----|-----|-----|-----|------|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFX TAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exit output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exit output 1. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exit output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exit output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | | PB14 | | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH2 | PC0 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | | | | | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | | | | | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | | | | Description |
|-----------|----------|------|-----|------|------|------|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| TIM1_CC0 | | | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | | | | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | | | | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.2.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG110 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.6. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | - | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | - | - | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

5.2.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG110 is shown in the following figure.

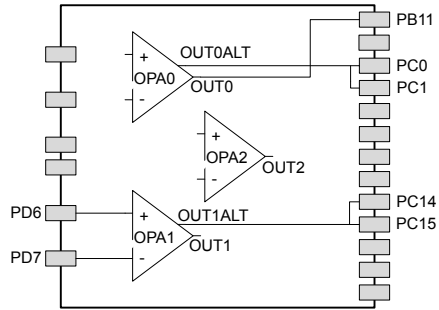


Figure 5.3. Opamp Pinout

5.3 EFM32TG210 (QFN32)

5.3.1 Pinout

The EFM32TG210 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

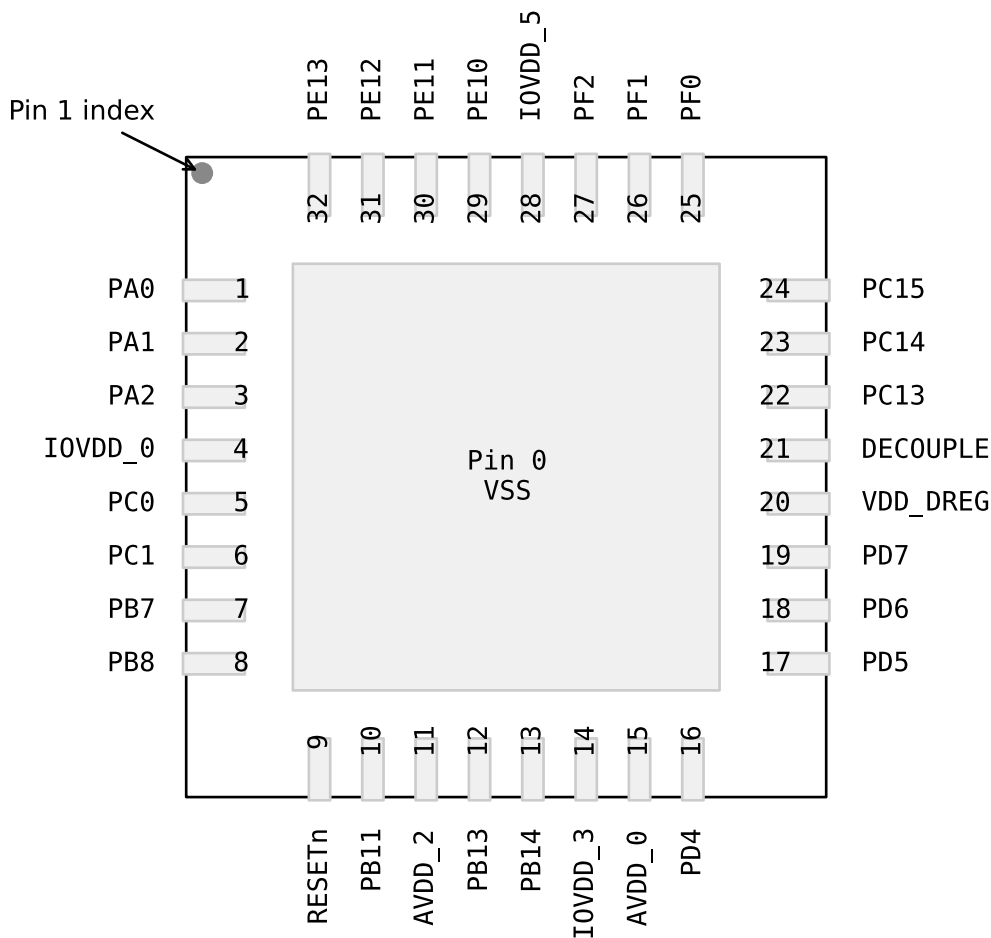


Figure 5.4. EFM32TG210 Pinout (top view, not to scale)

Table 5.7. Device Pinout

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---------------------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 6 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 7 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 8 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 9 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 10 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| 11 | AVDD_2 | Analog power supply 2. | | | |
| 12 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 13 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 14 | IOVDD_3 | Digital IO power supply 3. | | | |
| 15 | AVDD_0 | Analog power supply 0. | | | |
| 16 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |
| 17 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |
| 18 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 19 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 20 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 21 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |

| QFN32 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|---|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 22 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 23 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 24 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 25 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| 26 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 |
| 27 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 28 | IOVDD_5 | Digital IO power supply 5. | | | |
| 29 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 30 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 31 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 32 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |

5.3.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.8. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|------------------------------------|----------|------|------|------|---|---|---|--|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT/ OPAMP_OUT0 ALT | PC0 | PC1 | | | | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT/ OPAMP_OUT1 ALT | | PC13 | PC14 | PC15 | | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | | | | | | | Operational Amplifier 2 output. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |

| Alternate | LOCATION | | | | | | | Description |
|-------------|----------|------|-----|-----|-----|-----|------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exit output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exit output 1. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exit output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exit output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exit output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|------|-----|------|------|------|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG210 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.9. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | PC13 | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

5.3.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG210 is shown in the following figure.

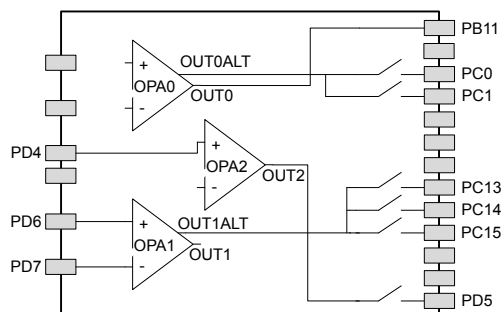


Figure 5.5. Opamp Pinout

5.4 EFM32TG222 (TQFP48)

5.4.1 Pinout

The EFM32TG222 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

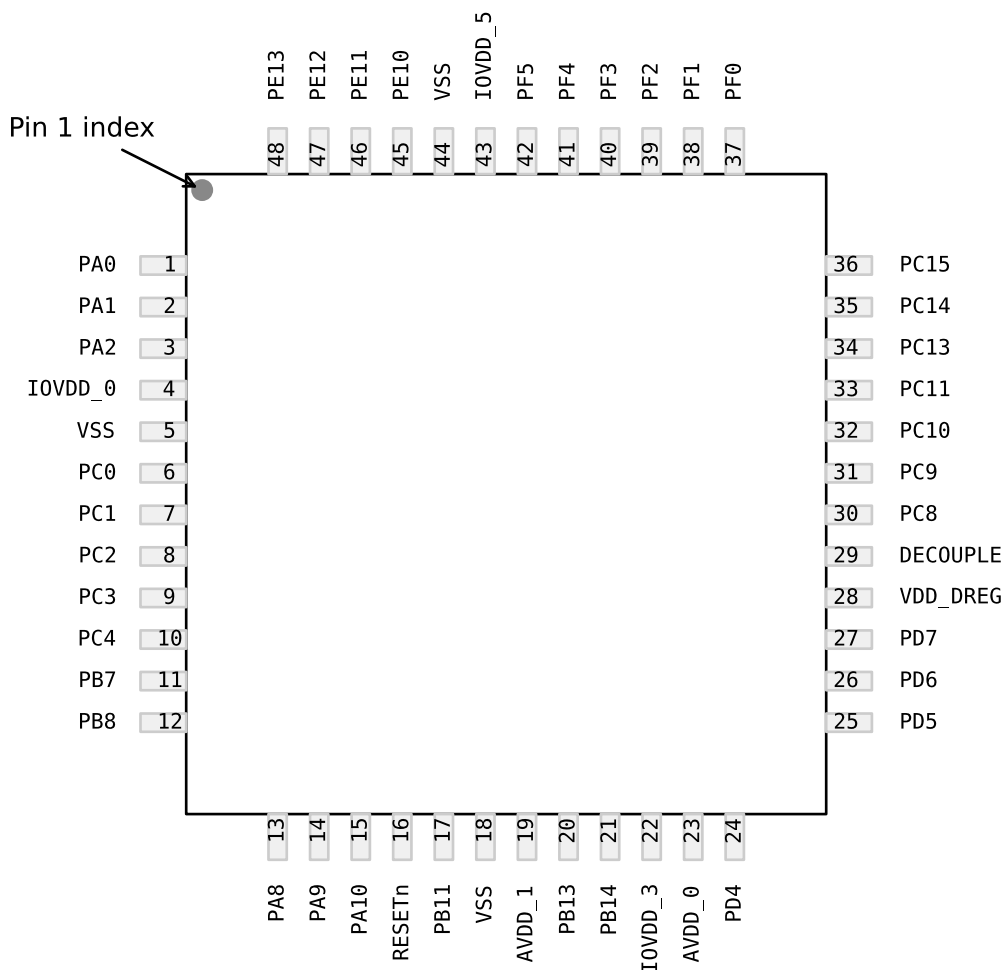


Figure 5.6. EFM32TG222 Pinout (top view, not to scale)

Table 5.10. Device Pinout

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|---------------------------------------|--------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | VSS | Ground. | | | |
| 6 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 7 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 8 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | | | LES_CH2 #0 |
| 9 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | | | LES_CH3 #0 |
| 10 | PC4 | ACMP0_CH4 DAC0_P0 / OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| 11 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 12 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 13 | PA8 | | | | |
| 14 | PA9 | | | | |
| 15 | PA10 | | | | |
| 16 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 17 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| 18 | VSS | Ground. | | | |
| 19 | AVDD_1 | Analog power supply 1. | | | |
| 20 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 21 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 22 | IOVDD_3 | Digital IO power supply 3. | | | |
| 23 | AVDD_0 | Analog power supply 0. | | | |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 24 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |
| 25 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |
| 26 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 27 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 28 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 29 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 30 | PC8 | ACMP1_CH0 | | US0_CS #2 | LES_CH8 #0 |
| 31 | PC9 | ACMP1_CH1 | | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 32 | PC10 | ACMP1_CH2 | | US0_RX #2 | LES_CH10 #0 |
| 33 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| 34 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 35 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 36 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 37 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| 38 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 |
| 39 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------|--|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 40 | PF3 | | | | PRS_CH0 #1 |
| 41 | PF4 | | | | PRS_CH1 #1 |
| 42 | PF5 | | | | PRS_CH2 #1 |
| 43 | IOVDD_5 | Digital IO power supply 5. | | | |
| 44 | VSS | Ground. | | | |
| 45 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 46 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 47 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 48 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |

5.4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.11. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|----------------------------|----------|---|------|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |

| Alternate | LOCATION | | | | | | | Description |
|--------------------------------|----------|------|------|------|-----|-----|------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| DAC0_OUT0ALT/ OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT/ OPAMP_OUT1ALT | | PC13 | PC14 | PC15 | | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | | | | | | | Operational Amplifier 2 output. |
| DAC0_P0/ OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exit output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exit output 1. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exit output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exit output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exit output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |

| Alternate | LOCATION | | | | | | | Description |
|-------------|----------|------|------|------|------|------|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | Description |
|-----------|----------|---|------|------|-----|-----|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG222 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.12. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | PC13 | - | PC11 | PC10 | PC9 | PC8 | - | - | - | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.4.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG222 is shown in the following figure.

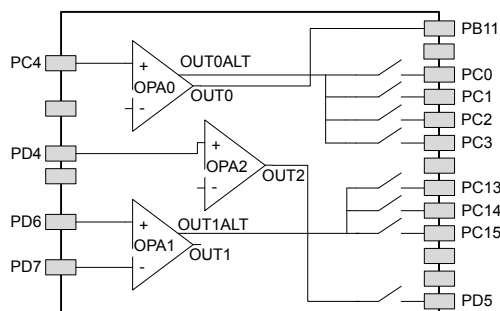


Figure 5.7. Opamp Pinout

5.5 EFM32TG225 (BGA48)

5.5.1 Pinout

The EFM32TG225 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

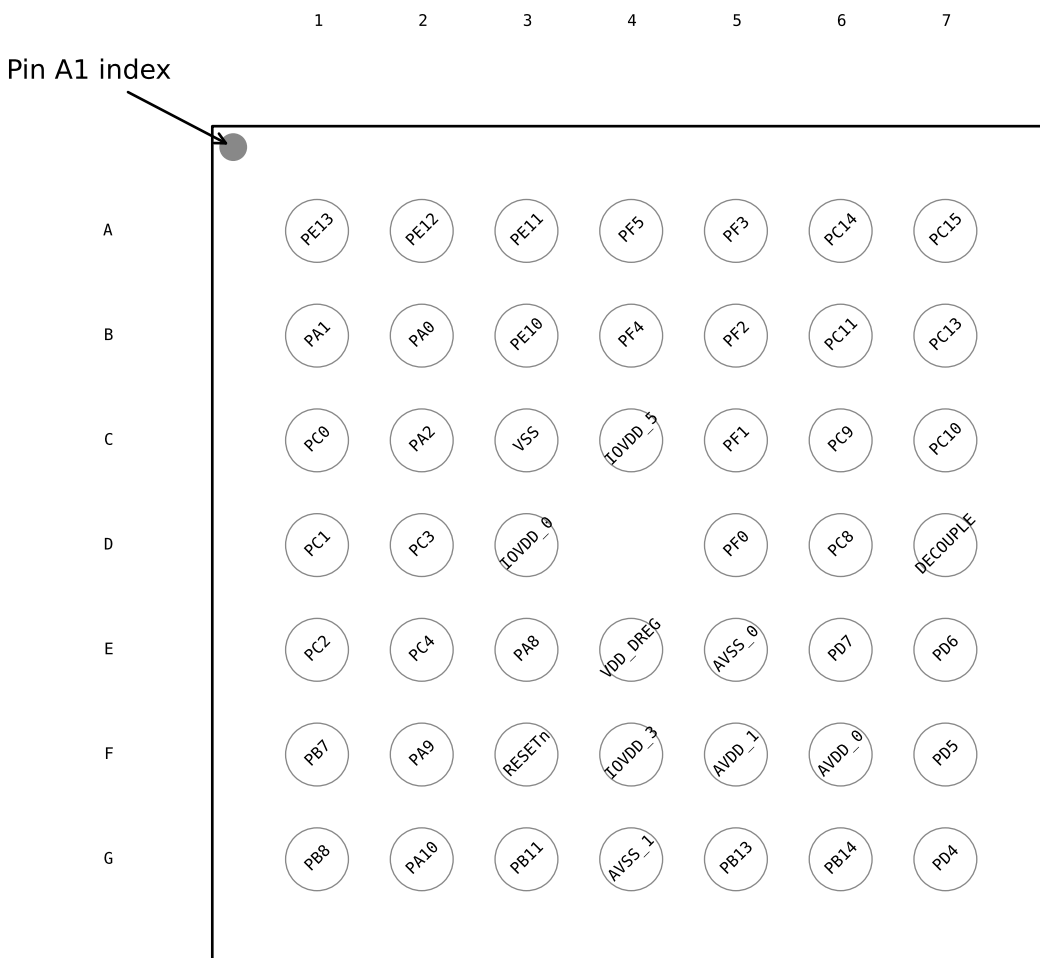


Figure 5.8. EFM32TG225 Pinout (top view, not to scale)

Table 5.13. Device Pinout

| BGA48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--------|---------------------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| A1 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |

| BGA48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|---|--|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| A2 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| A3 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| A4 | PF5 | | | | PRS_CH2 #1 |
| A5 | PF3 | | | | PRS_CH0 #1 |
| A6 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| A7 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| B1 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| B2 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| B3 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| B4 | PF4 | | | | PRS_CH1 #1 |
| B5 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| B6 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| B7 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| C1 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| C2 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| C3 | VSS | Ground. | | | |
| C4 | IOVDD_5 | Digital IO power supply 5. | | | |
| C5 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 |

| BGA48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| C6 | PC9 | ACMP1_CH1 | | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| C7 | PC10 | ACMP1_CH2 | | US0_RX #2 | LES_CH10 #0 |
| D1 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| D2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | | | LES_CH3 #0 |
| D3 | IOVDD_0 | Digital IO power supply 0. | | | |
| D5 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| D6 | PC8 | ACMP1_CH0 | | US0_CS #2 | LES_CH8 #0 |
| D7 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| E1 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | | | LES_CH2 #0 |
| E2 | PC4 | ACMP0_CH4 DAC0_P0/ OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| E3 | PA8 | | | | |
| E4 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| E5 | AVSS_0 | Analog ground 0. | | | |
| E6 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| E7 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| F1 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| F2 | PA9 | | | | |
| F3 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |

| BGA48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|----------------------------|-------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| F4 | IOVDD_3 | Digital IO power supply 3. | | | |
| F5 | AVDD_1 | Analog power supply 1. | | | |
| F6 | AVDD_0 | Analog power supply 0. | | | |
| F7 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |
| G1 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| G2 | PA10 | | | | |
| G3 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| G4 | AVSS_1 | Analog ground 1. | | | |
| G5 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| G6 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| G7 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |

5.5.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.14. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|----------------------------|----------|---|------|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |

| Alternate | LOCATION | | | | | | | Description |
|--------------------------------|----------|------|------|------|-----|-----|------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| DAC0_OUT0ALT/ OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT/ OPAMP_OUT1ALT | | PC13 | PC14 | PC15 | | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | | | | | | | Operational Amplifier 2 output. |
| DAC0_P0/ OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFX TAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exit output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exit output 1. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exit output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exit output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exit output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |

| Alternate | LOCATION | | | | | | | Description |
|-------------|----------|------|------|------|------|------|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|---|------|------|-----|-----|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG225 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.15. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | PC13 | - | PC11 | PC10 | PC9 | PC8 | - | - | - | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.5.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG225 is shown in the following figure.

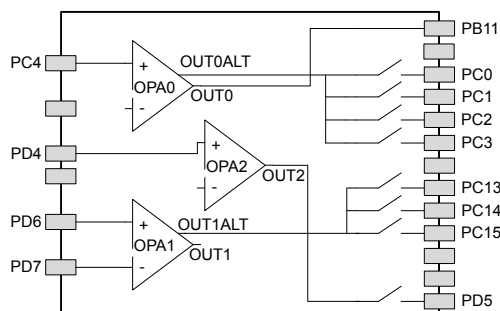


Figure 5.9. Opamp Pinout

5.6 EFM32TG230 (QFN64)

5.6.1 Pinout

The EFM32TG230 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

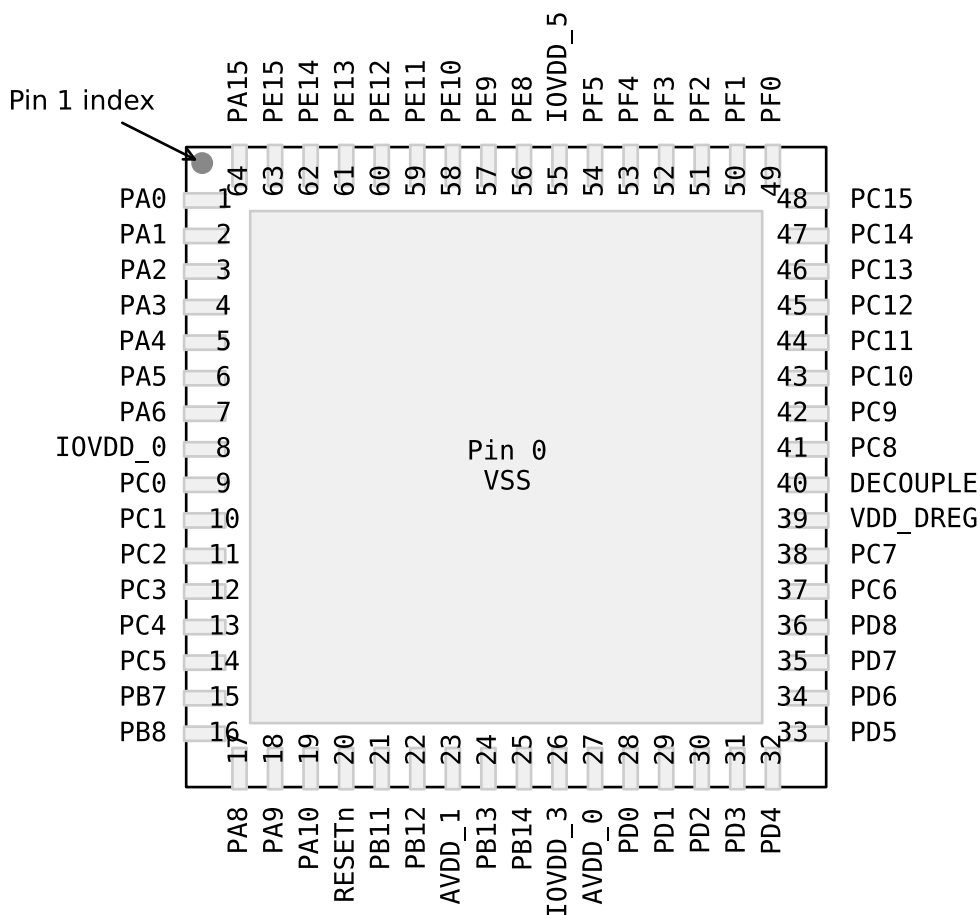


Figure 5.10. EFM32TG230 Pinout (top view, not to scale)

Table 5.16. Device Pinout

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|---------------------------------------|--------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | | | | LES_ALTEX2 #0 |
| 5 | PA4 | | | | LES_ALTEX3 #0 |
| 6 | PA5 | | | | LES_ALTEX4 #0 |
| 7 | PA6 | | | | GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 10 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 11 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | | | LES_CH2 #0 |
| 12 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | | | LES_CH3 #0 |
| 13 | PC4 | ACMP0_CH4 DAC0_P0/ OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0/ OPAMP_N0 | LETIM0_OUT1 #3 | | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA8 | | | | |
| 18 | PA9 | | | | |
| 19 | PA10 | | | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|----------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 22 | PB12 | DAC0_OUT1/ OPAMP_OUT1 | LETIM0_OUT1 #1 | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 35 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | I2C0_SDA #2 | LES_CH6 #0 |
| 38 | PC7 | ACMP0_CH7 | | I2C0_SCL #2 | LES_CH7 #0 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | | US0_CS #2 | LES_CH8 #0 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 42 | PC9 | ACMP1_CH1 | | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 43 | PC10 | ACMP1_CH2 | | US0_RX #2 | LES_CH10 #0 |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| 45 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | CMU_CLK0 #1 LES_CH12 #0 |
| 46 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 47 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 48 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 49 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| 50 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 |
| 51 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | PF3 | | | | PRS_CH0 #1 |
| 53 | PF4 | | | | PRS_CH1 #1 |
| 54 | PF5 | | | | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | | | | PRS_CH3 #1 |
| 57 | PE9 | | | | |
| 58 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------|--|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 60 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 61 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 62 | PE14 | | | LEU0_TX #2 | |
| 63 | PE15 | | | LEU0_RX #2 | |
| 64 | PA15 | | | | |

5.6.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.17. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|----------------------------|----------|---|-----|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | Description |
|------------------------------------|----------|------|------|------|-----|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | |
| ADC0_CH7 | PD7 | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0/ OPAMP_N0 | PC5 | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT/ OPAMP_OUT0 ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1/ OPAMP_OUT1 | PB12 | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT/ OPAMP_OUT1 ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | Operational Amplifier 2 output. |
| DAC0_P0/ OPAMP_P0 | PC4 | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | Description |
|-------------|----------|------|------|-----|-----|-----|------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|------|------|------|------|------|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.6.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG230 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.18. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | PA15 | - | - | - | - | PA10 | PA9 | PA8 | - | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | PB12 | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.6.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG230 is shown in the following figure.

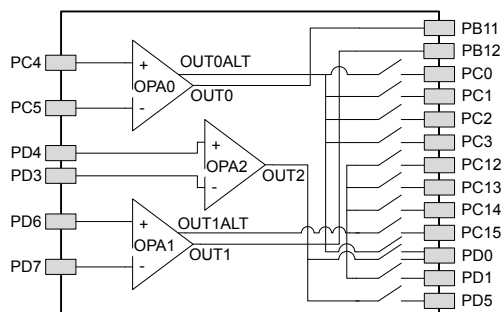


Figure 5.11. Opamp Pinout

5.7 EFM32TG232 (TQFP64)

5.7.1 Pinout

The EFM32TG232 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

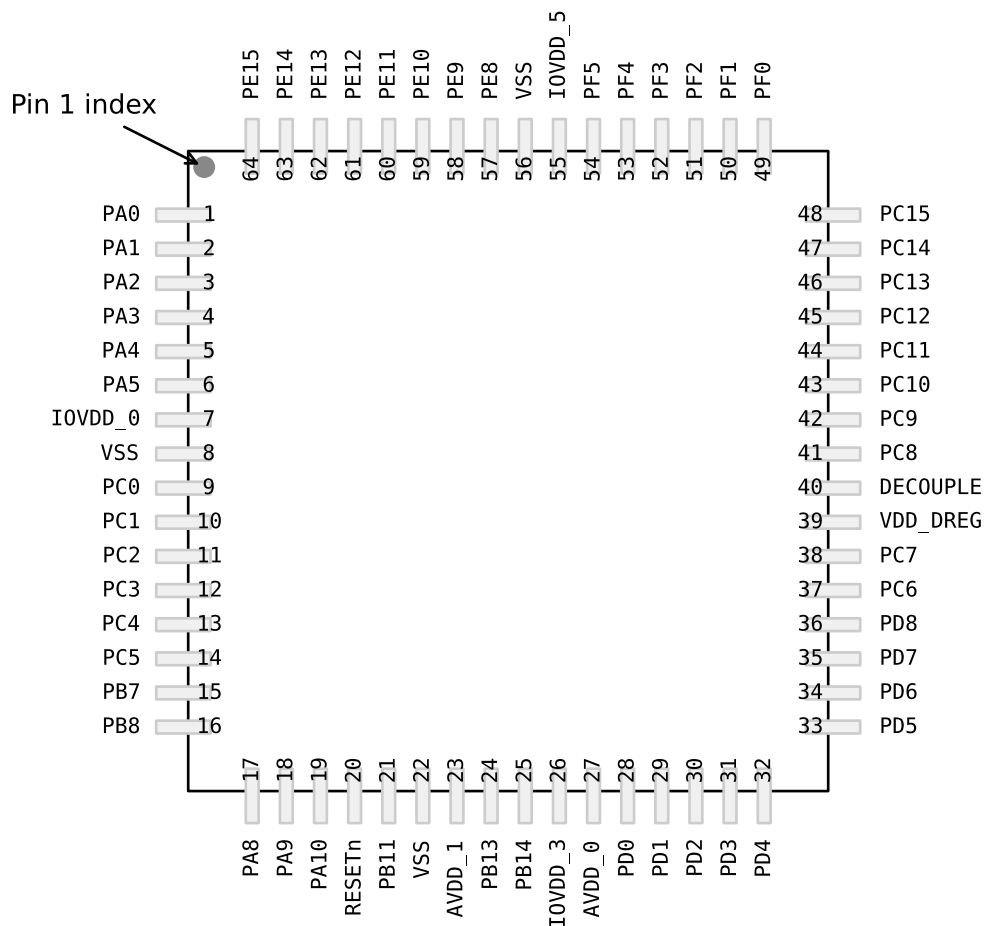


Figure 5.12. EFM32TG232 Pinout (top view, not to scale)

Table 5.19. Device Pinout

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|---------------------------------------|--------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PA3 | | | | LES_ALTEX2 #0 |
| 5 | PA4 | | | | LES_ALTEX3 #0 |
| 6 | PA5 | | | | LES_ALTEX4 #0 |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 10 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 11 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | | | LES_CH2 #0 |
| 12 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | | | LES_CH3 #0 |
| 13 | PC4 | ACMP0_CH4 DAC0_P0/ OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0/ OPAMP_N0 | LETIM0_OUT1 #3 | | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA8 | | | | |
| 18 | PA9 | | | | |
| 19 | PA10 | | | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|----------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 35 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | I2C0_SDA #2 | LES_CH6 #0 |
| 38 | PC7 | ACMP0_CH7 | | I2C0_SCL #2 | LES_CH7 #0 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 41 | PC8 | ACMP1_CH0 | | US0_CS #2 | LES_CH8 #0 |
| 42 | PC9 | ACMP1_CH1 | | US0_CLK #2 | LES_CH9 #0 GPIO_EM4WU2 |
| 43 | PC10 | ACMP1_CH2 | | US0_RX #2 | LES_CH10 #0 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 44 | PC11 | ACMP1_CH3 | | US0_TX #2 | LES_CH11 #0 |
| 45 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | CMU_CLK0 #1 LES_CH12 #0 |
| 46 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 47 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 48 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 49 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| 50 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 |
| 51 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | PF3 | | | | PRS_CH0 #1 |
| 53 | PF4 | | | | PRS_CH1 #1 |
| 54 | PF5 | | | | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | | | | PRS_CH3 #1 |
| 58 | PE9 | | | | |
| 59 | PE10 | | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 60 | PE11 | | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 61 | PE12 | | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--------|---------------------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 62 | PE13 | | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 63 | PE14 | | | LEU0_TX #2 | |
| 64 | PE15 | | | LEU0_RX #2 | |

5.7.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.20. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|----------------------------|----------|---|-----|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | Description |
|------------------------------------|----------|------|------|------|-----|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | |
| ADC0_CH7 | PD7 | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0/ OPAMP_N0 | PC5 | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT/ OPAMP_OUT0 ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT/ OPAMP_OUT1 ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | Operational Amplifier 2 output. |
| DAC0_P0/ OPAMP_P0 | PC4 | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | Pin can be used to wake the system up from EM4 |
| HFX TAL_N | PB14 | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |

| Alternate | LOCATION | | | | | | | Description |
|-------------|----------|------|------|-----|-----|-----|------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|------|------|------|------|------|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.7.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG232 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.21. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | - | - | - | - | PA10 | PA9 | PA8 | - | - | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.7.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG232 is shown in the following figure.



Figure 5.13. Opamp Pinout

5.8 EFM32TG822 (TQFP48)

5.8.1 Pinout

The EFM32TG822 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

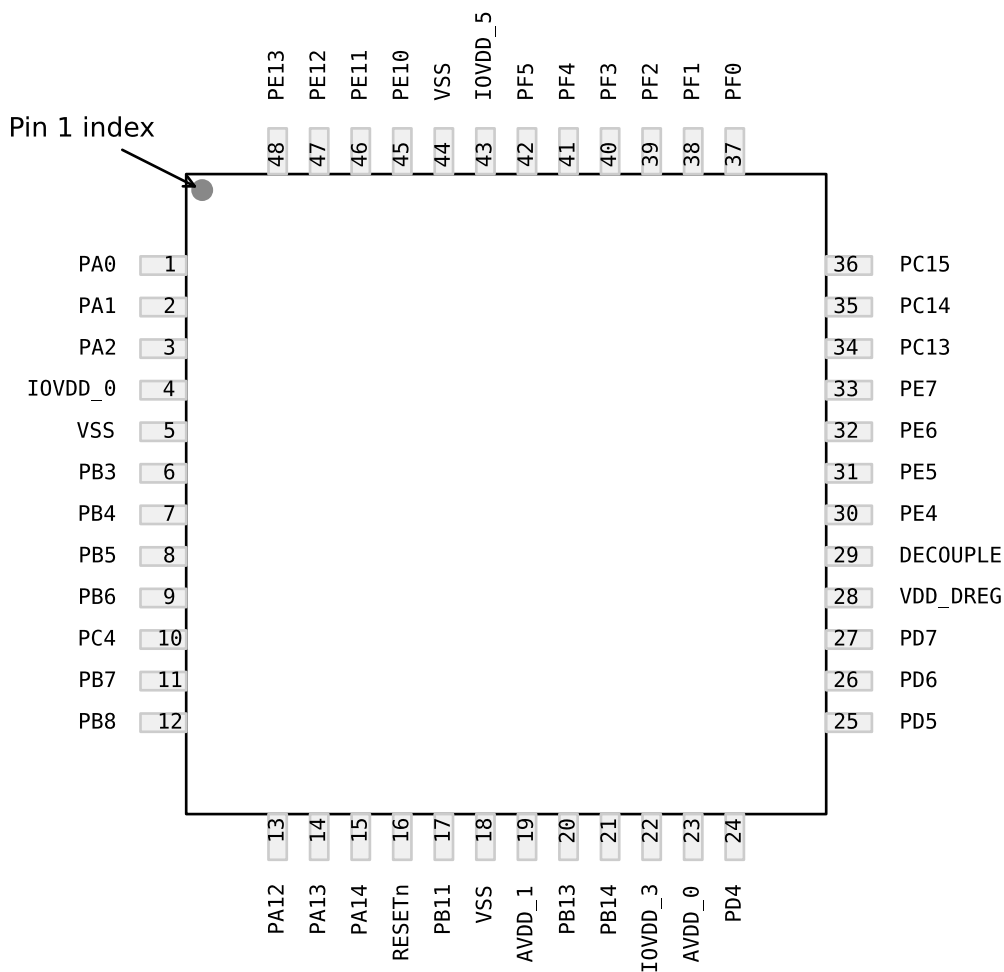


Figure 5.14. EFM32TG822 Pinout (top view, not to scale)

Table 5.22. Device Pinout

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|----------------------------|------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | IOVDD_0 | Digital IO power supply 0. | | | |
| 5 | VSS | Ground. | | | |
| 6 | PB3 | LCD_SEG20/ LCD_COM4 | | | |
| 7 | PB4 | LCD_SEG21/ LCD_COM5 | | | |
| 8 | PB5 | LCD_SEG22/ LCD_COM6 | | | |
| 9 | PB6 | LCD_SEG23/ LCD_COM7 | | | |
| 10 | PC4 | ACMP0_CH4 DAC0_P0/ OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| 11 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 12 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 13 | PA12 | LCD_BCAP_P | | | |
| 14 | PA13 | LCD_BCAP_N | | | |
| 15 | PA14 | LCD_BEXT | | | |
| 16 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 17 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| 18 | VSS | Ground. | | | |
| 19 | AVDD_1 | Analog power supply 1. | | | |
| 20 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 21 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 22 | IOVDD_3 | Digital IO power supply 3. | | | |
| 23 | AVDD_0 | Analog power supply 0. | | | |
| 24 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |
| 25 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 26 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 27 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 28 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 29 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 30 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 31 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 32 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 33 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 34 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 35 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 36 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 37 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| 38 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 |
| 39 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 40 | PF3 | LCD_SEG1 | | | PRS_CH0 #1 |
| 41 | PF4 | LCD_SEG2 | | | PRS_CH1 #1 |
| 42 | PF5 | LCD_SEG3 | | | PRS_CH2 #1 |
| 43 | IOVDD_5 | Digital IO power supply 5. | | | |
| 44 | VSS | Ground. | | | |

| QFP48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------|--|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 45 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 46 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 47 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 48 | PE13 | LCD_SEG9 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |

5.8.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.23. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|------------------------------------|----------|------|------|------|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT1ALT/ OPAMP_OUT1 ALT | | PC13 | PC14 | PC15 | | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | | | | | | | Operational Amplifier 2 output. |
| DAC0_P0/ OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |

| Alternate | LOCATION | | | | | | Description | |
|-------------|----------|------|---|---|---|-----|-------------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | | 6 |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFX TAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |

| Alternate | LOCATION | | | | | | | Description |
|------------------------|----------|------|-----|-----|-----|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|------|-----|------|------|------|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | PE12 | PB8 | | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | PE13 | PB7 | | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | | | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.8.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG822 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.24. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | PA14 | PA13 | PA12 | - | - | - | - | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | - | - | - |
| Port C | PC15 | PC14 | PC13 | - | - | - | - | - | - | - | - | PC4 | - | - | - | - |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | PE7 | PE6 | PE5 | PE4 | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.8.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG822 is shown in the following figure.

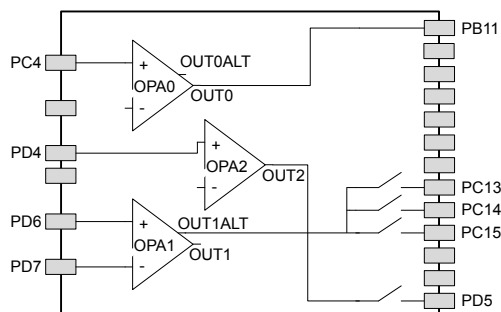


Figure 5.15. Opamp Pinout

5.9 EFM32TG825 (BGA48)

5.9.1 Pinout

The EFM32TG825 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

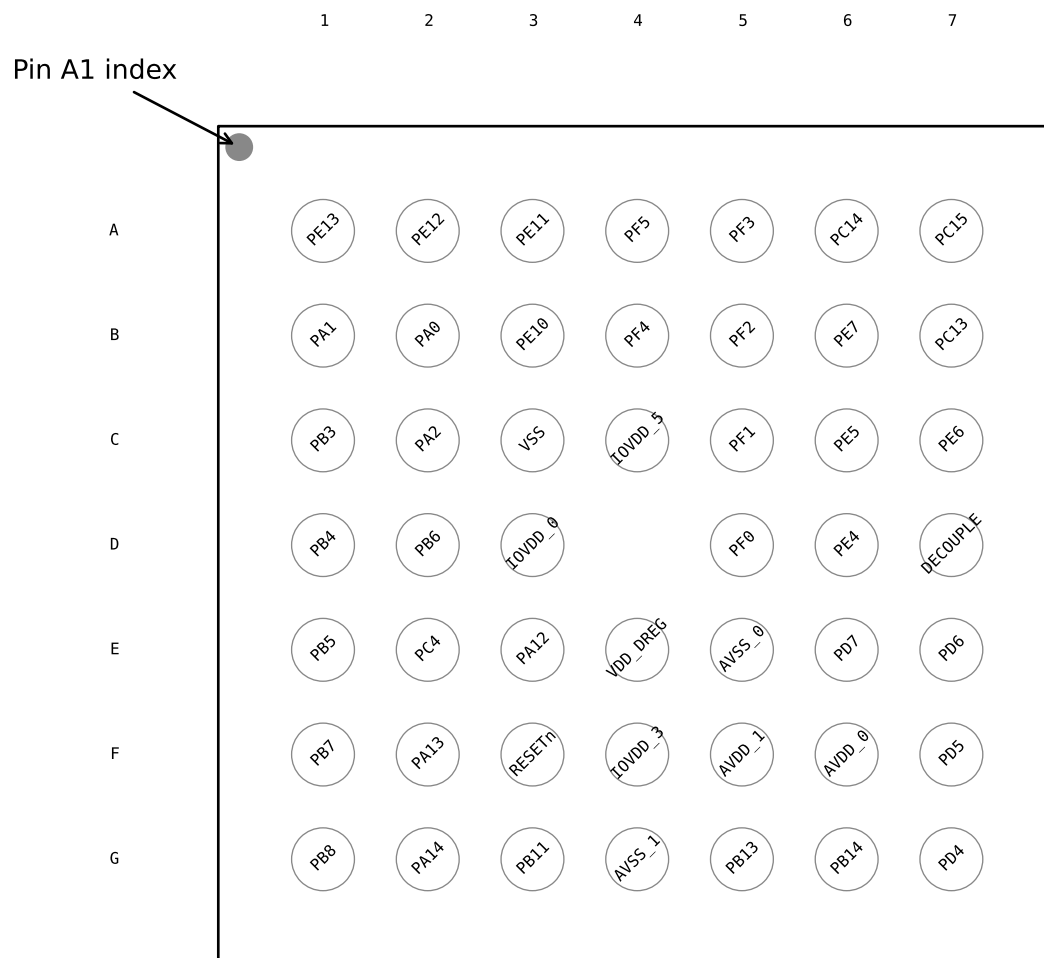


Figure 5.16. EFM32TG825 Pinout (top view, not to scale)

Table 5.25. Device Pinout

| BGA48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--------|---------------------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| A1 | PE13 | LCD_SEG9 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |

| BGA48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|---|--|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| A2 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| A3 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| A4 | PF5 | LCD_SEG3 | | | PRS_CH2 #1 |
| A5 | PF3 | LCD_SEG1 | | | PRS_CH0 #1 |
| A6 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| A7 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| B1 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| B2 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| B3 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| B4 | PF4 | LCD_SEG2 | | | PRS_CH1 #1 |
| B5 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| B6 | PE7 | LCD_COM3 | | US0_TX #1 | |
| B7 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| C1 | PB3 | LCD_SEG20/ LCD_COM4 | | | |
| C2 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| C3 | VSS | Ground. | | | |
| C4 | IOVDD_5 | Digital IO power supply 5. | | | |
| C5 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWIO #0/1 GPIO_EM4WU3 |
| C6 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| C7 | PE6 | LCD_COM2 | | US0_RX #1 | |

| BGA48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| D1 | PB4 | LCD_SEG21/ LCD_COM5 | | | |
| D2 | PB6 | LCD_SEG23/ LCD_COM7 | | | |
| D3 | IOVDD_0 | Digital IO power supply 0. | | | |
| D5 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| D6 | PE4 | LCD_COM0 | | US0_CS #1 | |
| D7 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| E1 | PB5 | LCD_SEG22/ LCD_COM6 | | | |
| E2 | PC4 | ACMP0_CH4 DAC0_P0/ OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| E3 | PA12 | LCD_BCAP_P | | | |
| E4 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| E5 | AVSS_0 | Analog ground 0. | | | |
| E6 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| E7 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| F1 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| F2 | PA13 | LCD_BCAP_N | | | |
| F3 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| F4 | IOVDD_3 | Digital IO power supply 3. | | | |
| F5 | AVDD_1 | Analog power supply 1. | | | |
| F6 | AVDD_0 | Analog power supply 0. | | | |
| F7 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |
| G1 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |

| BGA48 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|----------------------------|-------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| G2 | PA14 | LCD_BEXT | | | |
| G3 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| G4 | AVSS_1 | Analog ground 1. | | | |
| G5 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| G6 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| G7 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |

5.9.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.26. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|------------------------------------|----------|------|------|------|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT1ALT/ OPAMP_OUT1 ALT | | PC13 | PC14 | PC15 | | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | | | | | | | Operational Amplifier 2 output. |
| DAC0_P0/ OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |

| Alternate | LOCATION | | | | | | Description | |
|-------------|----------|------|---|---|---|-----|-------------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | | 6 |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFX TAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |

| Alternate | LOCATION | | | | | | | Description |
|------------------------|----------|------|-----|-----|-----|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|------|-----|------|------|------|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | | | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | | | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | PE12 | PB8 | | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | PE13 | PB7 | | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | | | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.9.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG825 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.27. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | PA14 | PA13 | PA12 | - | - | - | - | - | - | - | - | - | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | - | - | - |
| Port C | PC15 | PC14 | PC13 | - | - | - | - | - | - | - | - | PC4 | - | - | - | - |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | PD5 | PD4 | - | - | - | - |
| Port E | - | - | PE13 | PE12 | PE11 | PE10 | - | - | PE7 | PE6 | PE5 | PE4 | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.9.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG825 is shown in the following figure.

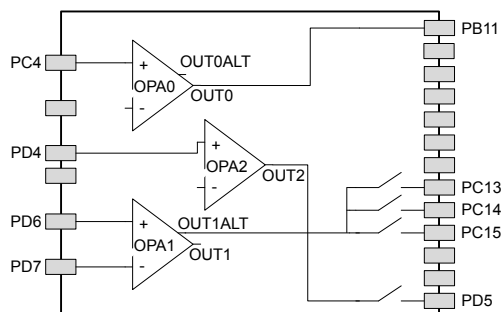


Figure 5.17. Opamp Pinout

5.10 EFM32TG840 (QFN64)

5.10.1 Pinout

The EFM32TG840 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

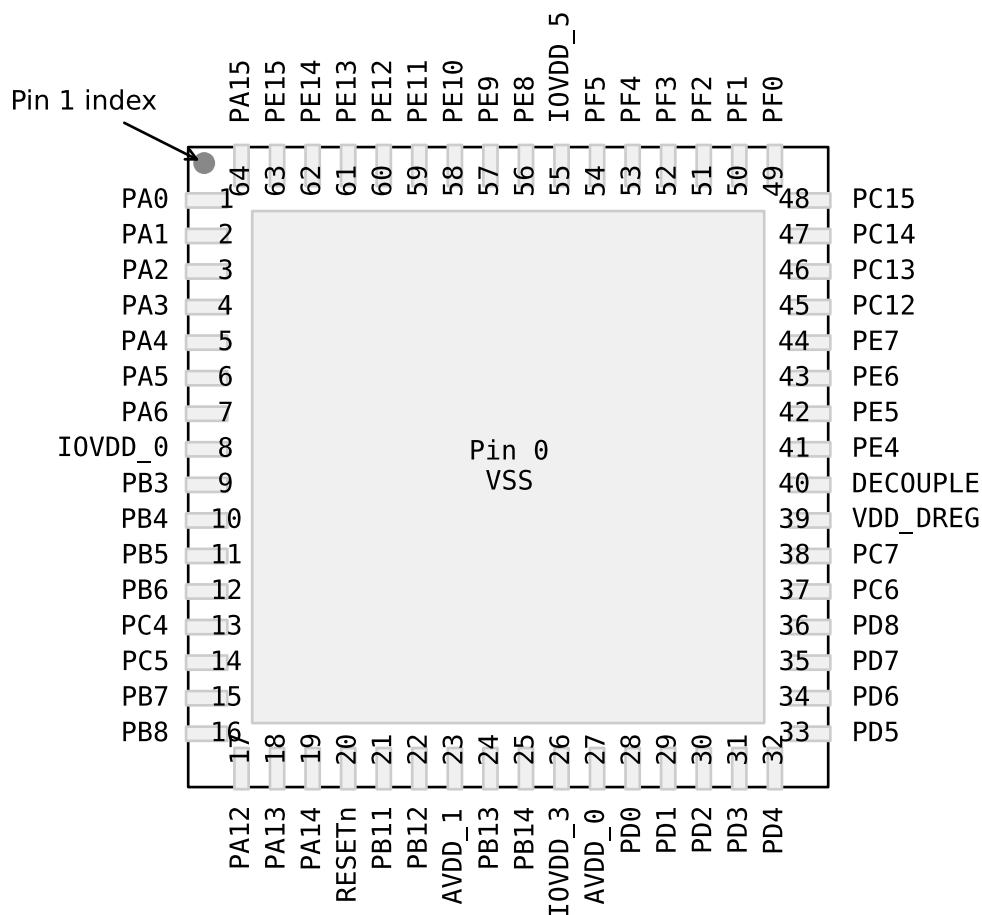


Figure 5.18. EFM32TG840 Pinout (top view, not to scale)

Table 5.28. Device Pinout

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|----------------------------|---------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PA3 | LCD_SEG16 | | | LES_ALTEX2 #0 |
| 5 | PA4 | LCD_SEG17 | | | LES_ALTEX3 #0 |
| 6 | PA5 | LCD_SEG18 | | | LES_ALTEX4 #0 |
| 7 | PA6 | LCD_SEG19 | | | GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PB3 | LCD_SEG20/ LCD_COM4 | | | |
| 10 | PB4 | LCD_SEG21/ LCD_COM5 | | | |
| 11 | PB5 | LCD_SEG22/ LCD_COM6 | | | |
| 12 | PB6 | LCD_SEG23/ LCD_COM7 | | | |
| 13 | PC4 | ACMP0_CH4 DAC0_P0/ OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N0/ OPAMP_N0 | LETIM0_OUT1 #3 | | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | | | |
| 18 | PA13 | LCD_BCAP_N | | | |
| 19 | PA14 | LCD_BEXT | | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| 22 | PB12 | DAC0_OUT1/ OPAMP_OUT1 | LETIM0_OUT1 #1 | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|---------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 35 | PD7 | ADC0_CH7 DAC0_P1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | I2C0_SDA #2 | LES_CH6 #0 |
| 38 | PC7 | ACMP0_CH7 | | I2C0_SCL #2 | LES_CH7 #0 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|---|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 45 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | CMU_CLK0 #1 LES_CH12 #0 |
| 46 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 47 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 48 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 49 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| 50 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 |
| 51 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | PF3 | LCD_SEG1 | | | PRS_CH0 #1 |
| 53 | PF4 | LCD_SEG2 | | | PRS_CH1 #1 |
| 54 | PF5 | LCD_SEG3 | | | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | LCD_SEG4 | | | PRS_CH3 #1 |
| 57 | PE9 | LCD_SEG5 | | | |
| 58 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 60 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 61 | PE13 | LCD_SEG9 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--------|---------------|-------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 62 | PE14 | LCD_SEG10 | | LEU0_TX #2 | |
| 63 | PE15 | LCD_SEG11 | | LEU0_RX #2 | |
| 64 | PA15 | LCD_SEG12 | | | |

5.10.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.29. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|----------------------------|----------|------|------|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0/ OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |

| Alternate | LOCATION | | | | | | Description | |
|------------------------------------|----------|------|------|------|-----|-----|-------------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | | 6 |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT/ OPAMP_OUT0 ALT | | | | | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1/ OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT/ OPAMP_OUT1 ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| DAC0_P0/ OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFX TAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFX TAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |

| Alternate | LOCATION | | | | | | Description | |
|------------|----------|---|---|---|---|---|-------------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | | 6 |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |

| Alternate | LOCATION | | | | | | | Description |
|------------------------|----------|------|------|-----|-----|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG19 | PA6 | | | | | | | LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|------|------|------|------|------|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | PE12 | PB8 | | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | PE13 | PB7 | | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | | PD1 | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | PD0 | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.10.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG840 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.30. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | PA15 | PA14 | PA13 | PA12 | - | - | - | - | - | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | PB12 | PB11 | - | - | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | - | - | - |
| Port C | PC15 | PC14 | PC13 | PC12 | - | - | - | - | PC7 | PC6 | PC5 | PC4 | - | - | - | - |
| Port D | - | - | - | - | - | - | - | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.10.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG840 is shown in the following figure.

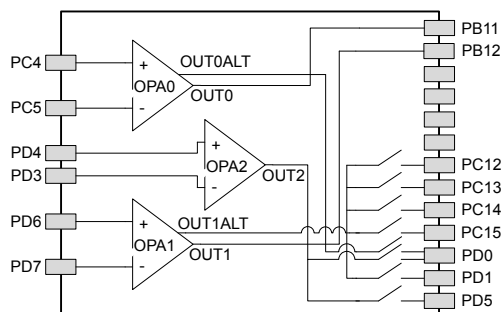


Figure 5.19. Opamp Pinout

5.11 EFM32TG842 (TQFP64)

5.11.1 Pinout

The EFM32TG842 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

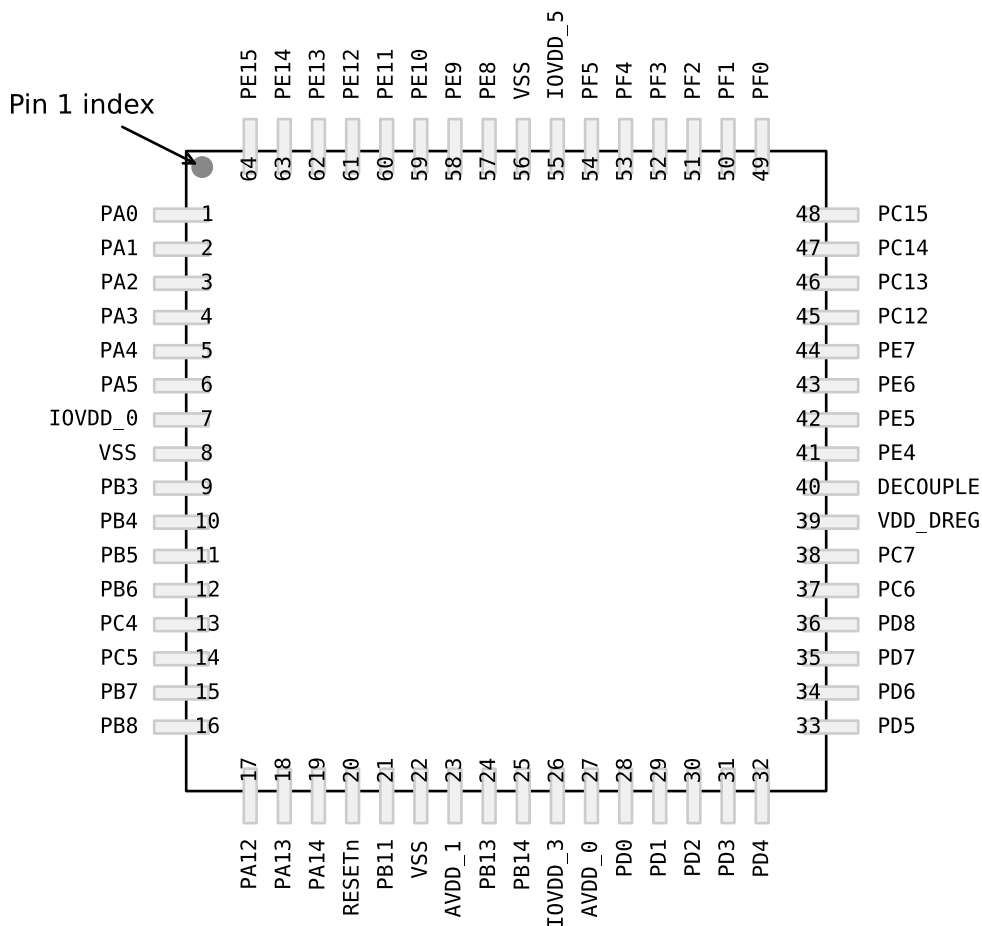


Figure 5.20. EFM32TG842 Pinout (top view, not to scale)

Table 5.31. Device Pinout

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-----------------|---------------------------|---------------------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|-------------------------------|----------------------------|---------------|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 4 | PA3 | LCD_SEG16 | | | LES_ALTEX2 #0 |
| 5 | PA4 | LCD_SEG17 | | | LES_ALTEX3 #0 |
| 6 | PA5 | LCD_SEG18 | | | LES_ALTEX4 #0 |
| 7 | IOVDD_0 | Digital IO power supply 0. | | | |
| 8 | VSS | Ground. | | | |
| 9 | PB3 | LCD_SEG20/ LCD_COM4 | | | |
| 10 | PB4 | LCD_SEG21/ LCD_COM5 | | | |
| 11 | PB5 | LCD_SEG22/ LCD_COM6 | | | |
| 12 | PB6 | LCD_SEG23/ LCD_COM7 | | | |
| 13 | PC4 | ACMP0_CH4 DAC0_P0/ OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 DAC0_N1/ OPAMP_N0 | LETIM0_OUT1 #3 | | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | | | |
| 18 | PA13 | LCD_BCAP_N | | | |
| 19 | PA14 | LCD_BEXT | | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0/ OPAMP_OUT0 | TIM1_CC2 #3 LETIM0_OUT0 #1 | | |
| 22 | VSS | Ground. | | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5 LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5 LEU0_RX #1 | |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|---|--|--------------------------|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1 | | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT | TIM0_CC0 #3 | US1_RX #1 | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | US1_CLK #1 | |
| 31 | PD3 | ADC0_CH3 OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | |
| 32 | PD4 | ADC0_CH4 OPAMP_P2 | | LEU0_TX #0 | |
| 33 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | LEU0_RX #0 | |
| 34 | PD6 | ADC0_CH6 DAC0_P1/ OPAMP_P1 | TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 |
| 35 | PD7 | ADC0_CH7 DAC0_N1/ OPAMP_N1 | TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 |
| 36 | PD8 | | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | I2C0_SDA #2 | LES_CH6 #0 |
| 38 | PC7 | ACMP0_CH7 | | I2C0_SCL #2 | LES_CH7 #0 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 45 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | CMU_CLK0 #1 LES_CH12 #0 |

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---------------------|----------|--|---|---|--|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 46 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | | LES_CH13 #0 |
| 47 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 | LES_CH14 #0 |
| 48 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | TIM1_CC2 #0 | US0_CLK #3 | LES_CH15 #0 DBG_SWO #1 |
| 49 | PF0 | | TIM0_CC0 #5 LETIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1 |
| 50 | PF1 | | TIM0_CC1 #5 LETIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1 GPIO_EM4WU3 |
| 51 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| 52 | PF3 | LCD_SEG1 | | | PRS_CH0 #1 |
| 53 | PF4 | LCD_SEG2 | | | PRS_CH1 #1 |
| 54 | PF5 | LCD_SEG3 | | | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | VSS | Ground. | | | |
| 57 | PE8 | LCD_SEG4 | | | PRS_CH3 #1 |
| 58 | PE9 | LCD_SEG5 | | | |
| 59 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 60 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| 61 | PE12 | LCD_SEG8 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| 62 | PE13 | LCD_SEG9 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| 63 | PE14 | LCD_SEG10 | | LEU0_TX #2 | |
| 64 | PE15 | LCD_SEG11 | | LEU0_RX #2 | |

5.11.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.32. Alternate functionality overview

| Alternate Functionality | LOCATION | | | | | | | Description |
|----------------------------|----------|------|------|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0/ OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1/ OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |

| Alternate | LOCATION | | | | | | | Description |
|------------------------------------|----------|------|------|------|-----|-----|------|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0/ OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT/ OPAMP_OUT0 ALT | | | | | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1ALT/ OPAMP_OUT1 ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| DAC0_P0/ OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1/ OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|---|---|---|---|---|---|--|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_BEXT | PA14 | | | | | | | <p>LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.</p> <p>An external LCD voltage may also be applied to this pin if the booster is not enabled.</p> <p>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.</p> |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |

| Alternate | LOCATION | | | | | | | Description |
|------------------------|----------|------|------|-----|-----|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | |
| LCD_SEG18 | PA5 | | | | | | | LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG20/ LCD_COM4 | PB3 | | | | | | | LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4 |
| LCD_SEG21/ LCD_COM5 | PB4 | | | | | | | LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5 |
| LCD_SEG22/ LCD_COM6 | PB5 | | | | | | | LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6 |
| LCD_SEG23/ LCD_COM7 | PB6 | | | | | | | LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7 |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exit output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exit output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exit output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exit output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exit output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exit output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exit output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exit output 7. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | | PD6 | | | | Pulse Counter PCNT0 input number 0. |

| Alternate | LOCATION | | | | | | | |
|---------------|----------|------|-----|------|------|------|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| PCNT0_S1IN | PC14 | | | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | PE5 | | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | | PE12 | PB8 | | | USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | | PE13 | PB7 | | | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | | PD1 | PD6 | | | | | USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | | PD0 | PD7 | | | | | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI). |

5.11.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32TG842 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.33. GPIO Pinout

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Port A | - | PA14 | PA13 | PA12 | - | - | - | - | - | - | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | - | - | - |
| Port C | PC15 | PC14 | PC13 | PC12 | - | - | - | - | PC7 | PC6 | PC5 | PC4 | - | - | - | - |
| Port D | - | - | - | - | - | - | - | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

5.11.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32TG842 is shown in the following figure.

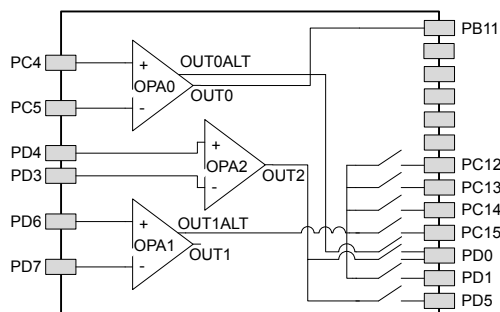
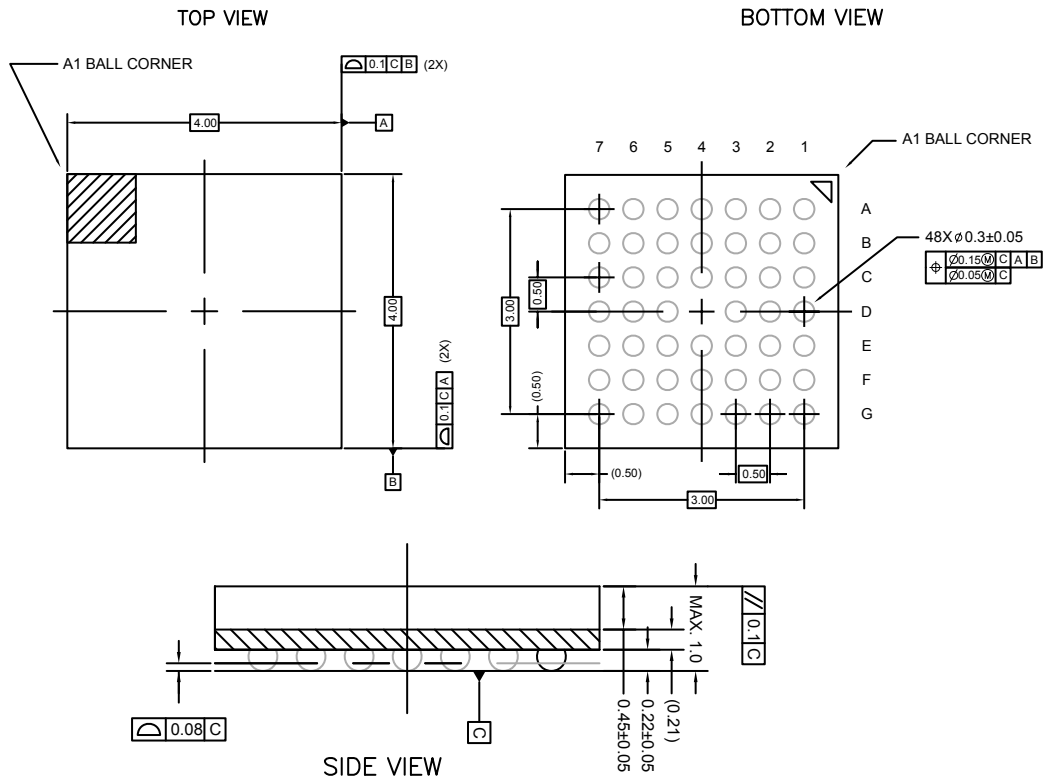


Figure 5.21. Opamp Pinout

6. BGA48 Package Specifications

6.1 BGA48 Package Dimensions



Rev: 97SP01420A_X01_24/FEB2012

Figure 6.1. BGA48

Note:

1. The dimensions in parenthesis are reference.
2. Datum 'C' and seating plane are defined by the crown of the solder balls.
3. All dimensions are in millimeters.

6.2 BGA48 PCB Layout

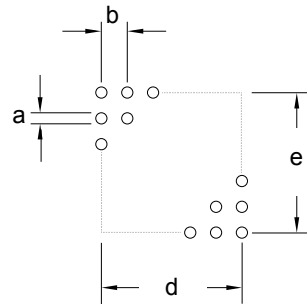


Figure 6.2. BGA48 PCB Land Pattern

Table 6.1. BGA48 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Row name and column number |
|--------|-----------|--------|----------------------------|
| a | 0.25 | r1 | A |
| b | 0.50 | m | G |
| d | 3.00 | c1 | 1 |
| e | 3.00 | cn | 7 |

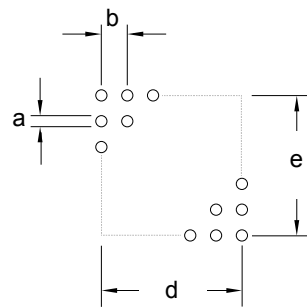


Figure 6.3. BGA48 PCB Solder Mask

Table 6.2. BGA48 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.28 |
| b | 0.50 |
| d | 3.00 |
| e | 3.00 |



Figure 6.4. BGA48 PCB Stencil Design

Table 6.3. BGA48 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.25 |
| b | 0.50 |
| d | 3.00 |
| e | 3.00 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

6.3 BGA48 Package Marking

In the illustration below package fields and position are shown.

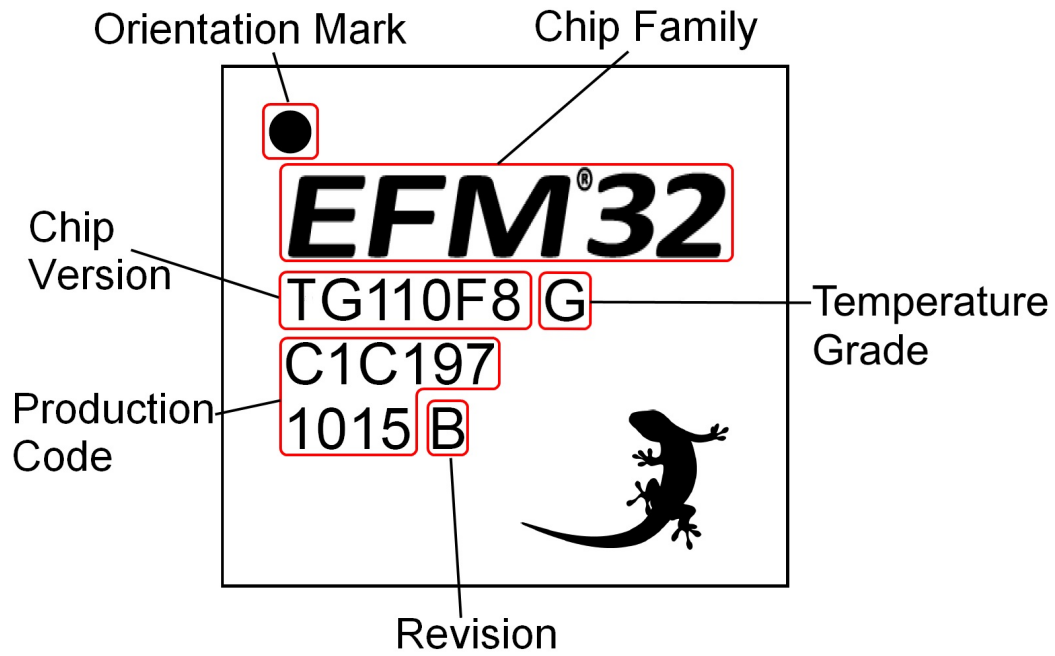


Figure 6.5. Example Chip Marking (Top View)

7. QFN24 Package Specifications

7.1 QFN24 Package Dimensions

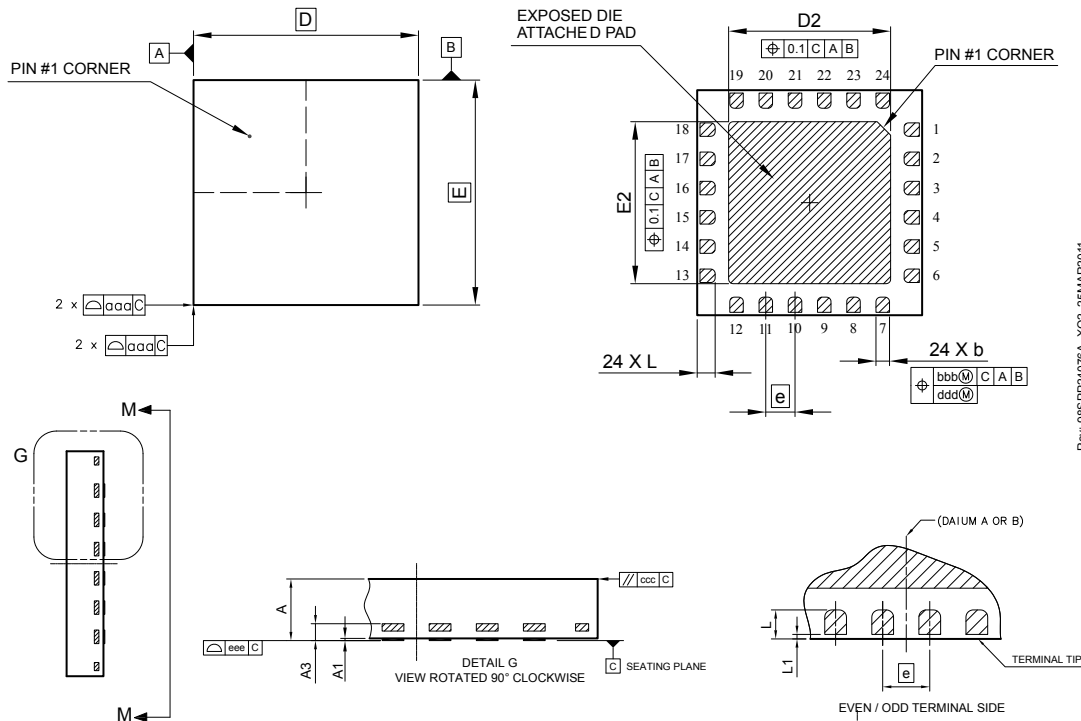


Figure 7.1. QFN24

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 7.1. QFN (Dimensions in mm)

| Symbol | A | A1 | A3 | b | D | E | D2 | E2 | e | L | L1 | aaa | bbb | ccc | ddd | eee | |
|--------|------|------|--------------|------|-------------|-------------|------|------|-------------|------|------|------|------|------|------|------|------|
| Min | 0.80 | 0.00 | 0.203 REF | 0.25 | 5.00 BSC | 5.00 BSC | 3.50 | 3.50 | 0.65 BSC | 0.35 | 0.00 | 0.10 | 0.10 | 0.10 | 0.05 | 0.08 | |
| Nom | 0.85 | — | | 0.30 | | | 3.60 | 3.60 | | | | | | | | | 0.40 |
| Max | 0.90 | 0.05 | | 0.35 | | | 3.70 | 3.70 | | | | | | | | | 0.45 |

The QFN24 package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

7.2 QFN24 PCB Layout

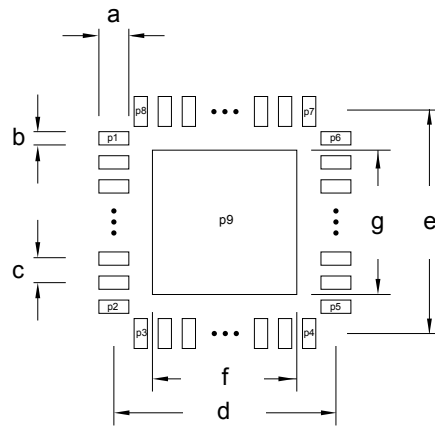


Figure 7.2. QFN24 PCB Land Pattern

Table 7.2. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 0.80 | P1 | 1 | P8 | 24 |
| b | 0.30 | P2 | 6 | P9 | 0 |
| c | 0.65 | P3 | 7 | - | - |
| d | 5.00 | P4 | 12 | - | - |
| e | 5.00 | P5 | 13 | - | - |
| f | 3.60 | P6 | 18 | - | - |
| g | 3.60 | P7 | 19 | - | - |

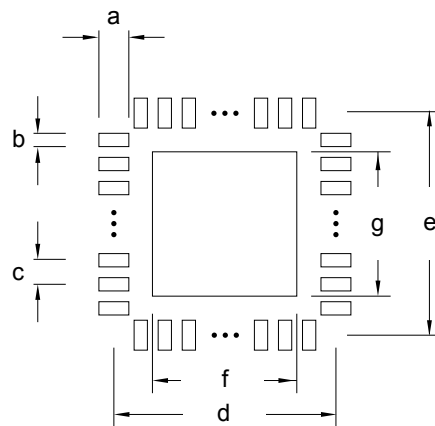


Figure 7.3. QFN24 PCB Solder Mask

Table 7.3. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.92 |
| b | 0.42 |
| c | 0.65 |

| Symbol | Dim. (mm) |
|--------|-----------|
| d | 5.00 |
| e | 5.00 |
| f | 3.72 |
| g | 3.72 |

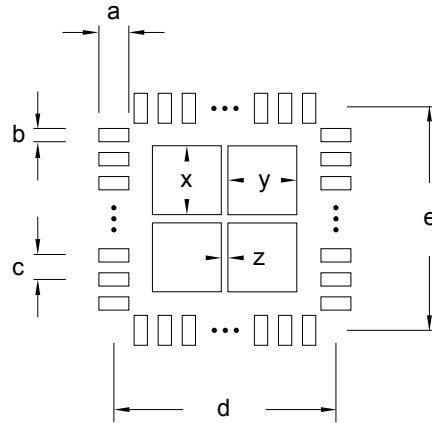


Figure 7.4. QFN24 PCB Stencil Design

Table 7.4. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.60 |
| b | 0.25 |
| c | 0.65 |
| d | 5.00 |
| e | 5.00 |
| x | 1.00 |
| y | 1.00 |
| z | 0.50 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

7.3 QFN24 Package Marking

In the illustration below package fields and position are shown.

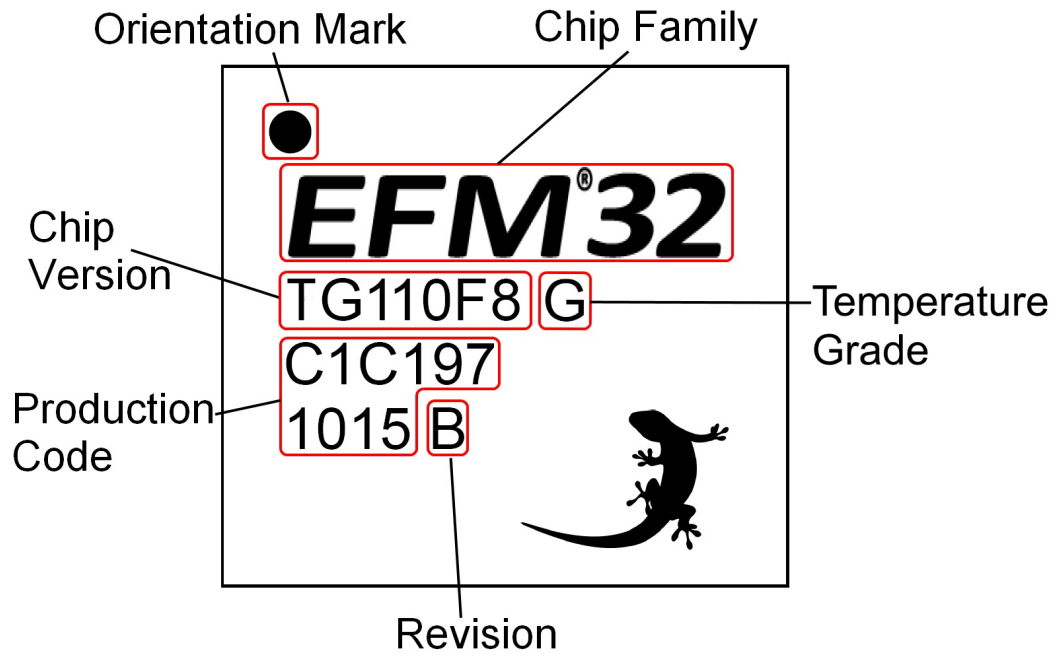
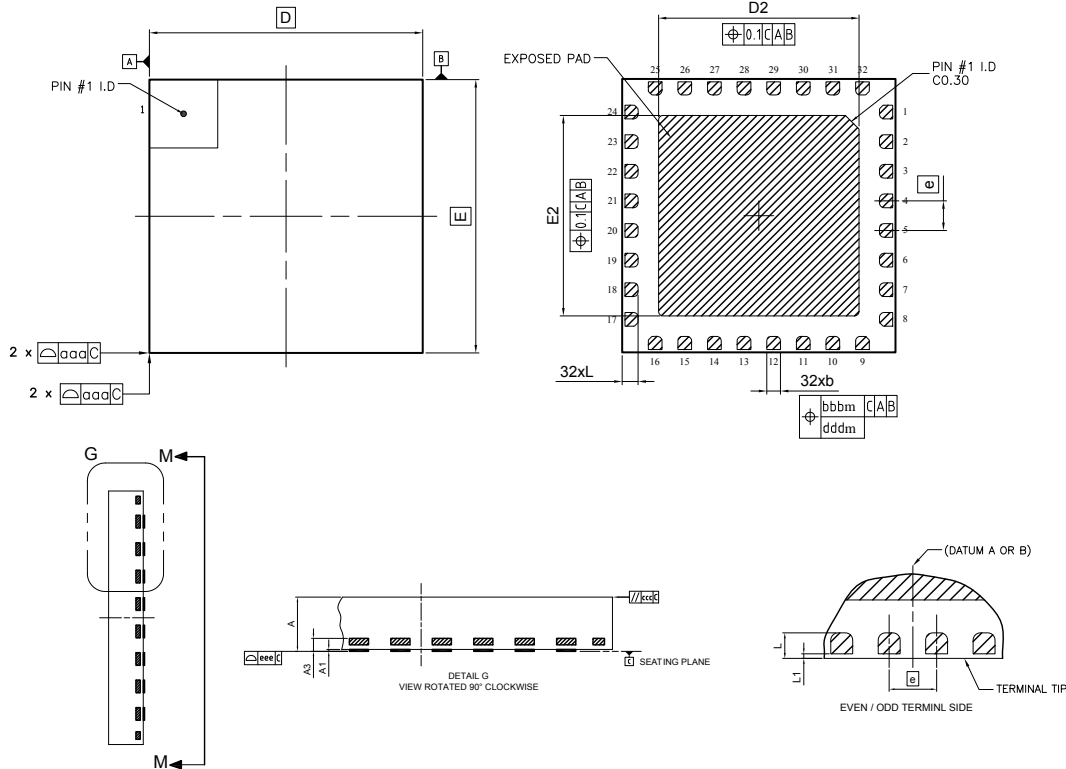


Figure 7.5. Example Chip Marking (Top View)

8. QFN32 Package Specifications

8.1 QFN32 Package Dimensions



Rev: 98SP2088A_X01_10MAR2011

Figure 8.1. QFN32

- Note:**
1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
 2. All dimensions are in millimeters. Angles are in degrees.
 3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
 4. Coplanarity applies to the exposed heat slug as well as the terminal.
 5. Radius on terminal is optional.

Table 8.1. QFN32 (Dimensions in mm)

| Symbol | A | A1 | A3 | b | D | E | D2 | E2 | e | L | L1 | aaa | bbb | ccc | ddd | eee |
|--------|------|------|--------------|------|-------------|-------------|------|------|-------------|------|------|------|------|------|------|------|
| Min | 0.80 | 0.00 | 0.203 REF | 0.25 | 6.00 BSC | 6.00 BSC | 4.30 | 4.30 | 0.65 BSC | 0.35 | 0.00 | 0.10 | 0.10 | 0.10 | 0.05 | 0.08 |
| Nom | 0.85 | — | | 0.30 | | | 4.40 | 4.40 | | 0.40 | | | | | | |
| Max | 0.90 | 0.05 | | 0.35 | | | 4.50 | 4.50 | | 0.45 | 0.10 | | | | | |

The QFN32 package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

8.2 QFN32 PCB Layout

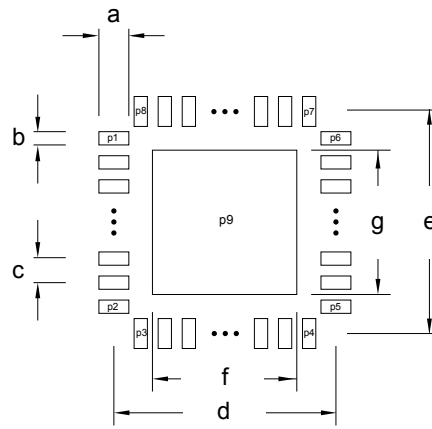


Figure 8.2. QFN32 PCB Land Pattern

Table 8.2. QFN32 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 0.80 | P1 | 1 | P6 | 24 |
| b | 0.35 | P2 | 8 | P7 | 25 |
| c | 0.65 | P3 | 9 | P8 | 32 |
| d | 6.00 | P4 | 16 | P9 | 0 |
| e | 6.00 | P5 | 17 | | |
| f | 4.40 | | | | |
| g | 4.40 | | | | |

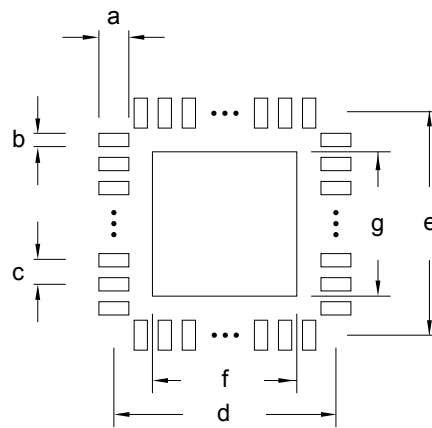


Figure 8.3. QFN32 PCB Solder Mask

Table 8.3. QFN32 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.92 |
| b | 0.47 |
| c | 0.65 |
| d | 6.00 |
| e | 6.00 |
| f | 4.52 |
| g | 4.52 |

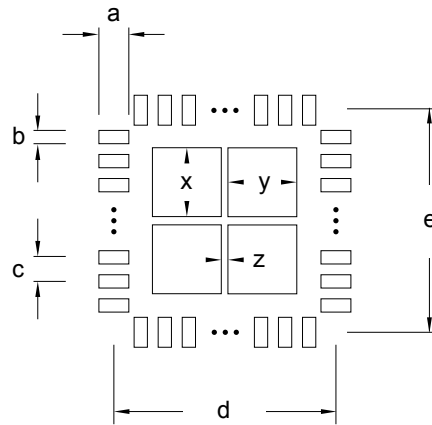


Figure 8.4. QFN32 PCB Stencil Design

Table 8.4. QFN32 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 0.70 |
| b | 0.25 |
| c | 0.65 |
| d | 6.00 |
| e | 6.00 |
| x | 1.30 |
| y | 1.30 |
| z | 0.50 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

8.3 QFN32 Package Marking

In the illustration below package fields and position are shown.

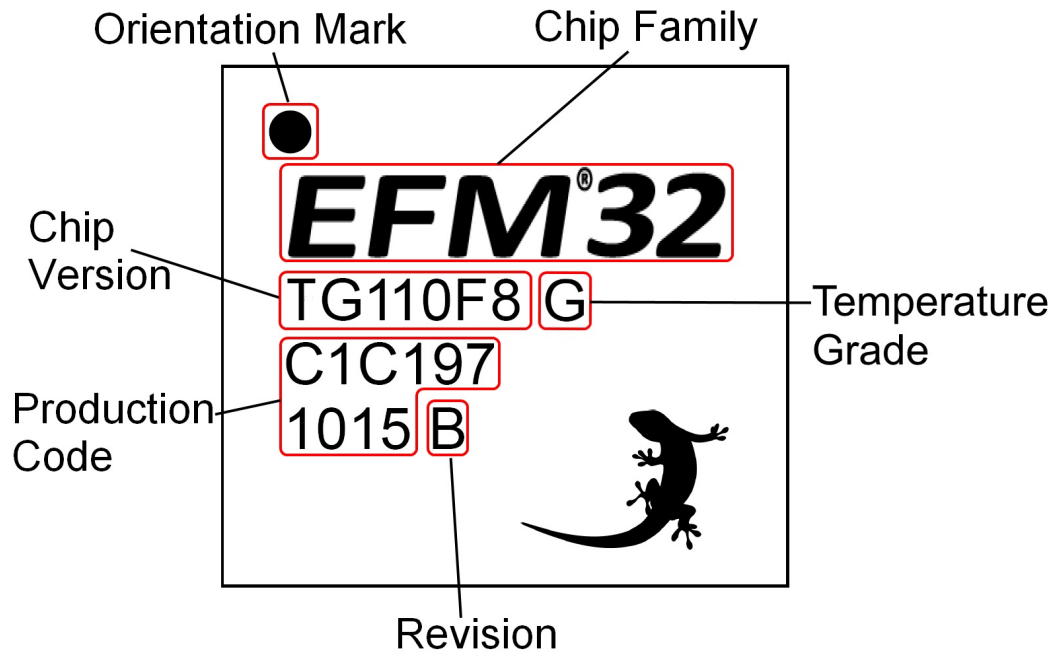
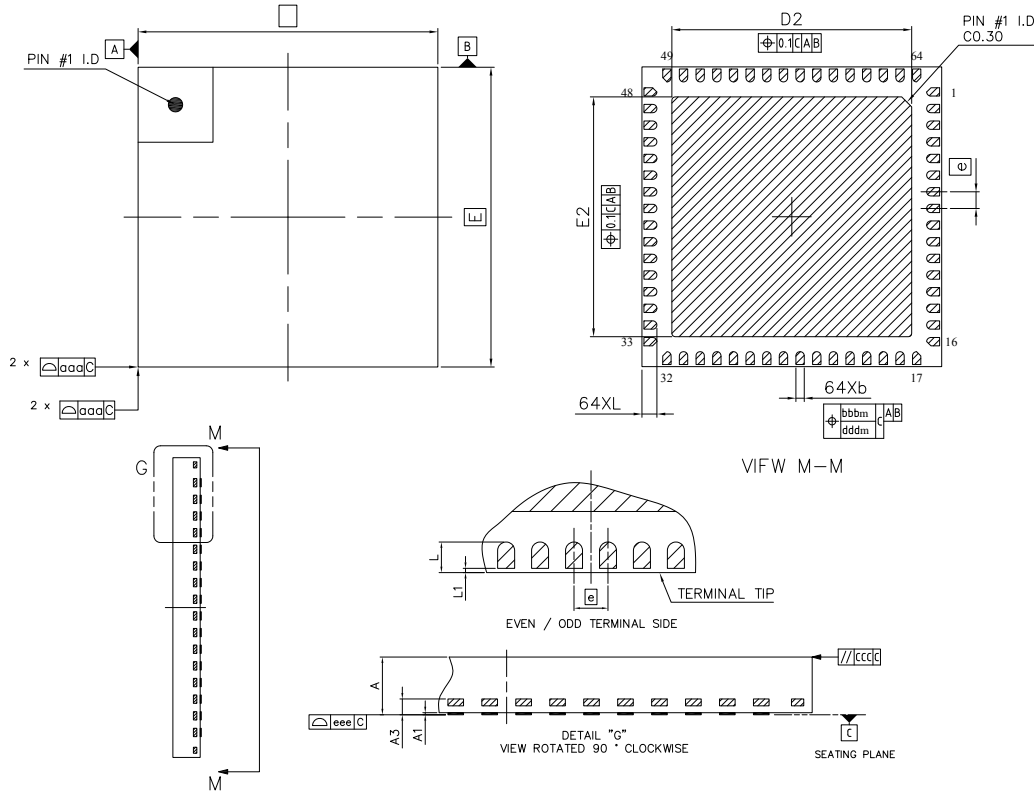


Figure 8.5. Example Chip Marking (Top View)

9. QFN64 Package Specifications

9.1 QFN64 Package Dimensions



Rev: 98SPR64048A_X01_08MAR2011

Figure 9.1. QFN64

Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.

Table 9.1. QFN64 (Dimensions in mm)

| Symbol | Min | Nom | Max |
|--------|-----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | — | 0.05 |
| A3 | 0.203 REF | | |
| b | 0.20 | 0.25 | 0.30 |
| D | 9.00 BSC | | |
| E | 9.00 BSC | | |
| D2 | 7.10 | 7.20 | 7.30 |
| E2 | 7.10 | 7.20 | 7.30 |
| e | 0.50 BSC | | |
| L | 0.40 | 0.45 | 0.50 |
| L1 | 0.00 | — | 0.10 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |

9.2 QFN64 PCB Layout

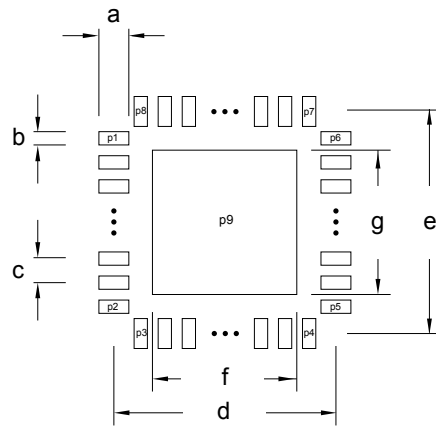


Figure 9.2. QFN64 PCB Land Pattern

Table 9.2. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 0.85 | P1 | 1 | P8 | 64 |
| b | 0.30 | P2 | 16 | P9 | 0 |
| c | 0.50 | P3 | 17 | | |
| d | 8.90 | P4 | 32 | | |
| e | 8.90 | P5 | 33 | | |
| f | 7.20 | P6 | 48 | | |
| g | 7.20 | P7 | 49 | | |

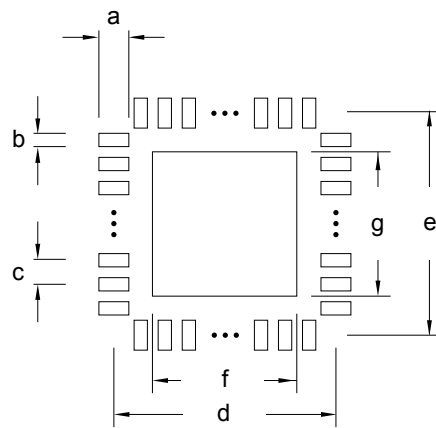


Figure 9.3. QFN64 PCB Solder Mask

Table 9.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|--------|-----------|--------|-----------|
| a | 0.97 | e | 8.90 |
| b | 0.42 | f | 7.32 |
| c | 0.50 | g | 7.32 |

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|--------|-----------|--------|-----------|
| d | 8.90 | - | - |

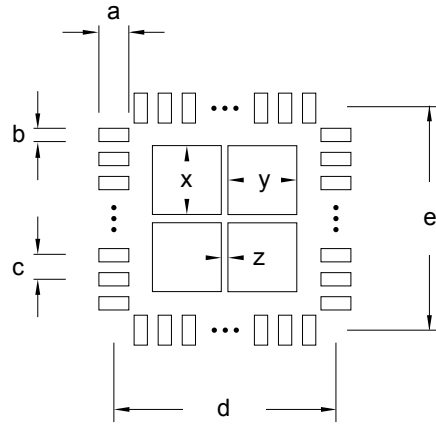


Figure 9.4. QFN64 PCB Stencil Design

Table 9.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|--------|-----------|--------|-----------|
| a | 0.75 | e | 8.90 |
| b | 0.22 | x | 2.70 |
| c | 0.50 | y | 2.70 |
| d | 8.90 | z | 0.80 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

9.3 QFN64 Package Marking

In the illustration below package fields and position are shown.

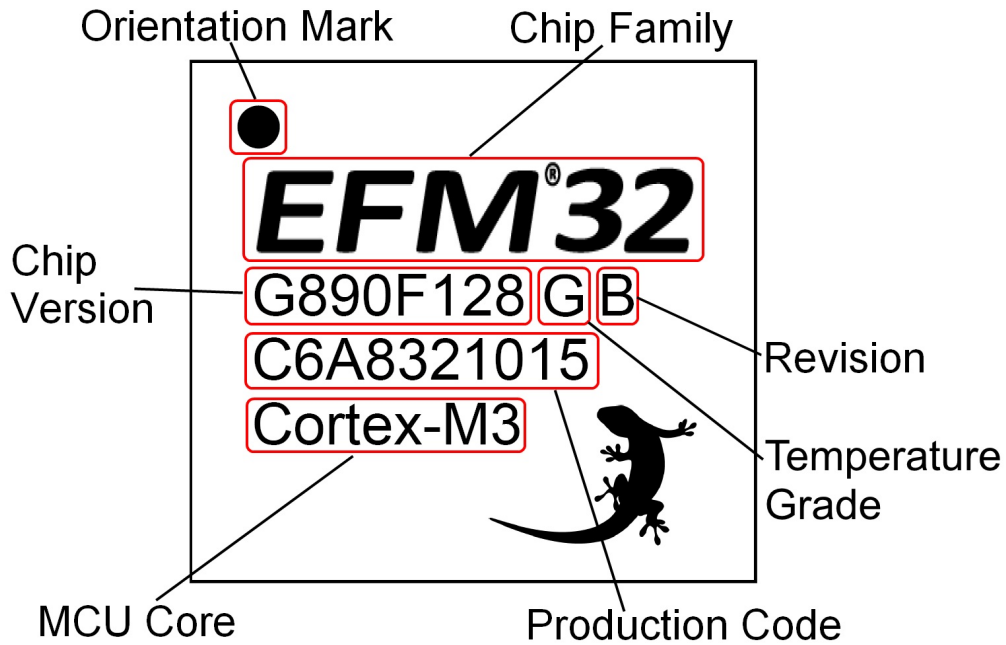
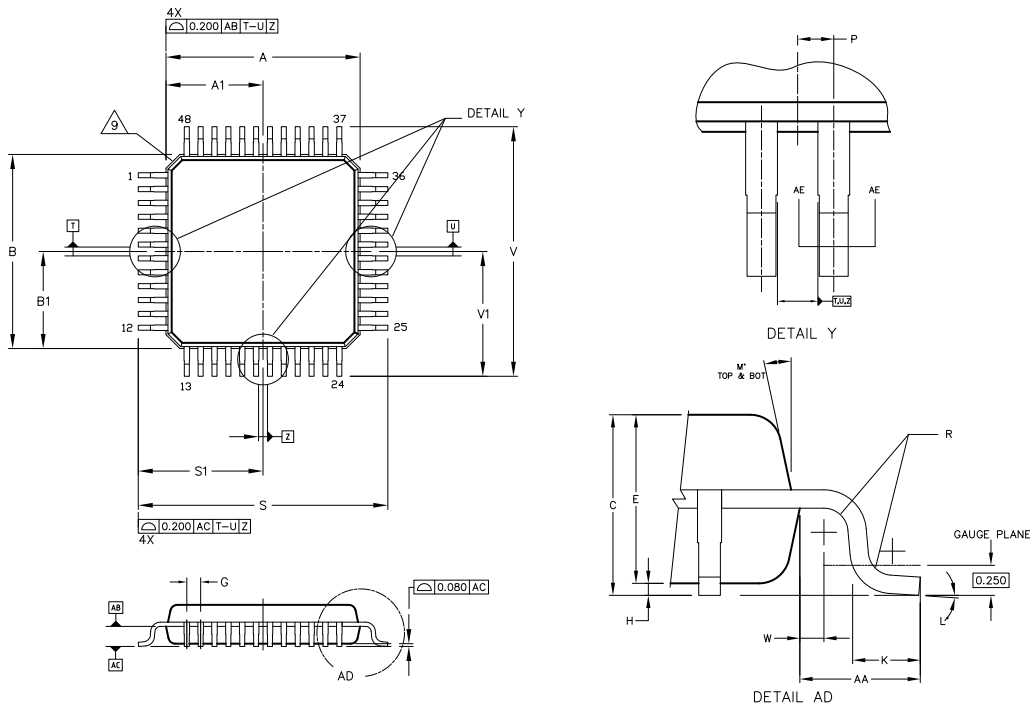


Figure 9.5. Example Chip Marking (Top View)

10. TQFP48 Package Specifications

10.1 TQFP48 Package Dimensions



Rev: 98SP48097A_XO_30Mar11

Figure 10.1. TQFP48

Note:

1. Dimensions and tolerance per ASME Y14.5M-1994
2. Control dimension: Millimeter
3. Datum plane AB is located at bottom of lead and is coincident with the lead where the lead exists from the plastic body at the bottom of the parting line.
4. Datums T, U and Z to be determined at datum plane AB.
5. Dimensions S and V to be determined at seating plane AC.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.250 per side. Dimensions A and B do include mold mismatch and are determined at datum AB.
7. Dimension D does not include dambar protrusion. Dambar protrusion shall not cause the D dimension to exceed 0.350.
8. Minimum solder plate thickness shall be 0.0076.
9. Exact shape of each corner is optional.

Table 10.1. QFP48 (Dimensions in mm)

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|-----|-------|-----------|-------|-----|-------|-----------|-------|
| A | — | 7.000 BSC | — | M | — | 12DEG REF | |
| A1 | — | 3.500 BSC | — | N | 0.090 | — | 0.160 |
| B | — | 7.000 BSC | — | P | — | 0.250 BSC | — |
| B1 | — | 3.500 BSC | — | R | 0.150 | — | 0.250 |
| C | 1.000 | — | 1.200 | S | — | 9.000 BSC | — |
| D | 0.170 | — | 0.270 | S1 | — | 4.500 BSC | — |
| E | 0.950 | — | 1.050 | V | — | 9.000 BSC | — |
| F | 0.170 | — | 0.230 | V1 | — | 4.500 BSC | — |
| G | — | 0.500 BSC | — | W | — | 0.200 BSC | — |
| H | 0.050 | — | 0.150 | AA | — | 1.000 BSC | — |
| J | 0.090 | — | 0.200 | | | | |
| K | 0.500 | — | 0.700 | | | | |
| L | 0DEG | — | 7DEG | | | | |

The TQFP48 package is 7 by 7 mm in size and has a 0.5 mm pin pitch.

The TQFP48 package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

10.2 TQFP48 PCB Layout

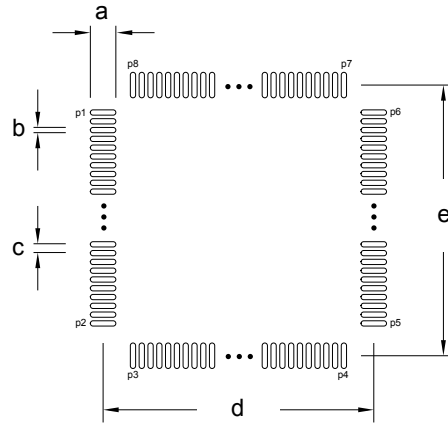


Figure 10.2. TQFP48 PCB Land Pattern

Table 10.2. TQFP48 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 1.60 | P1 | 1 | P6 | 36 |
| b | 0.30 | P2 | 12 | P7 | 37 |
| c | 0.50 | P3 | 13 | P8 | 48 |
| d | 8.50 | P4 | 24 | | |
| e | 8.50 | P5 | 25 | | |

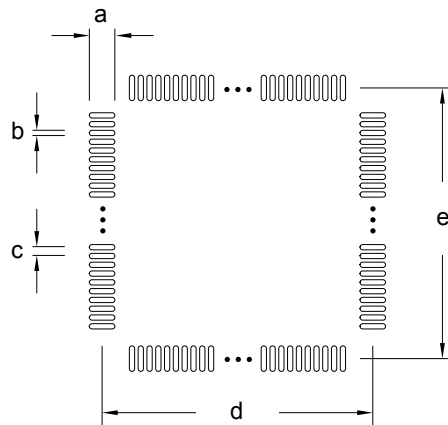


Figure 10.3. TQFP48 PCB Solder Mask

Table 10.3. TQFP48 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.72 |
| b | 0.42 |
| c | 0.50 |
| d | 8.50 |
| e | 8.50 |

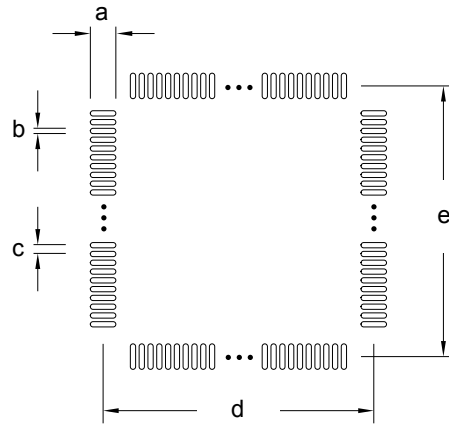


Figure 10.4. TQFP48 PCB Stencil Design

Table 10.4. TQFP48 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.50 |
| b | 0.20 |
| c | 0.50 |
| d | 8.50 |
| e | 8.50 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

10.3 TQFP48 Package Marking

In the illustration below package fields and position are shown.

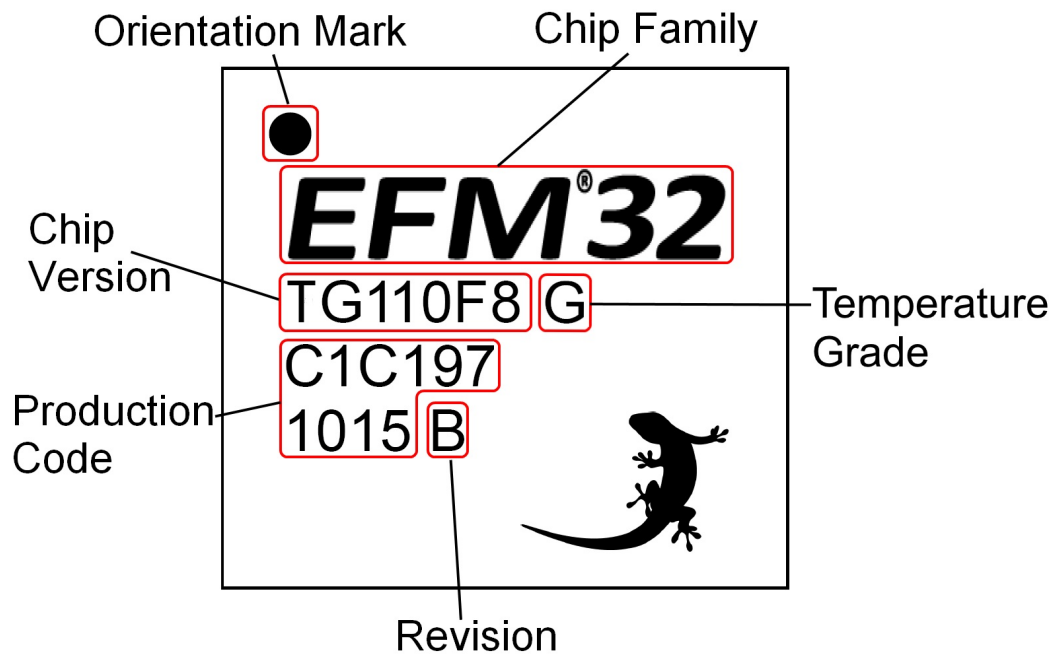
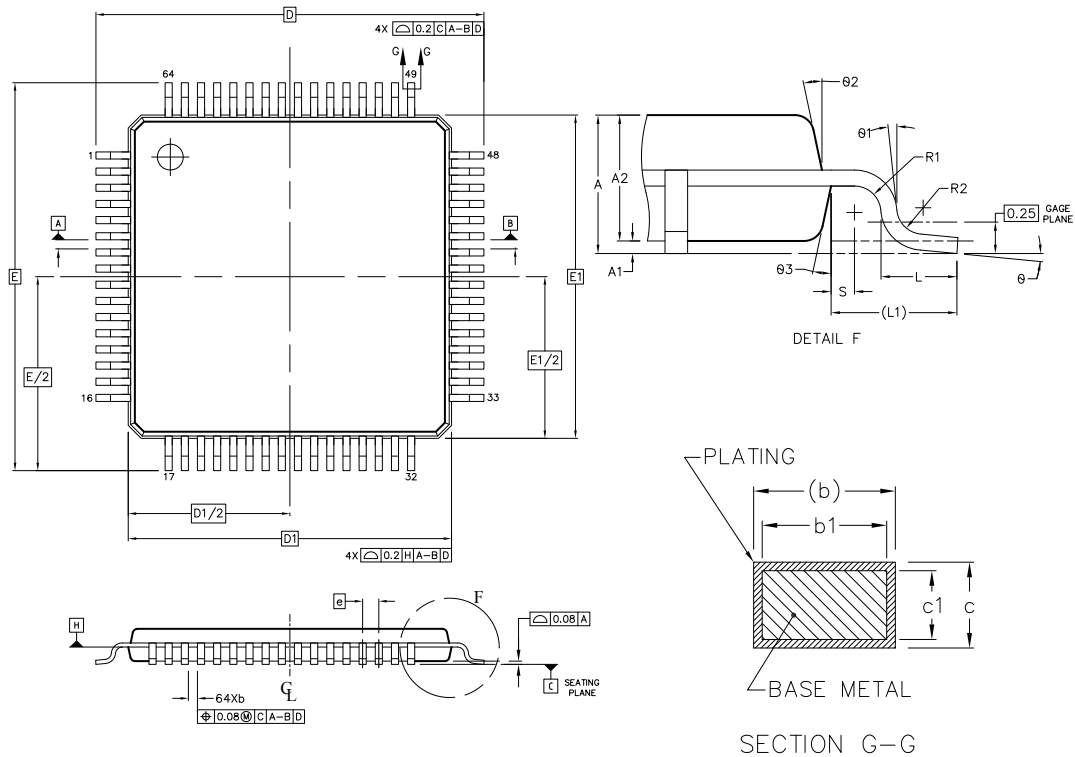


Figure 10.5. Example Chip Marking (Top View)

11. TQFP64 Package Specifications

11.1 TQFP64 Package Dimensions



Rev: 98SP64023A_X01_17MAR2011

Figure 11.1. TQFP64

Note:

1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package body size.
3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.
4. To be determined at seating place 'C'.
5. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side. 'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
6. Detail of Pin 1 indicatifier are option all but must be located within the zone indicated.
7. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
8. Exact shape of each corner is optional.
9. These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. All dimensions are in millimeters.

Table 11.1. QFP64 (Dimensions in mm)

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|-----|----------|------|------|-----|------|------|------|
| A | — | 1.10 | 1.20 | L1 | — | | |
| A1 | 0.05 | — | 0.15 | R1 | 0.08 | — | — |
| A2 | 0.95 | 1.00 | 1.05 | R2 | 0.08 | — | 0.20 |
| b | 0.17 | 0.22 | 0.27 | S | 0.20 | — | — |
| b1 | 0.17 | 0.20 | 0.23 | θ | 0° | 3.5° | 7° |
| c | 0.09 | — | 0.20 | θ1 | 0° | — | — |
| C1 | 0.09 | — | 0.16 | θ2 | 11° | 12° | 13° |
| D | 12.0 BSC | | | θ3 | 11° | 12° | 13° |
| D1 | 10.0 BSC | | | | | | |
| e | 0.50 BSC | | | | | | |
| E | 12.0 BSC | | | | | | |
| E1 | 10.0 BSC | | | | | | |
| L | 0.45 | 0.60 | 0.75 | | | | |

11.2 TQFP64 PCB Layout

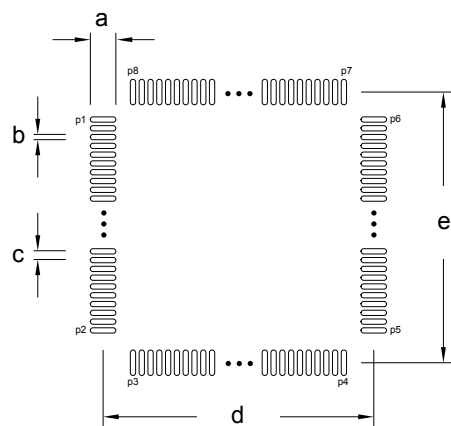


Figure 11.2. TQFP64 PCB Land Pattern

Table 11.2. TQFP64 PCB Land Pattern Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) | Symbol | Pin Number | Symbol | Pin Number |
|--------|-----------|--------|------------|--------|------------|
| a | 1.60 | P1 | 1 | P6 | 48 |
| b | 0.30 | P2 | 16 | P7 | 49 |
| c | 0.50 | P3 | 17 | P8 | 64 |
| d | 11.50 | P4 | 32 | | |
| e | 11.50 | P5 | 33 | | |

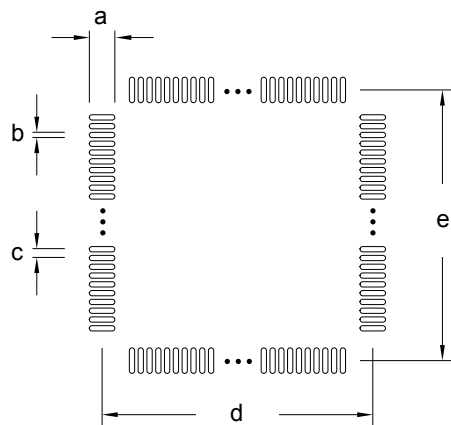


Figure 11.3. TQFP64 PCB Solder Mask

Table 11.3. TQFP64 PCB Solder Mask Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.72 |
| b | 0.42 |
| c | 0.50 |
| d | 11.50 |
| e | 11.50 |

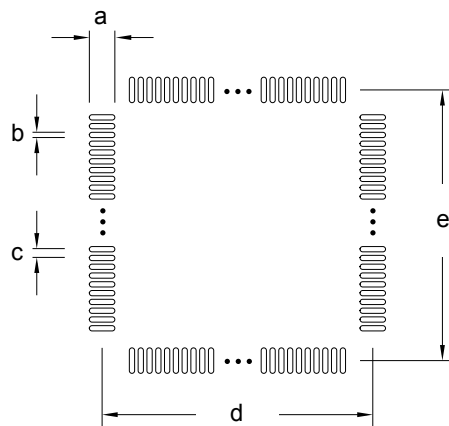


Figure 11.4. TQFP64 PCB Stencil Design

Table 11.4. TQFP64 PCB Stencil Design Dimensions (Dimensions in mm)

| Symbol | Dim. (mm) |
|--------|-----------|
| a | 1.50 |
| b | 0.20 |
| c | 0.50 |
| d | 11.50 |
| e | 11.50 |

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

11.3 TQFP64 Package Marking

In the illustration below package fields and position are shown.

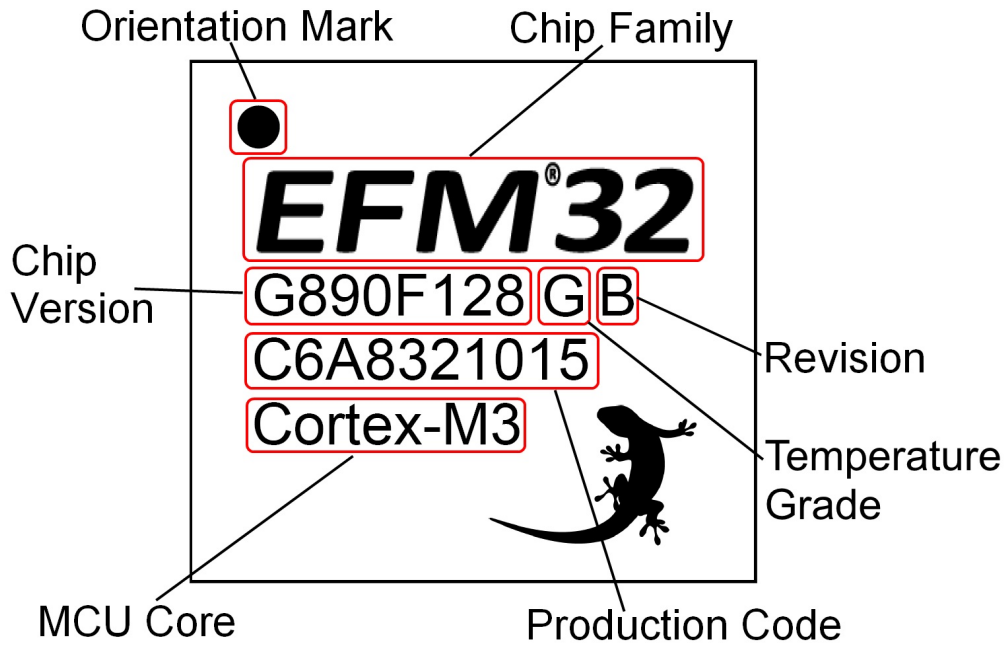


Figure 11.5. Example Chip Marking (Top View)

12. Chip Revision, Solder Information, Errata

12.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

12.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

12.3 Errata

See the errata document for description and resolution of device errata. This document is available in Simplicity Studio and online at: <http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

13. Revision History

Revision 2.11

July, 2020

- Updated [Figure 2.1 Ordering Code Decoder on page 5](#) to indicate reel, not tape.

Revision 2.10

November, 2019

- [1. Feature List](#) - Added SysTick.
- [2. Ordering Information](#) - Updated for release of revision D devices.
- [4.2 Absolute Maximum Ratings](#) - Removed footnote about storage temperature and added max sink/source current per I/O pin.
- [4.7 Flash](#) – Added word write cycles between erase (WWC_{FLASH}) specification.
- [4.10 Analog Digital Converter \(ADC\)](#) - Updated ADC input impedance.
- [4.11 Digital Analog Converter \(DAC\)](#) - Added max load current specification.
- [7.2 QFN24 PCB Layout](#) - Corrected pin number for symbol P9.
- [8.2 QFN32 PCB Layout](#) - Corrected pin number for symbol P9.
- [9.2 QFN64 PCB Layout](#) - Corrected pin number for symbol P9.

Revision 2.00

August, 2018

- Consolidated all EFM32TG data sheets:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- Added a Feature List section.
- [2. Ordering Information](#) – Added ordering code decoder.
- [3.3 Memory Map](#) – Separated the Memory Map into two figures – one for core and code space listing and one for peripheral listing.
- Environmental – Removed this section. Environmental specifications are available in the qualification report.
- Removed MSL information (Moisture Sensitivity Level). Instead, MSL information can be found in the Qual report that is available on the Silicon Labs website.
- For QFN32 packages, corrected pin number for symbol P3.
- [6.1 BGA48 Package Dimensions](#) – Removed statements regarding materials used.
- New formatting throughout.

Revision 1.40

March 6th, 2015

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- Updated Block Diagram.
- Updated Energy Modes current consumption.
- Updated Power Management section.
- Updated LFRCO and HFRCO sections.
- Added AUXHFRCO to block diagram and Electrical Characteristics.
- Corrected unit to kHz on LFRCO plots y-axis.
- For devices with ADC, updated ADC section and added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.
- For devices with DAC, updated ADC section and added clarification on conditions for INL_{DAC} and DNL_{DAC} parameters.
- For devices with OPAMP, updated OPAMP section.
- For devices with ACMP, updated ACMP section and the response time graph.
- For devices with VCMP, updated VCMP section.
- For QFN24 and QFN32 packages, updated Package dimensions table.
- Updated Digital Peripherals section.

Revision 1.30

July 2nd, 2014

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- Updated current consumption.
- Updated transition between energy modes.
- Updated power management data.
- Updated GPIO data.
- Updated LFXO, HFXO, HFRCO and ULFRCO data.
- Updated LFRCO and HFRCO plots.
- Updated ACMP data.

Revision 1.21

November 21st, 2013

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- Updated figures.
- Updated errata-link.
- Updated chip marking.
- Added link to Environmental and Quality information.
- For devices with DAC, re-added missing DAC-data.

Revision 1.20

September 30th, 2013

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- Added I2C characterization data.
- For devices with DAC, corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.
- Corrected GPIO operating voltage from 1.8 V to 1.85 V.
- For devices with ADC, corrected the ADC gain and offset measurement reference voltage from 2.25 to 2.5V.
- For devices with ADC, corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.
- For QFP48 devices, updated the Max V_{ESDCDM} value to 750 V.
- Document changed status from "Preliminary".
- Updated Environmental information.
- Updated trademark, disclaimer and contact information.
- Other minor corrections.

Revision 1.10

June 28th, 2013

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- For BGA packages, updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.
- Updated power requirements in the Power Management section.
- Removed minimum load capacitance figure and table. Added reference to application note.
- Other minor corrections.

Revision 1.00

September 11th, 2012

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- Updated the HFRCO 1 MHz band typical value to 1.2 MHz.
- Updated the HFRCO 7 MHz band typical value to 6.6 MHz.
- Added GPIO_EM4WU3, GPIO_EM4WU4 and GPIO_EM4WU5 pins and removed GPIO_EM4WU1 in the Alternate functionality overview table.
- Other minor corrections.

Revision 0.96

May 4th, 2012

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- For BGA48 packages, added PCB land pattern, Stencil design and solder mask.
- For BGA48 packages, corrected PCB footprint figures and tables.

Revision 0.95

February 27th, 2012

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- For BGA48 packages, initial preliminary release.
- For BGA48 packages, corrected operating voltage from 1.8 V to 1.85 V.
- For BGA48 packages, added rising POR level and corrected Thermometer output gradient in Electrical Characteristics section.
- For BGA48 packages, updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.
- For BGA48 packages, added Gain error drift and Offset error drift to ADC table.
- For devices with OPAMP in BGA48 packages, added Opamp pinout overview.
- For BGA48 packages, added reference to errata document.

Revision 0.92

July 22nd, 2011

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG222
 - EFM32TG225
 - EFM32TG230
 - EFM32TG232
 - EFM32TG822
 - EFM32TG825
 - EFM32TG840
 - EFM32TG842
- Updated current consumption numbers from latest device characterization data.
- For devices with OPAMP, updated OPAMP electrical characteristics.
- For devices with ADC, made ADC plots render properly in Adobe Reader.
- For EFM32TG822, corrected number of DAC channels available.
- For EFM32TG232, corrected number of DAC channels available.
- For EFM32TG842, corrected number of DAC channels available.
- For EFM32TG230, corrected number of DAC channels available.

Revision 0.91

February 4th, 2011

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG230
 - EFM32TG840
- Corrected max DAC sampling rate.
- Increased max storage temperature.
- Added data for <150°C and <70°C on Flash data retention.
- Changed latch-up sensitivity test description.
- Added IO leakage current.
- Added Flash current consumption.
- Updated HFRCO data.
- Updated LFRCO data.
- For devices with ADC, added graph for ADC Absolute Offset over temperature.
- For devices with ADC, added graph for ADC Temperature sensor readout.
- For devices with OPAMP, updated OPAMP electrical characteristics.

Revision 0.90

December 1st, 2010

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG230
 - EFM32TG840
- New peripherals added to pinout, including LESENSE and OpAmps.

April 14th, 2011

- This revision applies the following devices:
 - EFM32TG222
 - EFM32TG232
 - EFM32TG822
- Initial preliminary release.

June 30th, 2011

- This revision applies the following devices:
 - EFM32TG842
- Initial preliminary release.

Revision 0.70

August 16th, 2010

- This revision applies the following devices:
 - EFM32TG110
- Added pinout.

Revision 0.60

June 8th, 2010

- This revision applies the following devices:
 - EFM32TG230
- Corrected pinout.

Revision 0.50

May 25th, 2010

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG230
 - EFM32TG840
- Block diagram update.

Revision 0.40

March 26th, 2010

- This revision applies the following devices:
 - EFM32TG108
 - EFM32TG110
 - EFM32TG210
 - EFM32TG230
 - EFM32TG840
- Initial preliminary release.

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