THE DATASHEET OF

A3P250-QNG132

FPGA and SoC Product Catalog

Lowest Power, Proven Security, and Exceptional Reliability

Flash FPGAs

Flash SoC FPGAs

Military FPGAs

Automotive FPGAs

Ecosystem

Design Hardware

Intellectual Property

Technology Solutions

Microsemi

Power Matters.™

Delivering More Resources in Low-Density Devices with the Lowest Power, Proven Security, and Exceptional Reliability

Microsemi FPGAs and SoC FPGAs

Whether you're designing at the board or system level, Microsemi's SoC FPGAs and low-power FPGAs are your best choice. The unique, flash-based technology of Microsemi FPGAs and their history of reliability sets them apart from traditional FPGAs.

Design with Microsemi's FPGAs and SoC FPGAs for today's rapidly-growing markets of consumer and portable medical devices, or tomorrow's environmentally friendly data centers, industrial controls, and military and commercial aircraft. Only Microsemi can meet the power, size, cost, and reliability targets that reduce time-to-market and enable long-term profitability.

Product Highlights

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For the latest device information, valid ordering codes, and details regarding previous-generations of flash FPGAs, visit www.microsemi.com/fpga-soc or consult the corresponding product datasheets.

SmartFusion2 SoC FPGAs

More Resources in Low-Density Devices with ARM Cortex-M3 Processor

SmartFusion2 SoC FPGAs deliver more resources in low-density devices with the lowest power, proven security, and exceptional reliability. These devices are ideal for general purpose functions such as Gigabit Ethernet or dual-PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management, and secure connectivity. Microsemi SoC FPGAs are used by customers in Communications, Industrial, Medical, Defense, and Aviation markets.

- Embedded ARM Cortex-M3 microcontroller subsystem (MSS)
- PCIe Gen2 endpoints starting at 10K logic elements
- Embedded DDR3 memory controllers
- Small packages
- 1 mW in Flash*Freeze mode
- Instant-on
- Zero FIT FPGA configuration cells
- SECDED memory protection
- NRBG, AES-256, SHA-256, ECC cryptographic engine
- User physically unclonable function (PUF)
- CRI DPA pass-through license

SmartFusion2 Devices

SmartFusion2 Devices	Features	M2S005	M2S010	M2S025	M2S050	M2S060	M2S090	M2S150
Logic/DSP	Maximum logic elements (4LUT + DFF)	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 × 18)	11	22	34	72	72	84	240
	Fabric interface controllers (FICs)	1			2	1		2
	PLLs and CCCs	2		6				8
	Security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
MSS	Cortex-M3 + instruction cache	Yes						
	eNVM (KB)	128	256				512	
	eSRAM (KB)	64						
	eSRAM (KB) non-SECDED	80						
	CAN, 10/100/1000 Ethernet, HS USB	1 each						
	Multi-mode UART, SPI, I^2C, timer	2 each						
Fabric memory	LSRAM 18K blocks	10	21	31	69		109	236
	uSRAM 1K blocks	11	22	34	72		112	240
	Total RAM (kbits)	191	400	592	1,314		2,074	4,488
High-speed	DDR controllers (count × width)	1 × 18			2 × 36	1 × 18		2 x 36
	SERDES lanes	0	4		8	4		16
	PCIe endpoints	0	1		2			4
User I/O	MSIO (3.3 V)	115	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40		62	40		106
	DDRIO (2.5 V)	66	70		176	76		176
	Total user I/Os	209	233	267	377	387	425	574

I/Os per Package

	Package Options																			
Package type	FCS(G)325		VF(G)256		FCS(G)536		VF(G)400		FCV(G)484		TQ(G)144		FG(G)484		FG(G)676		FG(G)896		FC(G)1152	
Pitch (mm)	0.5		0.8		0.5		0.8				0.5		1.0		1.0		1.0		1.0	
Length × width (mm)	11 × 11		14 × 14		16 × 16		17 × 17		19 × 19		20 × 20		23 × 23		27 × 27		31 × 31		35 × 35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005 (S)			161				171				84		209							
M2S010 (S/T/TS)			138	2			195	4			84		233	4						
M2S025 (T/TS)	180	2	138	2			207	4					267	4						
M2S050 (T/TS)	200	2					207	4					267	4			377	8		
M2S060 (T/TS)	200	2					207	4					267	4	387	4				
M2S090 (T/TS)	180	4											267	4	425	4				
M2S150 (T/TS)					293	4			248	4									574	16

Notes:
1. M2S090 FCSG325 package dimension are 11 × 13.5.
2. Highlighted devices can migrate vertically in the same package.
3. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.

IGLOO2 FPGAs

More Resources in Low-Density Devices with High-Performance Memory Subsystem

IGLOO2 FPGAs deliver more resources in low-density devices with the lowest power, proven security, and exceptional reliability. These devices are ideal for general purpose functions such as Gigabit Ethernet or dual-PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management, and secure connectivity. Microsemi FPGAs are used by customers in Communications, Industrial, Medical, Defense, and Aviation markets.

- High-performance memory subsystem
- PCIe Gen2 endpoints starting at 10K logic elements
- Embedded DDR3 memory controllers
- SECDED memory protection
- 1 mW in Flash*Freeze mode
- Instant-on
- Zero FIT FPGA configuration cells
- CRI DPA pass-through license
- Small packages
- NRBG, AES-256, SHA-256, ECC cryptographic engine
- User physically unclonable function (PUF)

IGLOO2 Devices

IGLOO2 Devices	Features	M2GL005	M2GL010	M2GL025	M2GL050	M2GL060	M2GL090	M2GL150
Logic/DSP	Maximum logic elements (4LUT + DFF)	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 × 18)	11	22	34	72	72	84	240
	PLLs and CCCs	2		6				8
	SPI/HPDMA/PDMA	1 each						
	Fabric interface controllers (FICs)	1			2	1		2
	Data security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
Memory	eNVM (KB)	128	256				512	
	LSRAM 18K blocks	10	21	31	69		109	236
	uSRAM 1K blocks	11	21	34	72		112	240
	eSRAM (KB)	64						
	Total RAM (kbits)	703	912	1104	1826		2586	5000
High-speed	DDR controllers (count × width)	1 × 18			2 × 36	1 × 18		2 × 36
	SERDES lanes	0	4		8	4		16
	PCIe endpoints	0	1		2			4
User I/O	MSIO (3.3 V)	115	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40		62	40		106
	DDRIO (2.5 V)	66	70		176	76		176
	Total user I/Os	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M)	C, I	C, I, M					

Notes:
1. Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 and SmartFusion2 Fabric User Guide for details. 2. Feature availability is package dependent.

I/Os per Package

	Package Options																			
Package type	FCS(G)325		VF(G)256		FCS(G)536		VF(G)400		FCV(G)484		TQ(G)144		FG(G)484		FG(G)676		FG(G)896		FC(G)1152	
Pitch (mm)	0.5		0.8		0.5		0.8				0.5		1.0		1.0		1.0		1.0	
Length × width (mm)	11x11		14x14		16x16		17x17		19x19		20x20		23x23		27x27		31x31		35x35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2GL005 (S)			161				171				84		209							
M2GL010 (S/T/TS)			138	2			195	4			84		233	4						
M2GL025 (T/TS)	180	2	138	2			207	4					267	4						
M2GL050 (T/TS)	200	2					207	4					267	4			377	8		
M2GL060 (T/TS)	200	2					207	4					267	4	387	4				
M2GL090 (T/TS)	180	4											267	4	425	4				
M2GL150 (T/TS)					293	4			248	4									574	16

Notes:
1. M2GL090 FCS325 package dimension are 11 x 13.5. 2. Highlighted devices can migrate vertically in the same package. 3. (G) indicates that the package is RoHS 6/6 compliant/Pb-free

IGLOO Family: IGLOO/e FPGAs

The Ideal Low-Power, Programmable Solution for CPLD Replacement

The IGLOO family of reprogrammable and full-featured flash FPGAs is designed to meet the low-power and area requirements of today's portable electronics. Based on nonvolatile flash technology, the 1.2 V to 1.5 V operating voltage family offers the industry's lowest power consumption—as low as 5 µW. The IGLOO family supports up to 35K logic elements with up to 504 kbits of true dual-port SRAM, up to six embedded PLLs, and up to 620 user I/Os. Low-power applications that require 32-bit processing can use the ARM Cortex-M1 processor without license fees or royalties in M1 IGLOO devices. Developed specifically for implementation in FPGAs, Cortex-M1 devices offer an optimal balance between performance and size to minimize power consumption.

- Low-power FPGAs
- Flash*Freeze technology for low power consumption
- 1.2 V core and I/O voltage
- Instant-on
- AES-protected in-system programming (ISP)
- User nonvolatile FlashROM

IGLOO/e Devices

IGLOO devices	Features	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
ARM-Enabled IGLOO[1] devices					M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
Logic	Logic elements (approximate)	330	700	1,500	3,000	5,000	7,000	11,000	7,000	35,000
	System gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	3,000,000
	VersaNet globals[3]	6	18	18	18	18	18	18	18	18
	Flash*Freeze mode (typical, µW)	5	10	16	24	32	36	53	49	137
	AES-protected ISP[1]		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Integrated PLLs with CCC[2]		1	1	1	1	1	1	6	6
Fabric memory	RAM (1,024 bits)		18	36	36	54	108	144	108	504
	RAM blocks (4,608 bits)		4	8	8	12	24	32	24	112
	FlashROM kbits (1,024 bits)	1	1	1	1	1	1	1	1	1
User I/O	I/O banks	2	2	2	4	4	4	4	8	8
	Maximum user I/Os	81	96	133	143	194	235	300	270	620

Notes:
1. AES is not available for Cortex-M1 IGLOO devices.
2. AGL060 in CS121 does not support the PLL.
3. Six chip (main) and twelve quadrant global networks are available for AGL060 devices and above.

I/Os per Package

IGLOO/e Devices	I/O Package	QNG48	QNG68	UCG81	CSG81	CS(G)121	VQ(G)100	CS(G)196	FG(G)144	FG(G)256[3]	CS(G)281	FG(G)484[3]	FG(G)896
	Pitch (mm)	0.4	0.4	0.4	0.5	0.5	0.5	0.5	1.0	1.0	0.5	1.0	1.0
	Length × Width (mm)	6 × 6	8 × 8	4 × 4	5 × 5	6 × 6	16 × 16	8 × 8	13 × 13	17 × 17	10 × 10	23 × 23	31 × 31
AGL030	Single-end I/O	34	49	66	66		77						
AGL060	Single-end I/O					96	71						
AGL125	Single-end I/O					96	71	133	97				
AGL250/ M1AGL250	Single-end I/O[2]						68	143[1]	97				
	Differential I/O						13	35[1]	24				
AGL400	Single-end I/O[2]							143	97	178		194	
	Differential I/O							35	25	38		38	
AGL600/ M1AGL600	Single-end I/O[2]								97	177	215	235	
	Differential I/O								25	43	53	60	
AGL1000/ M1AGL1000	Single-end I/O[2]								97	177	215	300	
	Differential I/O								25	44	53	74	
AGLE600	Single-end I/O[2]									165		270	
	Differential I/O									79		135	
AGLE3000/ M1AGLE3000	Single-end I/O[2]											341	620
	Differential I/O											168	310

Notes:
1. The M1AGL250 device does not support CS196 package.
2. Each used differential pair reduces the number of single-end I/Os available by two.
3. FG256 and FG484 are footprint-compatible packages.

IGLOO Family: IGLOO nano FPGAs

The Industry's Lowest-Power, Smallest-Size Solution

IGLOO nano products offer groundbreaking possibilities in power, size, lead-times, operating temperature, and cost. Available in logic densities from 100–3K logic elements, the 1.2 V to 1.5 V IGLOO nano devices have been designed for high-volume applications where power and size are the key decision criteria. IGLOO nano devices are perfect ASIC or ASSP replacements, yet retain the historical FPGA advantages of flexibility and quick time-to-market in low-power and small footprint profiles.

- Ultra low power in Flash*Freeze mode, as low as 2 µW
- Small footprint packages from 14 mm × 14 mm to 3 mm × 3 mm
- Enhanced commercial temperature
- 1.2 V to 1.5 V single voltage operation
- Enhanced I/O features
- Embedded SRAM and non-volatile memory (NVM)
- ISP and security
- Instant-on

IGLOO nano Devices

IGLOO nano Devices	Features	AGLN010	AGLN020	AGLN060	AGLN125	AGLN250
Logic	Logic elements (approximate)	100	200	700	1,500	3,000
	System gates	10,000	20,000	60,000	125,000	250,000
	VersaNet globals	4	4	18	18	18
	Flash*Freeze mode (typical, µW)	2	4	10	16	24
	AES-protected ISP			Yes	Yes	Yes
	Integrated PLL in CCCs[1]			1	1	1
Fabric memory	RAM kbits (1,024 bits)			18	36	36
	4,608-bit blocks			4	8	8
	FlashROM kbits (1,024 bits)	1	1	1	1	1
User I/O	I/O banks	2	3	2	2	4
	Maximum user I/Os (packaged device)	34	52	71	71	68

Notes:
1. AGLN060, AGLN125 and AGLN250 in the CS(G)81 package do not support PLLs.

I/Os per Package

I/O Packages	UCG36	QNG48	QNG68	UCG81	CSG81	VQ(G)100[2]
Pitch (mm)	0.4	0.4	0.4	0.4	0.5	0.5
Length × width (mm)	3 × 3	6 × 6	8 × 8	4 × 4	5 × 5	16 × 16
AGLN010	23	34				
AGLN020			49	52	52	
AGLN060					60	71
AGLN125					60	71
AGLN250					60	68

Notes:
1. IGLOO nano devices do not support differential I/Os.
2. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.

IGLOO Family: IGLOO PLUS FPGAs

The Low-Power FPGA with Enhanced I/O Capabilities

IGLOO PLUS products deliver low power and enhanced I/Os in a feature-rich programmable device, offering more I/Os per logic element than the IGLOO devices, and supporting independent Schmitt trigger inputs, hot-swapping, and Flash*Freeze bus hold. Ranging from 330–1.5K logic elements, the 1.2V to 1.5V IGLOO PLUS devices have been optimized to meet the needs of I/O-intensive, power-conscious applications that require exceptional features.

- I/O-optimized FPGA
- Low power in Flash*Freeze mode, as low as 5 µW
- Small footprint and low-cost packages
- Reprogrammable flash technology
- 1.2 V to 1.5 V single voltage operation
- Embedded SRAM NVM
- AES-protected ISP
- Instant-on

IGLOO PLUS Devices

IGLOO PLUS Devices	Features	AGLP030	AGLP060	AGLP125
Logic	Logic elements (approximate)	330	7,000	1,500
	System gates	30,000	60,000	125,000
	VersaNet globals	6	18	18
	Flash*Freeze mode (typical, µW)	5	10	16
	AES-protected ISP		Yes	Yes
	Integrated PLL in CCCs[1]		1	1
Fabric memory	RAM (1,024 bits)		18	36
	4,608-bit blocks		4	8
	FlashROM kbits (1,024 bits)	1	1	1
User I/O	I/O banks	4	4	4
	Maximum user I/Os (packaged device)	120	157	212

Notes:
1. AGLP060 in CS(G)201 does not support the PLL.

I/Os per Package

IGLOO PLUS Devices	I/O Package	CS(G)201	CS(G)281	CS(G)289	VQ(G)176
	Pitch (mm)	0.5	0.5	0.8	0.4
	Length × width (mm)	8 × 8	10 × 10	14 × 14	22 × 22
AGLP030	Single-end I/O	120		120	
AGLP060	Single-end I/O	157		157	137
AGLP125	Single-end I/O		212	212	

Notes:
1. IGLOO Plus devices do not support differential I/Os.
2. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.

ProASIC3 Family: ProASIC3/E FPGAs

Low-Density CPLD Replacement FPGA

The ProASIC3 series of flash FPGAs offers a breakthrough in power, performance, density, and features for today's most demanding high-volume applications. The ProASIC3 devices support the ARM Cortex-M1 processor, offering the benefits of programmability and time-to-market at low cost. The ProASIC3 devices are based on nonvolatile flash technology and support 330–35K logic elements and up to 620 high-performance I/Os. For automotive applications, selected ProASIC3 devices are qualified to AEC-Q100 and are available with AEC T1 screening and PPAP documentation.

- 1.5 V single voltage operation
- 350 MHz system performance
- Instant-on
- Configuration memory error immune
- Advanced I/O standards
- Secure ISP

ProASIC3/E Devices

ProASIC3/E Devices	Features	A3P030	A3P060[2]	A3P125[2]	A3P250[2]	A3P400	A3P600	A3P1000[2]	A3PE600	A3PE1500	A3PE3000
ARM Cortex-M1 Devices					M1A3P250	M1A3P400	M1A3P600	M1A3P1000		M1A3PE1500	M1A3PE3000
Logic	Logic elements (approximate)	330	700	1,500	3,000	5,000	7,000	11,000	7,000	16,000	35,000
	System gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	1,500,000	3,000,000
	VersaNet globals[3]	6	18	18	18	18	18	18	18	18	18
	AES-protected ISP[1]		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Integrated PLL in CCCs		1	1	1	1	1	1	6	6	6
Fabric memory	RAM (1,024 bits)		18	36	36	54	108	144	108	270	504
	4,608-bit blocks		4	8	8	12	24	32	24	60	112
	FlashROM kbits (1,024 bits)	1	1	1	1	1	1	1	1	1	1
User I/O	I/O banks	2	2	2	4	4	4	4	8	8	8
	Maximum user I/Os	81	96	133	157	194	235	300	270	444	620

Notes:
1. AES is not available for ARM Cortex-M1 ProASIC3 devices.
2. Available as automotive "T" grade
3. Six chip (main) and three quadrant global networks are available for A3P060 and above.

I/Os per Package

ProASIC3	I/O Type	QNG48	QNG68	CS(G)121	VQ(G)100	TQ(G)144	PQ(G)208	FG(G)144	FG(G)256	FG(G)324	FG(G)484	FG(G)676	FG(G)896
	Pitch (mm)	0.4	0.4	0.5	0.5	0.5	0.5	1.0	1.0	1.0	1.0	1.0	1.0
	Length × width (mm)	6 × 6	8 × 8	6 × 6	16 × 16	20 × 20	30.6 × 30.6	13 × 13	17 × 17	19 × 19	23 × 23	27 × 27	31 × 31
A3P030	Single-end I/O	34	49		77								
A3P060	Single-end I/O			96	71	91		96					
A3P125	Single-end I/O				71	100	133	97					
A3P250/ M1A3P250	Single-end I/O				68		151	97	157				
	Differential I/O				13		34	24	38				
A3P400/ M1A3P400	Single-end I/O						151	97	178		194		
	Differential I/O						34	25	38		38		
A3P600/ M1A3P600	Single-end I/O						154	97	177		235		
	Differential I/O						35	25	43		60		
A3P1000/ M1A3P1000	Single-end I/O						154	97	177		300		
	Differential I/O						35	25	44		74		
A3PE600	Single-end I/O						147		165		270		
	Differential I/O						65		79		135		
A3PE1500/ M1A3PE1500	Single-end I/O						147				280	444	
	Differential I/O						65				139	222	
A3PE3000/ M1A3PE3000	Single-end I/O						147			221	341		620
	Differential I/O						65			110	168		310

Notes:
1. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.

ProASIC3 Family: ProASIC3 nano FPGAs

Low-Density CPLD Replacement FPGA with Small Package Footprint

Microsemi's innovative ProASIC3 nano devices bring a new level of value and flexibility to high-volume markets. When measured against the typical project metrics of performance, cost, flexibility, and time-to-market, the ProASIC3 nano devices provide an attractive alternative to ASICs and ASSPs in fast-moving or highly competitive markets. Customer-driven total-system cost reduction was a key design criteria for the ProASIC3 nano program. A single-chip implementation and a broad selection of small footprint packages, contribute to lower total system costs.

- 1.5 V core for low power
- 350 MHz system performance
- Configuration memory error immune
- Enhanced commercial temperature
- Enhanced I/O features
- ISP and security

ProASIC3 nano Devices

ProASIC3 nano Devices	Features	A3PN010	A3PN020	A3PN060	A3PN125	A3PN250
Logic	Logic elements (approximate)	100	200	700	1,500	3,000
	System gates	10,000	20,000	60,000	125,000	250,000
	VersaNet globals	4	4	18	18	18
	AES-protected ISP			Yes	Yes	Yes
	Integrated PLL in CCCs			1	1	1
Fabric memory	RAM (1,024 bits)			18	36	36
	4,608-bit blocks			4	8	8
	FlashROM kbits (1,024 bits)	1	1	1	1	1
User I/O	I/O banks	2	3	2	2	4
	Maximum user I/Os (packaged device)	34	49	71	71	68

I/Os per Package

I/O Packages	QNG48	QNG68	VQ(G)100[1]
Pitch (mm)	0.4	0.4	0.5
Length × width (mm)	6 × 6	8 × 8	16 × 16
A3PN010	34		
A3PN020		49	
A3PN060			71
A3PN125			71
A3PN250			68

Notes:

1. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.
2. ProASIC3 nano devices do not support differential I/Os.

ProASIC3 Family: ProASIC3L FPGAs

Low-Density, Low-Power CPLD Replacement FPGA

ProASIC3L FPGAs feature lower dynamic power and lower static power than the previous generation of ProASIC3 FPGAs, and orders of magnitude lower power than SRAM competitors, combining dramatically reduced power consumption with up to 350 MHz operation. The ProASIC3L family also supports the free implementation of an FPGA-optimized 32-bit ARM Cortex-M1 processor, enabling system designers to select the Microsemi flash FPGA solution that best meets their speed and power requirements, regardless of application or volume. Optimized software tools using power-driven layout (PDL) provide instant power reduction capabilities.

- Low power 1.2 V to 1.5 V core operation
- 700 Mbps DDR, LVDS capable I/Os
- Up to 350 MHz system performance
- Configuration memory error immune
- ISP and security
- Flash*Freeze technology for low power

ProASIC3L Low-Power Devices

ProASIC3L Devices	Features	A3P250L	A3P600L	A3P1000L	A3PE3000L
ARM Cortex-M1 Devices[1]			M1A3P600L	M1A3P1000L	M1A3PE3000L
Logic	Logic elements (approximate)	3,000	7,000	11,000	35,000
	System gates	250,000	600,000	1,000,000	3,000,000
	VersaNet globals	18	18	18	18
	AES-protected ISP[2]	Yes	Yes	Yes	Yes
	Integrated PLL in CCCs[3]	1	1	1	6
Fabric memory	RAM (1,024 bits)	36	108	144	504
	4,608-bit blocks	8	24	32	112
	FlashROM kbits (1,024 bits)	1	1	1	1
User I/O	I/O banks	4	4	4	8
	Maximum user I/Os (packaged device)	157	235	300	620

Notes:
1. Refer to the Cortex-M1 product brief for more information. 2. AES is not available for Cortex-M1 ProASIC3L devices. 3. For the A3PE3000L, the PQ208 package has six CCCs and two PLLs.

I/Os per Package

ProASIC3L Devices	I/O Type	VQ(G)100	PQ(G)208	FG(G)144	FG(G)256	FG(G)324	FG(G)484	FG(G)896
	Pitch (mm)	0.5	0.5	1.0	1.0	1.0	1.0	1.0
	Length × width (mm)	16 × 16	30.6 × 30.6	13 × 13	17 × 17	19 × 19	23 × 23	31 × 31
A3P250L	Single-end I/O	68	151	97	157			
	Differential I/O	13	34	24	38			
A3P600L/ M1A3P600L	Single-end I/O		154	97	177		235	
	Differential I/O		35	25	43		60	
A3P1000L/ M1A3P1000L	Single-end I/O		154	97	177		300	
	Differential I/O		35	25	44		74	
A3PE3000L/ M1A3PE3000L	Single-end I/O		147			221	341	620
	Differential I/O		65			110	168	310

Notes:
1. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.

SmartFusion SoC FPGAs

SmartFusion SoCs integrate an FPGA fabric, an ARM Cortex-M3 processor, and a programmable analog, offering full customization, IP protection, and ease-of-use. Based on Microsemi's proprietary flash process, SmartFusion SoCs are ideal for hardware and embedded designers who need a true system-on-chip that gives more flexibility than traditional fixed-function microcontrollers without the excessive cost of soft processor cores on traditional FPGAs.

- Available in commercial, industrial, and military grades
- Hard 100 MHz 32-bit ARM Cortex-M3 CPU
- Multi-layer AHB communications matrix with up to 16 Gbps throughput
- 10/100 Ethernet MAC
- Two peripherals of each type: SPI, I2C, UART, and 32-bit timers
- Up to 512 KB flash and 64 KB SRAM
- External memory controller (EMC)
- 8-channel DMA controller
- Integrated analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with 1 % accuracy
- On-chip voltage, current, and temperature monitors
- Up to ten 15 ns high-speed comparators
- Analog compute engine (ACE) offloads CPU from analog processing
- Up to 35 analog I/Os and 169 digital GPIOs

SmartFusion Devices

SmartFusion Devices	Features	A2F060	A2F200	A2F500
Logic	Logic elements (approximate)	700	2,000	6,000
	System gates	60,000	200,000	500,000
	RAM blocks (4,608 bits)	8	8	24
Microcontroller subsystem (MSS)	Flash (KB)	128	256	512
	SRAM (KB)	16	64	64
	Cortex-M3 with memory protection unit (MPU)	Yes	Yes	Yes
	10/100 Ethernet MAC	No	Yes	Yes
	External memory controller (EMC)	26-bit address, 16-bit data[1]	26-bit address, 16-bit data	26-bit address, 16-bit data[1]
	DMA	8 Ch	8 Ch	8 Ch
	I2C	2	2	2
	SPI	2	2	2
	16550 UART	2	2	2
	32-bit timer	2	2	2
	PLL	1	1	2[2]
	32 kHz low power oscillator	1	1	1
	100 MHz on-chip RC oscillator	1	1	1
	Main oscillator (32 KHz to 20 MHz)	1	1	1
Programmable analog	ADCs (8-/10-/12-bit SAR)	1	2	3[4]
	DACs (12-bit sigma-delta)	1	2	3[4]
	Signal conditioning blocks (SCBs)	1	4	5[4]
	Comparators[3]	2	8	10[4]
	Current monitors[3]	1	4	5[4]
	Temperature monitors[3]	1	4	5[4]
	Bipolar high voltage monitors[3]	2	8	10[4]

Notes:

1. Not available on A2F500 for the PQ208 package and A2F060 for the TQ144 package.
2. Two PLLs are available in CS288 and FG484, one PLL in FG256 and PQ208.
3. These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User's Guide for details.
4. Available on FG484 only. PQ208, FG256 and CS288 packages offer the same programmable analog capabilities as A2F200.

Package I/Os: MSS + FPGA I/Os

Device	A2F060[1]			A2F200[2]				A2F500[2]			
	TQ(G)144	CS(G)288	FG(G)256	PQ(G)208	CS(G)288	FG(G)256	FG(G)484	PQ(G)208	CS(G)288	FG(G)256	FG(G)484
Pitch (mm)	0.5	0.5	1.0	0.5	0.5	1.0	1.0	0.5	0.5	1.0	1.0
Length × width (mm)	20 × 20	11 × 11	17 × 17	30.6 × 30.6	11 × 11	17 × 17	23 × 23	30.6 × 30.6	11 × 11	17 × 17	23 × 23
Direct analog inputs	11	11	11	8	8	8	8	8	8	8	12
Shared analog inputs[1]	4	4	4	16	16	16	16	16	16	16	20
Total analog input	15	15	15	24	24	24	24	24	24	24	32
Total analog output	1	1	1	1	2	2	2	1	2	2	3
MSS I/Os[5]	21[4]	28[4]	26[4]	22	31	25	41	22	31	25	41
FPGA I/Os	33[3]	68	66	66	78	66	94	66[3]	78	66	128
Total I/Os	70	112	108	113	135	117	161	113	135	117	204

Notes:

1. There are no LVTTL-capable direct inputs available on A2F060 devices.
2. These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.
3. EMC is not available on the A2F500, PQ208, and A2F060 TQ144 package.
4. 10/100 Ethernet MAC is not available for A2F060.
5. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not required for MSS. These I/Os support Schmitt triggers, and support only LVTTL and LVCMOS (1.5 V/1.8 V/2.5 V/3.3 V) standards.
6. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.

Military SmartFusion2, IGLOO2 Devices

FPGAs for Military Applications

For over 25 years, Microsemi has been the leader for high reliability defense applications. Microsemi FPGAs are qualified to Mil Std 883 Class B and QML class Q. Based on flash architecture, Microsemi offers the industry's most reliable and low-power FPGAs and SoC FPGAs. Military grade FPGAs are available in IGLOO2, ProASICPlus, and ProASIC3/EL device families, and SoC FPGAs are available in SmartFusion2, SmartFusion, and Fusion device families. In addition to the advantages of the mainstream FPGAs, SoC FPGAs have an embedded ARM Cortex-M3 microcontroller on-chip. SmartFusion and Fusion devices integrate configurable analog peripherals to yield a true system-on-chip solution.

- Tested for high reliability at temperature range of –55° C to 125° C
- Product longevity
- ISO-9001 and AS-9100-certified quality management system
- PCI Express Gen1 endpoints
- Instant-on
- Small packages
- Zero FIT FPGA configuration cells
- SECDED memory protection
- Built-in tamper detection and zeroization capability
- NRBG, AES-256, SHA-256, and ECC cryptographic engine
- User physically unclonable function (PUF)
- CRI DPA pass-through license
- Lowest-power operation
- Embedded ARM Cortex-M3 microcontroller subsystem

Military SmartFusion2 and IGLOO2 Devices

SmartFusion2/ IGLOO2	Features	M2GL010 M2S010	M2GL025 M2S025	M2GL050 M2S050	M2GL060 M2S060	M2GL090 M2S090	M2GL150 M2S150
Logic/DSP	Maximum logic elements (4LUT+DFF)	12,084	27,696	56,340	56,520	86,184	146,124
	Mathblocks (18 × 18)	22	34	72	72	84	240
	PLLs and CCCs	2	6				8
	MSS (SmartFusion2) or HPMS (IGLOO2)	1					
	Security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF		
Memory	eNVM (KB)	256				512	
	eSRAM (KB)	64					
	LSRAM 18K blocks	21	31	69	69	109	236
	uSRAM 1K blocks	22	34	72	72	112	240
	Total fabric RAM (kbits)	400	592	1314	1314	2074	4488
	Total RAM (kbits)	912	1104	1826	1826	2586	5000
High-speed	DDR controllers	1x18					2x36
	SERDES lanes	4					16
	PCIe endpoints	1			2		4
User I/O	MSIO (3.3 V)	123	157	105	157	157	292
	MSIOD (2.5 V)	40	40	40	40	40	106
	DDRIO (2.5 V)	70	70	122	70	70	176
	Total user I/O	233	267	267	267	267	574
Package		FG(G)484M	FG(G)484M	FG(G)484M	FG(G)484M	FG(G)484M	FC(G)1152M

I/Os per Package

	Package Options			
Package Type	FG(G)484		FC(G)1152	
Pitch (mm)	1.0		1.0	
Length × width (mm)	23 × 23		35 × 35	
Device	I/O	Lanes	I/O	Lanes
M2S010/M2GL010 (T/TS)	233	4		
M2S025/M2GL025 (T/TS)	267	4		
M2S050/M2GL050 (T/TS)	267	4		
M2S060/M2GL060 (T/TS)	267	4		
M2S090/M2GL090 (T/TS)	267	4		
M2S150/M2GL150 (T/TS)			574	16

Notes:
1. Can migrate vertically in the same package.
2. Gold wire bonds are available for the FG484 package by appending X399 to the part number when ordering (for example, M2S090 (T/TS)-1FG484MX399).
3. All the packages are available with lead and lead free. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.

Military Smart Fusion, Fusion, and ProASIC3 Devices

Military SmartFusion, ProASIC3, and Fusion Devices

Devices	Features	A3P250	A3PE600L	A3P1000	A3PE3000L	AFS600	AFS1500	A2F060	A2F500
ARM Cortex-M1 devices[1]				M1A3P1000	M1A3PE3000L	M1AFS600	M1AFS1500	Hard 32-bit ARM Cortex-M3	Hard 32-bit ARM Cortex-M3
Logic	Logic elements (approximate)	3,000	7,000	11,000	35,000	7,000	16,000	700	6,000
	System gates	250,000	600,000	1,000,000	3,000,000	600,000	1,500,000	60,000	500,000
	PLL	1	6	1	6	2	2	1	2
	ADCs (8-,10-,12-bit SAR)					1	1	1	3
	AES-protected ISP[1]	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fabric memory	RAM (1,024 bits)	36	108	144	504	108	270	16	64
	RAM blocks (4,608 bits)	8	24	32	112	24	60	8	24
User I/O	Maximum user I/Os	68	270	300	620	212	263	108	204
	Digital I/Os	68	270	300	620	172	223	92	169
	Analog I/Os					40	40	16	35

Notes:
1. Refer to ARM Cortex-M1 product brief for more information.
2. AES is not available for ARM-enabled devices.

I/Os per Package

Devices	I/O Type	VQ(G)100	PQ(G)208	FG(G)144	FG(G)256	FG(G)484	FG(G)896
	Pitch (mm)	0.5	0.5	1.0	1.0	1.0	1.0
	Length × width (mm)	16 × 16	30.6 × 30.6	13 × 13	17 × 17	23 × 23	31 × 31
A3P250	Single-end I/O	68					
	Differential I/O	13					
A3PE600L	Single-end I/O					270	
	Differential I/O					135	
A3P1000/M1A3P1000	Single-end I/O		154	97	177	300	
	Differential I/O		35	25	44	74	
A3PE3000L/M1A3PE3000L	Single-end I/O					341	620
	Differential I/O					168	310
AFS600	Single-end I/O				119	172	
	Differential I/O				58	86	
AFS1500	Single-end I/O				119	223	
	Differential I/O				58	109	
A2F060	Analog I/O				16		
	FPGA I/O				66		
	MSS I/O				26		
A2F500	Analog I/O				26	35	
	FPGA I/O				66	128	
	MSS I/O				25	41	

Notes:
1. (G) indicates that the package is RoHS 6/6 compliant/Pb-free.

Automotive-Grade Products

Microsemi offers dedicated automotive-grade devices with various densities, features, footprints, and temperature grades. All devices and packages are AEC-Q100-qualified and tested at extended temperatures. PPAP documentation is available for ProASIC3 devices on request.

SmartFusion2 SoC FPGA Product Family

	Features	M2S005S	M2S010TS	M2S025TS	M2S060TS	M2S090TS
Logic/DSP	Maximum logic elements (4LUT + DFF)[1]	6,060	12,084	27,696	56,520	86,184
	Math blocks (18 × 18)	11	22	34	72	84
	Fabric interface controllers (FICs)	1				
	PLLs and CCCs	2		6		
	Data security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF	
MSS	Cortex-M3 + instruction cache	Yes				
	eNVM (KB)	128	256			512
	eSRAM (KB)	64				
	eSRAM (KB) non-SECDED	80				
	CAN, 10/100/1000 Ethernet, HS USB	1 each				
	Multi-mode UART, SPI, I2C, timer	1 each				
High-speed	DDR controllers (count x width)	1 × 18				
	SERDES lanes (T)	0	4			
	PCIe endpoints	0	1		2	
User I/Os	MSIO (3.3 V)	115	123	157	271	309
	MSIOD (2.5 V)	28	40	40	40	40
	DDRIO (2.5 V)	66	70	70	76	76
	Total user I/O	209	233	267	387	425

Notes :

1. Total logic may vary based on utilization of DSP and memories in the design.
2. Feature availability is package dependent.

Package Options

Type	VFG256[1]		VFG400[1]		FGG484[1]		FGG676[1]	
Pitch (mm)	0.8		0.8		1		1	
Length × width (mm)	14 × 14		17 × 17		23 × 23		27 × 27	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005S	161		171		209			
M2S010TS	138	2	195	4	233	4		
M2S025TS	138	2	207	4	267	4		
M2S060TS			207	4	267	4	387	4
M2S090TS					267	4	425	4

Note :

1. All Automotive packages are RoHS compliant and available in lead-free options only.
2. Shadeing indicates that device packages have vertical migration capability.

Automotive-Grade Products

IGLOO2 FPGA Product Family

	Features	M2GL005S	M2GL010TS	M2GL025TS	M2GL060TS	M2GL090TS
Logic/DSP	Maximum logic elements (4LUT + DFF)[1]	6,060	12,084	27,696	56,520	86,184
	Math blocks (18 × 18)	11	22	34	72	84
	PLLs and CCCs	2		6		
	SPI/HPDMA/PDMA	1 each				
	Fabric interface controllers (FICs)	1				
	Data security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF	
Memory	eNVM (KB)	128	256			512
	LSRAM 18K blocks	10	21	31	69	109
	uSRAM 1K blocks	11	22	34	72	112
	eSRAM (KB)	64				
	Total RAM (kbits)	703	912	1104	1826	2586
High speed	DDR Controllers (count × width)	1 × 18				
	SERDES lanes (T)	0	4			
	PCIe endpoints	0	1		2	
User I/Os	MSIO (3.3 V)	115	123	157	271	309
	MSIOD (2.5 V)	28	40	40	40	40
	DDRIO (2.5 V)	66	70	70	76	76
	Total user I/O	209	233	267	387	425

Notes:
1. Total logic may vary based on utilization of DSP and memories in the design.
2. Feature availability is package-dependent.

Package Options

Type	VFG2561		VFG4001		FGG4841		FGG6761	
Pitch (mm)	0.8		0.8		1		1	
Length × width (mm)	14 × 14		17 × 17		23 × 23		27 × 27	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005S	161		171	-	209			
M2S010TS	138	2	195	4	233	4		
M2S025TS	138	2	207	4	267	4		
M2S060TS			207	4	267	4	387	4
M2S090TS					267	4	425	4

Notes:
1. All automotive packages are RoHS compliant and available in lead free options only.
2. Shading indicates that device packages have vertical migration capability.

Automotive-Grade Products

The following table serves as a guide for choosing the right device for your applications. In addition, Microsemi offers more detailed product tables, Product Briefs, and Datasheets to assist in device selection.

Family	Logic Elements	Temperature Range	Maximum User I/Os	Maximum SERDES
IGLOO2[1]	6K to 86K	Grade 1 (–40 °C to 135 °C) Grade 2 (–40 °C to 125 °C)	Up to 425	4[1]
SmartFusion2	6K to 86K	Grade 2 (–40 °C to 125 °C)	Up to 425	4
ProASIC3	700K to 11K	Grade 1 (–40 °C to 135 °C) Grade 2 (–40 °C to 115 °C)	Up to 300	Not available

Notes:
1. SERDES is only supported in the IGLOO2 devices with Grade 2 temperature range, not on Grade 1 temperature range.

ProASIC3 FPGA Product Family

	Features	A3P060	A3P125	A3P250	A3P1000
Logic	System gates	60,000	125,000	250,000	1,000,000
	Equivalent LEs	700	1,500	3,000	11,000
	VersaNet globals	18	18	18	18
	AES-protected ISP[1]	Yes	Yes	Yes	Yes
	Integrated PLL in CCCs	1	1	1	1
Fabric memory	RAM (1,024 bits)	18	36	36	144
	4,608-bit blocks	4	8	8	32
	FlashROM kbits (1,024 bits)	1	1	1	1
User I/O	I/O banks	2	2	4	4
	Maximum user I/Os	96	133	157	300
Speed grade	Speed grades	Std., –1	Std., –1	Std., –1	Std., –1

Notes:
1. Six chip (main) and three quadrant global networks are available for A3P060 and above

Package Options

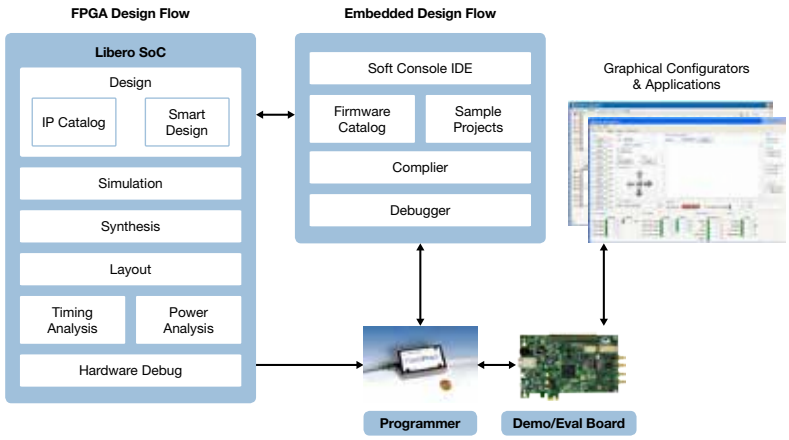
Features	A3P060	A3P125	A3P250	A3P1000
Pitch (mm)	0.5	1	1	1
Length × width (mm)	16 × 16	13 × 13	17 × 17	23 × 23
Device	I/O	I/O	I/O	I/O
A3P060	71	96		
A3P125	71	97		
A3P250	68/13	97/24		
A3P1000		97/25	177/44	300/74

Ecosystem for Microsemi FPGAs and SoC FPGAs

Libero® SoC and Libero® IDE

Libero Integrated Design Environment (IDE) is a comprehensive software toolset for designing with Microsemi FPGAs. Different versions of Libero support different families, as shown by the device support table.

Libero SoC manages the entire design flow from design entry, synthesis, and simulation, through place-and-route, timing, and power analysis, with enhanced integration of the embedded design flow. Microsemi's Libero SoC design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools that are used for designing with Microsemi's power-efficient flash-based devices. The suite integrates industry-standard Synopsys Synplify Pro synthesis and Mentor Graphics ModelSim simulation with best-in-class constraints management, debug capabilities, timing analysis, power analysis, secure production programming, and push button-design flow.



This comprehensive suite features an intuitive design flow with GUI wizards to guide the design process. Its easy-to-adopt, single-click synthesis-to-programming flow integrates industry-standard third-party tools, and a rich IP library of DirectCores and CompanionCores, and it supports complete reference designs and development kits.

Libero System Builder

Libero System Builder makes it easy to configure various subsystems and generate a required application programming interface (API) that implements a correct-by-construction infrastructure for your application. It can be used to configure the SmartFusion2 MSS block (peripherals and memory), FPGA fabric, peripherals, and memory based on high-level design specifications.

Libero SoftConsole

Libero SoftConsole provides a flexible, easy-to-use GUI for managing embedded software development projects. SoftConsole enables users to quickly develop, edit, and debug software programs.

IAR Embedded Workbench

IAR Embedded Workbench is the integrated development environment (IDE) from IAR Systems for building and debugging embedded applications of SmartFusion2 and SmartFusion. It includes project management, editing, build, and debugger tools.

Keil Microcontroller Development Kit

Keil Microcontroller Development Kit (MDK) provides an easy compiling-and-debugging tools library for embedded applications using the MSS block of SmartFusion2 and SmartFusion.

Embedded Design Support

CMSIS COMPLIANT	Microsemi	KEIL An ARM® Company	IAR SYSTEMS
Software IDE	**SoftConsole**	**Keil MDK**	**IAR Embedded Workbench®**
Free versions from microsemi	Free with Libero SoC	32K code limited	32K code limited
Available from vendor	N/A	Full version	Full version
Compiler	GNU GCC	RealView® C/C++	IAR ARM Compiler
Debugger	GDB debug	µVision Debugger	C-SPY® Debugger
Instruction set simulator	No	µVision Simulator	Yes
Debug hardware	FlashPro4/5	ULINK®2 or ULINK-ME	J-LINK™ or J-LINK lite
Trace capability	No	ULINKpro	JTAGjet-Trace

Ecosystem for Microsemi FPGAs and Soc FPGAs

Device Support

Product Family	Device	Software		License Type			
		Libero IDE	Libero SoC	Eval (Free)	Silver (Free)	Gold	Platinum/ Standalone
RTG4	RT4G150		✓	✓			✓
SmartFusion2, IGLOO2	M2S005, M2S010, M2S025 (T devices included) M2GL005, M2GL010, M2GL025 (T devices included)		✓	✓	✓	✓	✓
	All SmartFusion2 and IGLOO2 devices, (including S devices)		✓	✓		✓	✓
SmartFusion, IGLOO, ProASIC3, Fusion	All devices		✓	✓	✓	✓	✓
ProASIC and ProASIC^{PLUS}	All devices	✓				✓	✓
RTAX-S	RTAX250S, RTAX1000S	✓				✓	✓
	RTAX2000S, RTAX4000S	✓					✓
RTAX-DSP	RTAX2000D, RTAX4000D	✓					✓
RT ProASIC3	RT3PE600L		✓			✓	✓
	RT3PE3000L		✓				✓
RTSX-SU	All devices	✓				✓	✓
Axcelerator	AX125, AX250, AX500, AX1000	✓				✓	✓
	AX2000	✓					✓
SX-A, eX, MX	All devices	✓				✓	✓

License Types

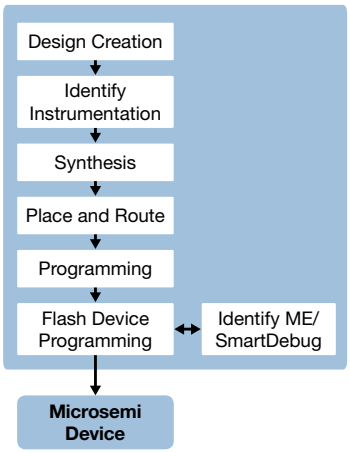
	Evaluation	Silver	Gold	Platinum	Standalone Archive	Standalone (1 year)
Validity	30 days	One year	One year	One year	Permanent (no upgrades)	One year
DirectCores	Libero IP bundle obfuscated and selected RTL IPs	Libero IP bundle obfuscated and selected RTL IPs	Libero IP bundle obfuscated and selected RTL IPs	RTL for Libero IP bundle cores	RTL for Libero IP bundle cores	Libero IP bundle obfuscated and selected RTL IPs
Simulation	ModelSim ME Pro mixed language simulation	ModelSim ME single language simulation	ModelSim ME Pro mixed language simulation	ModelSim ME Pro mixed language simulation	Not applicable	Not applicable
Synthesis	Synplify Pro	Synplify Pro	Synplify Pro	Synplify Pro	Not applicable	Not applicable
Programming	Not supported	Supported	Supported	Supported	Supported	Supported
Identify	Not supported	Supported	Supported	Supported	Not supported	Not supported
Price/Renewal	$0	$0	$995/$695	$3495/$2995 (node locked) $3995/$3495 (floating)	$6995	$1995/$1495

Debug

Microsemi's debug tools and device features complement design simulations and development by allowing verification and troubleshooting at the hardware level. Having successfully passed functional and post-layout simulations, Microsemi's design debug tools can help provide the designer with a pre-system-level implementation early warning for other design issues. Microsemi design debug focuses on analysis of the key elements of a design, such as the embedded non-volatile memory (eNVM) data, SRAM data, logic elements, and system builder blocks.

Microsemi's debug software is available in two variants: SmartDebug and Identify ME.

Identify ME SmartDebug Flow



SmartDebug

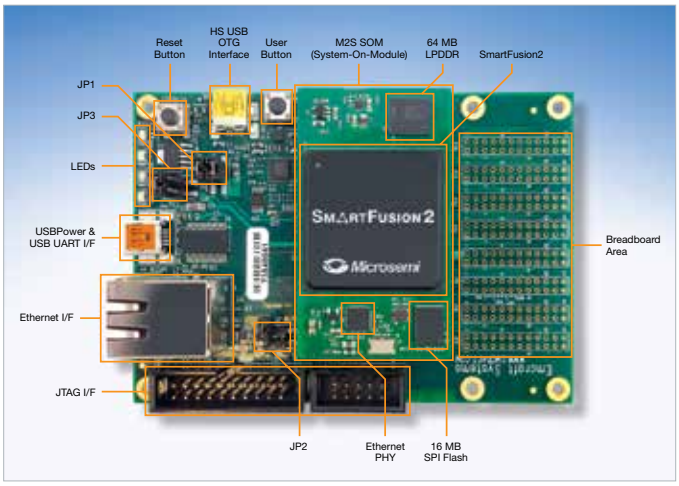
A Microsemi proprietary tool that allows FPGA designers to quickly find and correct functional design bugs by probing the internal static and dynamic signals, eNVM and u/LSRAM memory block, and the SERDES block of the FPGA. This tool supports IGLOO2 and SmartFusion2 only.

Identify ME®

Identify ME is a third-party, on-chip debugging tool from Synopsys that allows the Microsemi FPGA designer to quickly find and correct functional design bugs by probing internal signals of the design directly from the flash FPGA at the system speed.

Development Kits

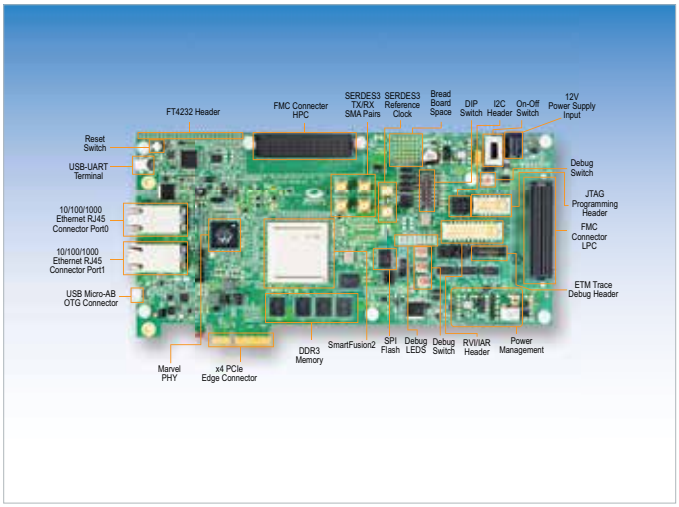
SmartFusion2 Starter Kit



- Cost-efficient development platform for SmartFusion2 SoC FPGA
- Supports industry-standard interfaces, including Ethernet, USB, SPI, I²C, and UART
- Preloaded with uClinux image to support Linux-based development environments
- Comes with FlashPro4 programmer, USB cables, and USB WiFi module
- Board features
  - 50K LE or 10K LE SmartFusion2 device
  - JTAG interface for programming and debug
  - 10/100 Ethernet
  - USB 2.0 On-The-Go
  - 64 MB LPDDR, 16 MB SPI flash memory
  - Four LEDs and two push-button switches

Ordering Code	Supported Device	Price
SF2-STARTER-KIT	M2S050-FGG484	$299
SF2-484-STARTER-KIT	M2S010-FGG484	$299
SF2060-STARTER-KIT	M2S060-FGG484	$299

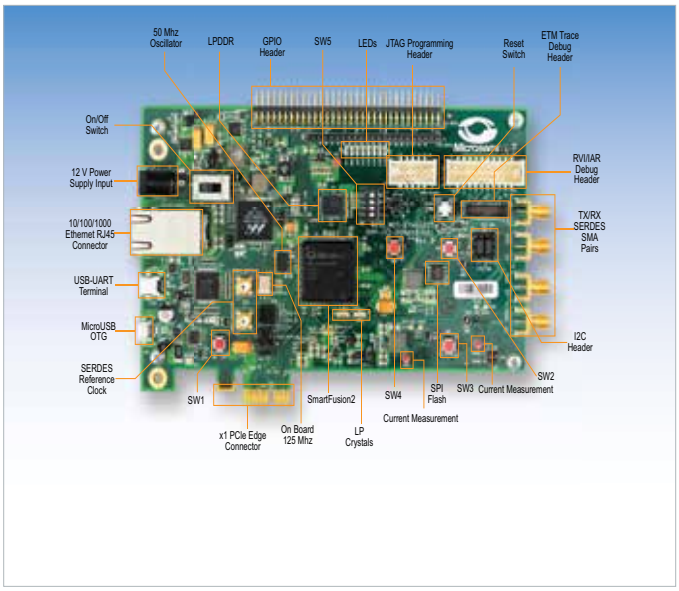
SmartFusion2 Advanced Development Kit



- Full featured kit to develop applications using SmartFusion2 SoC FPGAs
- Enables power measurement
- Two FMC connectors with HPC/LPC pinout for expansion
- Various communication interfaces, switches, and LEDs for prototyping
- Kit comes with free 1-year Gold Libero SoC license
- Board features
  - 150K LE SmartFusion2 device
  - DDR3 SDRAM, SPI flash
  - Current measurement test points
  - A pair of SMA connectors, two FMC connectors, PCIe x4 edge connector
  - 2xRJ45 interface for 10/100/1000 Ethernet USB micro-AB connector
  - FTDI programmer interface to program the external SPI flash
  - JTAG/SPI programming interface, RVI header for application programming, and debug
  - Quad 2:1 MUX/DEMUX high-bandwidth bus switch
  - Dual in-line package (DIP) switches for user application
  - Push-button switches and LEDs for demo purposes

Ordering Code	Supported Device	Price
M2S150-ADV-DEV-KIT	M2S150TS-1FCG1152	$999

SmartFusion2 Security Evaluation Kit



- Evaluate the data security features of SmartFusion2 SoC FPGAs
- Develop and test PCI Express Gen2 x1 lane designs
- Test the signal quality of the FPGA transceiver using full-duplex SERDES SMA pairs
- Measure the low power consumption of the SmartFusion2 SoC FPGA
- Quickly create a working PCIe link with the included PCIe control plane demo
- Kit includes free 1-year Gold Libero SoC license
- Board features
  - 90 K LE SmartFusion2 device
  - 64 Mbit SPI flash memory
  - 512 MB LPDDR
  - PCI Express Gen2 x1 interface
  - Four SMA connector for testing of full-duplex SERDES channel
  - RJ45 interface for 10/100/1000 Ethernet
  - JTAG/SPI programming interface
  - Headers for I²C, SPI, GPIOs
  - Push-button switches and LEDs for demo purposes
  - Current Measurement Test Points

Ordering Code	Supported Device	Price
M2S090TS-EVAL-KIT	M2S090TS-FGG484	$399

Development Kits

Arrow SF2+ Development Kit

The SF2+ Development Kit Includes

- M2S010 SOM with LPDDR, SPI Flash, Ethernet PHY (Additional Emcraft SmartFusion2 SOMs available)
- Timberwolf Audio Processor with 2 MEMs MICs and Speaker Jack
- Microsemi's LX7186A switching regulator and LX8213 LDO
- Arduino and PMOD Connectors
- Push Buttons, DIP Switches, LEDs
- RJ45 Ethernet Connector
- Embedded FlashPro5
- USB for Power, UART and Debug
- Test Points

- Along with the SF2+ Development Kit hardware, three separate designs are delivered:
  - 90 K LE SmartFusion2 device
  - Low power application that features the Flash*Freeze capabilities of the SmartFusion2 SoC FPGA.
  - Audio application that features the Timberwolf audio processor to record and play back audio.
  - uClinux boot demo only
    Note the uClinux boot is demo only, source is not provided. Customers can access details from Emcraft directly:emcraft.com/products/255

Ordering Code	Supported Device	Price
SF2PLUS-DEV-KIT	M2S010-FCG484	$125 available from ARROW

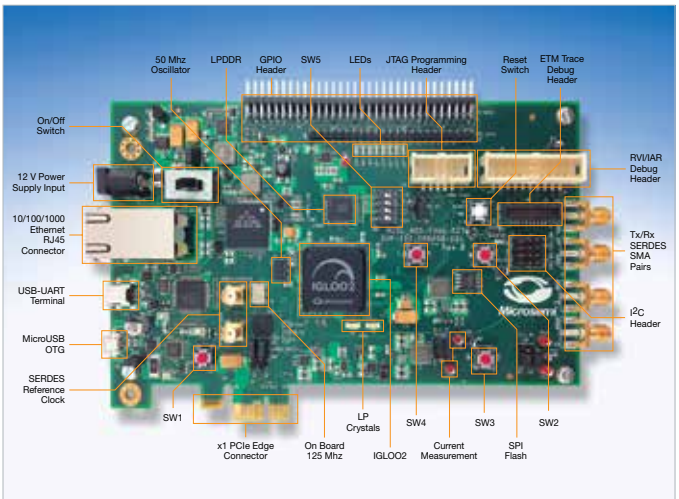
Future Creative Development Board

Future's Creative Development Board includes

- Microsemi IGLOO2 FPGA or SmartFusion2 SoC FPGA
- Microsemi LX7167 DC/DC
- Alliance 32M × 16-bit DDR2 synchronous DRAM (SDRAM)
- Microchip 64 Mbit serial flash
- Microchip six synchronous sampling 16/24-bit resolution Delta-Sigma A/D converters
- On-board FTDI USB-JTAG adaptor
- Arduino™-compatible expansion headers
- MikroBUS™-compatible expansion headers
- PMOD™-compatible expansion connector
- User buttons and LED
- Available in two variants, one with an IGLOO2 FPGA and one with a SmartFusion2 SoC FPGA
- 25K (LE) FPGA, offering the lowest cost-of-entry for both software and hardware engineers who want to evaluate and implement their own unique designs
- Microsemi's LX series power devices

Ordering Code	Supported Device	Price
FUTUREM2GL-EVB	M2GL025	$49.95 (available from Future Electronics)
FUTUREM2SF-EVB	M2S025	

IGLOO2 Evaluation Kit



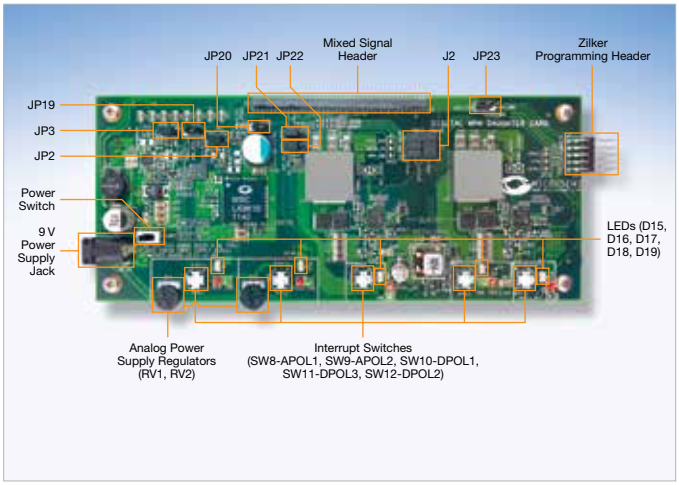
- Gives designers access to IGLOO2 FPGAs that offer leadership in I/O density, security, reliability, and low-power for mainstream applications
- Supports industry-standard interfaces including Gigabit Ethernet, USB 2.0 OTG, SPI, I²C, and UART
- Comes preloaded with a PCIe control plane demo
- Can be powered by a 12 V power supply or the PCIe connector, and includes a FlashPro4 programmer

- Board features
  - IGLOO2 FPGA in the FGG484 package (M2GL010T-1FGG484)
  - JTAG/SPI programming interface
  - Gigabit Ethernet PHY and RJ45 connector
  - USB 2.0 OTG interface connector
  - 1 GB LPDDR, 64 MB SPI flash
  - Headers for I²C, UART, SPI, GPIOs
  - ×1 Gen2 PCIe edge connector
  - Tx/Rx/Clk SMP pairs

Ordering Code	Supported Device	Price
M2GL-EVAL-KIT	M2GL010T-1FGG484	$399

Development Kits

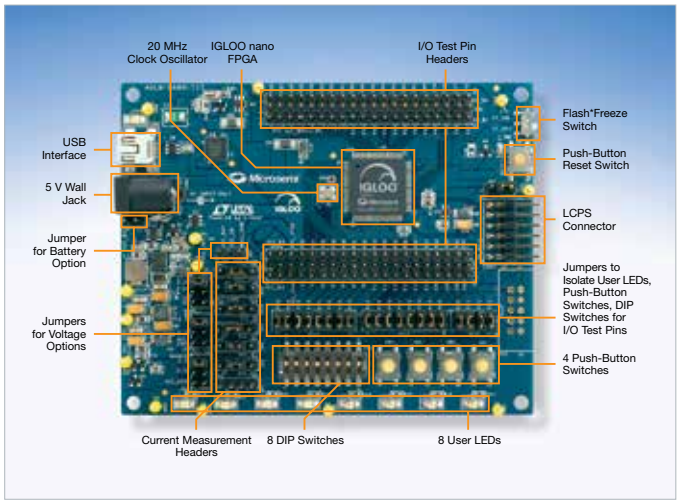
DMPM Daughter Card



- Supports power management design with the SmartFusion Evaluation Kit and SmartFusion Development Kit
- MPM v5.0 design example implements configurable power management in SmartFusion SoC FPGA
- Graphical configuration dialog
- In-system reconfigurable
- 9V power supply
- Board features
  - Two analog PoLs, three Digital PoLs
  - Two potentiometers to control analog regulators
  - Five power supply regulator interrupt switches
  - Five power supply regulator status LEDs
  - Mixed signal header connector connects to SmartFusion board

Ordering Code	Supported Device	Price
DMPM-DC-KIT	AGLN250V2-VQG100	$330

IGLOO nano Starter Kit

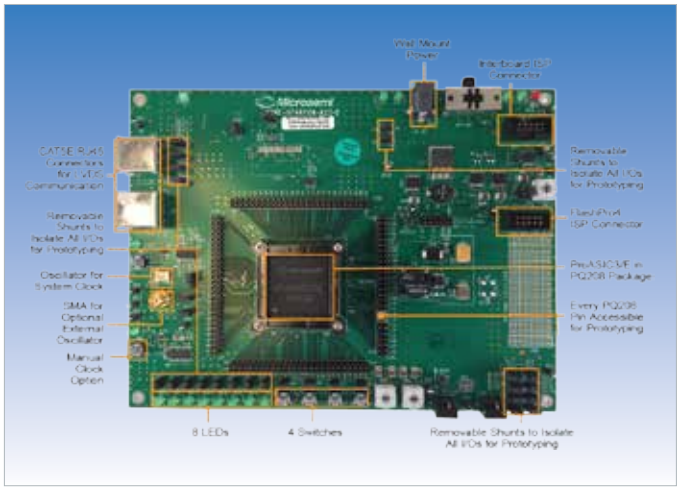


- Supports basic ProASIC3 FPGA design and LVDS I/O usage
- Free one-year Libero SoC software with Silver license
- FlashPro3 or FlashPro4 Programmer
- 9 V power supply and international adapters
- Kit user's guide, Libero SoC tutorial, and design examples
- PCB schematics, layout files, and BOM
- Board features
  - Eight I/O banks with variety of voltage options
  - Oscillator for system clock or manual clock option
  - LEDs and switches for simple inputs and outputs
  - LCD display module
  - Two CAT5E RJ45 connectors for high-speed LVDS communications
  - All I/Os available for external connections
  - Not RoHS-compliant

Ordering Code	Supported Device	Price
AGLN-NANO-KIT*	AGLN250V2-VQG100	$99

Note:
* Replaces -Z version of the nano Starter Kit.

ProASIC3 Starter Kit



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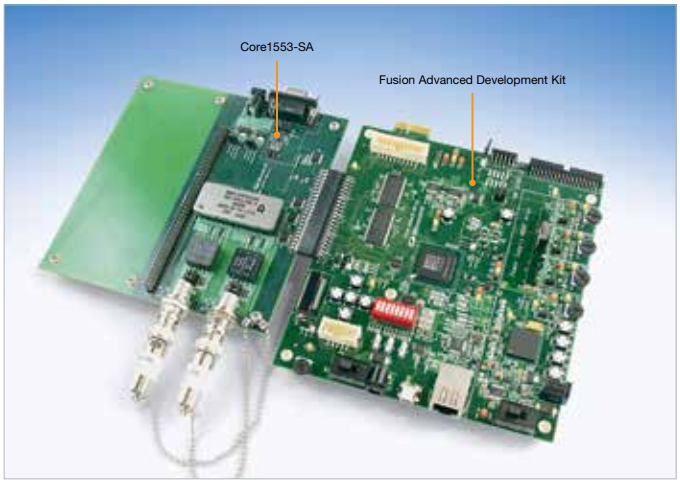
- 9 V power supply and international adapters
- Kit user's guide, Libero SoC tutorial, and design examples
- PCB schematics, layout files, and BOM
- Board features
  - Eight I/O banks with a variety of voltage options
  - Oscillator for system clock or manual clock option
  - LEDs and switches for simple inputs and outputs
  - LCD display module
  - Two CAT5E RJ45 connectors for high-speed LVDS communications
  - All I/Os available for external connections
  - Not RoHS-compliant

Ordering Code	Supported Device	Price
A3PE-STARTER-KIT-2	A3PE1500-PQ208	$580

Development Kits

Core1553 Development Kit



- Allows users to evaluate the functionality of Microsemi's Core1553BRM without having to create a complete MIL-STD-1553B compliant system
- Fusion advanced development kit with two 9V power supplies
- Core1553 daughter card
- User guide, tutorial, and design example
- PCB schematics, layout files and BOM
- Purchasing the kit gives the owner the right to the programming file of the demo, but not an evaluation of the IP. The IP evaluation or purchase is quoted separately.
- Board features
  - MIL-STD-1553B transceiver, two transformers, and two concentric twinax connectors are included on the Core1553 daughter board
  - MIL-STD-1553B concentric twinax connectors are center pin signal high and cylindrical contact signal low
  - Connectivity is MIL-C-49142-compliant
  - Evaluate and develop medium speed on-board data communications bus solutions for MIL-STD-1553B/ UK DEF-STAN 00-18 (Pt.2)/ NATO STANAG 3838 AVS/Avionic Standards Coordinating Committee Air-Std 50/2
  - CAN bus interface support
  - Connector to ARINC 429 daughter board (CORE429-SA)

Ordering Code	Description	Price
CORE1553-DEV-KIT	Core1553 development kit	$3,500
CORE1553-SA	Core1553 daughter card	$2,600

Additional Hardware Kits

Microsemi offers hardware choices for SoC FPGA and FPGA products. The following table lists additional popular kits available. Full details of these kits can also be found online with user's guides and accompanying tutorials.

FPGA Family	Ordering Code	Name	Device	Price	Power
SmartFusion	MIXED-SIGNAL-DC	Mixed signal daughter card	None	$65	
SmartFusion	A2F-EVAL-KIT-2	SmartFusion evaluation kit	A2F200M3F-FGG484	$99	USB
Fusion	AFS-EVAL-KIT	Fusion starter kit	AFS600-FG256	$380	9 V
Fusion	M1AFS-ADV-DEV-KIT-PWR-2	Fusion advanced development kit	M1AFS1500-FGG484	$820	9 V
Fusion	M1AFS-EMBEDDED-KIT-2	Fusion embedded development kit	M1AFS1500-FGG484	$300	5 V
IGLOO	AGLN-NANO-KIT	IGLOO nano starter kit	AGLN250V2-ZVQG100	$99	USB
IGLOO	AGLP-EVAL-KIT	IGLOO PLUS starter kit	AGLP125V2-CSG289	$299	5 V
IGLOO	M1AGL1000-DEV-KIT	ARM Cortex-M1 IGLOO development kit	M1AGL1000V2-FGG484	$600	5 V
ProASIC3	M1A3PL-DEV-KIT	ARM Cortex-M1 ProASIC3L development kit	M1A3P1000L-FGG484	$600	5 V

Programming

Microsemi's solution makes programming and debugging easy, secure, and convenient.

Programming Resources

- JTAG programming
- SPI-slave programming
- MSS in-system-programming (SoC FPGAs only)
- Auto programming
- Auto update
- In-application-programming (IAP)

FlashPro

The Microsemi FlashPro programming system is a combination FlashPro software and hardware programmer. Together, they provide in-system programming (ISP) for the following families: IGLOO2, SmartFusion2, IGLOO, ProASIC3 (including RT ProASIC3), SmartFusion, Fusion, ProASICPLUS, and ProASIC.

For more information about adapter modules, see:
http://www.microsemi.comproducts/fpga-soc/design-resources/programming/flashpro

FlashPro Programming Software

FlashPro programming software comes bundled with the Libero SoC or as a standalone download. The programming software is also available in two variants, FlashPro software (Windows only), and FlashPro Express software (Windows and Linux).

SiliconSculptor3

Silicon Sculptor 3 is an FPGA programming tool that delivers high-data throughput and promotes ease of use, while lowering the overall cost of ownership.

Silicon Sculptor 3 includes a high-speed USB 2.0 interface that allows you to connect as many as 12 programmers to a single PC using a standalone software. Silicon Sculptor is an ideal solution for programming multiple high-density devices concurrently in the production environment.

For more information about adapter modules, see:
http://www.microsemi.com/products/fpga-soc/design-resources/programming/silicon-sculptor-3

Programmer	Supported Device	Support	Price
FlashPro5	ProASIC3/E, ProASIC nano, IGLOO/e, IGLOO Plus, IGLOO nano, Fusion, SmartFusion, SmartFusion2, IGLOO2, RTProASIC3	USB 2.0 Windows and Linux	$49
FlashPro4	ProASIC3/E, ProASIC nano, IGLOO/e, IGLOO Plus, IGLOO nano, Fusion, SmartFusion, SmartFusion2, IGLOO2, RTProASIC3	USB 2.0 Windows	$49
FlashPro Lite	ProASIC^{PLUS}	Parallel port only Windows	$150
		Software support until 9.1	
Silicon Sculptor III	All Flash and antifuse devices	USB 2.0 Windows	$3,960

DirectC/SPI-DirectC

DirectC and SPI-DirectC can be used for making minor modifications to the source code, adding the necessary application programming interface (API), and compiling the source code and the API to create a binary executable.

STAPL Player

The STAPL Player can be used to program ProASIC^{PLUS}, as well as third-generation flash devices such as SmartFusion2, IGLOO2, SmartFusion, IGLOO, ProASIC3, ProASIC3L, and Fusion. It interprets the contents of a STAPL file, which is generated by Microsemi's Libero SoC and IDE software tools. The STAPL Player reads the STAPL file and executes the file's programming instructions.

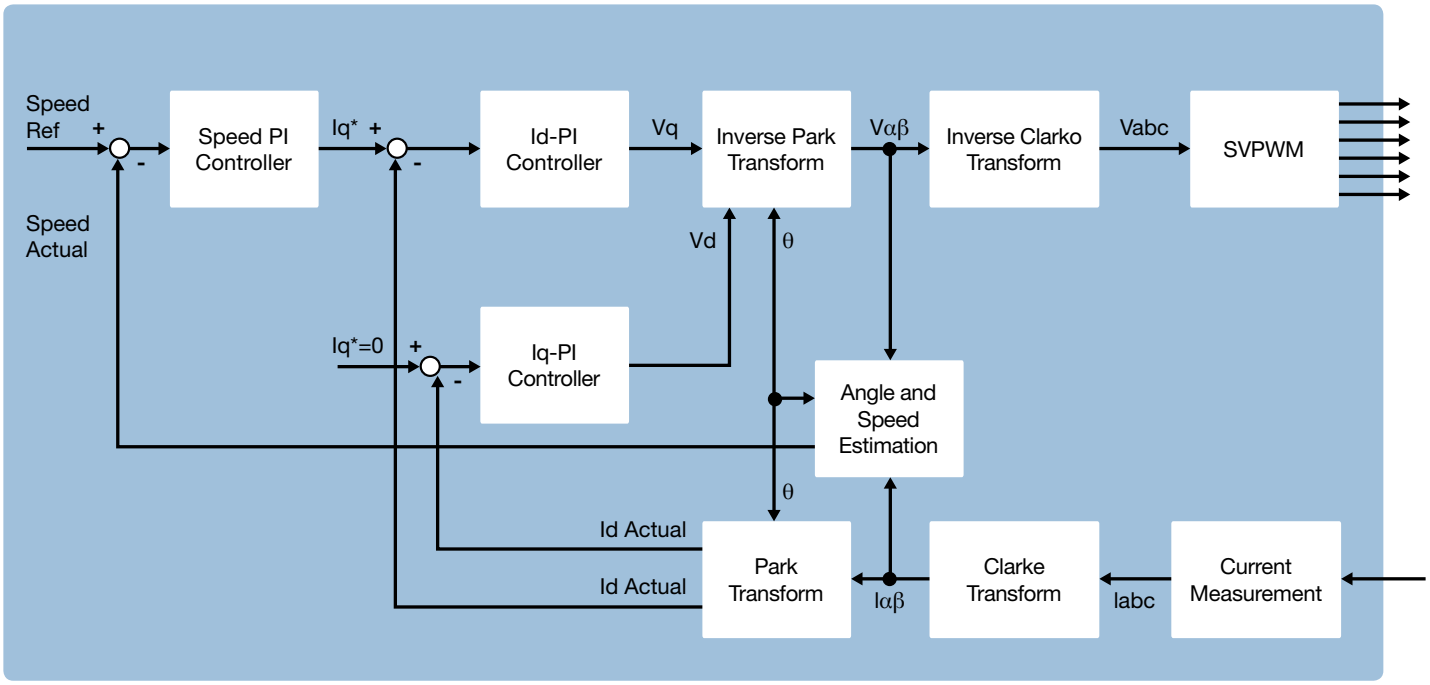
Motor Control Solution

Build Safe and Reliable Deterministic Motor Control Applications

Microsemi's Deterministic Motor Control Solution is specially designed to meet the challenging requirements of performance, reliability, and safety in an easy-to-use environment. The solution is compliant with industry coding standards for developing safe and reliable software for embedded applications. Microsemi offers a modular intellectual property (IP) portfolio, tools, reference designs, kits, and software to control motors such as permanent-magnet synchronous motor (PMSM)/brushless DC (BLDC), and stepper motors.

Ordering Code	Supported Device	Price
SF2-MC-STARTER-KIT	M2S010-FG484	$899

Field Oriented Control-System Diagram



Reference Design Features

- Dual-axis deterministic motor control on a single system-on-chip (SoC) field programmable gate array (FPGA).
- Efficient, reliable, and safe drive/motor control with product longevity.
- A compact solution that saves board space and reduces product size.
- Motor performance is tested for speeds exceeding 100,000 RPM for sensorless field-oriented control (FOC).
- Low latency of 1 µs for FOC loop from ADC measurement to PWM enables switching frequencies up to 500 kHz.
- Design flexibility with modular IP suite.
- Advanced safety features, such as automatic motor restart and overcurrent protection.
- SoC integration of system functions lowers total cost of ownership (TCO).

Microsemi Intellectual Property

Microsemi enhances your design productivity by providing an extensive suite of proven and optimized IP Cores for use with Microsemi FPGAs and SoC FPGA that covers key markets and applications. IPs are organized as either Microsemi-developed DirectCores™ or third-party-developed CompanionCores.™

IP cores are searchable at: http://soc.microsemi.com/products/ip/search/default.aspx

Microsemi DirectCore

Microsemi develops and supports DirectCore IP cores for applications with the widest possible interest. Most DirectCores are available for free within our Libero tool suite. Common communications interfaces, peripherals, and processing elements are all available as DirectCores. The following list shows Microsemi's DirectCore offerings.

Functionality	DirectCore Examples
Connectivity	UART,16550, 429, PCI, JESD204B
DSP	CIC, FFT, FIR, CORDIC, RS
Memory Controller	FIFO, DDR, QDR, SDR, MemCtrl, MMC
Processor	Cortex-M3, 8051, 8051s, ARM7TDMI
Ethernet	MII, RGMII, GMII, SGMII
Security	DES, 3DES, AES, SHA
Error Correction	EDAC, RC

Microsemi CompanionCore

Microsemi CompanionCore Partners use their detailed system knowledge of common applications to craft optimized solutions targeted for Microsemi FPGAs and SoC FPGA. CompanionCores are available for purchase from our partners and are easily integrated into your design using our Libero tool suite. The following list shows examples of CompanionCore Partners offerings.

Functionality	CompanionCore Examples
Connectivity	CAN, CANFD, PCIE, VME
DSP	FFT, JPEG, RS, DVBMOD
Memory Controller	SDRAMDDR, Flash, SD
Processor	80188, 80186, LEON3, 6809
Security	MD5, ARC4, RNG, ZUC, AES, SHA, 802.1ae (MACSec)
Error Correction	RS

Microsemi IP Available for Use with Libero

Please contact your local Microsemi sales representative for information on price and licensing , as certain Microsemi IPs may require a separate license. CompanionCores supported by Microsemi are available at the following website: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores#companioncores.

Product Name	Obfuscated RTL Available for Purchase	RTL Source Available for Purchase
CoreFFT	Not available	RTL source
Core1553BRM	Obfuscated RTL	RTL source
Core1553BRT, Core1553BRT_APB	Obfuscated RTL	RTL source
Core429, Core429_APB	Obfuscated RTL	RTL source
CorePCIF, CorePCIF_AHB	Obfuscated RTL	RTL source
CoreTSE, CoreTSE_AHB	Obfuscated RTL	RTL source
CoreCIC	Not available	RTL source

Notes:
1. Additional cores and configurations can be found on the website and in core handbooks.

High-Speed Serial Interfaces

The high-speed serial interface solution is comprised of configurable functional blocks, IPs, and reference designs. The high-speed serial interface block in SmartFusion2 and IGLOO2 product families—also known as serializer/deserializer (SERDES)—integrates several functional blocks to support multiple protocols like PCIe, Ethernet, XAUI, and EPCS.

- Gen1/Gen2 rates at x1, x2, and x4 links.
- Endpoint topology.
- Single-function/single-VC.
- Receiver and transmit buffers support error correction and coding (ECC).
- Fabric interface options of AXI3 master/slave or AHB32 master/slave.
- Address translation window support between PCIe and local device address space.

For more information about SERDES solutions, see http://www.microsemi.com/products/fpga-soc/technology-solutions/serdes-pci-express#overview.

PCIe

Microsemi offers an implementation of the PCIe protocol using the high-speed SERDES blocks. These blocks provide a fully hardened PCIe endpoint implementation, in compliance with PCIe base specification revisions 1.1 and 2.0.

- Data rates ranging from 1 Gbps to 5 Gbps per lane.
- Supports 16 lanes up to 5 Gbps each.
- Two reference clocks per SERDES block with 4 lanes each.
- Embedded PRBS generation/checking, debug, and loopback functions supported with the SmartDebug module of Libero SoC.
- User programmable emphasis and continuous time linear equalization.
- Data rates lower than 1 Gbps supported with a 3x oversampling reference design.

For more information about PCIe solution, see http://www.microsemi.com/products/fpga-soc/technology-solutions/serdes-pci-express#pci-express.

Ethernet

IEEE 802.3-specified high-data rates are supported using the embedded Ethernet MAC and PCS layer of the MSS and soft IP blocks. Reference designs and application notes enable rapid development of SGMII, GMII, and XAUI protocols.

- Support for 10/100/1000 Mbps up to 100 Gbps.
- Embedded XAUI block as part of the SERDES block.
- Microcontroller subsystem (MSS) Ethernet MAC — fully embedded MAC with SGMII or GMII physical layer interface.

For more information about Ethernet solutions, see http://www.microsemi.com/products/fpga-soc/technology-solutions/serdes-pci-express#ethernet.

JESD204B

A complete solution for implementing the JEDEC JESD204B serial interface standard is available to interface external data converters using the SERDES blocks. CoreJESD204BTX (transmitter) can be used to interface digital-to-analog convertors and JESD204BRX (receiver) can be used to interface to analog-to-digital convertors. Rx and Tx IP cores support data rates up to 3.2 Gbps at link widths of x1, x2, and x4. The cores can be reconfigured through the APB interface to allow EPCS mode to achieve a higher data rate.

- Enables interfacing JESD204B-compliant ADC/DAC convertors.
- Supports x1, x2, or x4 lanes.
- Performs word alignment and 8 B/10 B decoding and encoding.
- Recovers link configuration parameters and sources it with user-selected parameter values during the initial lane synchronization sequence.
- Lane alignment sequence generation, buffering, monitoring, and correction.
- Performs user-enabled frame alignment, monitoring, and correction.
- Performs octet reconstruction, user-enabled descrambling/scrambling, alignment character generation, and error detection.

For more information about JESD204B solution, see http://www.microsemi.com/products/fpga-soc/technology-solutions/serdes-pci- express#jesd204b

Microsemi is continually adding new products to its industry-leading portfolio.

For the most recent updates to our product line and for detailed information and specifications, please call, email, or visit our website.

Toll-free: 800-713-4113

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www.microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View A3P250-QNG132 on WIN SOURCE
- Microsemi Corporation Information

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- Alternative Solution
- Excess Inventory Management