THE DATASHEET OF

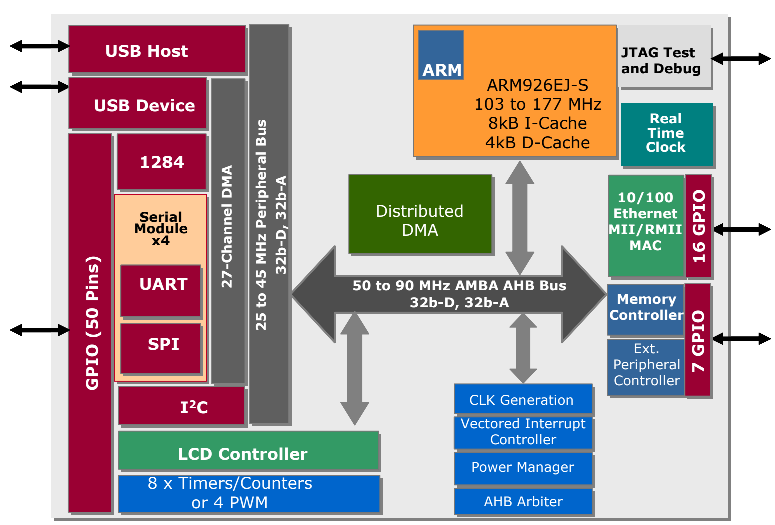
NS9360B-0-C103

NS9360 Datasheet

The Digi NS9360 is a single chip 0.13μm CMOS network-attached processor. The CPU is the ARM926EJ-S core with MMU, DSP extensions, Jazelle Java accelerator, and 8 kB of instruction cache and 4 kB of data cache in a Harvard architecture. The NS9360 runs up to 177 MHz, with a 88 MHz system and memory bus and 44 MHz peripheral bus. The NS9360 operates at a 1.5V core and 3.3V I/O ring voltages.

With its extensive set of I/O interfaces, Ethernet high-speed performance and processing capacity, the NS9360 is the most capable highly-integrated 32-bit network-attached processor available. The NS9360 is designed specifically for use in high-performance intelligent networked devices and Internet appliances including high-performance/low-latency remote I/O, intelligent networked information displays, and streaming and surveillance cameras. The NS9360 is a member of the award-winning NET+ARM family of system-on-chip (SOC) solutions for embedded systems.

NS9360
272 - pin BGA, lead-free, RoHS compliant



The NS9360 offers a connection to an external bus expansion module as well as a glueless connection to SDRAM, PC100 DIMM, Flash, EEPROM, and SRAM memories. It includes a versatile embedded LCD controller supporting up to 64K color TFT or 3375 color STN LCD display. The NS9360 features a USB port for applications requiring WLAN, external storage, or external sensors, imagers, or scanners. Four multi-function serial ports, an I^2C port, and 1284 parallel port provide a standard glueless interface to a variety of external peripherals. The NS9360 features up to 73 general purpose I/O (GPIO) pins and highly-configurable power management with sleep mode.

NET+ARM processors are the foundation for the NET+Works® family of integrated hardware and software solutions for device networking. These comprehensive platforms include drivers, operating systems, networking software, development tools, APIs, and complete development boards.

Using the NS9360 and associated Net+Works packages allows system designers to achieve dramatic time-to-market reductions with pre-integrated and tested NET+ARM hardware, NET+Works software, and tools. Product unit costs are reduced dramatically with complete system-on-chip, including Ethernet, display support, a robust peripheral set, and the processing headroom to meet the most demanding applications. Customers save engineering resources, as no network development is required. Companies will reduce their design risk with a fully integrated and tested solution.

A complete NET+Works development package includes ThreadX™ picokernel RTOS, Green Hills™ MULTI® 2000 IDE or Microcross GNU X-Tools™, drivers, networking protocols and services with APIs, NET+ARM-based development board, Digi-supplied utilities, Integrated File System, JTAG In Circuit Emulator (ICE), and support for Boundary Scan Description Language (BSDL). One year software maintenance and technical support is available.

Contents

NS9360 Features

32-bit ARM926EJ-S RISC processor

- 103 to 177 MHz
- 5-stage pipeline with interlocking
- Harvard architecture
- 8 kB instruction cache and 4 kB data cache
- 32-bit ARM and 16-bit Thumb instruction sets. Can be mixed for performance/code density tradeoffs
- MMU to support virtual memory-based OSs such as Linux, WinCE/Pocket PC, VxWorks, others
- DSP instruction extensions, improved divide, single cycle MAC
- ARM Jazelle, 1200CM (coffee marks) Java accelerator
- EmbeddedICE-RT debug unit
- JTAG boundary scan, BSDL support

External system bus interface

- 32-bit data, 32-bit internal address bus, 28-bit external address bus
- Glueless interface to SDRAM, SRAM, EEPROM, buffered DIMM, Flash
- 4 static and 4 dynamic memory chip selects
- 1-32 wait states per chip select

  A shared Static Extended Wait register allows transfers to have up to 16368 wait states that can be externally terminated.
- Self-refresh during system sleep mode
- Automatic dynamic bus sizing to 8 bits, 16 bits, 32 bits
- Burst mode support with automatic data width adjustment
- Two external DMA channels for external peripheral support

System Boot

- High-speed boot from 8-bit, 16-bit, or 32-bit ROM or Flash
- Hardware-supported low cost boot from serial EEPROM through SPI port (patent pending)

High performance 10/100 Ethernet MAC

- 10/100 Mbps MII/RMII PHY interfaces
- Full-duplex or half-duplex
- Station, broadcast, or multicast address filtering
- 2 kB RX FIFO
- 256 byte TX FIFO with on-chip buffer descriptor ring
  - Eliminates underruns and decreases bus traffic
- Separate TX and RX DMA channels
- Intelligent receive-side buffer size selection
- Full statistics gathering support
- External CAM filtering support

Flexible LCD controller

- Supports most commercially available displays:
  - 18-bit active Matrix color TFT displays
  - Single and dual panel color STN displays
  - Single and dual-panel monochrome STN displays
- Formats image data and generates timing control signals
- Internal programmable palette LUT and grayscaler support different color techniques
- Programmable panel-clock frequency

USB ports

- USB v.2.0 full speed (12 Mbps) and low speed (1.5 Mbps)
- Independent OHCI Host and Device ports
- Internal USB PHY
- External USB PHY interface
- USB device supports one bidirectional control endpoint and 10 unidirectional endpoints
- All endpoints supported by a dedicated DMA channel
- 32 byte FIFO per endpoint

Serial ports

- 4 serial modules, each independently configurable to UART mode, SPI master mode, or SPI slave mode
- Bit rates from 75 bps to 921.6 kbps: asynchronous x16 mode
- Bit rates from 1.2 kbps to 11.25 Mbps: synchronous mode
- UART provides:
  - High-performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7, or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers
- Internal or external clock support, digital PLL for RX clock extraction
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 channels total
- 32 byte TX FIFO and 32 byte RX FIFO per module

I^2C port

- I^2C v.1.0, configurable to master or slave mode
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes
- Supports I^2C bus arbitration

1284 parallel peripheral port

- All standard modes: ECP, byte, nibble, compatibility (also known as SPP or "Centronix")
- RLE (run length encoding) decoding of compressed data in ECP mode
- Operating clock from 100 kHz to 2 MHz

High performance multiple-master/distributed DMA system

- Intelligent bus bandwidth allocation (patent pending)
- System bus and peripheral bus

System bus:

- Every system bus peripheral is a bus master with a dedicated DMA engine

Peripheral bus:

- One 12-channel DMA engine supports USB device
  - 2 DMA channels support control endpoint
  - 10 DMA channels support 10 endpoints
- One 12-channel DMA engine supports:
  - 4 serial modules (8 DMA channels)
  - 1284 parallel port (4 DMA channels)
- All DMA channels support fly-by mode

External peripheral:

- One 2-channel DMA engine supports external peripheral connected to memory bus
- Each DMA channel supports memory-to-memory transfers

Power management (patent pending)

- Power save during normal operation
  - Disables unused modules
- Power save during sleep mode
  - Sets memory controller to refresh
  - Disables all modules except selected wakeup modules
  - Wakeup on valid packets or characters

Vector interrupt controller

- Decreased bus traffic and rapid interrupt service
- Hardware interrupt prioritization

General purpose timers/counters

- 8 independent 16-bit or 32-bit programmable timers or counters
  - Each with an I/O pin
- Mode selectable into:
  - Internal timer mode
  - External gated timer mode
  - External event counter
- Can be concatenated
- Resolution to measure minute-range events
- Source clock selectable: internal clock or external pulse event
- Each can be individually enabled/disabled

System timers

- Watchdog timer
- System bus monitor timer
- System bus arbiter timer
- Peripheral bus monitor timer

General purpose I/O

- 73 programmable GPIO pins (muxed with other functions)
- Software-readable powerup status registers for every pin for customer-defined bootstrapping

External interrupts

- 4 external programmable interrupts
  - Rising or falling edge-sensitive
  - Low level- or high level-sensitive

Clock generator

- Low cost external crystal
- On-chip phase locked loop (PLL)
- Software programmable PLL parameters
- Optional external oscillator
- Separate PLL for USB

Operating grades/Ambient temperatures

- 177 MHz: 0 – 70° C
- 155 MHz: -40 – +85° C
- 103 MHz: 0 – 70° C

System-level interfaces

Figure 1 shows the NS9360 system-level hardware interfaces.

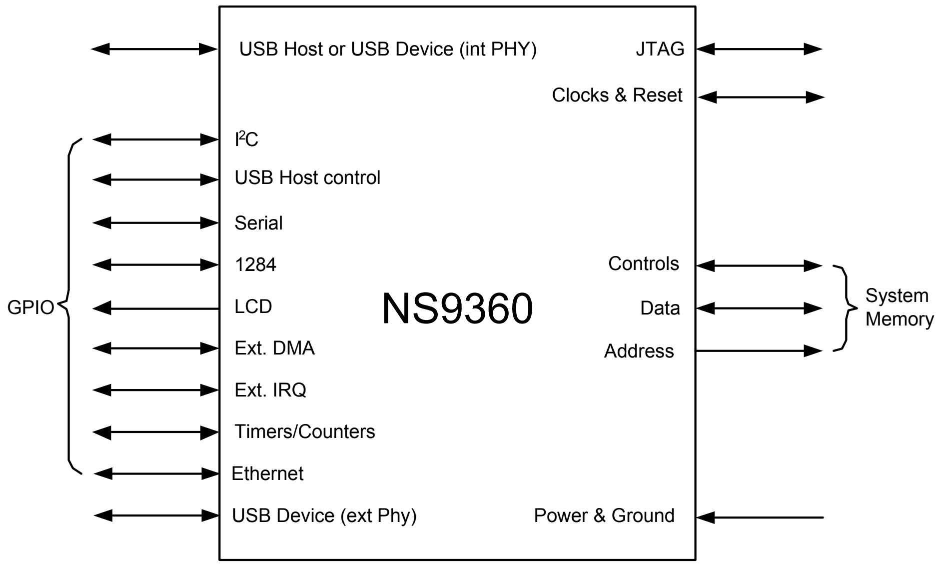


Figure 1: System-level hardware interfaces

NS9360 interfaces

- Ethernet MII/RMII interface to an external PHY
- System Memory interface
  - Glueless connection to SDRAM
  - Glueless connection to buffered PC100 DIMM
  - Glueless connection to SRAM
  - Glueless connection to Flash memory or ROM
- USB Host or Device interface using internal USB PHY
- I^2C interface
- 73 GPIO pins muxed with:
  - Four 8-pin-each serial ports, each programmable to UART or SPI
  - 1284 port
  - LCD controller interface
  - Two external DMA channels
  - Four external interrupt pins programmed to rising or falling edge, or to high or low level
  - Sixteen 16-bit or 32-bit programmable timers or counters
  - Two control signals to support USB host
- Ethernet interface — USB Device interface to external USB PHY
- JTAG development interface
- Clock interfaces for crystal or external oscillator
  - System clock
  - USB clock
- Clock interface for optional LCD external oscillator
- Power and ground

System configuration

The PLL and other system configuration settings can be configured at powerup before the CPU boots. External pins configure the necessary control register bits at powerup. External pulldown resistors can be used to configure the PLL and system configuration registers depending on the application. The recommended value is 2.2k ohm to 2.4k ohm.

Table 1 shows how each bit is used to configure the powerup settings, where 1 indicates the internal pullup resistor and 0 indicates an external pulldown resistor. Table 2 shows PLL ND[4:0] multiplier values.

Pin name	Configuration bits
rtck_out	**Chip select 1 byte_lane_enable_n/write_enable_n configuration bootstrap select** 0 write_enable_n for byte wide devices (default) 1 byte_lane_enable_n (2.4K pulldown added)
gpio[24] gpio[20]	**Chip select 1 data width bootstrap select** 00 16 bits 01 8 bits 11 32 bits
gpio[49]	Chip select polarity 0 Active high 1 Active low
gpio[44]	Endian mode 0 Big endian 1 Little endian
reset_done	Bootup mode 0 Boot from SDRAM using serial SPI EEPROM 1 Boot from flash/ROM
gpio[19]	Reserved. This pin must not be pulled to logic 0 until reset_done is a logic 1.
gpio[17], gpio[12], gpio[10], gpio [8], gpio[4]	PLL ND[4:0] (PLL multiplier, ND+1) (See Table 2: PLL ND[4:0] multiplier values.)
gpio[2], gpio[0]	PLL FS[1:0] (PLL frequency select) **GPIO FS Divide by** 10 00 1 11 01 2 00 10 4 01 11 8

Table 1: Configuration pins— Bootstrap initialization

Register configuration: gpio 17, 12, 10, 8, 4	Multiplier
1 1 0 1 0	32
0 0 1 0 0	31
1 1 0 0 0	30
1 1 0 0 1	29
1 1 1 1 0	28
1 1 1 1 1	27
1 1 1 0 0	26
1 1 1 0 1	25
1 0 0 1 0	24
1 0 0 1 1	23
1 0 0 0 0	22
1 0 0 0 1	21
1 0 1 1 0	20
1 0 1 1 1	19
1 0 1 0 0	18
1 0 1 0 1	17
0 1 0 1 0	16
0 1 0 1 1	15
0 1 0 0 0	14
0 1 0 0 1	13
0 1 1 1 0	12
0 1 1 1 1	11
0 1 1 0 0	10
0 1 1 0 1	9
0 0 0 1 0	8
0 0 0 1 1	7
0 0 0 0 0	6
0 0 0 0 1	5
0 0 1 1 0	4
0 0 1 1 1	3
0 0 1 0 0	2

Table 2: PLL ND[4:0] multiplier values

Register configuration: gpio 17, 12, 10, 8, 4	Multiplier
0 0 1 0 1	1

Table 2: PLL ND[4:0] multiplier values

These are sample frequency settings for each speed grade:

- 176.9472 MHz: pulldown gpio[12], gpio[10], gpio[4]
- 154.8288 MHz: pulldown gpio[12], gpio[10], gpio[8]
- 103.2192 MHz: pulldown gpio[17], gpio[10], gpio[8], gpio[4]

There are 32 additional GPIO pins that are used to create a general purpose, user-defined ID register. These are external signals that are registered at powerup.

gpio[41]	gpio[40]	gpio[39]	gpio[38]
gpio[37]	gpio[36]	gpio[35]	gpio[34]
gpio[33]	gpio[32]	gpio[31]	gpio[30]
gpio[29]	gpio[28]	gpio[27]	gpio[26]
gpio[25]	gpio[23]	gpio[22]	gpio[21]
gpio[18]	gpio[16]	gpio[15]	gpio[14]
gpio[13]	gpio[11]	gpio[9]	gpio[7]
gpio[6]	gpio[5]	gpio[3]	gpio[1]

Read these signals for general purpose status information.

System boot

There are two ways to boot the NS9360 system:

- From a fast Flash over the system memory bus.
- From an inexpensive, but slower, serial EEPROM through SPI port B.

Both boot methods are glueless. The bootstrap pin, RESET_DONEn, indicates where to boot on a system powerup. Flash boot can be done from 8-bit, 16-bit, or 32-bit ROM or Flash.

Serial EEPROM boot is supported by NS9360 hardware. A configuration header in the EEPROM specifies total number of words to be fetched from EEPROM, as well as a system memory configuration and a memory controller configuration. The boot engine configures the memory controller and system memory, fetches data from low-cost serial EEPROM, and writes the data to external system memory, holding the CPU in reset.

Reset

Master reset using an external reset pin resets the NS9360. Only the AHB bus error status registers retain their values; software read resets these error status registers. The input reset pin can be driven by a system reset circuit or a simple power-on reset circuit.

RESET_DONE as an input

Used at bootup only:

- When set to 0, the system boots from SDRAM through the serial SPI EEPROM.
- When set to 1, the system boots from Flash/ROM. This is the default.

SPI boot sequence

1. When the system reset turns to inactive, the reset signal to the CPU is still held active.
2. An I/O module on the peripheral bus (BBus) reads from a serial ROM device that contains the memory controller settings and the boot program.
3. The BBus-to-AHB bridge requests and gets the system bus.
4. The memory controller settings are read from the serial EEPROM and used to initialize the memory controller.
5. The BBus-to-AHB bridge loads the boot program into the SDRAM, starting at address 0.
6. The reset signal going to the CPU is released once the boot program is loaded. RESET_DONE is now set to 1.
7. The CPU begins to execute code from address 0x0000 0000.

RESET_DONE as an output

Sets to 1, per Step 6 in the boot sequence:

If the system is booting from serial EEPROM through the SPI port, the boot program must be loaded into the SDRAM before the CPU is released from reset. The memory controller is powered up with dy_cs_n[0] enabled with a default set of SDRAM configurations. The default address range for dy_cs_n[0] is from 0x0000 0000. The other chip selects are disabled.

You can use one of these software resets to reset NS9360. Select the reset by setting the appropriate bit in the appropriate register:

- Watchdog timer can issue reset upon Watchdog timer expiration.
- Software reset can reset individual internal modules or all modules except memory and CPU.
- The system is reset whenever software sets the PLL SW change bit, in the PLL Configuration register, to 1.

Hardware reset duration is 4ms for PLL to stabilize. Software reset duration depends on speed grade, as shown:

Speed grade	CPU clock cycles	Duration
177 MHz	128	723 ns
155 MHz	128	826 ns
103 MHz	128	1243 ns

Table 3: Software reset duration

The minimum reset pulse width is 10 crystal clocks.

System Clock

The system clock is provided to NS9360 by either a crystal or an external oscillator; this table shows sample clock frequency settings for each chip speed grade.

Speed	cpu_clk	ahb_clk (main bus)	bbus_clk
177 MHz	176.9472	88.4736	44.2368
155 MHz	154.8288	77.4144	38.7072
103 MHz	103.2192	51.6096	24.8048

Table 4: Sample clock frequency settings with 29.4912 MHz crystal

Pulldowns are required as follows:

- To produce 176.9472 MHz, pull down gpio[12], gpio[10], gpio[4].
- To produce 154.8288 MHz, pull down gpio[12], gpio[10], gpio[8].
- To produce 103.2192 MHz, pull down gpio[17], gpio[10], gpio[8], gpio[4].

Using an oscillator

If an oscillator is used, it must be connected to the x1_sys_osc input (C8 pin) on the NS9360. If a crystal is used, it must be connected with a circuit such as the one shown in Figure 2, "NS9360 system clock".

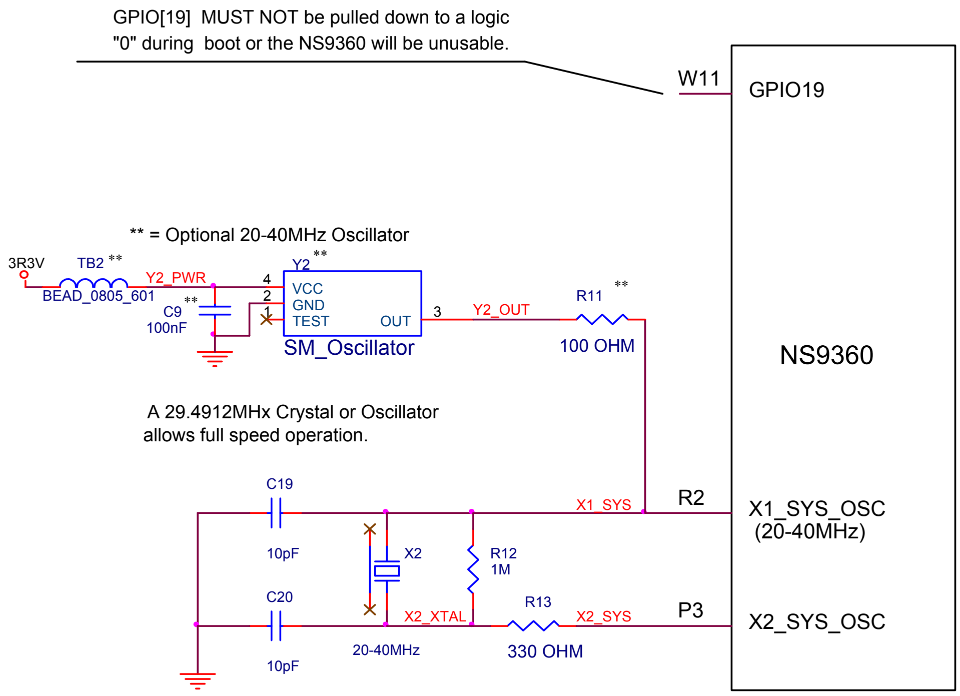


Figure 2: NS9360 system clock

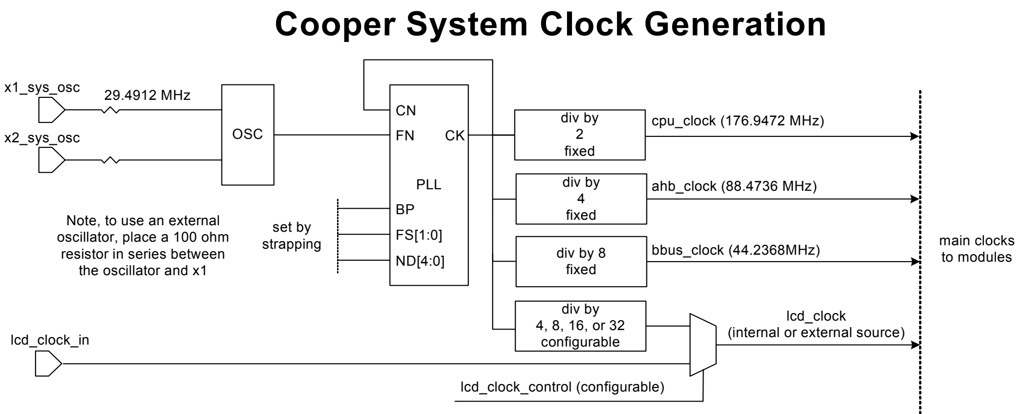
The PLL parameters are initialized on powerup reset, and can be changed by software. For a 177 MHz grade, the CPU may change from 177 MHz to 103 MHz, the AHB system bus may change from 88 MHz to 51 MHz, and the peripheral BBus may change from 44 MHz to 26 MHz. If changed by software, the system resets automatically after the PLL stabilizes (approximately 4 ms).

The system clock provides clocks for CPU, AHB system bus, peripheral BBus, LCD, timers, memory controller, and BBus modules (serial modules and 1284 parallel port).

The Ethernet MAC uses external clocks from a MII PHY or a RMII PHY. For a MII PHY, these clocks are input signals: rx_clk on pin V4 for receive clock and tx_clk on pin V2 for transmit clock. For a RMII, there is only one clock, and it connects to the rx_clk on pin V4. In this case, the transmit clock, tx_clk, should be tied low.

LCD controller, serial modules (UART, SPI), and the 1284 port optionally can use external clock signals.

Figure 3 shows how the PLL clock is used to provide the NS9360 system clocks by an external 48 MHz oscillator.



Sample Clock Frequency Settings With 29.4912MHz Crystal (FS= 01, div by 2)

ND+1	f_{VCO}	cpu_clk	hclk	bbus_clk	lcd_clk
24	353.8944	176.9472	88.4736	44.2368	88.7872 - 11.0592
23	339.1488	169.5744	84.7872	42.3936	84.7872 - 10.5984
22	324.4032	162.2016	81.1008	40.5504	81.1008 - 10.1376
21	309.6576	154.8288	77.4144	38.7072	77.4144 - 9.6768
20	294.9120	147.4560	73.7280	36.8640	73.7280 - 9.2160
19	280.1644	140.0832	70.0416	35.0208	70.0416 - 8.7552
18	265.4208	132.7104	66.3552	33.1776	66.3552 - 8.2944
17	250.6752	125.3376	62.6688	31.3344	62.6688 - 7.8336
16	235.9296	117.9648	58.9824	29.4912	58.9824 - 7.3728
15	221.1840	110.5920	55.2960	27.6480	55.2960 - 6.9120
14	206.4384	103.2192	51.6096	24.8048	51.6096 - 6.4512

Figure 3: NS9360 system clock generation (PLL)

You can use this formula to calculate the system clock frequencies if a different system oscillator frequency is used:

You can use this formula to calculate the system clock frequencies if a different system oscillator frequency is used:

f_{vco} = $(f_{osc} \times (ND + 1) / FS)$

f_{cpu_clk} = $f_{vco} / 2$

f_{hclk} = $f_{vco} / 4$

f_{bbuys_clk} = $f_{vco} / 8$

f_{lcd_clk} = programmable, f_{vco} / 4, 8, 16, or 32

USB clock

USB is clocked by a separate PLL driven by an external 48 MHz crystal, or it can be driven directly by an external 48 MHz oscillator.

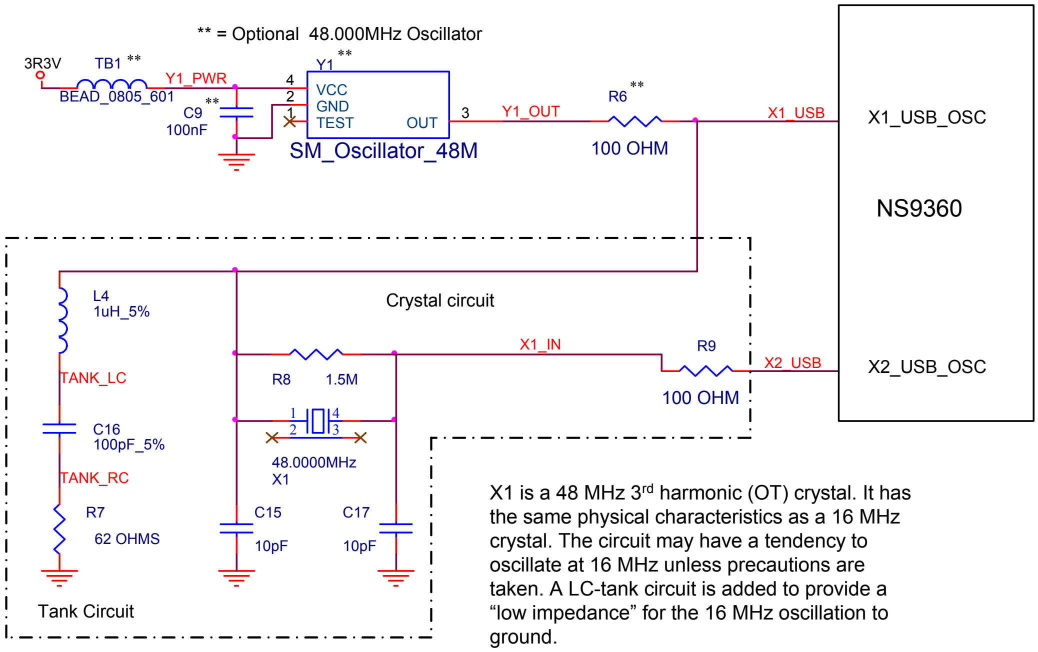


Figure 4: USB clock

NS9360 pinout and signal descriptions

Each pinout table applies to a specific interface, and contains the following information:

Heading	Description
Pin #	Pin number assignment for a specific I/O signal.
Signal	Pin name for each I/O signal. Some signals have multiple function modes and are identified accordingly. The mode is configured through firmware using one or more configuration registers. **_n** in the signal name indicates that this signal is active *low*.
U/D	U or D indicates whether the pin has an internal pullup resistor or a pulldown resistor: ■ **U** — Pullup (input current source) ■ **D** — Pulldown (input current sink) If no value appears, that pin has neither an internal pullup nor pulldown resistor.
I/O	The type of signal: input, output, or input/output.
OD (mA)	The output drive of an output buffer. NS9360 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

More detailed signal descriptions are provided for selected modules.

System Memory interface

Some system memory interface signals are muxed behind gpio. These signals are noted in the *Signal name / muxed behind* column. If there is no slash and no gpio pin indicated, the signal is not muxed behind a gpio signal.

Pin #	Signal Name / muxed behind	U/D	OD (mA)	I/O	Description
P18	addr[0]		8	O	Address bus signal
R20	addr[1]		8	O	Address bus signal
P19	addr[2]		8	O	Address bus signal
P20	addr[3]		8	O	Address bus signal
N18	addr[4]		8	O	Address bus signal
N19	addr[5]		8	O	Address bus signal
N20	addr[6]		8	O	Address bus signal
M18	addr[7]		8	O	Address bus signal
M19	addr[8]		8	O	Address bus signal

Table 5: System Memory interface pinout

Pin #	Signal Name / muxed behind	U/D	OD (mA)	I/O	Description
M20	addr[9]		8	O	Address bus signal
L19	addr[10]		8	O	Address bus signal
L18	addr[11]		8	O	Address bus signal
L20	addr[12]		8	O	Address bus signal
K20	addr[13]		8	O	Address bus signal
K18	addr[14]		8	O	Address bus signal
K19	addr[15]		8	O	Address bus signal
J20	addr[16]		8	O	Address bus signal
J19	addr[17]		8	O	Address bus signal
J18	addr[18]		8	O	Address bus signal
H20	addr[19]		8	O	Address bus signal
H18	addr[20]		8	O	Address bus signal
G20	addr[21]		8	O	Address bus signal
H19	addr[22] / gpio[66]		8	O	Address bus signal
E18	addr[23] / gpio[67]		8	O	Address bus signal
D19	addr[24] / gpio[68]		8	O	Address bus signal
C20	addr[25] / gpio[69]		8	O	Address bus signal
A17	addr[26] / gpio[70]		8	O	Address bus signal
B16	addr[27] / gpio[71]		8	O	Address bus signal
D19	clk_en[0] / gpio[68]		8	O	SDRAM clock enable
C20	clk_en[1] / gpio[69]		8	O	SDRAM clock enable
A17	clk_en[2] / gpio[70]		8	O	SDRAM clock enable
B16	clk_en[3] / gpio[71]		8	O	SDRAM clock enable
C15	clk_out[0]		8	O	SDRAM clock
A12	clk_out[1]		8	O	SDRAM reference clock. Connect to clk_in using AC termination.
A7	clk_out[2]		8	O	SDRAM clock
G1	clk_out[3]		8	O	SDRAM clock
A16	data[0]		8	I/O	Data bus signal
B15	data[1]		8	I/O	Data bus signal
C14	data[2]		8	I/O	Data bus signal
A15	data[3]		8	I/O	Data bus signal

Table 5: System Memory interface pinout

Pin #	Signal Name / muxed behind	U/D	OD (mA)	I/O	Description
B14	data[4]		8	I/O	Data bus signal
A14	data[5]		8	I/O	Data bus signal
C13	data[6]		8	I/O	Data bus signal
B13	data[7]		8	I/O	Data bus signal
A13	data[8]		8	I/O	Data bus signal
C12	data[9]		8	I/O	Data bus signal
B12	data[10]		8	I/O	Data bus signal
B11	data[11]		8	I/O	Data bus signal
C11	data[12]		8	I/O	Data bus signal
A11	data[13]		8	I/O	Data bus signal
A10	data[14]		8	I/O	Data bus signal
C10	data[15]		8	I/O	Data bus signal
B10	data[16]		8	I/O	Data bus signal
A9	data[17]		8	I/O	Data bus signal
B9	data[18]		8	I/O	Data bus signal
C9	data[19]		8	I/O	Data bus signal
A8	data[20]		8	I/O	Data bus signal
B8	data[21]		8	I/O	Data bus signal
C8	data[22]		8	I/O	Data bus signal
B7	data[23]		8	I/O	Data bus signal
A6	data[24]		8	I/O	Data bus signal
C7	data[25]		8	I/O	Data bus signal
B6	data[26]		8	I/O	Data bus signal
A5	data[27]		8	I/O	Data bus signal
C6	data[28]		8	I/O	Data bus signal
B5	data[29]		8	I/O	Data bus signal
A4	data[30]		8	I/O	Data bus signal
C5	data[31]		8	I/O	Data bus signal
F2	data_mask[0]		8	O	SDRAM data mask signal
G3	data_mask[1]		8	O	SDRAM data mask signal
F1	data_mask[2]		8	O	SDRAM data mask signal
G2	data_mask[3]		8	O	SDRAM data mask signal

Table 5: System Memory interface pinout

Pin #	Signal Name / muxed behind	U/D	OD (mA)	I/O	Description
J2	clk_in			I	SDRAM feedback clock. Connect to clk_out[1].
D1	byte_lane_sel_n[0]		8	O	Static memory byte_lane_enable[0] or write_enable_n[0] for byte-wide device signals
E2	byte_lane_sel_n[1]		8	O	Static memory byte_lane_enable[1] or write_enable_n[1] for byte-wide device signals
F3	byte_lane_sel_n[2]		8	O	Static memory byte_lane_enable[2] or write_enable_n[2] for byte-wide device signals
E1	byte_lane_sel_n[3]		8	O	Static memory byte_lane_enable[3] or write_enable_n[3] for byte-wide device signals
H1	cas_n		8	O	SDRAM column address strobe
B4	dy_cs_n[0]		8	O	SDRAM chip select signal
A3	dy_cs_n[1]		8	O	SDRAM chip select signal
D5	dy_cs_n[2]		8	O	SDRAM chip select signal
C4	dy_cs_n[3]		8	O	SDRAM chip select signal
H2	st_oe_n		8	O	Static memory output enable
J3	ras_n		8	O	SDRAM row address strobe
B3	st_cs_n[0]		8	O	Static memory chip select signal
C1	st_cs_n[1]		8	O	Static memory chip select signal
D2	st_cs_n[2]		8	O	Static memory chip select signal
E3	st_cs_n[3]		8	O	Static memory chip select signal
H3	we_n		8	O	SDRAM write enable. Used for static and SDRAM devices.
J1	ta_strb / gpio[72]			I	Slow peripheral transfer acknowledge

Table 5: System Memory interface pinout

System Memory interface signals

Table 6 describes the System Memory interface signals in more detail. All signals are internal to the chip.

Name	I/O	Description
addr[27:0]	O	Address output. Used for both static and SDRAM devices. SDRAM memories use bits [14:0]; static memories use bits [27:0]. Note: Address bits [27:22] are muxed behind gpio[71:66].

Table 6: System Memory interface signal descriptions

Name	I/O	Description
clk_en[3:0]	O	SDRAM clock enable. Used for SDRAM devices. These signals are muxed behind gpio[71:68]. Note: The clk_en signals are associated with the dy_cs_n signals. If clock enables are used, a pullup resistor is required to prevent floating during startup, and to avoid SDRAM lockup during manual or brown out conditions. If not used, connect the clock enables in the SDRAM devices directly to 3.3v or a pullup resistor.
clk_out[3:0]	O	SDRAM clocks. Used for SDRAM devices. SDRAM clk_out[1] is connected to clk_in.
data[31:0]	I/O	Read data from memory. Used for the static memory controller and the dynamic memory controller.
data_mask[3:0]	O	Data mask output to SDRAMs. Used for SDRAM devices.
clk_in	I	Feedback clock. Always connects to clk_out[1].
byte_lane_sel_n[3:0]	O	Static memory byte_lane_select, active low, or write_enable_n for byte-wide devices.
cas_n	O	Column address strobe. Used for SDRAM devices.
dy_cs_n[3:0]	O	SDRAM chip selects. Used for SDRAM devices.
st_oe_n	O	Output enable for static memories. Used for static memory devices.
ras_n	O	Row address strobe. Used for SDRAM devices.
st_cs_n[3:0]	O	Static memory chip selects. Default active low. Used for static memory devices.
we_n	O	Write enable. Used for SDRAM and static memories.
ta_strb	I	*Slow peripheral transfer acknowledge* can be used to terminate static memory cycles sooner than the number of wait states programmed in the chip select setup register. This signal is muxed being gpio[72].

Table 6: System Memory interface signal descriptions

Figure 5, "SDRAM clock termination," on page 19, shows an example of NS9360 SDRAM clock termination. clk_out[1] is shown, but you can use any clk_out signal (0, 1, 2, or 3).

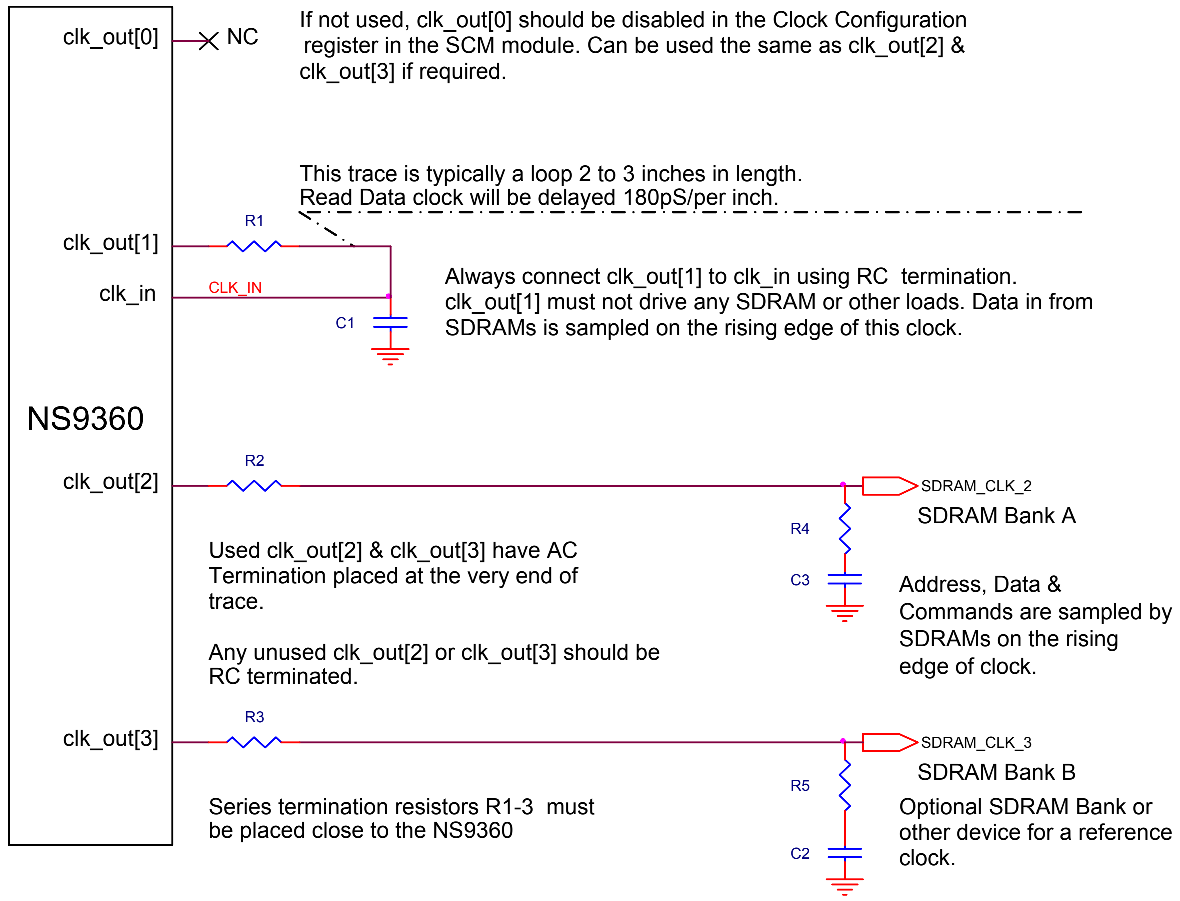


Figure 5: SDRAM clock termination

Ethernet interface

Notes:

- Most Ethernet MII signals are muxed behind gpio. These are noted in the *Signal name: MII / muxed behind* column. If there is no slash and no gpio pin indicated, the Ethernet signal is not muxed behind a gpio signal.
- N/C indicates *No Connect* or *ground*, as indicated in the description for the pin.

Pin #	Signal name		U/D	OD (mA)	I/O	Description	
	MII / muxed behind	RMII				MII	RMII
P2	col / gpio[63]	N/C			I	Collision	Pull low external to NS9360
R1	crs / gpio[64]	crs_dv			I	Carrier sense	Carrier sense/data valid

Table 7: Ethernet interface pinout

Pin #	Signal name: MII / muxed behind	Signal name: RMII	U/D	OD (mA)	I/O	Description: MII	Description: RMII
P1	enet_phy_int_n / gpio[65]	enet_phy_int_n	U		I	Ethernet PHY interrupt	Ethernet PHY interrupt
L2	mdc	mdc		4	O	MII management interface clock	MII management interface clock
K2	mdio / gpio[50]	mdio		2	I/O	MII management data	MII management data
V4	rx_clk	ref_clk			I	Receive clock	Reference clock
U3	rx_dv / gpio[51]	N/C			I	Receive data valid	Pull low external to NS9360
V1	rx_er / gpio[52]	rx_er			I	Receive error	Optional signal; pull low external to NS9360 if not used
N3	rxd[0] / gpio[53]	rxd[0]			I	Receive data bit 0	Receive data bit 0
N2	rxd[1] / gpio[54]	rxd[1]			I	Receive data bit 1	Receive data bit 1
N1	rxd[2] / gpio[55]	N/C			I	Receive data bit 2	Pull low external to NS9360
M3	rxd[3] / gpio[56]	N/C			I	Receive data bit 3	Pull low external to NS9360
V2	tx_clk	N/C			I	Transmit clock	Pull low external to NS9360
M2	tx_en / gpio[57]	tx_en		2	O	Transmit enable	Transmit enable
M1	tx_er / gpio[58]	N/C		2	O	Transmit error	N/A
L3	txd[0] / gpio[59]	txd[0]		2	O	Transmit data bit 0	Transmit data bit 0
L1	txd[1] / gpio[60]	txd[1]		2	O	Transmit data bit 1	Transmit data bit 1
K1	txd[2] / gpio[61]	N/C		2	O	Transmit data bit 2	N/A
K3	txd[3] / gpio[62]	N/C		2	O	Transmit data bit 3	N/A

Table 7: Ethernet interface pinout

Clock generation/system pins

Pin #	Signal name	U/D	OD (mA)	I/O	Description
R2	x1_sys_osc			I	System clock crystal oscillator circuit input
P3	x2_sys_osc			O	System clock crystal oscillator circuit output
T1	sys_osc_vdd				System oscillator 3.3V power
F18	x1_usb_osc			I	USB clock crystal oscillator circuit input. (Connect to GND if USB is not used.)

Table 8: Clock generation/system pins pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Description
E20	x2_usb_osc			O	USB clock crystal oscillator circuit output
E19	usb_osc_vdd				USB oscillator 3.3V power
W4	reset_done	U	2	I/O	CPU is enabled once the boot program is loaded. Reset_done is set to 1.
U5	reset_n	U		I	System reset input signal
W3	sreset_n	U		I	System reset. sreset_n is the same as reset but does *not* reset the system PLL.
V5	bist_en_n			I	Enable internal BIST operation
U6	pll_test_n			I	Enable PLL testing
Y3	scan_en_n			I	Enable internal scan testing
R3	sys_pll_dvdd				System clock PLL 1.5V digital power
T2	sys_pll_dvss				System clock PLL digital ground
U2	sys_pll_avdd				System clock PLL 3.3V analog power
U1	sys_pll_avss				System clock PLL analog ground
T3	pll_lpf			O	PLL diagnostic output
V10	lcdclk / gpio[15]	U		I	External LCD clock input (muxed behind gpio[15])

Table 8: Clock generation/system pins pinout

bist_en_n, pll_test_n, and scan_en_n

Table 9 is a truth/termination table for bist_en_n, pll_test_n, and scan_en_n.

	Normal operation	Arm debug	
pll_test_n	pull up	pull up	10K recommended
bist_en_n	pull down	pull up	10K pullup = debug 2.4K pulldown = normal
scan_en_n	pull down	pull down	2.4K recommended

Table 9: bist_en_n, pll_test_n, & scan_en_n truth/termination table

GPIO MUX

- The BBus utility contains the control pins for each GPIO MUX bit. Each pin can be selected individually; that is, you can select any option (00, 01, 02, 03) for any pin, by setting the appropriate bit in the appropriate register.
- Some signals are muxed to two different GPIO pins, to maximize the number of possible applications. These duplicate signals are marked as such in the Descriptions column in the table. Selecting the primary GPIO pin and the duplicate GPIO pin for the same function is not

recommended. If both the primary GPIO pin and duplicate GPIO pin are programmed for the same function, however, the primary GPIO pin has precedence and will be used.

- The 00 option for the serial ports (B, A, C, and D) are configured for UART and SPI mode, respectively; that is the UART option is shown first, followed by the SPI option if there is one. If only one value appears, it is the UART mode value. SPI options all begin with *SPI*.
- The I^2C module must be held in reset until the GPIO assigned to the I^2C has been configured.
- GPIO pins 42, 43, 50-64, and 66-72 (24 pins total) do not have internal pullups. All GPIO pins are reset at powerup to be inputs. Any of these pins not being used should be pulled high with an external 10K resistor. Some of these GPIO pins might need external 10K pullup or pulldown resistors to prevent them from floating before being programmed, depending on how they are being used.

  For example, gpio[66] is being used as *mem addr [22]* to address a flash chip. gpio[66] should be pulled down with a 10K resistor to prevent the pin from floating until the software is loaded and can program the pin using GPIO Configuration Register 9 to drive *mem addr [22]* from pin gpio[66].

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
W5	gpio[0][1]	U	2	I/O	00	Ser port B TXData / SPI port B dout
					01	DMA ch 1 done (duplicate)
					02	Timer 1 (duplicate)
					03	GPIO 0
V6	gpio[1]	U	2	I/O	00	Ser port B RXData / SPI port B din
					01	DMA ch 1 req (duplicate)
					02	Ext IRQ 0
					03	GPIO 1
Y5	gpio [2][1]	U	2	I/O	00	Ser port B RTS
					01	Timer 0
					02	DMA ch 2 read enable
					03	GPIO 2
W6	gpio[3]	U	2	I/O	00	Ser port B CTS
					01	1284 nACK (peripheral-driven)
					02	DMA ch 1 req
					03	GPIO 3
V7	gpio[4][1]	U	2	I/O	00	Ser port B DTR
					01	1284 busy (peripheral-driven)
					02	DMA ch 1 done
					03	GPIO 4

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
Y6	gpio[5]	U	2	I/O	00	Ser port B DSR
					01	1284 PError (peripheral-driven)
					02	DMA ch 1 read enable
					03	GPIO 5
W7	gpio[6]	U	2	I/O	00	Ser port B RI / SPI port B clk
					01	1284 nFault (peripheral-driven)
					02	Timer 7 (duplicate)
					03	GPIO 6
Y7	gpio[7]	U	2	I/O	00	Ser port B DCD / SPI port B enable
					01	DMA ch 1 read enable (duplicate)
					02	Ext IRQ 1
					03	GPIO 7
V8	gpio[8][1]	U	2	I/O	00	Ser port A TXData / SPI port A dout
					01	Reserved
					02	Reserved
					03	GPIO 8
W8	gpio[9]	U	2	I/O	00	Ser port A RXData / SPI port A din
					01	Reserved
					02	Reserved
					03	GPIO 9
Y8	gpio[10][1]	U	2	I/O	00	Ser port A RTS
					01	Reserved
					02	PWM ch 0 (duplicate)
					03	GPIO 10
V9	gpio[11]	U	2	I/O	00	Ser port A CTS
					01	Ext IRQ2 (duplicate)
					02	Timer 0 (duplicate)
					03	GPIO 11
W9	gpio[12][1]	U	2	I/O	00	Ser port A DTR
					01	Reserved
					02	PWM ch 1 (duplicate)
					03	GPIO 12
Y9	gpio[13]	U	2	I/O	00	Ser port A DSR
					01	Ext IRQ 0 (duplicate)
					02	PWM ch 2 (duplicate)
					03	GPIO 13
W10	gpio[14]	U	2	I/O	00	Ser port A RI / SPI port A clk
					01	Timer 1
					02	PWM ch 3 (duplicate)
					03	GPIO 14

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
V10	gpio[15]	U	2	I/O	00	Ser port A DCD / SPI port A enable
					01	Timer 2
					02	LCD clock input
					03	GPIO 15
Y10	gpio[16][2]	U	2	I/O	00	USB overcurrent
					01	1284 nFault (peripheral-driven, duplicate)
					02	Reserved
					03	GPIO 16
Y11	gpio[17][1, 2]	U	2	I/O	00	USB power relay
					01	Reserved
					02	Reserved
					03	GPIO 17
V11	gpio[18]	U	4	I/O	00	Ethernet CAM reject
					01	LCD power enable
					02	Ext IRQ 3 (duplicate)
					03	GPIO 18
W11	gpio[19][1]	U	4	I/O	00	Ethernet CAM req
					01	LCD line-horz sync
					02	DMA ch 2 read enable (duplicate)
					03	GPIO 19
Y12	gpio[20][1]	U	8	I/O	00	Ser port C DTR
					01	LCD clock
					02	Reserved
					03	GPIO 20
W12	gpio[21]	U	4	I/O	00	Ser port C DSR
					01	LCD frame pulse-vert
					02	Reserved
					03	GPIO 21
V12	gpio[22]	U	4	I/O	00	Ser port C RI / SPI port C clk
					01	LCD AC bias-data enable
					02	Reserved
					03	GPIO 22
Y13	gpio[23]	U	4	I/O	00	Ser port C DCD / SPI port C enable
					01	LCD line end
					02	Reserved
					03	GPIO 23
W13	gpio[24][1]	U	4	I/O	00	Ser port D DTR
					01	LCD data bit 0
					02	Reserved
					03	GPIO 24

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
V13	gpio[25]	U	4	I/O	00	Ser port D DSR
					01	LCD data bit 1
					02	Reserved
					03	GPIO 25
Y14	gpio[26]	U	4	I/O	00	Ser port D RI / SPI port D clk
					01	LCD data bit 2
					02	Timer 3
					03	GPI0 26
W14	gpio[27]	U	4	I/O	00	Ser port D DCD / SPI port D enable
					01	LCD data bit 3
					02	Timer 4
					03	GPIO 27
Y15	gpio[28]	U	4	I/O	00	Ext IRQ 1 (duplicate)
					01	LCD data bit 4
					02	LCD data bit 8 (duplicate)
					03	GPIO 28
V14	gpio[29]	U	4	I/O	00	Timer 5
					01	LCD data bit 5
					02	LCD data bit 9 (duplicate)
					03	GPIO 29
W15	gpio[30]	U	4	I/O	00	Timer 6
					01	LCD data bit 6
					02	LCD data bit 10 (duplicate)
					03	GPIO 30
Y16	gpio[31]	U	4	I/O	00	Timer 7
					01	LCD data bit 7
					02	LCD data bit 11 (duplicate)
					03	GPIO 31
V15	gpio[32]	U	4	I/O	00	Ext IRQ 2
					01	1284 Data 1 (bidirectional)
					02	LCD data bit 8
					03	GPIO 32
W16	gpio[33]	U	4	I/O	00	Reserved
					01	1284 Data 2 (bidirectional)
					02	LCD data bit 9
					03	GPIO 33
Y17	gpio[34]	U	4	I/O	00	iic_scl
					01	1284 Data 3 (bidirectional)
					02	LCD data bit 10
					03	GPIO 34

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)
U15	gpio[35]	U	4	I/O	00 iic_sda 01 1284 Data 4 (bidirectional) 02 LCD data bit 11 03 GPIO 35
V16	gpio[36]	U	4	I/O	00 PWM ch 0 01 1284 Data 5 (bidirectional) 02 LCD data bit 12 03 GPIO 36
W17	gpio[37]	U	4	I/O	00 PWM ch 1 01 1284 Data 6 (bidirectional) 02 LCD data bit 13 03 GPIO 37
Y18	gpio[38]	U	4	I/O	00 PWM ch2 01 1284 Data 7 (bidirectional) 02 LCD data bit 14 03 GPIO 38
U16	gpio[39]	U	4	I/O	00 PWM ch3 01 1284 Data 8 (bidirectional) 02 LCD data bit 15 03 GPIO 39
V17	gpio[40]	U	4	I/O	00 Ser port C TXData / SPI port C dout 01 Ext IRQ 3 02 LCD data bit 16 03 GPIO 40
W18	gpio[41]	U	4	I/O	00 Ser port C RXData / SPI port C din 01 Reserved 02 LCD data bit 17 03 GPIO 41
U18	gpio[42]		2	I/O	00 Ser port C RTS 01 Reserved 02 USB phy data + (TX and RX data for bidirectional PHY or TX data only for unidirectional PHY) 03 GPIO 42
V20	gpio[43]		2	I/O	00 Ser port C CTS 01 1284 transceiver direction control 02 USB phy data - (TX and RX data for bidirectional PHY or TX data only for unidirectional PHY) 03 GPIO 43

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
U19	gpio[44][1]	U	2	I/O	00	Ser port D TXData / SPI port D dout
					01	1284 Select (peripheral-driven)
					02	USB phy tx output enable
					03	GPIO 44
U20	gpio[45]	U	2	I/O	0	Ser port D RXData / SPI port D din
					01	1284 nStrobe (host-driven)
					02	USB phy rx data
					03	GPIO 45
T19	gpio[46]	U	2	I/O	00	Ser port D RTS
					01	1284 nAutoFd (host-driven)
					02	USB phy rx data + (unidirectional phy only; for bidirectional USB PHY applications, do not configure for option 02)
					03	GPIO 46
R18	gpio[47]	U	2	I/O	00	Ser port D CTS
					01	1284 nInit (host-driven)
					02	USB phy rx data - (unidirectional phy only; for bidirectional USB PHY applications, do not configure for option 02)
					03	GPIO 47
T20	gpio[48]	U	2	I/O	00	USB phy suspend
					01	1284 nSelectIn (host-driven)
					02	DMA ch 2 req
					03	GPIO 48
R19	gpio[49][1]	U	2	I/O	00	USB phy speed
					01	1284 peripheral logic high (peripheral-driven)
					02	DMA ch 2 done
					03	GPIO 49
K2	gpio[50]		2	I/O	00	MII/RMII management data
					01	USB phy data + (duplicate) (TX and RX data for bidirectional PHY or TX data only for unidirectional PHY)
					02	Reserved
					03	GPIO 50
U3	gpio[51]		2	I/O	00	MII rx data valid
					01	USB phy data - (duplicate) (TX and RX data for bidirectional PHY or TX data only for unidirectional PHY)
					02	Reserved
					03	GPIO 51

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
V1	gpio[52]		2	I/O	00	MII rx error
					01	USB phy tx output enable (duplicate)
					02	Reserved
					03	GPIO 52
N3	gpio[53]		2	I/O	00	MII/RMII rx data bit 0
					01	USB phy rx data (duplicate)
					02	Reserved
					03	GPIO 53
N2	gpio[54]		2	I/O	00	MII/RMII rx data bit 1
					01	USB phy suspend (duplicate)
					02	Reserved
					03	GPIO 54
N1	gpio[55]		2	I/O	00	MII rx data bit 2
					01	USB phy speed (duplicate)
					02	Reserved
					03	GPIO 55
M3	gpio[56]		2	I/O	00	MII rx data bit 3
					01	USB rx data + (duplicate) (unidirectional phy only; for bidirectional USB PHY applications, do not configure for option 01)
					02	Reserved
					03	GPIO 56
M2	gpio[57]		2	I/O	00	MII/RMII tx enable
					01	USB rx data - (duplicate) (unidirectional phy only; for bidirectional USB PHY applications, do not configure for option 01)
					02	Reserved
					03	GPIO 57
M1	gpio[58]		2	I/O	00	MII tx error
					01	Reserved
					02	Reserved
					03	GPIO 58
L3	gpio[59]		2	I/O	00	MII/RMII tx data bit 0
					01	Reserved
					02	Reserved
					03	GPIO 59
L1	gpio[60]		2	I/O	00	MII/RMII tx data bit 1
					01	Reserved
					02	Reserved
					03	GPIO[60]

Table 10: GPIO MUX pinout

Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
K1	gpio[61]		2	I/O	00	MII tx data bit 2
					01	Reserved
					02	Reserved
					03	GPIO 61
K3	gpio[62]		2	I/O	00	MII tx data bit 3
					01	Reserved
					02	Reserved
					03	GPIO 62
P2	gpio[63]		2	I/O	00	MII collision
					01	Reserved
					02	Reserved
					03	GPIO 63
R1	gpio[64]		2	I/O	00	MII/RMII carrier sense
					01	Reserved
					02	Reserved
					03	GPIO 64
P1	gpio[65]	U	2	I/O	00	MII/RMII enet phy interrupt
					01	Reserved
					02	Reserved
					03	GPIO 65
H19	gpio[66]		8	I/O	00	Mem addr[22]
					01	Reserved
					02	Reserved
					03	GPIO 66
E18	gpio[67]		8	I/O	00	Mem addr[23]
					01	Reserved
					02	Reserved
					03	GPIO 67
D19	gpio[68]		8	I/O	00	Mem addr[24]
					01	Mem clk_en[0]
					02	Ext IRQ 0 (duplicate)
					03	GPIO 68
C20	gpio[69]		8	I/O	00	Mem addr[25]
					01	Mem clk_en[1]
					02	Ext IRQ 1 (duplicate)
					03	GPIO 69
A17	gpio[70]		8	I/O	00	Mem addr[26]
					01	Mem clk_en[2]
					02	iic_scl (duplicate)
					03	GPIO 70

Table 10: GPIO MUX pinout

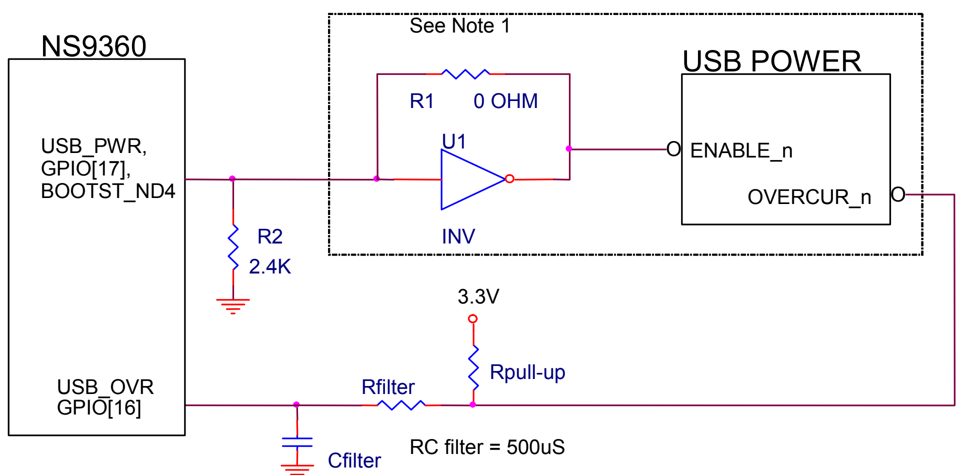
Pin #	Signal name	U/D	OD (mA)	I/O	Descriptions (4 options: 00, 01, 02, 03)	
B16	gpio[71]		8	I/O	00	Mem addr[27]
					01	Mem clk_en[3]
					02	iic_sda (duplicate)
					03	GPIO 71
J1	gpio[72]		8	I/O	00	Mem ta_strb
					01	Reserved
					02	Reserved
					03	GPIO 72

1 This pin is used for bootstrap initialization (see Table 1, "Configuration pins— Bootstrap initialization," on page 5). Note that the GPIO pins used as bootstrap pins have a defined powerup state that is required for the appropriate NS9360 configuration. If these GPIO pins are also used to control external devices (for example, power switch enable), the powerup state for the external device should be compatible with the bootstrap state. If the powerup state is not compatible with the bootstrap state, either select a different GPIO pin to control the external device or add additional circuitry to reach the proper powerup state to the external device.

2 gpio[17] is used as both a bootstrap input pin for PLL_ND and an output that controls a power switch for USB Host power. If the power switch needs to powerup in the inactive state, the enable to the power switch must be the same value as the bootstrap value for PLL_ND; for example, if PLL_ND requires high on gpio[17], a high true power switch must be selected. gpio[16] is used for USB_OVR and should have a noise filter to prevent false indications of overcurrent, unless the USB power IC has this filter built in. See "Example: Implementing gpio[16] and gpio[17]" on page 30 for an illustration.

Table 10: GPIO MUX pinout

Example: Implementing gpio[16] and gpio[17]



1 Powerup: GPIO[17] = Bootstrap ND4. Can be high or pulled low depending in required CPU speed.

– If pulled low R2 in; populate inverter U1

– If not pulled low; populate R1

R1 and U1 can be eliminated by selecting the ENABLE_n polarity of the USB power IC to match the bootstrap state.

2 Code initializes USB registers. USP_PWR driven by USB IP.

3 Code sets gpio[16] and gpio[17] to mode 0 — USB.

– Sets the INV function for USB_OVR;

– If R2 and U1 are populated, set the INV function for USB_PWR

LCD module signals

The LCD module signals are multiplexed with GPIO pins. They include six control signals and up to 18 data signals. Table 11 describes the control signals.

Signal name	Type	Description
CLPOWER	Output	LCD panel power enable
CLLP	Output	Line synchronization pulse (STN) / horizontal synchronization pulse (TFT)
CLCP	Output	LCD panel clock
CLFP	Output	Frame pulse (STN) / vertical synchronization pulse (TFT)
CLAC	Output	STN AC bias drive or TFT data enable output
CLD[17:0]	Output	LCD panel data
CLLE	Output	Line end signal

Table 11: LCD module signal descriptions

The CLD[17:0] signal has seven modes of operation:

- TFT 18-bit interface
- Color STN single panel
- Color STN dual panel
- 4-bit mono STN single panel
- 4-bit mono STN dual panel
- 8-bit mono STN single panel
- 8-bit mono STN dual panel

Table 12 shows which CLD[17:0] pins provide the pixel data to the STN panel for each mode of operation.

Legend:

– Ext pin = External pin
– CUSTN = Color upper panel STN, dual and/or single panel
– CLSTN = Color lower panel STN, dual
– MUSTN = Mono upper panel STN, dual and/or single panel
– MLSTN = Mono lower panel STN, dual
– N/A = not used

– 01 and 02 = The option number/position in the Description field of the GPIO mux pinout. See "GPIO MUX" on page 21 for more information.

Ext pin	GPIO pin & description	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[17]	W18=LCD data bit 17 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[16]	V17=LCD data bit16 (02)	N/A	N/A	N/A	N/A	N/A	N/A
CLD[15]	U16=LCD data bit 15 (02)	N/A	CLSTN[0][1]	N/A	N/A	N/A	MLSTN[0][1]
CLD[14]	Y18=LCD data bit 14 (02)	N/A	CLSTN[1]	N/A	N/A	N/A	MLSTN[1]
CLD[13]	W17=LCD data bit 13 (02)	N/A	CLSTN[2]	N/A	N/A	N/A	MLSTN[2]
CLD[12]	V16=LCD data bit 12 (02)	N/A	CLSTN[3]	N/A	N/A	N/A	MLSTN[3]
CLD[11]	U15=LCD data bit 11 (02) Y16=LCD data bit 11 (02)	N/A	CLSTN[4]	N/A	MLSTN[0][1]	N/A	MLSTN[4]
CLD[10]	Y17=LCD data bit 10 (02) W15=LCD data bit 10 (02)	N/A	CLSTN[5]	N/A	MLSTN[1]	N/A	MLSTN[5]
CLD[9]	W16=LCD data bit 9 (02) V14=LCD data bit 9 (02)	N/A	CLSTN[6]	N/A	MLSTN[2]	N/A	MLSTN[6]
CLD[8]	V15=LCD data bit 8 (02) Y15=LCD data bit 8 (02)	N/A	CLSTN[7]	N/A	MLSTN[3]	N/A	MLSTN[7]
CLD[7]	Y16=LCD data bit 7 (01)	CUSTN[0][1]	CUSTN[0][1]	N/A	N/A	MUSTN[0]	MUSTN[0][1]
CLD[6]	W15=LCD data bit 6 (01)	CUSTN[1]	CUSTN[1]	N/A	N/A	MUSTN[1]	MUSTN[1]
CLD[5]	V14=LCD data bit 5 (01)	CUSTN[2]	CUSTN[2]	N/A	N/A	MUSTN[2]	MUSTN[2]
CLD[4]	Y15=LCD data bit 4 (01)	CUSTN[3]	CUSTN[3]	N/A	N/A	MUSTN[3]	MUSTN[3]
CLD[3]	W14=LCD data bit 3 (01)	CUSTN[4]	CUSTN[4]	MUSTN[0]	MUSTN[0][1]	MUSTN[4]	MUSTN[4]
CLD[2]	Y14=LCD data bit 2 (01)	CUSTN[5]	CUSTN[5]	MUSTN[1]	MUSTN[1]	MUSTN[5]	MUSTN[5]
CLD[1]	V13=LCD data bit 1 (01)	CUSTN[6]	CUSTN[6]	MUSTN[2]	MUSTN[2]	MUSTN[6]	MUSTN[6]
CLD[0]	W13=LCD data bit 0 (01)	CUSTN[7]	CUSTN[7]	MUSTN[3]	MUSTN[3]	MUSTN[7]	MUSTN[7]

1 This data bit corresponds to the first "pixel position." For example, for an 8-bit mono STN display, CUSTN[0] is the leftmost pixel on the panel and CUSTN[7] is the rightmost pixel within the 8-bit data. For a color STN display, bits [7, 6, 5] form the leftmost pixel.

Table 12: CLD[17:0] pin descriptions for STN display

Table 13 shows which CLD[17:0] pins provide the pixel data to the TFT panel for each of the multiplexing modes of operation.

External pin	TFT 15 bit
CLD[17]	BLUE[4]
CLD[16]	BLUE[3]
CLD[15]	BLUE[2]
CLD[14]	BLUE[1]
CLD[13]	BLUE[0]
CLD[12]	Intensity bit
CLD[11]	GREEN[4]
CLD[10]	GREEN[3]
CLD[9]	GREEN[2]
CLD[8]	GREEN[1]
CLD[7]	GREEN[0]
CLD[6]	Intensity bit
CLD[5]	RED[4]
CLD[4]	RED[3]
CLD[3]	RED[2]
CLD[2]	RED[1]
CLD[1]	RED[0]
CLD[0]	Intensity bit

Table 13: CLD[17:0] pin descriptions for TFT display

This LCD TFT panel signal multiplexing table shows the RGB alignment to a 15-bit TFT with the intensity bit not used. The intensity bit, if used, should be connected to the LSB (that is, RED[0], GREEN[0], BLUE[0]) input of an 18-bit LCD TFT panel as shown in the next table.

	4	3	2	1	0	Intensity
18-bit TFT	5	4	3	2	1	0
15-bit TFT	4	3	2	1	0	x
12-bit TFT	3	2	1	0	x	x
9-bit TFT	2	1	0	x	x	x

Table 14: RGB bit alignment according to TFT interface size (one color shown)

If you want reduced resolution, the least significant color bits can be dropped, starting with Red[0], Green[0], and Blue[0].

I^2C interface

Note: The I^2C signals are muxed behind gpio, as noted in the *Signal name / muxed behind* column.

Pin #	Signal name / muxed behind	U/D	OD (mA)	I/O	Description
Y17	iic_scl / gpio[34]		4	I/O	I^2C serial clock line. Add a 10K resistor to VDDA(3.3V) if used.
U15	iic_sda / gpio[35]		4	I/O	I^2C serial data line. Add a 10K resistor to VDDA(3.3V) if used.

Table 15: I^2C interface pinout

USB Interface

Notes:

- If not using the USB interface, these pins should be pulled down to ground through a 15K ohm resistor.
- All output drivers for USB meet the standard USB driver specification.

Pin #	Signal name	U/D	OD (mA)	I/O	Description
B17	usb_dm			I/O	USB data -
A18	usb_dp			I/O	USB data +

Table 16: USB interface pinout

JTAG interface for ARM core/boundary scan

Note: trst_n must be pulsed low to initialize the JTAG when a debugger is not attached.

Pin #	Signal name	U/D	OD (mA)	I/O	Description
G18	tck			I	Test clock
D20	tdi	U		I	Test data in
G19	tdo		2	O	Test data out
F19	tms	U		I	Test mode select
F20	trst_n	U		I	Test mode reset
Y4	rtck	U	2	I/O	Returned test clock, ARM core only

Table 17: JTAG interface/boundary scan pinout

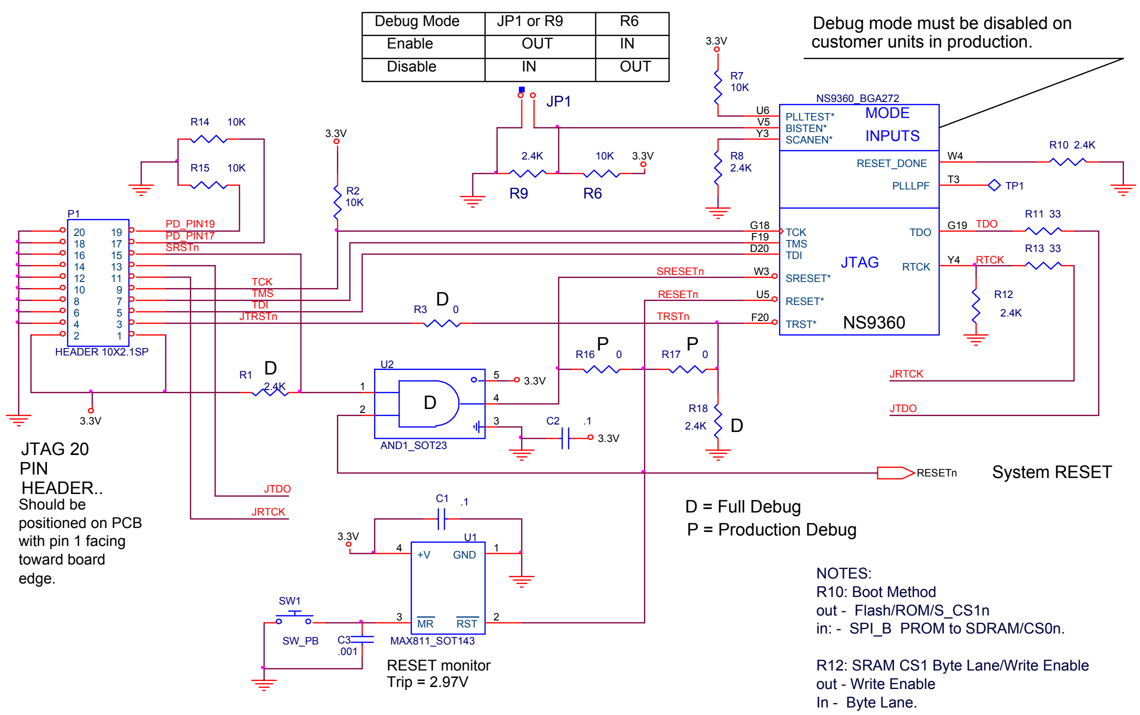


Figure 6: JTAG interface

Reserved pins

Pin#	Description
T18	No connect

Table 18: Reserved pins

Power and ground

Pin #	Signal name	Description
A2, A1, B2, B1, C3, D4, W1, Y1, W2, Y2, V3, U4, Y19, Y20, W19, W20, V18, U17, B20, A20, B19, A19, C18, D17, E4, H4, J4, C16, H17, E17, M17, N17, T17, D13, D12, D9, D8, U12, U9, T4, N4, C2, D3, D16, C17, D18, B18, C19, V19, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12	VSS	Ground
F4, G4, P4, R4, U8, U7, U13, U14, P17, R17, F17, G17, D15, D14, D7, D6	VDDS	+3.3V
K4, L4, M4, U10, U11, J17, K17, L17, D11, D10	VDDC	+1.5V

Table 19: Power and ground pins

Address and register maps

System address map

The system memory address is divided to allow access to the internal and external resources on the system bus, as shown in Table 20.

Address range	Size	System functions
0x0000 0000 – 0x0FFF FFFF	256 MB	System memory chip select 0 - Dynamic memory (default)
0x1000 0000 – 0x1FFF FFFF	256 MB	System memory chip select 1 - Dynamic memory (default)
0x2000 0000 – 0x2FFF FFFF	256 MB	System memory chip select 2 - Dynamic memory (default)
0x3000 0000 – 0x3FFF FFFF	256 MB	System memory chip select 3 - Dynamic memory (default)
0x4000 0000 – 0x4FFF FFFF	256 MB	System memory chip select 0 - Static memory (default)
0x5000 0000 – 0x5FFF FFFF	256 MB	System memory chip select 1 - Static memory (default)
0x6000 0000 – 0x6FFF FFFF	256MB	System memory chip select 2 - Static memory (default)
0x7000 0000 – 0x7FFF FFFF	256 MB	System memory chip select 3 - Static memory (default)
0x8000 0000 – 0x8FFF FFFF	256 MB	Reserved
0x9000 0000 – 0x9FFF FFFF	256 MB	BBus peripherals
0xA000 0000 – 0xA03F FFFF	4 MB	Reserved
0xA040 0000 – 0xA04F FFFF	1 MB	BBus-to-AHB bridge
0xA050 0000 – 0xA05F FFFF	1 MB	Reserved
0xA060 0000 – 0xA06F FFFF	1 MB	Ethernet Communication module
0xA070 0000 – 0xA07F FFFF	1 MB	Memory controller
0xA080 0000 – 0xA08F FFFF	1 MB	LCD controller
0xA090 0000 – 0xA09F FFFF	1 MB	System Control module
0xA0A0 0000 – 0xFFFF FFFF	1526 MB	Reserved

Table 20: System address memory map

BBus peripheral address map

The BBus bridge configuration registers are located at base address 0xA040 0000. The BBus peripherals are located at base address 0x9000 0000 and span a 256 MB address space. Each BBus peripheral, with the exception of the SER port controllers, resides in a separate 1 MB address space. This table shows the address space given to each peripheral.

Base address	Peripheral
0x9000 0000	BBus DMA controller
0x9010 0000	Reserved
0x9020 0000	SER Port B
0x9020 0040	SER Port A
0x9030 0000	SER Port C
0x9030 0040	SER Port D
0x9040 0000	IEEE 1284 controller
0x9050 0000	I^2C controller
0x9060 0000	BBus utility
0x9070 0000	Real Time Clock
0x9080 0000	USB Host
0x9090 0000	USB Device

Table 21: BBus peripheral address map

Electrical characteristics

The NS9360 operates at a 1.5V core, with 3.3V I/O ring voltages.

Absolute maximum ratings

Important: Permanent device damage can occur if the absolute maximum ratings are exceeded even for an instant.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	-0.3 to +3.9	V
DC input voltage	V_{INA}	-0.3 to V_{DDA}+0.3	V
DC output voltage	V_{OUTA}	-0.3 to V_{DDA}+0.3	V
DC input current	I_{IN}	±10	mA
Storage temperature	T_{STG}	-40 to +125	^{o}C
† V_{DDA}, V_{INA}, V_{OUTA}: Ratings of I/O cells for 3.3V interface			

Recommended operating conditions

Recommended operating conditions specify voltage and temperature ranges over which a circuit's correct logic function is guaranteed. The specified DC electrical characteristics (see "DC electrical characteristics" on page 41) are satisfied over these ranges.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	3.0 to 3.6	V
	V_{DDC} (core) V_{DDC} (PLL)	1.4 to 1.6 1.425 to 1.575	V
Maximum junction temperature	T_J	125	^{o}C
† V_{DDA}: Ratings of I/O cells for 3.3V interface V_{DDC}: Ratings of internal cells			

Power dissipation

This table shows the *maximum power dissipation* for I/O and core:

CPU clock		Full	No LCD	No LCD, no serial
Total @ 177 MHz		639 mW	599 mW	599 mW
	Core	276 mW	269 mW	269 mW
	I/O	363 mW	330 mW	330 mW
Total @ 155 MHz		593 mW	564 mW	564 mW
	Core	243 mW	237 mW	237 mW
	I/O	350 mW	327 mW	327 mW
Total @ 103 MHz		475 mW	450 mW	450 mW
	Core	164 mW	159 mW	159 mW
	I/O	311 mW	291 mW	291 mW

Table 22: NS9360 power dissipation

This table shows the *refresh only* power dissipation for I/O and core.

CPU clock		Refresh only
Total @ 177 MHz		255.5 mW
	Core	61.5 mW
	I/O	194 mW
Total @ 155 MHz		237.5 mW
	Core	54 mW
	I/O	183.5 mW
Total @ 103 MHz		197.4 mW
	Core	39 mW
	I/O	158.4 mW

Table 23: Refresh only mode

DC electrical characteristics

DC electrical characteristics specify the worst-case DC electrical performance of the I/O buffers that are guaranteed over the specified temperature range.

Inputs

All electrical inputs are 3.3V interface.

Note: V_{SS} = 0V (GND)

Sym	Parameter	Condition	Value		Unit
V_{IH}	High-level input voltage: LVTTL level		Min	2.0	V
V_{IL}	Low-level input voltage: LVTTL level		Max	0.8	V
I_{IH}	High-level input current (no pulldown) Input buffer with pulldown	$V_{INA}=V_{DDA}$	Min/Max Min/Max	-10/10 10/200	µA µA
I_{IL}	Low-level input current (no pullup) Input buffer with pullup	$V_{INA}=V_{SS}$	Min/Max Min/Max	-10/10 10/200	µA µA
I_{OZ}	High-impedance leakage current	$V_{OUTA}=V_{DDA}$ or V_{SS}	Min/Max	-10/10	µA
I_{DDS}	Quiescent supply current	$V_{INA}=V_{DDA}$ or V_{SS}	Max	TBD	

USB internal PHY DC electrical inputs

Symbol	Parameter	Min	Max	Units	Notes
V_{IH}	Input high level (driven)	2.0		V	
V_{IZ}	Input high level (floating)	2.7	3.6	V	
V_{IL}	Input low level		0.8	V	
V_{DI}	Differential input sensitivity	0.2		V	1
V_{CM}	Differential common mode range	0.8	2.5	V	2

Notes:

1 |(usb_dp) - (usb_dm)|

2 Includes V_{DI} range.

Outputs

All electrical outputs are 3.3V interface.

Sym	Parameter	Value		Unit
V_{OH}	High-level output voltage (LVTTL)	Min	V_{DDA}-0.6	V
V_{OL}	Low-level output voltage (LVTTL)	Max	0.4	V

USB internal PHY DC electrical outputs

Symbol	Parameter	Min	Max	Units	Notes
V_{OL}	Output low level	0.0	0.3	V	1
V_{OH}	Output high level	2.8	3.6	V	2
V_{CRS}	Output signal crossover voltage	1.3	2.0	V	3

Notes:

1 Measured with R_L of 1.425k ohm to 3.6V.

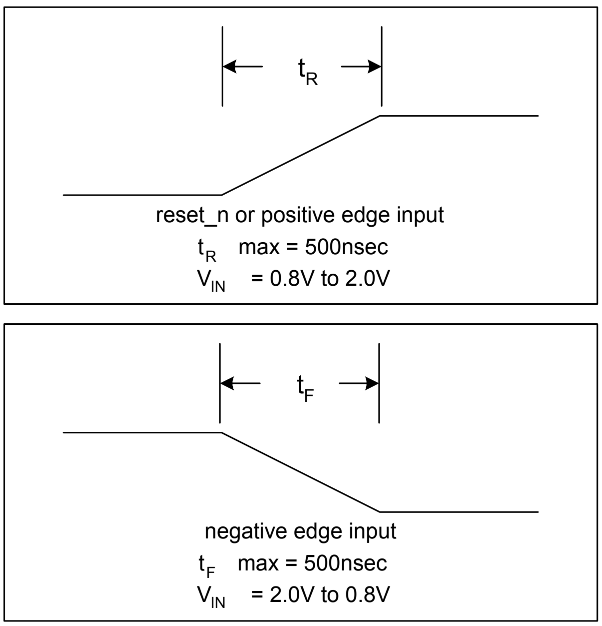
2 Measured with R_L of 14.25k ohm to GND.

3 Excluding the first transition from the idle state.

Reset and edge sensitive input timing requirements

The critical timing requirement is the rise and fall time of the input. If the rise time is too slow for the reset input, the hardware strapping options may be registered incorrectly. If the rise time of a positive-edge-triggered external interrupt is too slow, then an interrupt may be detected on both the rising and falling edge of the input signal.

A maximum rise and fall time must be met to ensure that reset and edge sensitive inputs are handled correctly. With Digi processors, the maximum is 500 nanoseconds as shown:

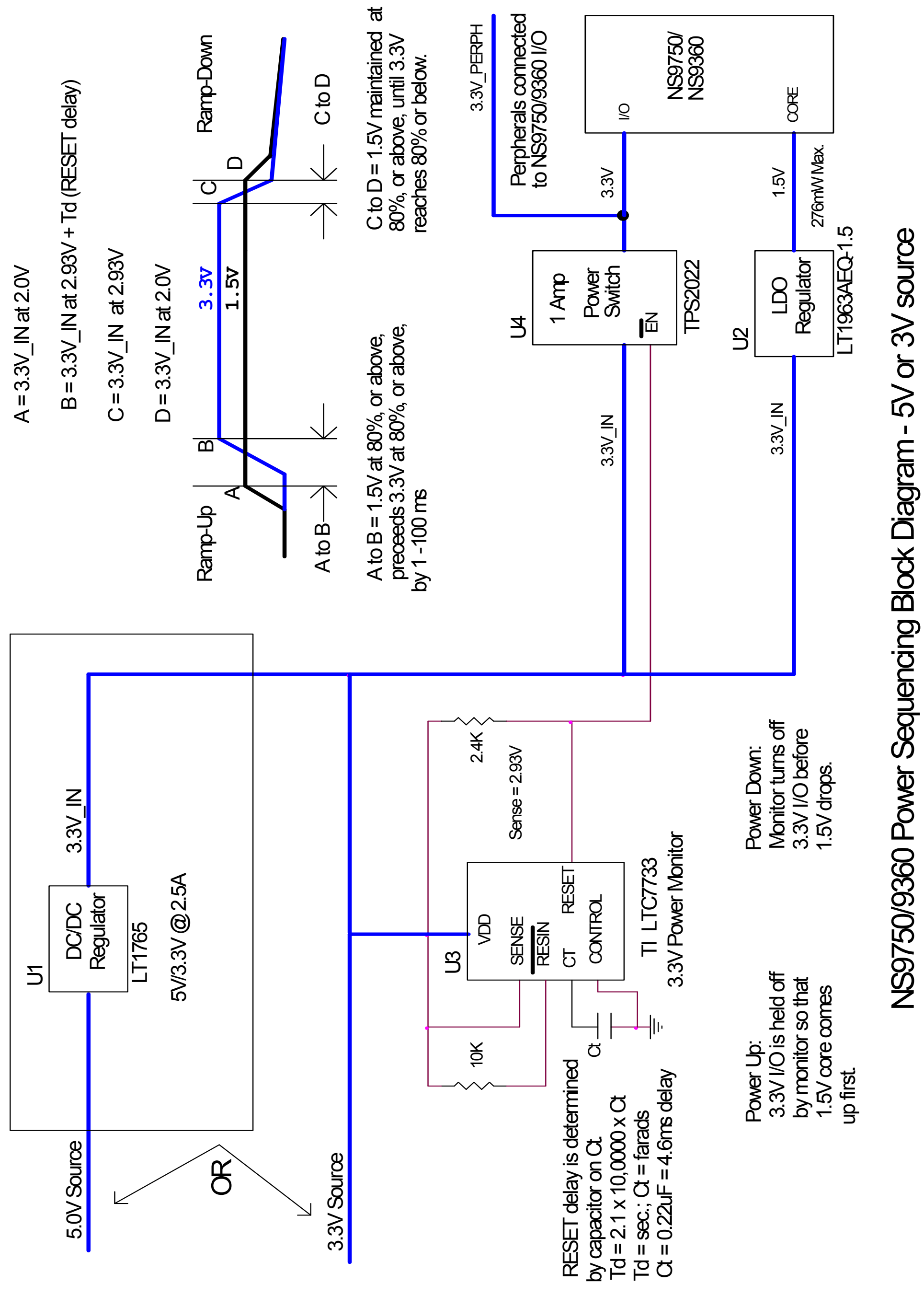


If an external device driving the reset or edge sensitive input on a Digi processor cannot meet the 500ns maximum rise and fall time requirement, the signal must be buffered with a Schmitt trigger device. Here are sample Schmitt trigger device part numbers:

Manufacturer	Part number	Description
Fairchild	NC7SP17	Single Schmitt trigger buffer, available in 5-lead SC70 and 6-lead MicroPak packages
Philips	74LVC1G17GW	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages
TI	SN74LVC1G17DCK	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages
ON Semi	NL17SZ17DFT2	Single Schmitt trigger buffer, available in 5-lead SC70 and SOT 353 packages.

Power sequencing

Use these requirements for power sequencing.



Memory timing

Memory AC characteristics are measured with 35pF.

Memory timing contains parameters and diagrams for both SDRAM and SRAM timing.

SDRAM timing diagrams

Table 24 describes the values shown in the SDRAM timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
M1	data input setup time to rising	1.0		ns	
M2	data input hold time to rising	0.0		ns	
M3	clk_out high to clk_en high		6.4	ns	
M4	clk_out high to address valid		6.4	ns	
M5	clk_out high to data_mask		6.4	ns	1, 2
M6	clk_out high to dy_cs_n low		6.4	ns	3, 4
M7	clk_out high to ras_n low		6.4	ns	
M8	clk_out high to cas_n low		6.4	ns	
M9	clk_out high to we_n low		6.4	ns	
M10	clk_out high to data out		6.6	ns	
M11	address hold time	4.0			
M12	data out hold time	4.0			
M13	clk_en high to sdram access	2	2	clock	
M14	end sdram access to clk_en low	2	2	clocks	

Table 24: SDRAM timing parameters

Notes:

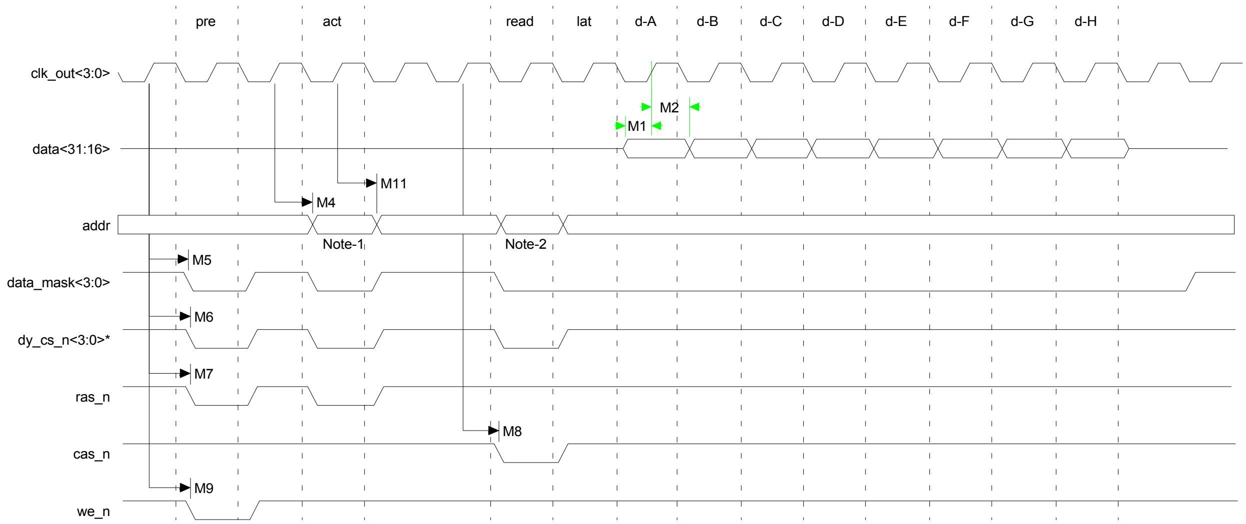
1 All four data_mask signals are used for all transfers.

2 All four data_mask signals will go low during a read cycle, for both 16-bit and 32-bit transfers.

3 Only one of the four clk_out signals is used.

4 Only one of the four dy_cs_n signals is used.

SDRAM burst read (16-bit)

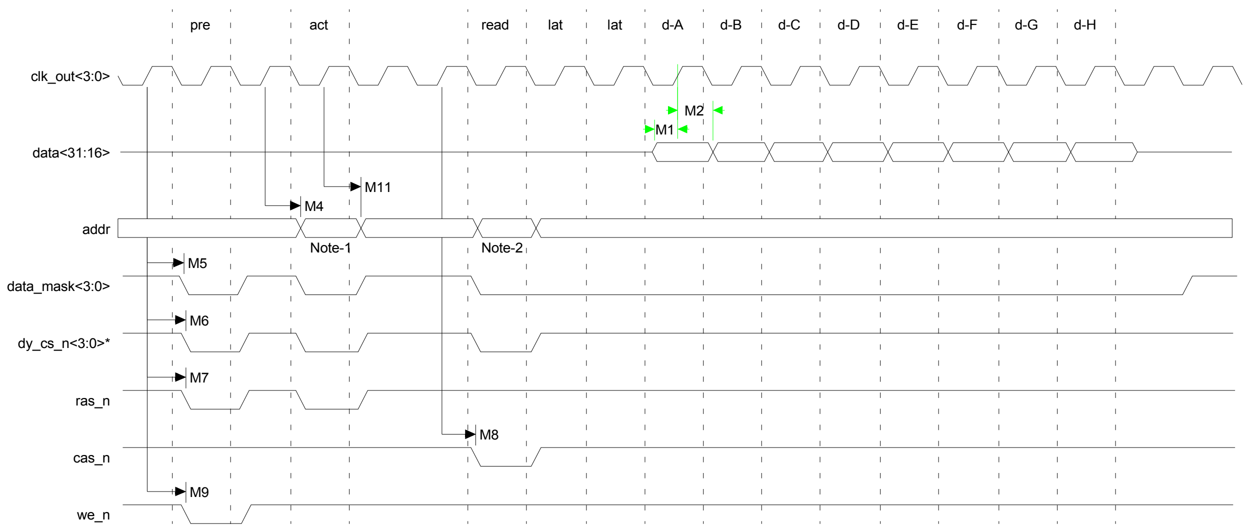


Notes:

1 This is the bank and RAS address.

2 This is the CAS address.

SDRAM burst read (16-bit), CAS latency = 3

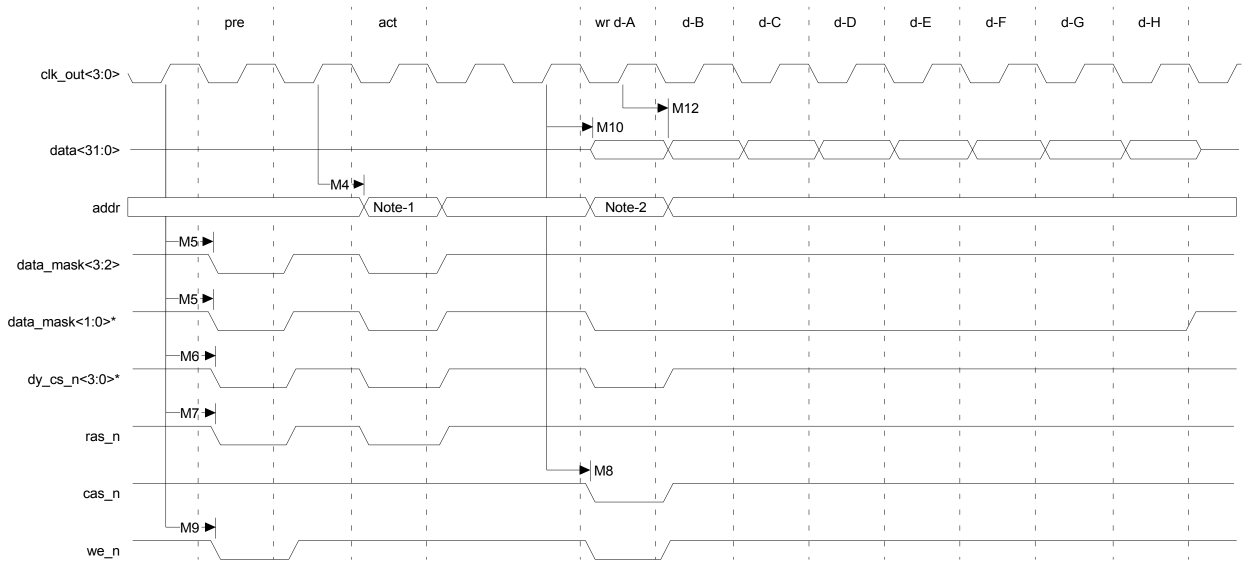


Notes:

1 This is the bank and RAS address.

2 This is the CAS address.

SDRAM burst write (16-bit)

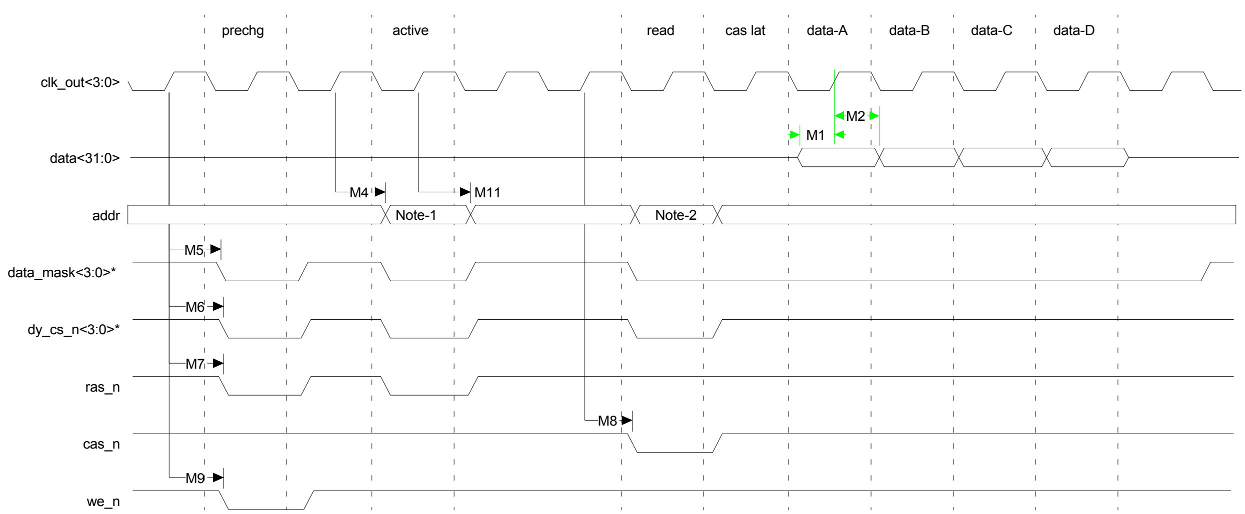


Notes:

1 This is the bank and RAS address.

2 This is the CAS address.

SDRAM burst read (32-bit)

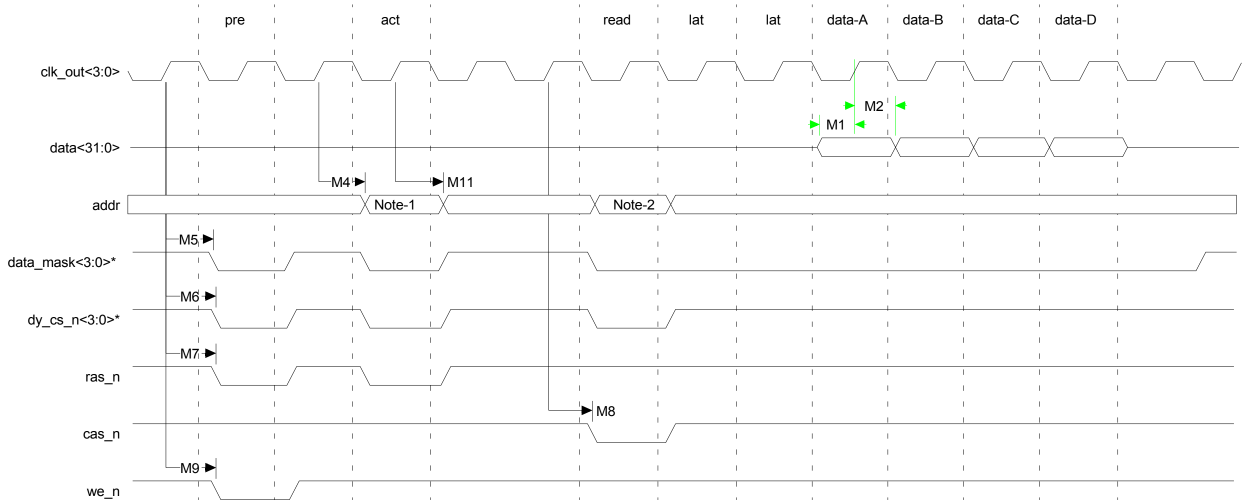


Notes:

1 This is the bank and RAS address.

2 This is the CAS address.

SDRAM burst read (32-bit), CAS latency = 3

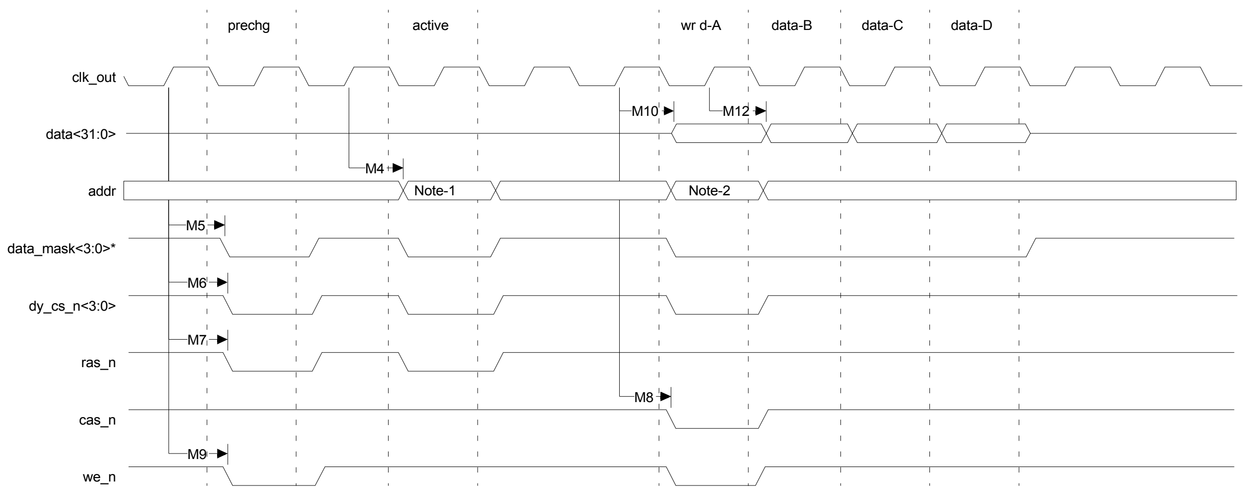


Notes:

1 This is the bank and RAS address.

2 This is the CAS address.

SDRAM burst write (32-bit)

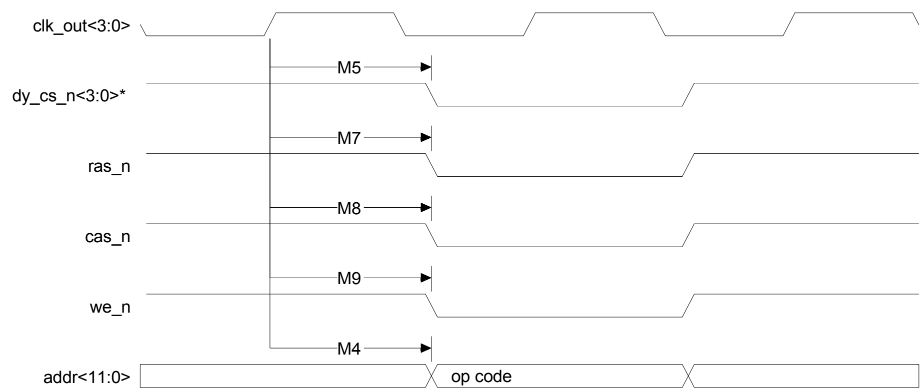


Notes:

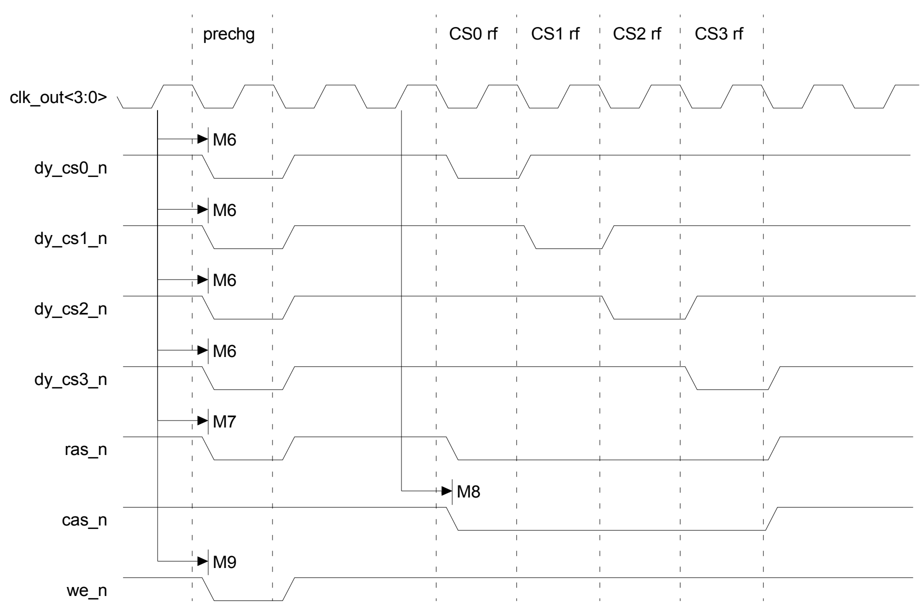
1 This is the bank and RAS address.

2 This is the CAS address.

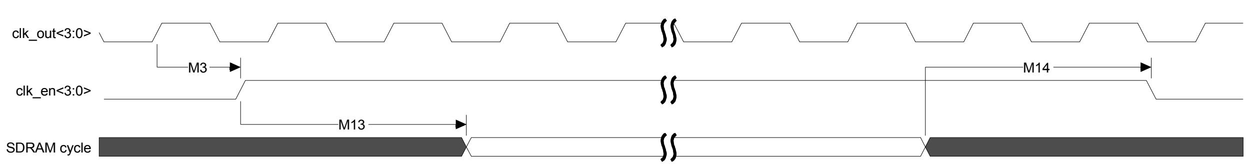
SDRAM load mode



SDRAM refresh mode



Clock enable timing



SRAM timing diagrams

Table 25 describes the values shown in the SRAM timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
M15	clock high to data out valid	-2	+2	ns	
M16	data out hold time from clock high	-2	+2	ns	
M17	clock high to address valid	-2	+2	ns	
M18	address hold time from clock high	-2	+2	ns	
M19	clock high to st_cs_n low	-2	+2	ns	2
M20	clock high to st_cs_n high	-2	+2	ns	2
M21	clock high to we_n low	-2	+2	ns	
M22	clock high to we_n high	-2	+2	ns	
M23	clock high to byte_lanes low	-2	+2	ns	
M24	clock high to byte_lanes high	-2	+2	ns	
M25	data input setup time to rising clk	10		ns	
M26	data input hold time to rising clk	0		ns	
M27	clock high to oe_n low	-2	+2	ns	
M28	clock high to oe_n high	-2	+2	ns	

Table 25: SRAM timing parameters

Notes:

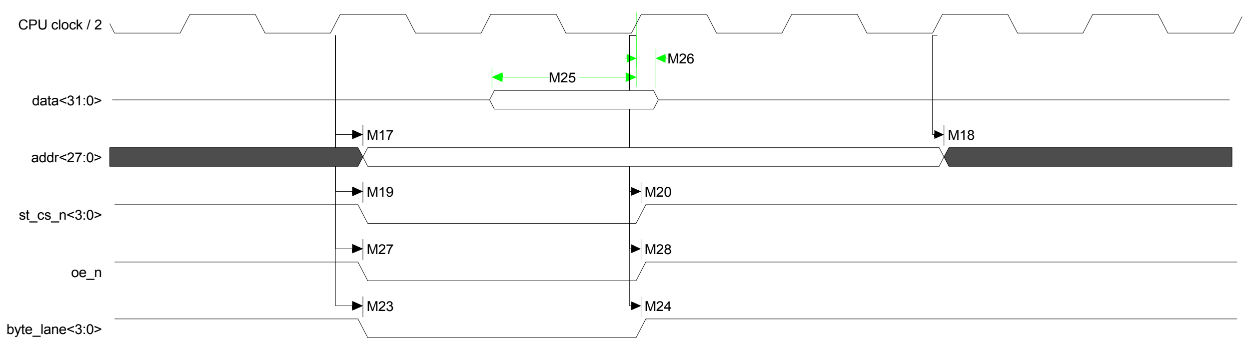
1 The (CPU clock out / 2) signal is for reference only.

2 Only one of the four dy_cs_n signals is used. The diagrams show the active low configuration, which can be reversed (active high) with the PC field.

3 Use this formula to calculate the length of the st_cs_n signal:

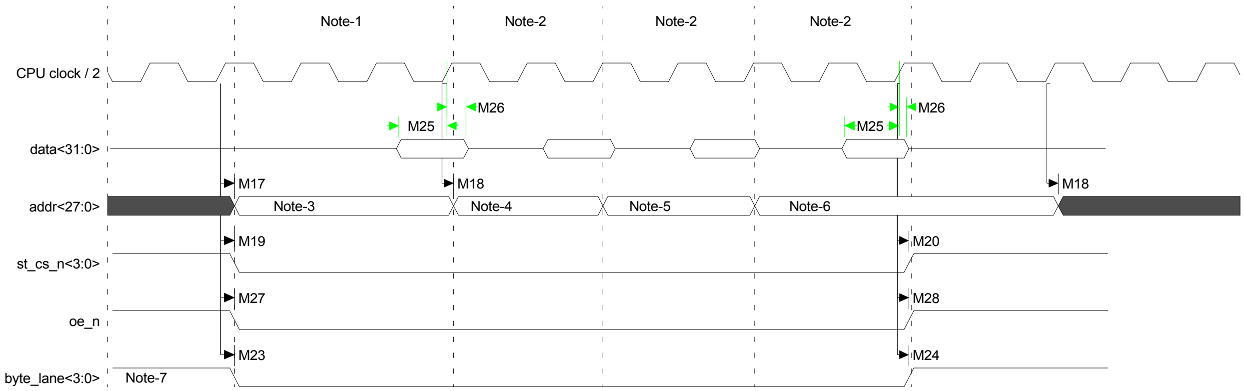
Tacc + board delay + (optional buffer delays, both address out and data in) + 10ns

Static RAM read cycles with 1 wait states



- WTRD = 1
  WOEN = 0
- If the PB field is set to 1, all four byte_lane signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- If the PB field is set to 0, the byte_lane signal will always be high.

Static RAM asynchronous page mode read, WTPG = 1



- WTPG = 1
  WTRD = 2
- If the PB field is set to 1, all four byte_lane signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- The asynchronous page mode will read 16 bytes in a page cycle. A 32-bit bus will do four 32-bit reads, as shown (3-2-2-2). A 16-bit bus will do eight 16-bit reads (3-2-2-2-3-2-2-2) per page cycle, and an 8-bit bus will do sixteen reads (3-2-2-2-3-2-2-2-3-2-2-2-3-2-2-2) per page cycle. 3-2-2-2 is the example used here, but the WTRD and WTPG field can set them differently.

Notes:

1 The length of the first cycle in the page is determined by the WTRD field.

2 The length of the 2nd, 3rd, and 4th cycles is determined by the WTPG field.

3 This is the starting address. The least significant two bits will always be ‘00.’

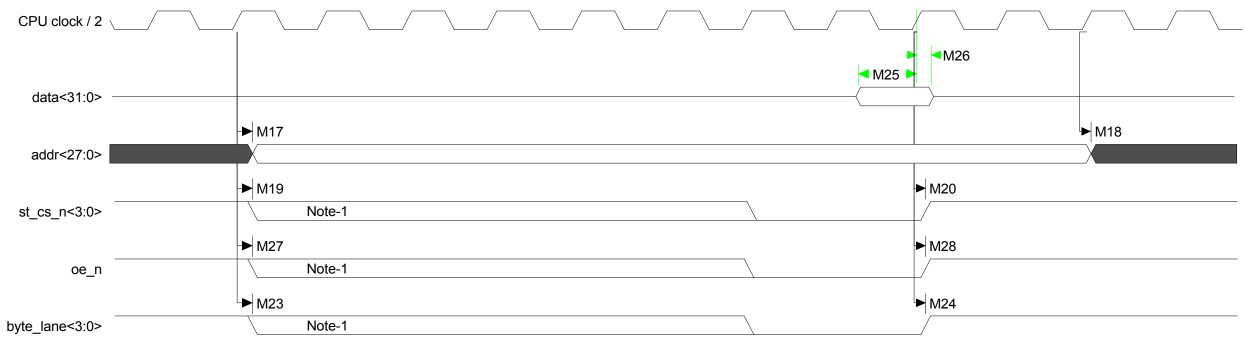
4 The least significant two bits in the second cycle will always be ‘01.’

5 The least significant bits in the third cycle will always be ‘10.’

6 The least significant two bits in the fourth cycle will always be ‘11.’

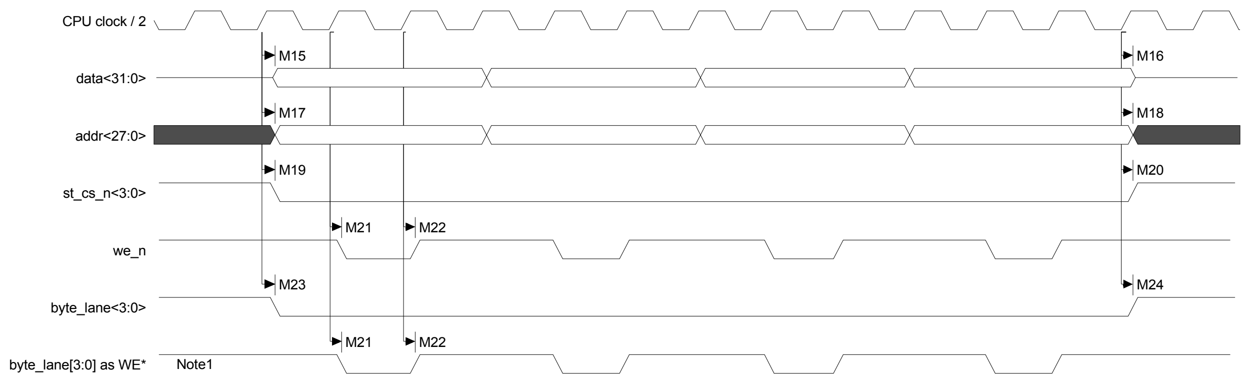
7 If the PB field is set to 0, the byte_lane signal will always be high during a read cycle.

Static RAM read cycle with configurable wait states



- WTRD = from 1 to 15
  WOEN = from 0 to 15
- If the PB field is set to 1, all four byte_lane signals will go low for 32-bit, 16-bit, and 8-bit read cycles.
- If the PB field is set to 0, the byte_lane signal will always be high.

Static RAM sequential write cycles

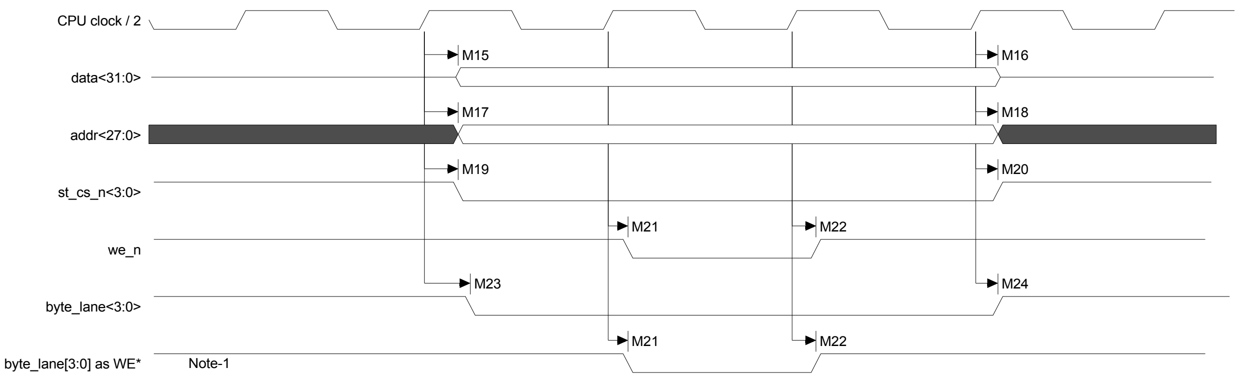


- WTWR = 0
  WWEN = 0
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Note:

1 If the PB field is set to 0, the byte_lane signals will function as write enable signals and the we_n signal will always be high.

Static RAM write cycle

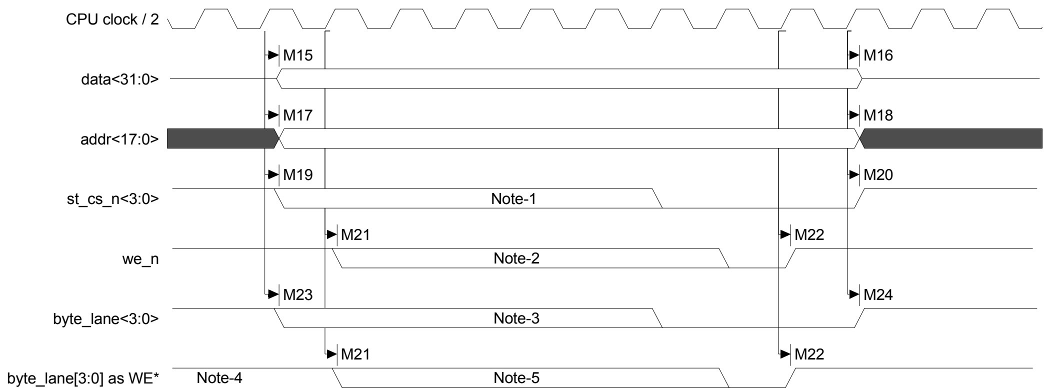


- WTWR = 0
  WWEN = 0
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Note:

1 If the PB field is set to 0, the byte_lane signals will function as write enable signals and the we_n signal will always be high.

Static write cycle with configurable wait states



- WTWR = from 0 to 15
  WWEN = from 0 to 15
- The WTWR field determines the length on the write cycle.
- During a 32-bit transfer, all four byte_lane signals will go low.
- During a 16-bit transfer, two byte_lane signals will go low.
- During an 8-bit transfer, only one byte_lane signal will go low.

Notes:

1 Timing of the st_cs_n signal is determined with a combination of the WTWR and WWEN fields. The st_cs_n signal will always go low at least one clock before we_n goes low, and will go high one clock after we_n goes high.

2 Timing of the we_n signal is determined with a combination of the WTWR and WWEN fields.

3 Timing of the byte_lane signals is determined with a combination of the WTWR and WWEN fields. The byte_lane signals will always go low one clock before we_n goes low, and will go one clock high after we_n goes high.

4 If the PB field is set to 0, the byte_lane signals will function as the write enable signals and the we_n signal will always be high.

5 If the PB field is set to 0, the timing for the byte_lane signals is set with the WTWR and WWEN fields.

Slow peripheral acknowledge timing

Table 26 describes the values shown in the slow peripheral acknowledge timing diagrams.

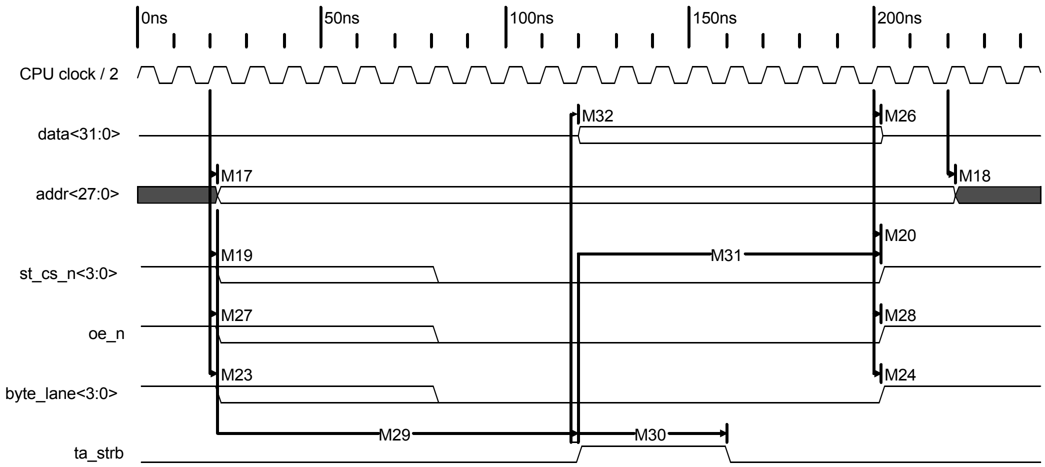
Parameter	Description	Min	Max	Unit	Notes
M15	clock high to data out valid	-2	+2	ns	
M16	data out hold time from clock high	-2	+2	ns	
M17	clock high to address valid	-2	+2	ns	
M18	address hold time from clock high	-2	+2	ns	
M19	clock high to st_cs_n low	-2	+2	ns	1
M20	clock high to st_cs_n high	-2	+2	ns	1
M21	clock high to we_n low	-2	+2	ns	
M22	clock high to we_n high	-2	+2	ns	
M23	clock high to byte_lanes low	-2	+2	ns	
M24	clock high to byte_lanes high	-2	+2	ns	
M26	data input hold time to rising clk	0		ns	
M27	clock high to oe_n low	-2	+2	ns	
M28	clock high to oe_n high	-2	+2	ns	
M29	address/chip select valid to ta_strb high	2		CPU cycles	
M30	ta_strb pulse width	4	8	CPU cycles	
M31	ta_strb rising to chip select/address change	4	10	CPU cycles	
M32	data setup to ta_strb rising	0		ns	

Table 26: Slow peripheral acknowledge

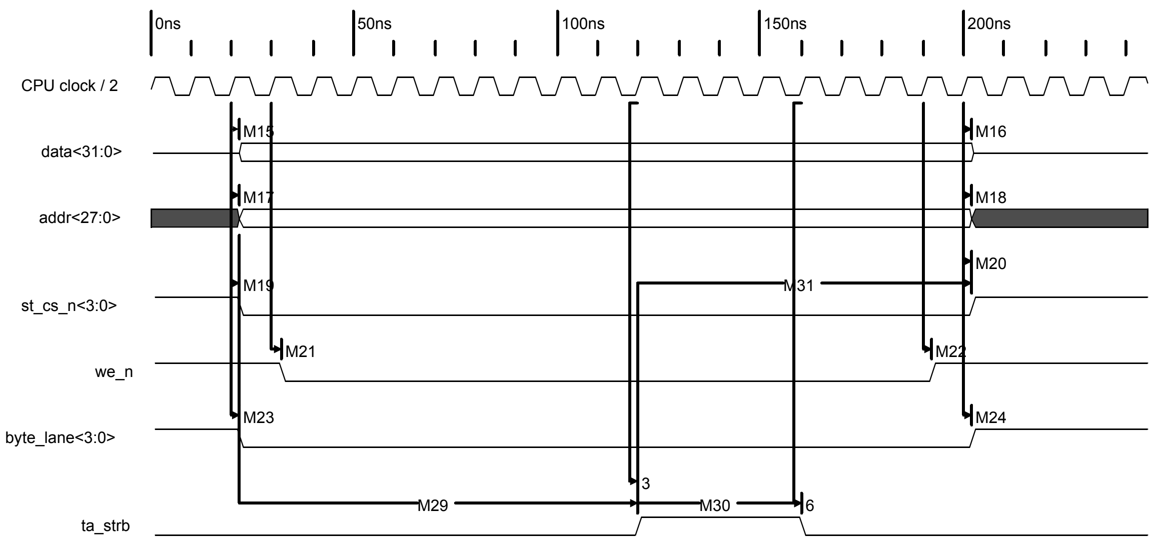
Note:

1 Only one of the four st_cs_n signals is used. The diagrams show the active low configuration, which can be reversed (active high) with PC field.

Slow peripheral acknowledge read



Slow peripheral acknowledge write



Ethernet timing

Ethernet AC characteristics are measured with 10pF.

Table 27 describes the values shown in the Ethernet timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
E1	MII tx_clk to txd, tx_en, tx_er	3	11	ns	2
E2	MII rxd, rx_en, rx_er setup to rx_clk rising	3		ns	
E3	MII rxd, rx_en, rx_er hold from rx_clk rising	1		ns	
E4	mdio (input) setup to mdc rising	10		ns	
E5	mdio (input) hold from mdc rising	0		ns	
E6	mdc to mdio (output)	20	36	ns	1, 2
E7	mdc period	91		ns	4
E8	RMII ref_clk to txd, tx_en	3	12	ns	2
E9	RMII rxd, crs, rx_er setup to ref_clk rising	3		ns	
E10	RMII rxd, crs, rx_er hold from ref_clk rising	1		ns	
E11	MII rx_clk to cam_req	3	10	ns	
E12	MII cam_reject setup to rx_clk rising	N/A		ns	3
E13	MII cam_reject hold from rx_clk rising	N/A		ns	3

Table 27: Ethernet timing characteristics

Notes:

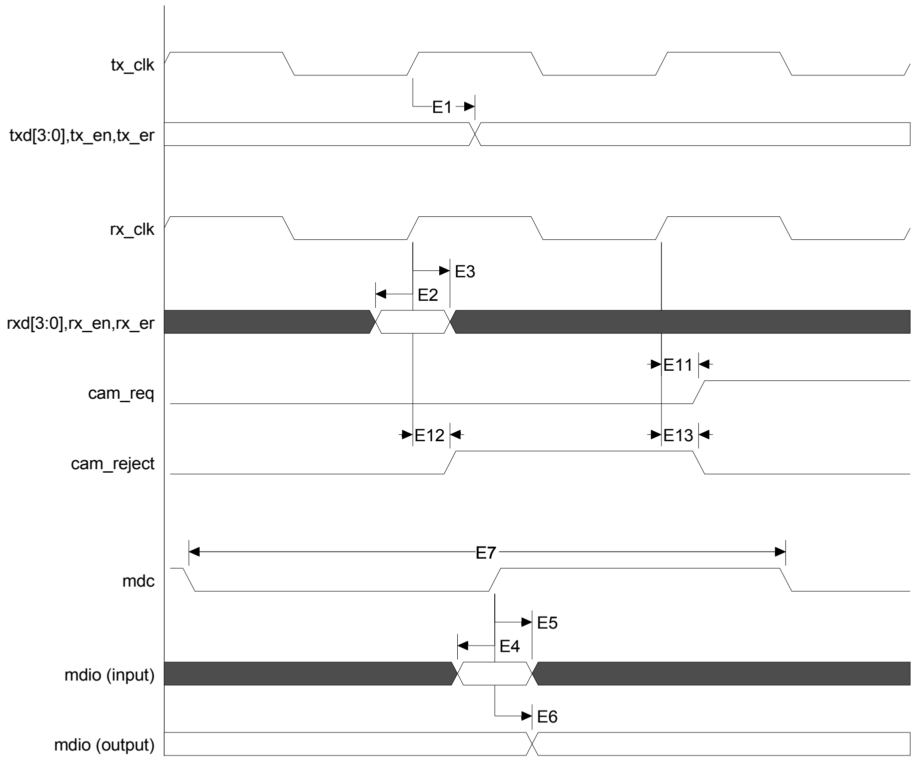
1 Minimum specification is for fastest AHB bus clock of 88.5 MHz. Maximum specification is for slowest AHB bus clock of 51.6 MHz.

2 C_{load} = 10pf for all outputs and bidirects.

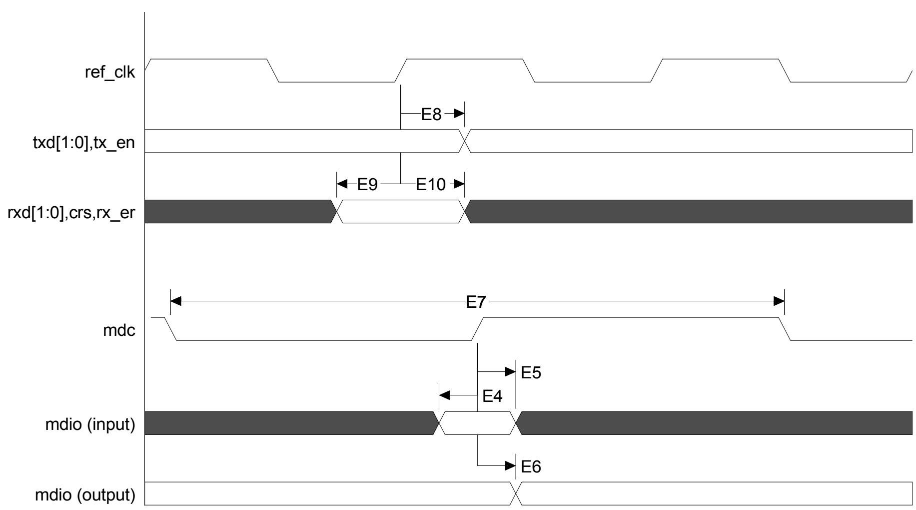
3 No setup and hold requirements for cam_reject because it is an asynchronous input. This is also true for RMII PHY applications.

4 Minimum specification is for fastest AHB bus clock of 88.5 MHz.

Ethernet MII timing



Ethernet RMII timing



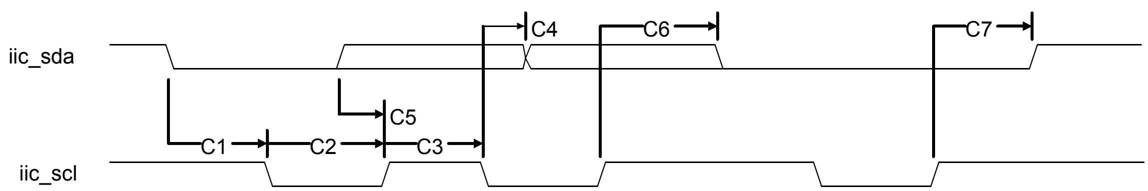
I^2C timing

I^2C AC characteristics are measured with 10pf.

Table 28 describes the values shown in the I^2C timing diagram.

		Standard mode		Fast mode		
Parm	**Description**	**Min**	**Max**	**Min**	**Max**	**Unit**
C1	iic_sda to iic_scl START hold time	4.0		0.6		µs
C2	iic_scl low period	4.7		1.3		µs
C3	iic_scl high period	4.7		1.3		µs
C4	iic_scl to iic_sda DATA hold time	0		0		µs
C5	iic_sda to iic_scl DATA setup time	250		100		ns
C6	iic_scl to iic_sda START setup time	4.7		0.6		µs
C7	iic_scl to iic_sda STOP setup time	4.0		0.6		µs

Table 28: I^2C timing parameters



LCD timing

LCD AC characteristics are measured with 10pF.

Table 29 describes the values shown in the LCD timing diagrams.

Parameter	Description	Register	Value	Units
L1	Horizontal front porch blanking	LCDTiming0	HFP+1	CLCP periods
L2	Horizontal sync width	LCDTiming0	HSW+1	CLCP periods
L3	Horizontal period	N/A	L1+L2+L15+L4	CLCP periods
L4	Horizontal backporch	LCDTiming0	HBP+1	CLCP periods
L5	TFT active line	LCDTiming0	16*(PPL+1) (see note 3)	CLCP periods
L6	LCD panel clock frequency	LCDTiming1	**For BCD=0:** CLCDCLK/(PCD+2) **For BCD=1:** CLCDCLK (see notes 1 & 10)	MHz
L7	TFT vertical sync width	LCDTiming1	VSW+1	H lines
L8	TFT vertical lines/frame	N/A	L7+L9+L10+L11	H lines
L9	TFT vertical back porch	LCDTiming1	VBP	H lines
L10	TFT vertical front porch	LCDTiming1	VFP	H lines
L11	Active lines/frame	LCDTiming1	LPP+1	H lines
L12	STN HSYNC inactive to VSYNC active	LCDTiming0	HBP+1	CLCP periods
L13	STN vertical sync width	N/A	1	H lines
L14	STN vertical lines/frame	N/A	L11+L16	H lines
L15	STN active line	LCDTiming1	CPL+1 (see note 4)	CLCP periods
L16	STN vertical blanking	LCDTiming1	VSW+VFP+VBP+1	H lines
L17	STN CLCP inactive to HSYNC active	LCDTiming0	HFP+1.5	CLCP periods
L18	CLCP to data/control (see notes 7 and 8)		–2.0 (min) +2.0 (max)	ns
L19	CLCP high (see notes 8, 9)		50%±0.5ns	ns
L20	CLCP low (see notes 8, 9)		50%±0.5ns	ns
L21	TFT VSYNC active to HSYNC active (see note 8)		-0.1ns (min) +0.1ns (max)	ns
L22	TFT VSYNC active to HSYNC inactive	LCDTiming0	HSW	CLCP periods

Table 29: LCD timing parameters

Parameter	Description	Register	Value	Units
L23	STN VSYNC active to HSYNC inactive	LCDTiming0	**STN color:** 14+HSW+HFP **STN Mono8:** 6+HSW+HFP **STN Mono4:** 10+HSW+HFP	CLCP periods
L24	STN HSYNC inactive to VSYNC inactive	LCDTiming0	HBP+1	CLCP periods
L25	STN VSYNC inactive to HSYNC active	LCDTiming0	**STN color:** HFP+13 **STN Mono8:** HFP+15 **STN Mono4:** HFP+9	CLCP periods
L26	CLCP period		22.22 (minimum)	ns

Table 29: LCD timing parameters

Notes:

1 CLCDCLK is selected from 5 possible sources:
- — lcdclk/2 (lcdclk is an external oscillator)
- — AHB clock
- — AHB clock/2
- — AHB clock/4
- — AHB clock/8

See the LCD chapter in the *NS9360 Hardware Reference* for acceptable clock frequencies for the different display configurations.

2 The polarity of CLLP, CLFP, CLCP, and CLAC can be inverted using control fields in the LCDTiming1 register.

3 The CPL field in the LCDTiming1 register must also be programmed to T5-1 (see the LCD chapter in the *NS9360 Hardware Reference*).

4 The PPL field in the LCDTiming0 register must also be programmed correctly (see the LCD chapter in the *NS9360 Hardware Reference*).

5 These data widths are supported:
- — 4-bit mono STN single panel
- — 8-bit mono STN single panel
- — 8-bit color STN single panel
- — 4-bit mono STN dual panel (8 bits to LCD panel)
- — 8-bit mono STN dual panel (16 bits to LCD panel)
- — 8-bit color STN dual panel (16 bits to LCD panel)
- — 18-bit TFT

6 See the LCD chapter in the *NS9360 Hardware Reference* for definitions of the bit fields referred to in this table.

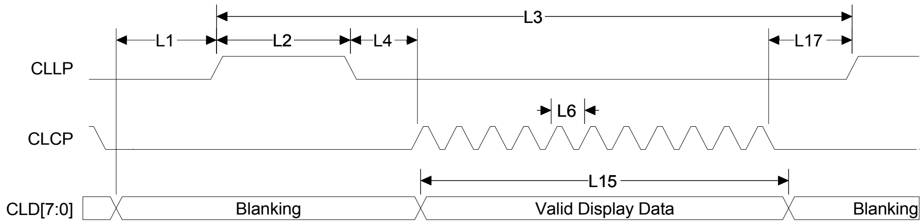
7 Note that data is sampled by the LCD panel on the falling edge of the CLCP in the LCD output timing diagram. If the polarity of CLCP is inverted, this parameter is relative to CLCP falling instead.

8 C_{load} = 10pf on all outputs.

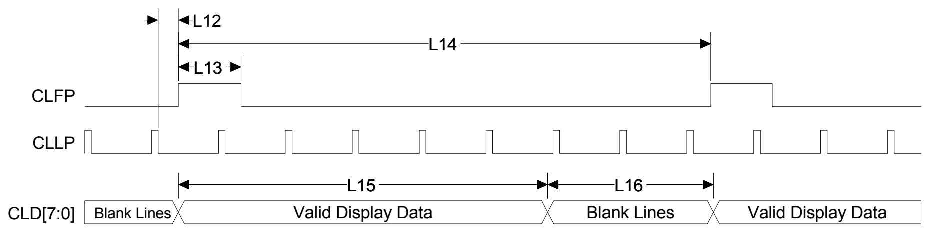
9 CLCP high and low times specified as 50% of the clock period ±0.5ns.

10 Maximum allowable LCD panel clock frequency is 45 MHz.

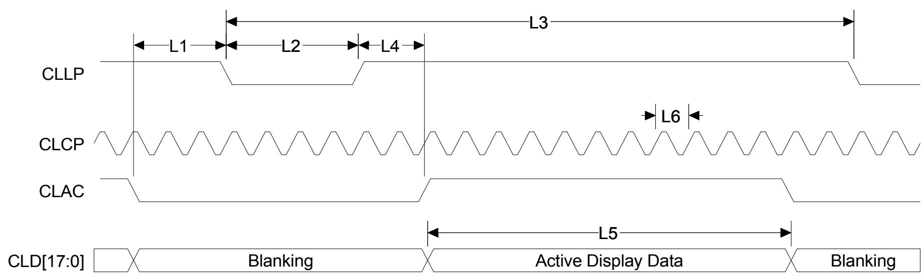
Horizontal timing for STN displays



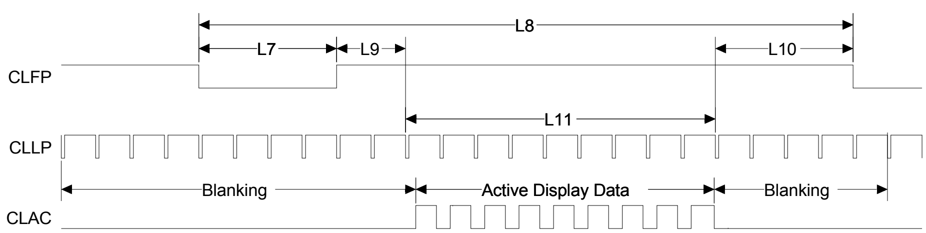
Vertical timing for STN displays



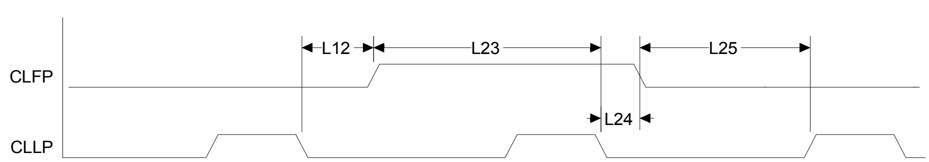
Horizontal timing for TFT displays



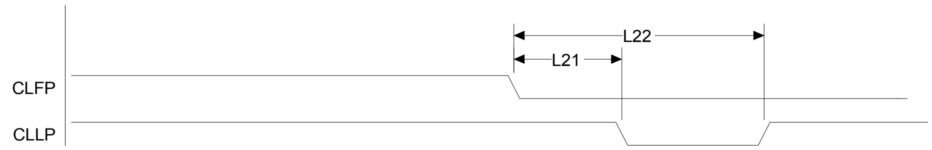
Vertical timing for TFT displays



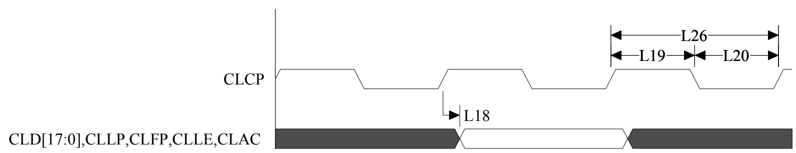
HSYNC vs VSYNC timing for STN displays



HSYNC vs VSYNC timing for TFT displays



LCD output timing



SPI timing

SPI AC characteristics are measured with 10pF, unless otherwise noted.

Table 30 describes the values shown in the SPI timing diagrams.

Parm	Description	Min	Max	Unit	Modes	Notes
SPI master parameters						
SP0	SPI enable low setup to first SPI CLK out rising	$3*T_{BCLK}$-10		ns	0, 3	1, 3
SP1	SPI enable low setup to first SPI CLK out falling	$3*T_{BCLK}$-10		ns	1, 2	1, 3
SP3	SPI data in setup to SPI CLK out rising	30		ns	0, 3	
SP4	SPI data in hold from SPI CLK out rising	0		ns	0, 3	
SP5	SPI data in setup to SPI CLK out falling	30		ns	1, 2	
SP6	SPI data in hold from SPI CLK out falling	0		ns	1, 2	
SP7	SPI CLK out falling to SPI data out valid		10	ns	0, 3	6
SP8	SPI CLK out rising to SPI data out valid		10	ns	1, 2	6
SP9	SPI enable low hold from last SPI CLK out falling	$3*T_{BCLK}$-10		ns	0, 3	1, 3
SP10	SPI enable low hold from last SPI CLK out rising	$3*T_{BCLK}$-10		ns	1, 2	1, 3
SP11	SPI CLK out high time	SP13*45%	SP13*55%	ns	0, 1, 2, 3	4
SP12	SPI CLK out low time	SP13*45%	SP13*55%	ns	0, 1, 2, 3	4
SP13	SPI CLK out period	$T_{BCLK}*6$		ns	0, 1, 2, 3	3
SPI slave parameters						
SP14	SPI enable low setup to first SPI CLK in rising	30		ns	0, 3	1
SP15	SPI enable low setup to first SPI CLK in falling	30		ns	1, 2	1
SP16	SPI data in setup to SPI CLK in rising	0		ns	0, 3	
SP17	SPI data in hold from SPI CLK in rising	60		ns	0, 3	
SP18	SPI data in setup to SPI CLK in falling	0		ns	1, 2	
SP19	SPI data in hold from SPI CLK in falling	60		ns	1, 2	
SP20	SPI CLK in falling to SPI data out valid	20	70	ns	0, 3	6
SP21	SPI CLK in rising to SPI data out valid	20	70	ns	1, 2	6
SP22	SPI enable low hold from last SPI CLK in falling	15		ns	0, 3	1
SP23	SPI enable low hold from last SPI CLK in rising	15		ns	1, 2	1
SP24	SPI CLK in high time	SP26*40%	SP26*60%	ns	0, 1, 2, 3	5
SP25	SPI CLK in low time	SP26*40%	SP26*60%	ns	0, 1, 2, 3	5

Table 30: SPI timing parameters

Parm	Description	Min	Max	Unit	Modes	Notes
SP26	SPI CLK in period	T_{BCLK}*8		ns	0, 1, 2, 3	

Table 30: SPI timing parameters

Notes:

1 Active level of SPI enable is inverted (that is, 1) if the CSPOL bit in Serial Channel B/A/C/D Control Register B (see the *NS9360 Hardware Reference*) is set to 1. Note that in SPI slave mode, only a value of 0 (low enable) is valid; the SPI slave is fixed to an active low chip select.

2 SPI data order is reversed (that is, LSB last and MSB first) if the BITORDR bit in Serial Channel B/A/C/D Control Register B (see the *NS9360 Hardware Reference*) is set to 0.

3 T_{BCLK} is a period of BBus clock.

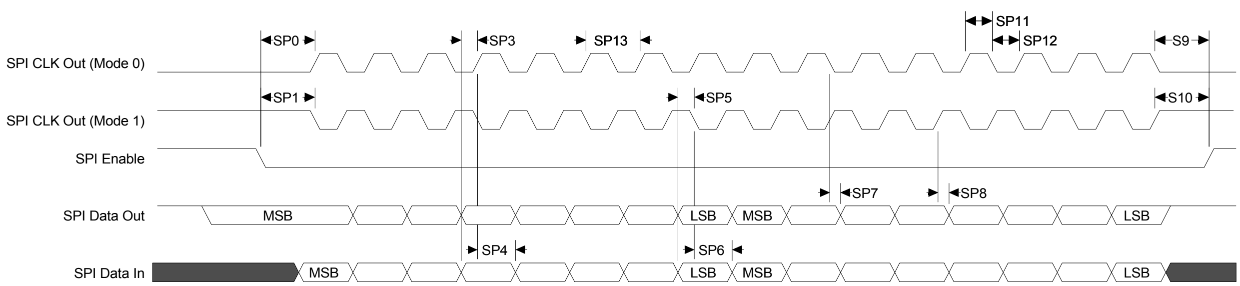
4 ±5% duty cycle skew.

5 ±10% duty cycle skew.

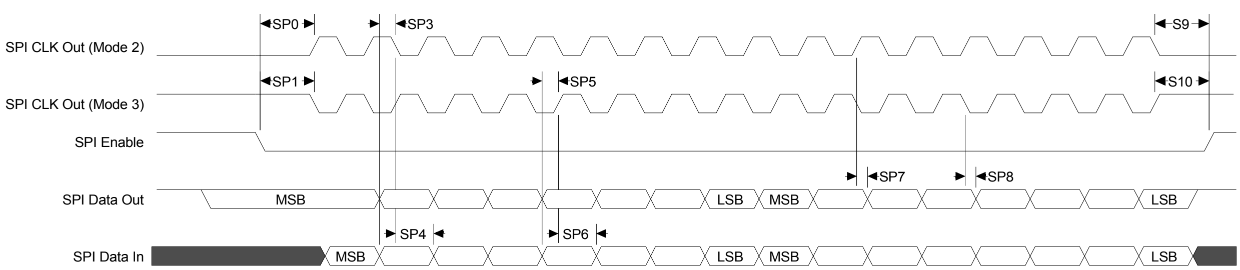
6 C_{load} = 5pf for all outputs.

7 SPI data order can be reversed such that LSB is first. Use the BITORDR bit in Serial Channel B/A/C/D Control Register A.

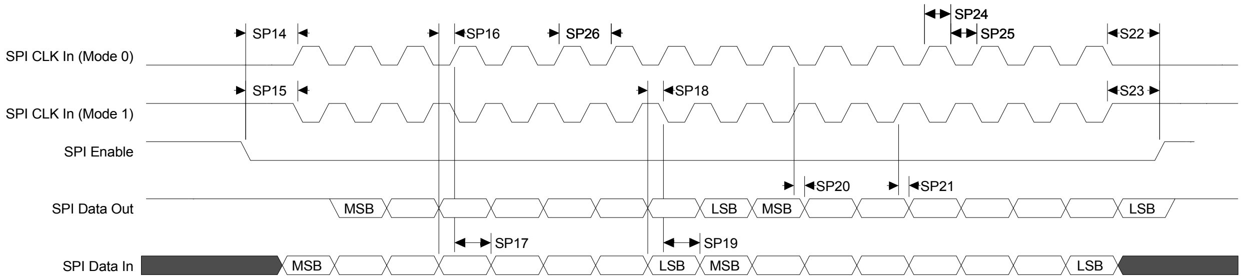
SPI master mode 0 and 1: 2-byte transfer *(see note 7)*



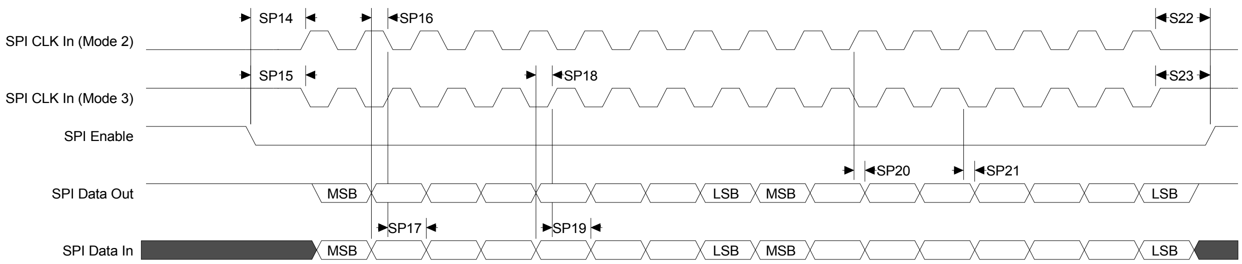
SPI master mode 2 and 3: 2-byte transfer *(see note 7)*



SPI slave mode 0 and 1: 2-byte transfer *(see note 7)*



SPI slave mode 2 and 3: 2-byte transfer *(see note 7)*



IEEE 1284 timing

IEEE 1284 AC characteristics are measured with 10pF.

Table 31 describes the values shown in the IEEE 1284 timing diagram.

Parameter	Description	Min	Max	Unit	Note
IE1	Busy-while-Strobe	0	511	ns	1
IE2	Busy high to nAck low	0		ns	
IE3	Busy high		1022	ns	2
IE4	nAck low		511	ns	3
IE5	nAck high to Busy low		511	ns	3

Table 31: IEEE 1284 timing parameters

Notes:

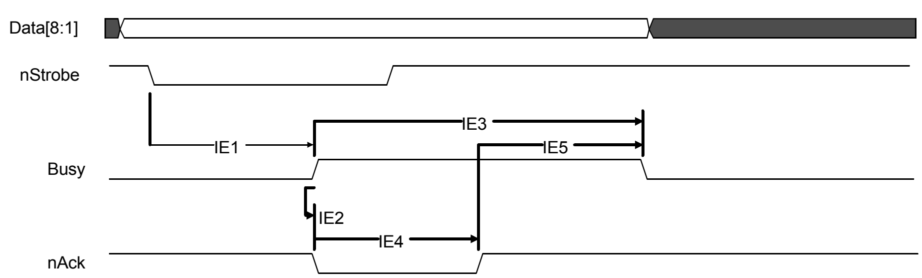
1 The range is 0ns up to one time unit.

2 Two time units.

3 One time unit.

IEEE 1284 timing example

The IEEE 1284 timing is determined by the BBus clock and the Granularity Count register (GCR) setting. In this example, the BBus clock is 45 MHz and the Granularity Count register is set to 23. The basic time unit is 1/45 MHz x 23, which is 511ns (the basic time unit must be at least 511 ns).



USB internal PHY timing

Table 32 and Table 33 describe the values shown in the USB internal PHY timing diagrams.

Parameter	Description	Min	Max	Unit	Notes
U1	Rise time (10%–90%)	4	20	ns	1
U2	Fall time (10%–90%)	4	20	ns	1
U3	Differential rise and fall time matching	90	111.11	%	1, 2, 5
U4	Driver output resistance	28	44	ohms	3

Table 32: USB internal PHY full speed timing parameters

Parameter	Description	Min	Max	Unit	Notes
U1	Rise time (10%–90%)	75	300	ns	4
U2	Fall time (10%–90%)	75%	300	ns	4
U3	Differential rise and fall time matching	80	125	%	2, 4, 5

Table 33: USB internal PHY low speed timing parameters

Notes:

1 Load shown in "USB internal PHY full speed load."

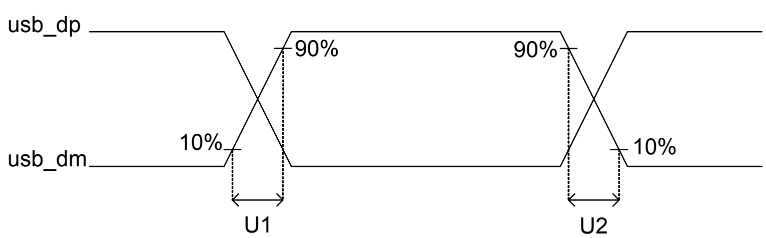
2 U1/U2.

3 Includes resistance of 27 ohm ±2 ohm external series resistor.

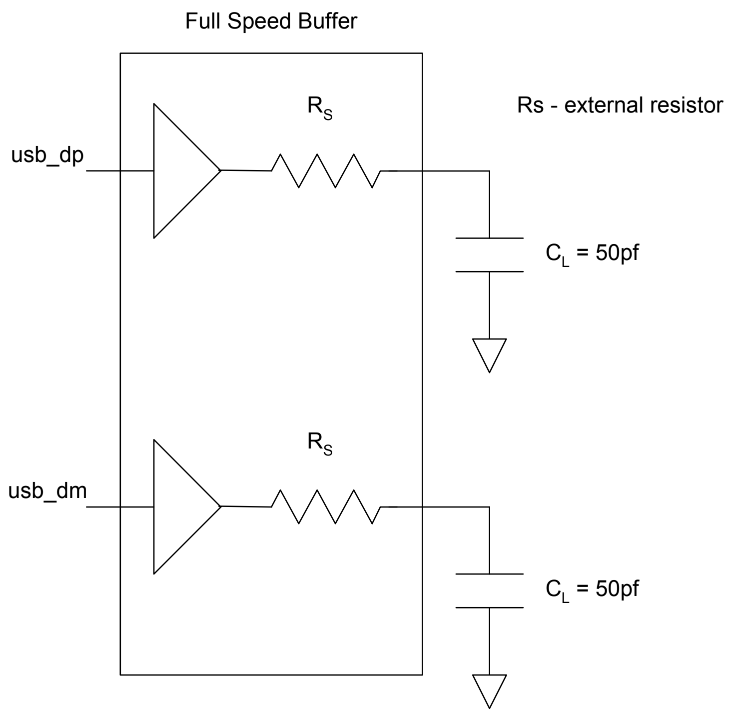
4 Load shown in "USB internal PHY low speed load."

5 Excluding the first transition from the idle state.

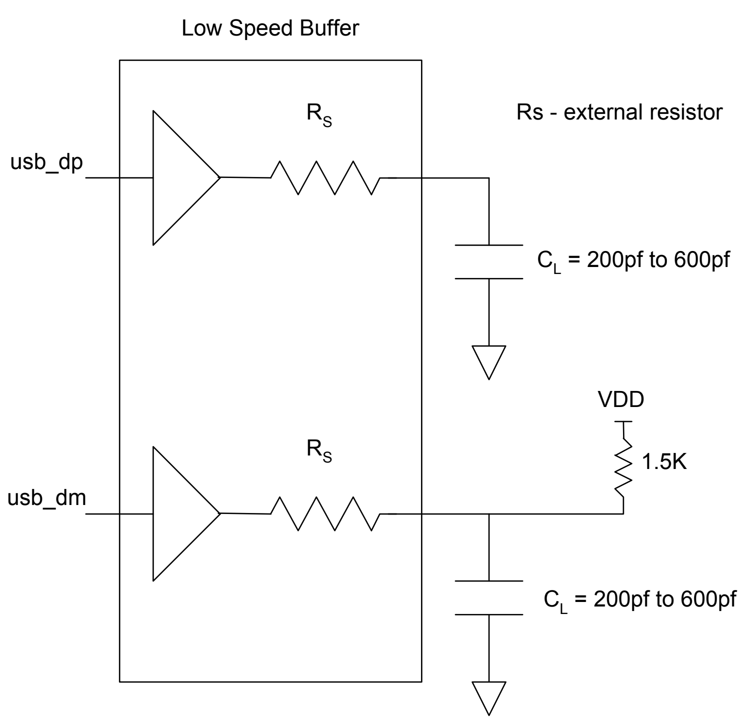
USB internal PHY differential data timing



USB internal PHY full speed load



USB internal PHY low speed load



USB external PHY interface

USB external PHY AC characteristics are measured with 10pF.

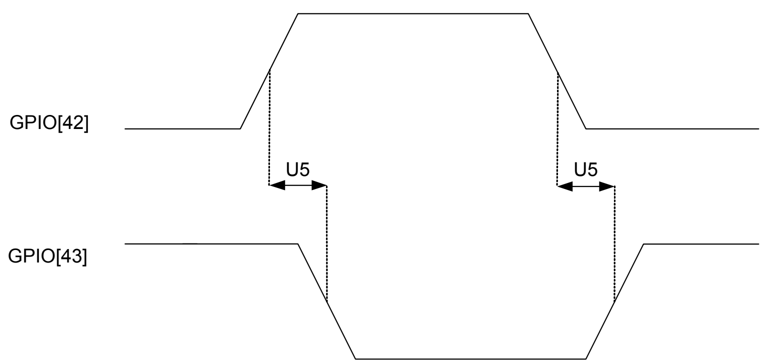
Table 34 describes the values shown in the USB external PHY timing diagram.

Parameter	Description	Min	Max	Unit	Notes
U5	Output skew	-0.25	0.25	ns	1

Table 34: USB external PHY interface output timing parameters

Note:

1 Output skew between any of the output signals that interface to an external USB PHY; that is, GPIO[44:42] and GPIO[49:48] for primary interface or GPIO[52:50] and GPIO[55:54] for duplicate interface.



Reset and hardware strapping timing

Reset and hardware strapping AC characteristics are measured with 10pF.

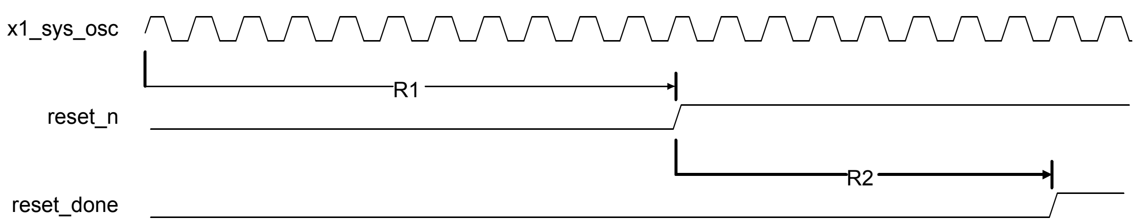
Table 35 describes the values shown in the reset and hardware strapping timing diagram.

Parameter	Description	Min	Typ	Unit	Notes
R1	reset_n minimum time	10		x1_sys_osc clock cycles	1
R2	reset_n to reset_done		NOR flash:4.5 SPI flash: 15	ms	

Table 35: Reset and hardware strapping timing parameters

Note:

1 The hardware strapping pins are latched 5 clock cycles after reset_n is deasserted (goes high).



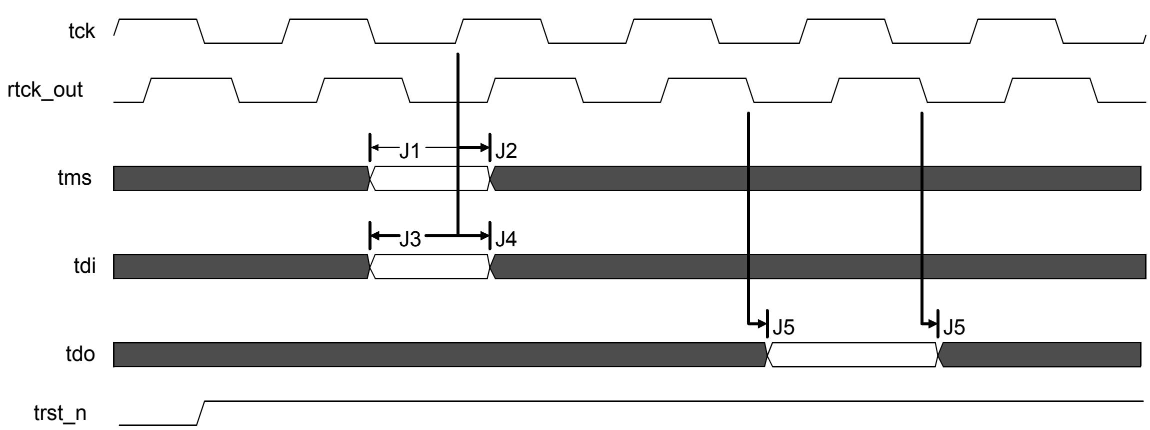
JTAG timing

JTAG AC characteristics are measured with 10pF.

Table 36 describes the values shown in the JTAG timing diagram.

Parameter	Description	Min	Max	Unit
J1	tms (input) setup to tck rising	5		ns
J2	tms (input) hold to tck rising	2		ns
J3	tdi (input) setup to tck rising	5		ns
J4	tdi (input) hold to tck rising	2		ns
J5	tdo (output) to tck falling	2.5	10	ns

Table 36: JTAG timing parameters



- Maximum tck rate is 10 MHz.
- rtck_out is an asynchronous output, driven off of the CPU clock.
- trst_n is an asynchronous input.

Clock timing

Clock AC characteristics are measured with 10pF.

The next timing diagrams pertain to clock timing.

USB crystal/external oscillator timing

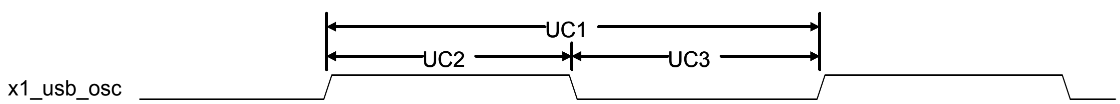
Table 37 describes the values shown in the USB crystal/external oscillator timing diagram.

Parameter	Description	Min	Max	Unit	Notes
UC1	x1_usb_osc cycle time	20.831	20.835	ns	1
UC2	x1_usb_osc high time	(UC1/2) x 0.4	(UC1/2) x 0.6	ns	
UC3	x1_usb_osc low time	(UC1/2) x 0.4	(UC1/2) X 0.6	ns	

Table 37: USB crystal/external oscillator timing parameters

Note:

1 If using a crystal, the tolerance must be ±100 ppm or better.



LCD input clock

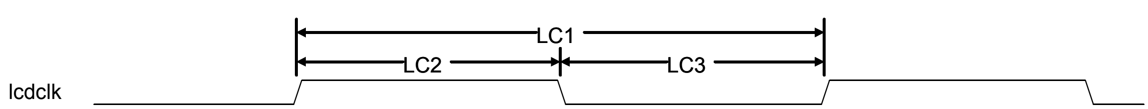
Table 38 describes the values shown for the LCD input clock timing diagram.

Parameter	Description	Min	Max	Unit	Notes
LC1	lcdclk cycle time	11.11		ns	1
LC2	lcdclk high time	(LC1/2) x 0.4	(LC1/2) x 0.6	ns	
LC3	lcdclk low time	(LC1/2) x 0.4	(LC1/2) x 0.6	ns	

Table 38: LCD input clock timing parameters

Note:

1 The clock rate supplied on lcdclk is twice the actual LCD clock rate.



System PLL reference clock timing

Table 39 describes the values shown in the system PLL reference clock timing diagram.

Parameter	Description	Min	Max	Unit
SC1	x1_sys_osc cycle time	50	25	ns
SC2	x1_sys_osc high time	(SC1/2) x 0.45	(SC1/2) x 0.55	ns
SC3	x1_sys_osc low time	(SC1/2) x 0.45	(SC1/2) x 0.55	ns

Table 39: System PLL reference clock timing parameters

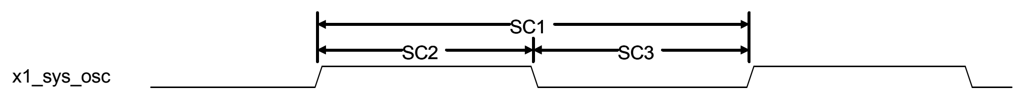


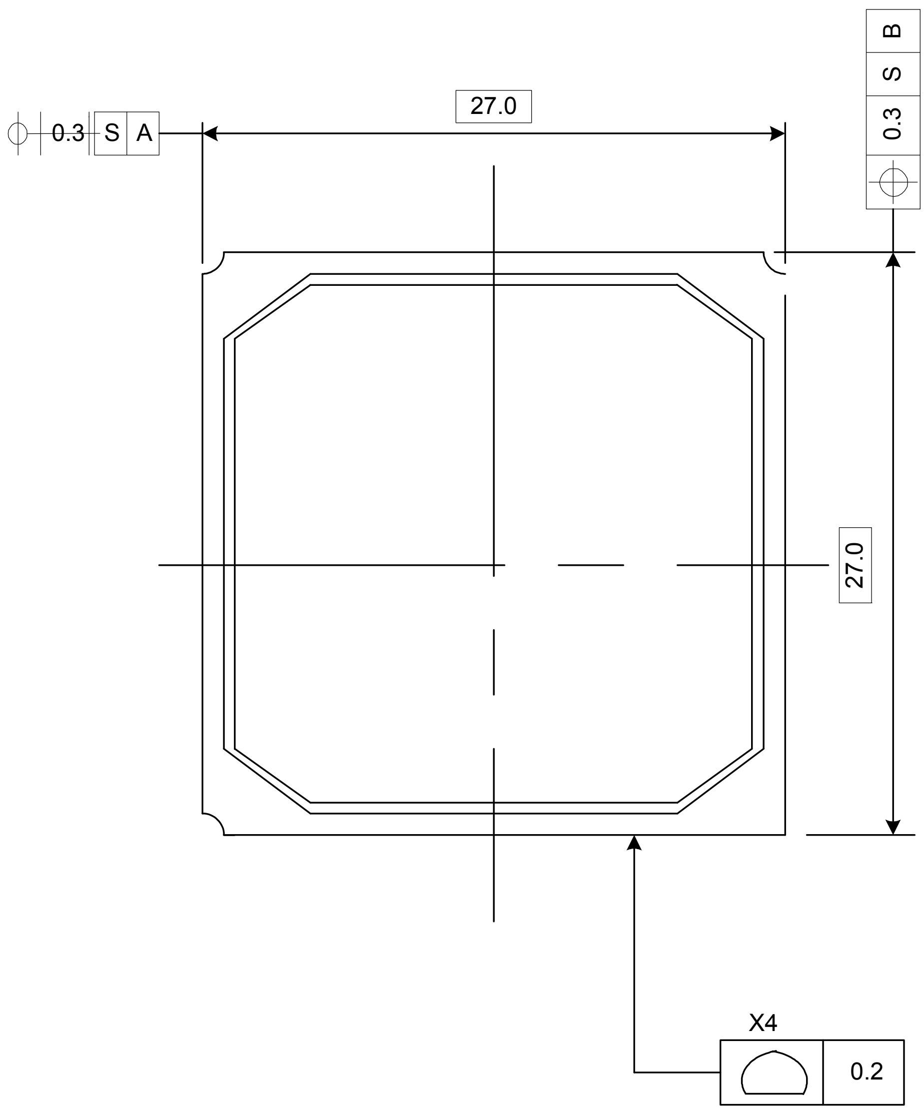
Figure 7: System PLL reference clock timing

Packaging

The next figures show the top view/dimensions and side and bottom view/dimensions of the NS9360.

The recommended pad size for this package configuration is 0.60 mm.

Top view



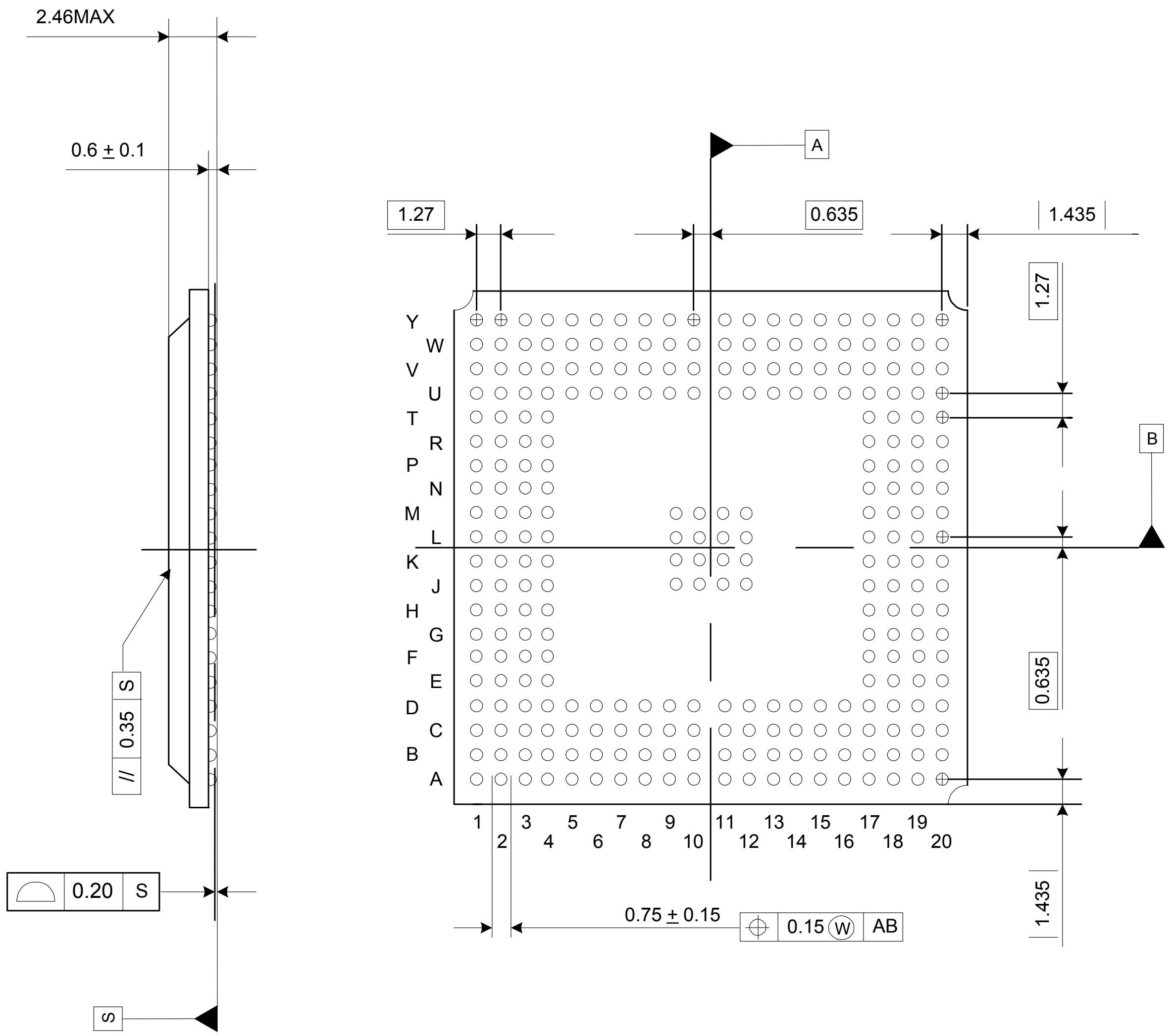

2.46MAX
0.6 ± 0.1
// 0.35 S
0.20 S
S
A
1.27
0.635
1.435
1.27
B
0.635
1.435
Y W V U T R P N M L K J H G F E D C B A
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
0.75 ± 0.15
0.15 W AB

Figure 8 shows the layout of theNS9360, for use in setting up the board.

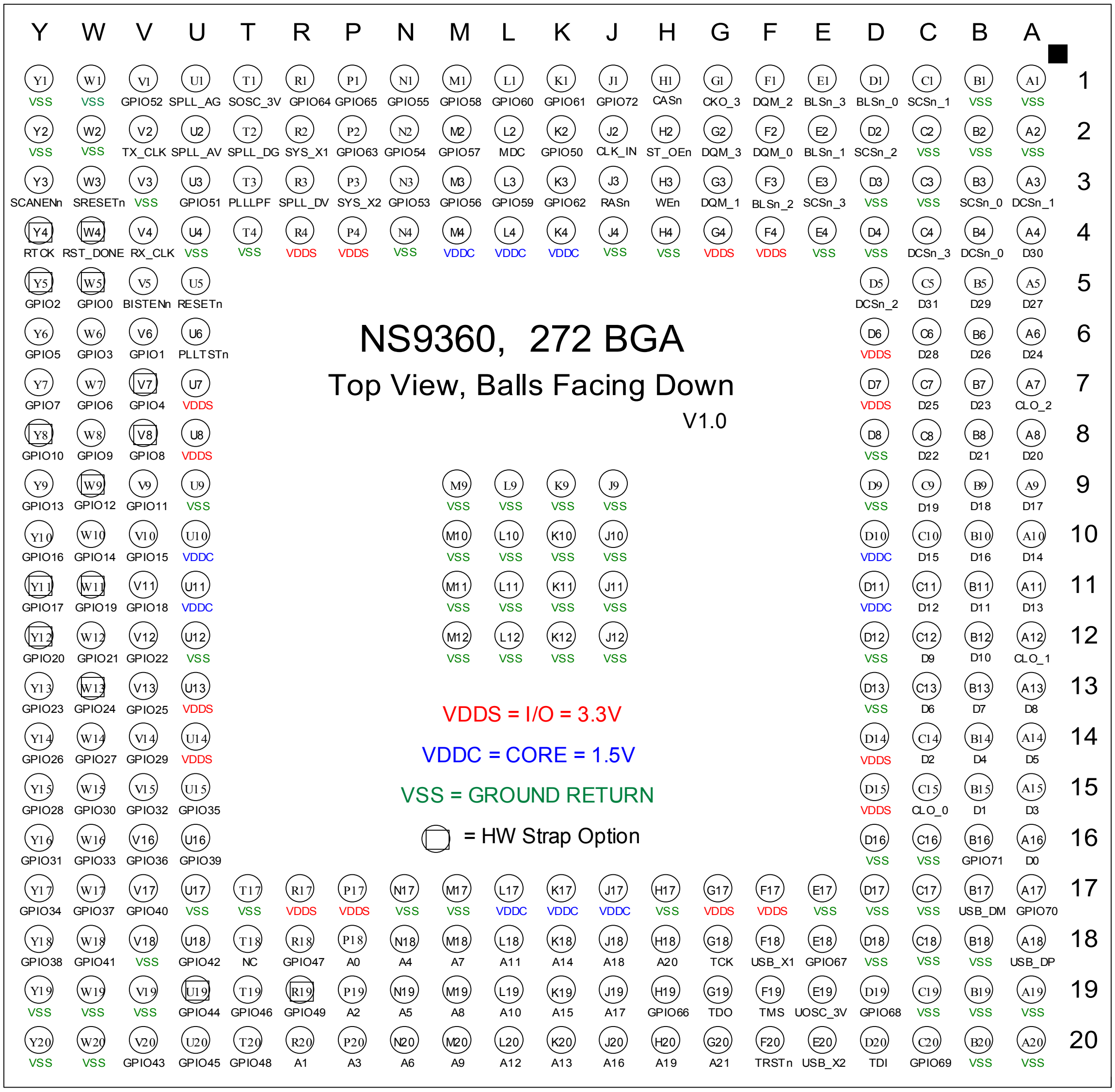


Figure 8: NS9360 BGA layout

For information about hardware strapping options, see Table 1, “Configuration pins— Bootstrap initialization,” on page 5.

Product specifications

These tables provide additional information about the NS9360.

ROHS substance	PPM level
Lead	0
Mercury	0
Cadmium	0
Hexavalent Chromium	0
Polybrominated biphenyls	0
Polybrominated diphenyl ethers	0

Table 40: NS9360 ROHS specifications

Component	Weight [mg]	Material		Weight [mg]	Content [%]
		CAS no.	Name		
Chip	15.22	7440-21-3	Silicon	14.90	0.57
		n/a	PI	0.32	0.01
Substrate	938.44	n/a	Resin	441.07	16.97
		7440-50-8	Copper	375.40	14.45
		7440-02-0	Nickel	4.70	0.18
		7440-57-5	Gold	0.90	0.04
		n/a	Brominated epoxy	93.80	3.61
		n/a	Other	22.57	0.87
Die attach	1.81	7440-22-4	Silver	1.39	0.05
		n/a	Epoxy resin	0.42	0.02
Wire bond	6.36	7440-57-5	Gold	6.36	0.25
Mold resin	1099.29	7440-21-3	Silica	1000.35	38.50
		n/a	Epoxy resin	49.47	1.90
		n/a	Phenol resin	49.47	1.90
Solder ball	537.49	7440-31-5	Tin	518.68	19.96
		7440-22-4	Silver	16.12	0.62
		7440-50-8	Copper	2.69	0.10
Total weight	2598.61			2598.61	100.000

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