THE DATASHEET OF

LTM4634EY#PBF

Triple Output 5A/5A/4A Step-Down DC/DC µModule® Regulator

FEATURES

- **Three Independent High Efficiency Regulator Channels**
- **$I_{OUT1,2}$ = 5A, I_{OUT3} = 4A**
- **Input Voltage Range: 4.75V to 28V**
- **Independent V_{IN} for Each Channel**
- **$V_{OUT1,2}$ Voltage Range: 0.8V to 5.5V**
- **V_{OUT3} Voltage Range: 0.8V to 13.5V**
- **±1.5% Maximum Total DC Output Error**
- **Current Mode Control/Fast Transient Response**
- **Frequency Synchronization**
- **Output Overvoltage and Overcurrent Protection**
- **PolyPhase® Operation with Current Sharing**
- **General Purpose Temperature Monitors**
- Soft-Start/Voltage Tracking
- Power Good Monitors
- SnPb or RoHS Compliant Finish
- 15mm × 15mm × 5.01mm BGA Package

APPLICATIONS

- Telecom, Networking and Industrial Equipment
- High Density Point of Load Voltage Regulation

DESCRIPTION

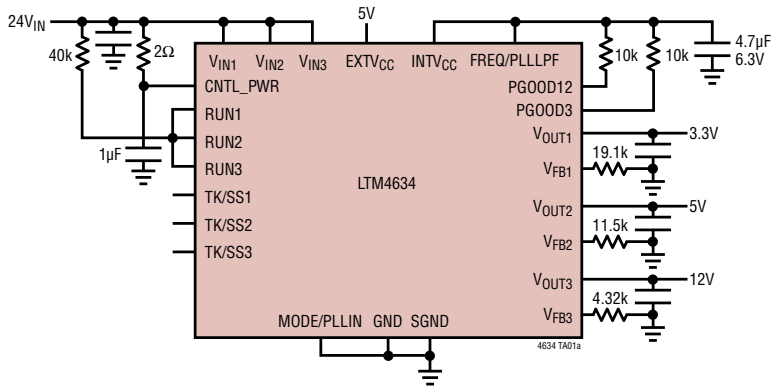
The LTM®4634 integrates three complete 5A/5A/4A high efficiency switching mode DC/DC converters into one small package. Switching controllers, power FETs, inductors, and most support components are included. Operating over an input voltage range of 4.75V to 28V, the LTM4634 provides three independent output voltages. V_{OUT1} and V_{OUT2} are adjustable from 0.8V to 5.5V, while V_{OUT3} is adjustable from 0.8V to 13.5V. Each output voltage is set by a single external resistor.

High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The device supports frequency synchronization, multiphase parallel operation, soft-start and output voltage tracking for supply rail sequencing.

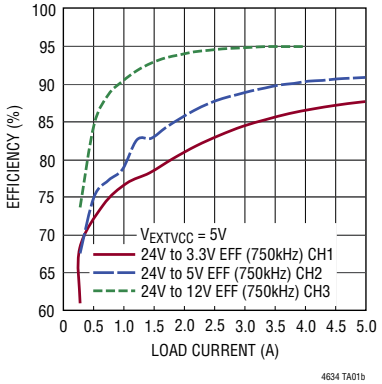
Fault protection features include overvoltage protection, overcurrent protection and temperature monitoring. The power module is offered in a space saving, thermally enhanced 15mm × 15mm × 5.01mm BGA package. The LTM4634 is available with SnPb (BGA) or RoHS compliant terminal finish.

TYPICAL APPLICATION

24V Input to 3.3V, 5V and 12V Output Regulator



24V Input Efficiency

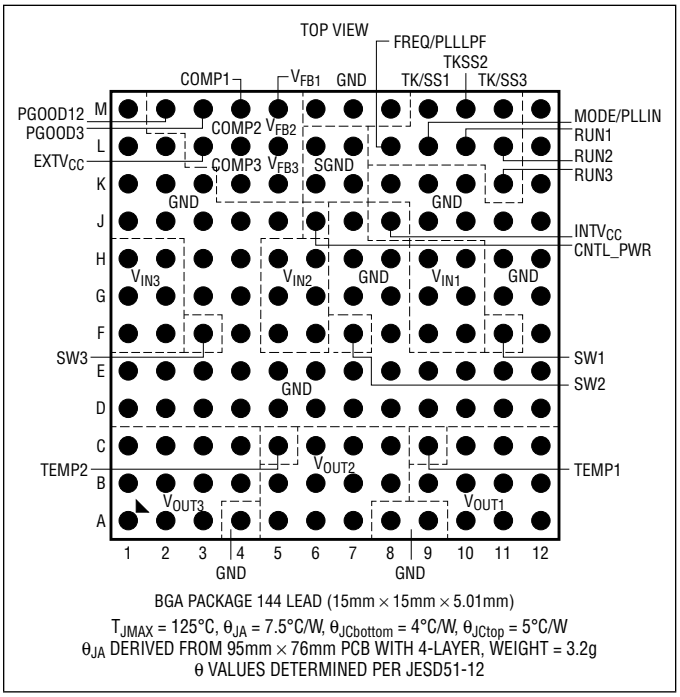


ABSOLUTE MAXIMUM RATINGS

(Note 1)

CNTL_PWR ..... –0.3V to 30V
V_{IN1}, V_{IN2}, V_{IN3} ..... –0.3V to 30V
V_{OUT1}, V_{OUT2} ..... –0.3V to 5.75V
V_{OUT3} ..... –0.3V to 14V
Switch Voltage (SW1, SW2 and SW3) ..... –1V to 30V
MODE/PLLIN, TK/SS1, TK/SS2, TK/SS3,
FREQ/PLLLPF ..... –0.3V to $INTV_{CC}$
COMP1, COMP2, COMP3, V_{FB1}, V_{FB2}, V_{FB3}
(Note 3) ..... –0.3V to $INTV_{CC}$
RUN1, RUN2, RUN3, $INTV_{CC}$, $EXTV_{CC}$,
PGOOD12, PGOOD3 ..... –0.3V to 6V
TEMP1, TEMP2 ..... –0.3V to 0.8V
$INTV_{CC}$ Peak Output Current 100mA
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 245°C

PIN CONFIGURATION



BGA PACKAGE 144 LEAD (15mm × 15mm × 5.01mm)
T_{JMAX} = 125°C, θ_{JA} = 7.5°C/W, $\theta_{JCbottom}$ = 4°C/W, θ_{JCtop} = 5°C/W
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4-LAYER, WEIGHT = 3.2g
θ VALUES DETERMINED PER JESD51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (See Note 2)
		DEVICE	FINISH CODE			
LTM4634EY#PBF	SAC305 (RoHS)	LTM4634Y	e1	BGA	4	–40°C to 125°C
LTM4634IY#PBF	SAC305 (RoHS)	LTM4634Y	e1	BGA	4	–40°C to 125°C
LTM4634IY	SnPb (63/37)	LTM4634Y	e0	BGA	4	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Markings:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 24V, per the typical application for each regulator channel.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage	CNTL_PWR Powered Tied to Input Supply		●	4.75		28	V
$V_{OUT(RANGE)}$	Output Voltage Range V_{OUT1}, V_{OUT2} Output Voltage Range V_{OUT3}			● ●	0.8 0.8		5.5 13.5	V V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load, V_{OUT1}, V_{OUT2}, V_{OUT3}	C_{IN} = 22µF × 3, C_{OUT} = 100µF Ceramic × 3, R_{FB} = 11.5k, MODE/PLLIN = 0V, V_{IN} = 5.5V to 28V, $I_{OUT1,2}$ = 0A to 5A, I_{OUT3} = 0A to 4A (Note 4)		●	4.925	5.0	5.075	V
Input Specifications								
V_{RUN}	RUN1, RUN2, RUN3 Pin ON Threshold	V_{RUN} Rising			1.15	1.3	1.4	V
$V_{RUN(HYS)}$	RUN Pin Hysteresis					175		mV
$I_{Q(VIN)}$	Input Supply Bias Current Each Channel	V_{OUT} = 5V, Burst Mode Operation, I_{OUT} = 0A V_{OUT} = 5V, Pulse-Skipping Mode, I_{OUT} = 0A V_{OUT} = 5V, Switching Continuous, I_{OUT} = 0A Shutdown, RUN = 0V, V_{IN} = 24V				0.5 1.6 45 10		mA mA mA µA
$I_{S(VIN)}$	Input Supply Current Each Channel	V_{IN} = 12V, $EXTV_{CC}$ = $5V_{OUT}$ $V_{OUT1,2}$ = 5V, V_{OUT3} = 5V	$I_{OUT1,2}$ = 5A			2.21		A
			I_{OUT3} = 4A			1.76		A
Output Specifications (Note 4)								
$I_{OUT(DC)}$	Output Continuous Current Range Each Channel	$V_{OUT1,2}$ = 5V V_{OUT3} = 5V			0 0		5 4	A A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy per Channel	V_{OUT1} = V_{IN} from 5.5V to 28V I_{OUT} = 0A, CNTL_PWR Tie to V_{IN}		●		0.015	0.02	%/V
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy per Channel	V_{OUT} = 5V, $I_{OUT1,2}$ = 0A to 5A Ch1, Ch2, I_{OUT3} = 0A to 4A		●		0.3	0.5	%
$V_{OUT(AC)}$	Output Ripple Voltage per Channel	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic × 3, V_{IN} = 24V, V_{OUT} = 5V				75		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot per Channel	C_{OUT} = 100µF Ceramic × 3, V_{OUT} = 5V, I_{OUT} = 0A, TK/SS = 0.01µF				50		mV
t_{START}	Turn-On Time per Channel	C_{OUT} = 100µF Ceramic × 3, V_{OUT} = 5V, I_{OUT} = 0A, TK/SS = 0.01µF				6		ms
V_{OUTLS}	Peak Deviation for Dynamic Load per Channel	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic × 3, V_{OUT} = 5V Typical Bench Data				200		mV
t_{SETTLE}	Settling Time for Dynamic Load Step per Channel	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic × 3, V_{OUT} = 5V Typical Bench Data				50		µs
$I_{OUT(PK)}$	Output Current Limit per Channel	V_{OUT} = 5V				8		A
Control Specifications								
V_{FB}	Voltage at V_{FB} Pin per Channel	I_{OUT} = 0A, V_{OUT} = 5V		 ●	0.794 0.792	0.80 0.80	0.806 0.808	V V
I_{FB}	Current at V_{FB} Pin per Channel	(Note 3)				–10	–50	nA
V_{OVL}	Feedback Overvoltage Lockout per Channel			●	0.84	0.86	0.88	V
$I_{TK/SS}$	Track Pin Soft-Start Pull-Up Current per Channel	TK/SS = 0V			1.1	1.5	1.9	µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 3)				90		ns
Max DC	Maximum Duty Cycle	5.5V to 5V at 5A (Note 5)				95		%
R_{FBHI}	Resistor Between V_{OUT} and V_{FB} Pins				60.0	60.4	60.8	kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 24V, per the typical application for each regulator channel.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{PGOOD}	PGOOD Trip Level PGOOD12 PGOOD3	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive				 –7.5 7.5		 % %
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA				0.1	0.3	V
$INTV_{CC}$ Linear Regulator								
V_{INTVCC}	Internal V_{CC} Voltage	Float MODE/PLLIN	6V < V_{IN} < 28V, I_{CC} = 0mA		4.8	5	5.2	V
V_{LDOINT}	$INTV_{CC}$ Load Regulation		I_{CC} = 0mA to 100mA			1		%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage		$EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
V_{LDOEXT}	$EXTV_{CC}$ Voltage Drop		I_{CC} = 20mA, V_{EXTVCC} = 5V			30	75	mV
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis					200		mV
Oscillator and Phase-Locked Loop								
f_{SYNC}	SYNC Capture Range	Clock Input Duty Cycle = 50%			250		750	kHz
f_S	Switching Frequency	$V_{FREQ/PLLLPF}$ = $INTV_{CC}$			700	750	825	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance					250		kΩ
$V_{IH(MODE/PLLIN)}$	Clock Input Level High				2.0			V
$V_{IL(MODE/PLLIN)}$	Clock Input Level Low						0.8	V
Clock Phase	V_{OUT2} to V_{OUT1} Phase V_{OUT3} to V_{OUT2} Phase V_{OUT1} to V_{OUT3} Phase	$V_{FREQ/PLLLPF}$ = 1.2V (Note 3)				120 120 120		Deg Deg Deg
$V_{TEMP1,2}$	Temperature Diode Forward Voltage	I_{TEMP} = 100µA				0.598		V
TC V_{TEMP}	Temperature Coefficient					–2.0		mV/°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4634 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4634E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4634I is guaranteed to meet specifications over the –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

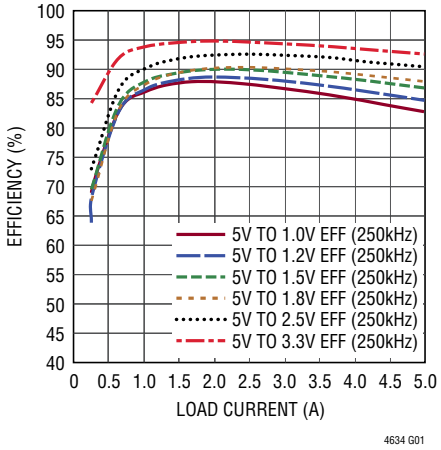
Note 3: 100% tested at wafer level.

Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

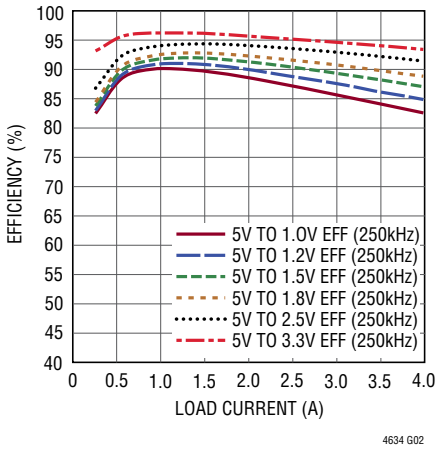
Note 5: High duty designs need to be validated based on maximum temperature rise and derating in ambient conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

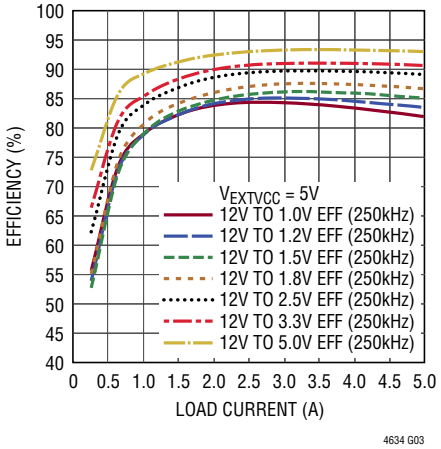
5V Input Efficiency (Ch1 and Ch2)



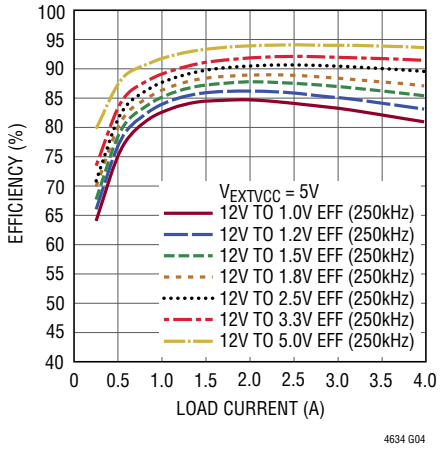
5V Input Efficiency (Ch3)



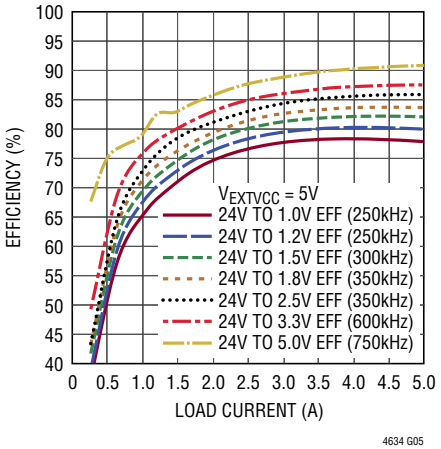
12V Input Efficiency (Ch1 and Ch2)



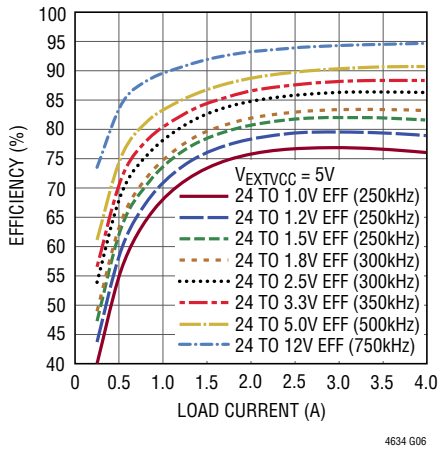
12V Input Efficiency (Ch3)



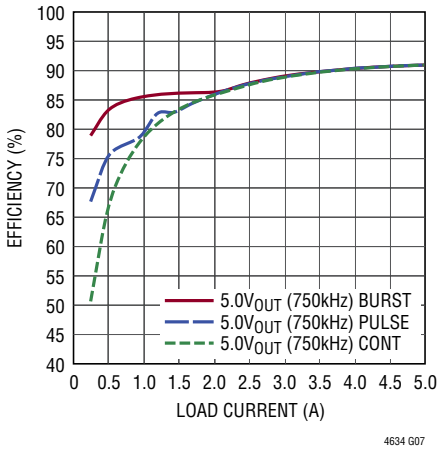
24V Input Efficiency (Ch1 and Ch2)



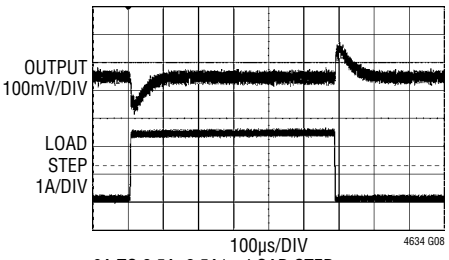
24V Input Efficiency (Ch3)



24V Input Continuous, Pulse-Skipping and Burst Mode Operation

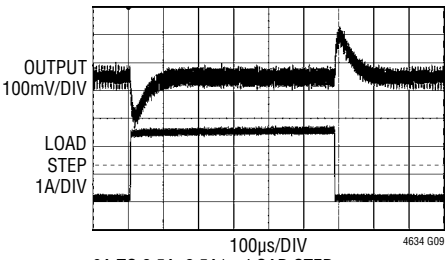


24V to 3.3V Load Step Response



0A TO 2.5A, 2.5A/µs LOAD STEP
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR

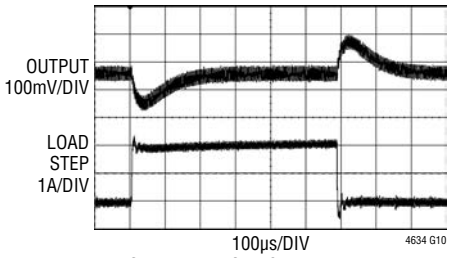
24V to 5V Load Step Response



0A TO 2.5A, 2.5A/µs LOAD STEP
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR

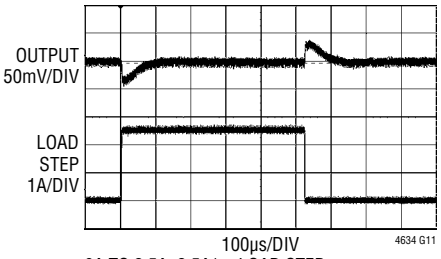
TYPICAL PERFORMANCE CHARACTERISTICS

24V to 12V Load Step Response



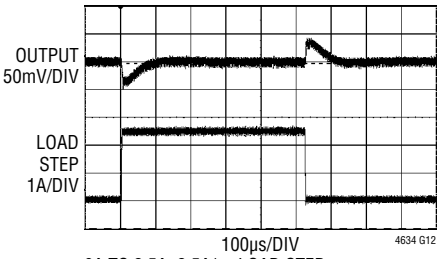
0A TO 2A, 2A/µs LOAD STEP
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR
AND 100µF 16V 16TQC100MYF POS CAPACITOR

12V to 1V Load Step Response



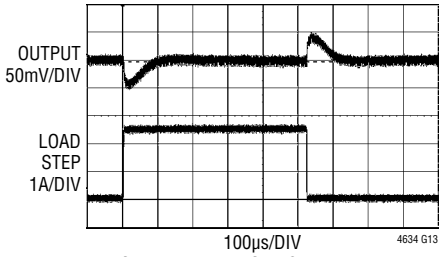
0A TO 2.5A, 2.5A/µs LOAD STEP
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR
AND 470µF 2V 2TPE470MAJB POS CAPACITOR

12V to 1.2V Load Step Response



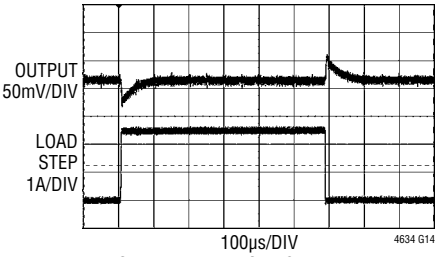
0A TO 2.5A, 2.5A/µs LOAD STEP
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR
AND 470µF 2V 2TPE470MAJB POS CAPACITOR

12V to 1.5V Load Step Response



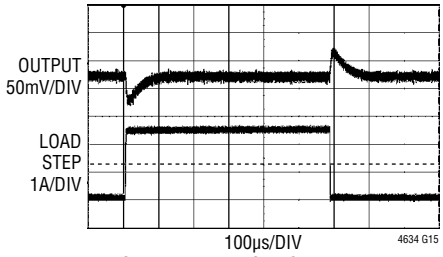
0A TO 2.5A, 2.5A/µs LOAD STEP
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR
AND 470µF 2V 2TPE470MAJB POS CAPACITOR

12V to 1.8V Load Step Response



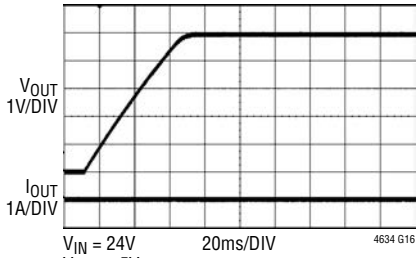
0A TO 2.5A, 2.5A/µs LOAD STEP
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR

12V to 2.5V Load Step Response



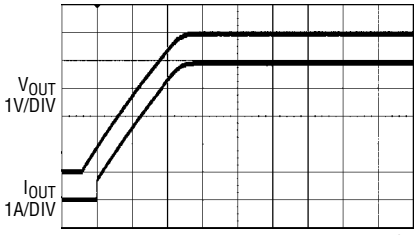
0A TO 2.5A, 2.5A/µs LOAD STEP
C_{OUT} = 2 × 100µF CERAMIC CAPACITOR

24V to 5V No Load Start-Up



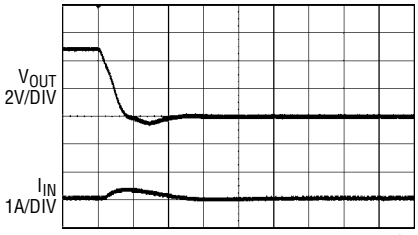
V_{IN} = 24V
V_{OUT} = 5V
I_{OUT} = 0A
C_{OUT} = 2 × 100µF X5R 1210

24V to 5V Full Load Start-Up



V_{IN} = 24V
V_{OUT} = 5V
I_{OUT} = 5A
C_{OUT} = 2 × 100µF X5R 1210

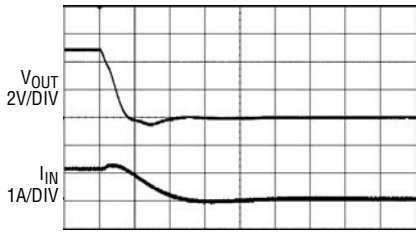
24V to 5V No Load Short



V_{IN} = 24V
V_{OUT} = 5V
I_{OUT} = 0A
C_{OUT} = 2 × 100µF X5R 1210

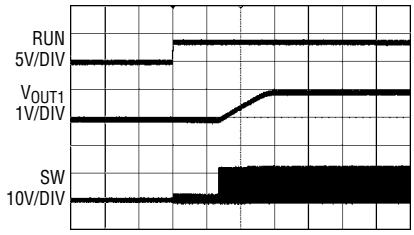
TYPICAL PERFORMANCE CHARACTERISTICS

24V to 5V Full Load Short



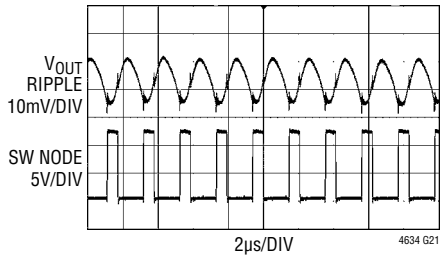
V_{IN} = 24V
V_{OUT} = 5V
I_{OUT} = 5A
C_{OUT} = 2 × 100µF X5R 1210

Start-Up into Pre-Bias



PREBIAS 1.5V OUTPUT STARTING AT 0.5V BIAS
12V INPUT

Steady-State Output Ripple



12V TO 3.3V AT 5A LOAD

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (A4, A8-A9, D1- D12, E1-E12, F4, F8, F12, G3-G4, G7-G8, G11-G12, H3-H4, H7-H8, H11-H12, J1-J5, J7, J9-J12, K1-K3, K8-K10, K12,L1-L2,L12, M1, M6-M8, M12): Ground Pins for Both Input and Output Returns. All ground pins need to connect with large copper areas underneath the unit.

V_{OUT1}, V_{OUT2}, V_{OUT3} (A10-A12, B9-B12, and C10-C12); (A5-A7, B5-B8, C6-C8); (A1-A3, B1-B4, C1-C4): Power Output Pins. Apply output load between these pins and the GND pins. Recommend placing output decoupling capacitance directly between these pins and the GND pins. See Table 4.

TEMP1 AND TEMP2 (C9, C5): Two Onboard Temperature Diodes for Monitoring the VBE Junction Voltage Change with Temperature. Each of these two temperature diode connected PNP transistors is placed in the middle of channel 1 and channel 2, and in the middle of channel 2 and channel 3. See the Applications Information section and an example in Figure 25. Leave floating if not used.

V_{IN1},V_{IN2},V_{IN3} (F9-F10,G9-G10,H9-H10);(F5-F6,G5-G6,H5-H6);(F1-F2,G1-G2,H1-H2): Power Input Pins. Apply input voltage between these pins and the GND pins. Recommend placing input decoupling capacitance directly between the V_{IN} pins and the GND pins. The V_{IN} paths can be all combined from one power source, or powered from independent power sources. See the Applications Information section.

SW1 (F11), SW2 (F7), SW3 (F3): The internal switch node for each of the regulator channels for monitoring the switching waveform. An R-C snubber circuit can be placed on these pins to ground to eliminate switch node ringing noise.

CNTL_PWR (J6): Input Supply to an Internal Bias LDO to Power the Internal Controller and MOSFET Drivers. The operating voltage range is 4.75V to 28V under all conditions. If the voltage at CNTL_PWR is ≤5.8V, the $INTV_{CC}$ pin should be tied to CNTL_PWR for optimum efficiency. If the voltage at CNTL_PWR is >5.8V, leave $INTV_{CC}$ floating with the recommended decoupling capacitor. To eliminate power loss in the onboard linear regulator and improve efficiency connect a 5V supply at $EXTV_{CC}$. Ensure CNTL_PWR > $EXTV_{CC}$ at all times to avoid reverse polarity on the internal bias LDO.

PIN FUNCTIONS

$INTV_{CC}$ (J8): Output of the Internal Bias LDO for Powering Internal Control Circuitry. Connect a 4.7µF ceramic capacitor to ground for decoupling. If the voltage at CNTL_PWR is ≤5.8V, tie the $INTV_{CC}$ pin to CNTL_PWR for optimum efficiency. If the voltage at CNTL_PWR is >5.8V, leave $INTV_{CC}$ floating. See the Applications Information section.

SGND (K6-K7, L6-L7): Signal Ground Connections. The signal ground connection in the module is separated from normal power ground (GND) by an internal 2.2Ω resistor. This allows the designer to connect the signal ground pin close to GND near the external output capacitors on the regulator channel's outputs. The entire internal small-signal feedback circuitry is referenced to SGND, thus allowing for better output regulation. See the recommended layout in the Applications Information section.

$EXTV_{CC}$ (L3): External Bias Power Input. The internal bias LDO is bypassed whenever the voltage at $EXTV_{CC}$ is above 4.7V. Never exceed 6V at this pin and ensure CNTL_PWR > $EXTV_{CC}$ at all times to avoid reverse polarity on the internal bias LDO. Connect a 1µF capacitor to ground when used otherwise leave floating. Use a 5V bias or 5V output to power this pin to improve efficiency.

FREQ/PLLLPF (L8): Frequency Set and PLL Lowpass Filter Pin. This pin is driven with a DC voltage to set the operating frequency. The recommended operating frequency will be supplied in the efficiency graphs for optimal performance. A specific frequency can be chosen as long as the minimum on-time is not violated, and inductor ripple current is optimized. When an external clock is used, then the FREQ/PLLLPF pin must not be connected to any DC voltage. The pin must be floating and will have the proper internal compensation for the internal loop filter. See the Applications Information section.

MODE/PLLIN (L9): Forced Continuous Mode, Burst Mode, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force all channels into the continuous mode of operation. Connect to $INTV_{CC}$ to enable pulse-skipping mode of operation. Leave floating to enable Burst Mode operation. A clock on the pin will force the controller into continuous mode of operation and synchronize the internal oscillator. See the Applications Information section.

RUN1, RUN2, RUN3 (L10, L11, K11): Run Control Inputs. A voltage above 1.3V on any RUN pin turns on that particular channel. However, forcing any of these RUN pins below 1.15V causes that channel to shut down. Each of the RUN pins has an internal 10k resistor to ground. This resistor can be used with an external pull-up resistor to the input voltage to set a UVLO for that channel, or simply to turn on the channel. The RUN pins have a maximum voltage of 6V. See the Applications Information section.

PGOOD12, PGOOD3 (M2, M3): Output Voltage Power Good Indicator for V_{OUT1} and V_{OUT2} Combined, and V_{OUT3} Separate. The open-drain logic output is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

COMP1, COMP2, COMP3 (M4, L4, K4): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The LTM4634 regulator channels are all internally compensated for proper stability. COMP1 and COMP2 can be tied together for PolyPhase 10A parallel operation. See the Applications Information section.

V_{FB1}, V_{FB2}, V_{FB3} (M5, L5, K5): The Negative Input of the Error Amplifier for Each of the Three Channels. Internally, each of these pins is connected to their respective output with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between each individual V_{FB} pin and ground. In PolyPhase operation, tying the V_{FB1} and V_{FB2} pins together allows for parallel operation up to 10A. See the Applications Information section for details.

TK/SS1, TK/SS2, TK/SS3 (M9, M10, M11): Output Voltage Tracking and Soft-Start Inputs. When one particular channel is configured to be the master, a capacitor to ground at this pin sets the ramp rate for the master channel's output voltage. When the channel is configured to be the slave, the V_{FB} voltage of the master channel is reproduced by a resistor divider and applied to this pin. Internal soft-start currents of 1.5µA are charging the soft-start capacitors. In dual output (2 + 1) mode, TK/SS1 and TK/SS2 need to be shorted externally.

BLOCK DIAGRAM

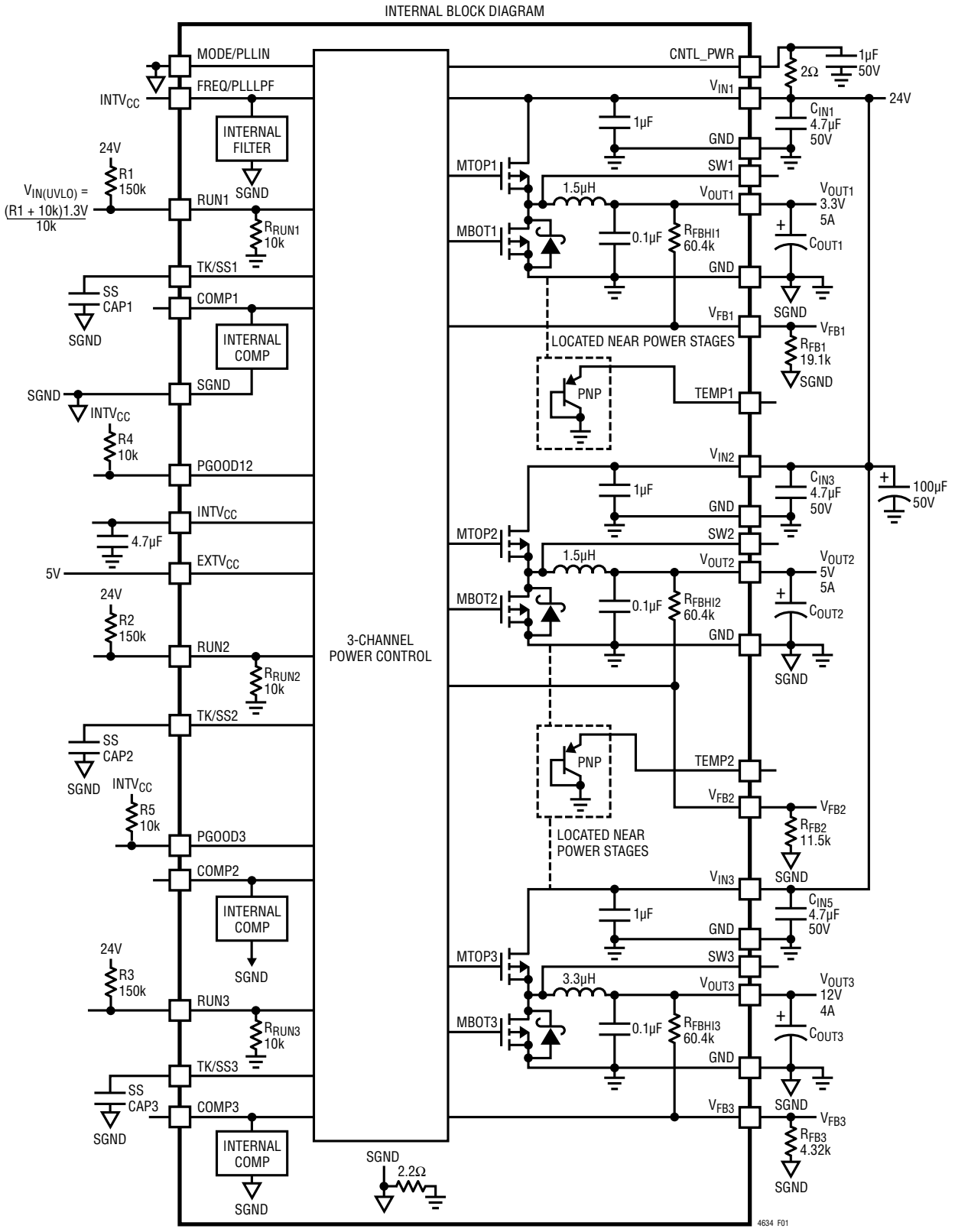


Figure 1. Simplified LTM4634 Block Diagram

OPERATION

Power Module Description

The LTM4634 µModule regulator is a high performance triple output nonisolated switching mode DC/DC power supply. It can provide 5A/5A/4A outputs with a few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from 0.8V DC to 5.5V DC (V_{OUT1} and V_{OUT2}), and 0.8V DC to 13.5V DC (V_{OUT3}). When applying control bias in the range from 4.75V to 5.8V, then connect the bias to CNTL_PWR and $INTV_{CC}$, otherwise if >5.8V only the CNTL_PWR pin needs to be biased. The typical application schematic is shown in Figure 22.

The LTM4634 has three integrated constant-frequency current mode regulators, power MOSFETs, power inductors, and other supporting discrete components. The typical switching frequency is 750kHz. For switching noise-sensitive applications, it can be externally synchronized from 250kHz to 750kHz. Operating frequency range will be dependent upon specific V_{IN} and V_{OUT} requirements as they pertain to minimum on-time and inductor ripple current of less than 60% of the load current. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4634 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit in an overcurrent condition. An internal overvoltage monitor protects the output voltages in the event of an overvoltage >10%. The top MOSFET is turned off and the bottom MOSFET is turned on until the output overvoltage is cleared. There are two temperatures monitors in the LTM4634. TEMP1 monitors the close relative temperature of channels 1 and 2, and TEMP2 monitors the close relative temperature of channels 2 and 3. The two diode connected PNP transistors are grounded in the module and can be used as general purpose temperature monitors using a device that is designed to monitor the single-ended connection.

Pulling any of the RUN pins below 1.15V forces that regulator channel into a shutdown state. The TK/SS pins are used for programming the output voltage ramp and voltage tracking during start-up for each of the channels. See the Applications Information section.

The LTM4634 is internally compensated to be stable over all operating conditions. Table 4 provides a guideline for input and output capacitances for several operating conditions. The LTpowerCAD™ software tool is provided for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground.

Each of the channels, operate 120° phase shift for multiphase operation. V_{OUT1} and V_{OUT2} can be combined to provide a single 10A output. The two channels will not be operating 180° phase shift, but 120° phase when combined for a 10A design. So the input RMS current may be higher than a 180° phase shifted design. See the Applications Information section for details.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE/PLLIN pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

The typical LTM4634 application circuit is shown in Figure 22. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 4 for specific external capacitor requirements for particular applications.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage. The V_{IN} to V_{OUT} minimum dropout is a function of load current and at very low input voltage and high duty cycle applications output power may be limited as the internal top power MOSFET is not rated for 5A operation at higher ambient temperatures. At very low duty cycles the minimum 100ns on-time must be maintained. See the Frequency Adjustment section and temperature derating curves.

Output Voltage Programming

The PWM controller has an internal 0.8V ±1% reference voltage. As shown in the Block Diagram, a 60.4k precision internal feedback resistor connects the V_{OUT} and V_{FB} pins together.

The output voltage will default to 0.8V with no feedback resistor. Adding a resistor R_{FB} from V_{FB} to ground programs the output voltage:

$$V_{OUT} = 0.8V \bullet \left(\frac{60.4k + R_{FB}}{R_{FB}} \right) \text{ or } R_{FB} = \frac{48.32k}{V_{OUT} - 0.8}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}(V)	0.8	1.0	1.2	1.5	1.8	2.5	3.3	5.0	12.0
R_{FB} (kΩ)	Open	243	121	69.8	48.7	28.7	19.1	11.5	4.32

In the parallel operation the following pins should be tied together, V_{FB1} and V_{FB2} pins, COMP1 and COMP2 pins, TK/SS1 and TK/SS2, and RUN1 and RUN2.

For parallel operation of V_{OUT1} and V_{OUT2}, connect V_{FB1} and V_{FB2} together with a single resistor to ground whose value is determined by:

$$R_{FB} = \frac{\frac{60.4k}{2}}{\frac{V_{OUT}}{0.8} - 1}$$

Input Capacitors

The LTM4634 module should be connected to a low AC impedance DC source. Additional input capacitors are needed for the RMS input ripple current rating. The $I_{CIN(RMS)}$ equation which follows can be used to calculate the input capacitor requirement for each channel. Typically 4.7µF to 10µF X7R ceramics are a good choice with RMS ripple current ratings of ~2A each. A 47µF to 100µF surface mount aluminum electrolytic capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)} \qquad (1)$$

In the previous equation, η% is the estimated efficiency of the power module in decimal form (0.nn) for a given V_{OUT}-to-V_{IN} ratio.

The selection of C_{IN} is simplified by the 3-phase architecture and its impact on the worst-case RMS current draw occurs when only one channel is operating. This is true when the three channels are powered from a common V_{IN}. The channel with the highest duty cycle D peaking at 0.5 and maximum load current needs to be used in the above formula. This will give the maximum RMS capacitor current requirement. Increasing the output current drawn from the other channels will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 50% when compared to a single phase power supply solution. If the three channels are powered from independent input sources, then each

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of the input RMS current ratings will need to be calculated specific to that channel.

Output Capacitors

The LTM4634 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, low ESR Polymer capacitor or ceramic capacitor. The typical output capacitance range is from 200µF to 470µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 4 matrix, and LTpowerCAD is available for stability analysis. LTpowerCAD can calculate the output ripple reduction as the number of implemented phases increases by N times.

Burst Mode Operation

The LTM4634 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply float the MODE/PLLIN pin. During Burst Mode operation, the peak current of the inductor is set to approximately 30% of the maximum peak current value in normal operation even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise, the internal sleep line goes low, and the LTM4634 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4634 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE/PLLINpin to $INTV_{CC}$ enables pulse-skipping operation. With pulse-skipping mode at light load, the internal current comparator may remain tripped for several cycles, thus skipping operation cycles. This mode has lower ripple than Burst Mode operation and maintains a higher frequency operation than Burst Mode operation.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE/PLLIN pin to ground. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4634 output voltage is in regulation.

Frequency Synchronization

The LTM4634 device operates up to 750kHz. It can also be synchronized with an input clock that has a high level above 2V and a low level below 0.8V at the MODE/PLLIN pin. The FREQ/PLLLPF pin must be floating when synchronized to an incoming clock. Once the LTM4634 is synchronized to an external clock frequency, it will always be running in forced continuous operation. The synchronizing range is from 250kHz to 750kHz. For $V_{OUT1,2,3} \leq 1.5V$ use 250kHz to 300kHz, $1.5V \leq V_{OUT1,2,3} \leq 2.5V$ use 400kHz, $2.5V \leq V_{OUT1,2,3} \leq 5V$ use 600kHz. If V_{OUT3} is greater than 5V up to 12V set the operating frequency to 750kHz. These

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frequencies optimize efficiency, eliminate minimum on-time issues for less than 1V output, and control the inductor ripple currents over the input and output voltage ranges.

24V input applications that convert to output voltages equal to 5V ($V_{OUT1,2}$) and up to 12V (V_{OUT3}) will be required to set the LTM4634 switching frequency to 750kHz. This is required to maintain less than 60% inductor ripple current at the higher output voltages. The 750kHz requirement for these higher output conversions from 24V will limit output voltages on other channels to be no lower than 1.5V due to minimum on-time considerations. There is a way around this issue by taking one of these outputs, either 5V or 12V, and using it as the source for the 0.8V to 1.5V output. An example circuit is shown in Figure 26. 5V and 12V input conversions on all three channels can be operated at lower frequencies across the output ranges so that minimum on-time is not an issue at low output voltages. The minimum on-time equation on the next page can be used to verify that no switching frequency is violating this parameter. The equations for checking I_{RIPPLE} %:

$$\frac{(V_{IN}-V_{OUT})V_{OUT}}{L \bullet I_{RIPPLE} \bullet V_{IN}} = FREQ, \frac{I_{RIPPLE}}{CH\#MaxLoad} = I_{RIPPLE}\%$$

This verifies that the operating frequencies are selected to limit inductor ripple currents to be below 60% of maximum load, where FREQ is selected frequency in Hertz, I_{RIPPLE} and maximum load current in amps, and L is inductance in Henrys. Ch1, Ch2 L = 1.5µH, and Ch3 L = 3.3µH. Maximum load current $I_{OUT1,2}$ = 5A, and I_{OUT3} = 4A, therefore I_{RIPPLE} should try to stay below 2.5A for Ch1, Ch2, and 2A for Ch3, except for 12V output. The efficiency curves will show the recommended optimal operating frequency for the different conversions

A DC voltage should be applied to the FREQ/PLLLPF pin to set the operating frequency when clock synchronization is not used. Figure 2 shows the frequency selection as a function of the applied DC voltage. This can be done with a voltage divider from the $INTV_{CC}$ (5V) pin to SGND. A 10k resistor can be selected as the bottom resistor. The top resistor, R_{FREQ}, can be determined by using equation:

$$R_{FREQ} = \frac{5V \bullet 10k}{FREQV} - 10k$$

where FREQV is the voltage at the FREQ/PLLLPF pin in Figure 2 that corresponds to a particular frequency. See Figure 25 for an example.

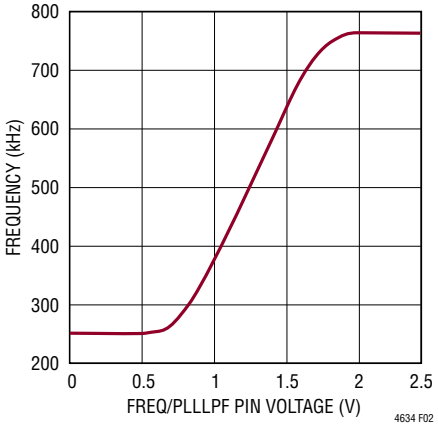

Figure 2. Relationship Between Oscillator Frequency and Voltage at the FREQ/PLLLPF Pin

Parallel Channel Operation

For outputs that demand more than 5A of load current, the LTM4634 device can parallel V_{OUT1} and V_{OUT2} to supply 10A of load current. The two channels will operate at 120° of phase shift. The input RMS ripple current can be calculated using Equation 1. For example, 12V to 1.2V at 10A equates to duty cycle D = 0.1.

$$I_{CIN(RMS)} = \frac{10A}{0.85} \bullet \sqrt{0.1 \bullet (1-0.1)}$$

$I_{CIN(RMS)} = 3.5A_{RMS}$, use $2 \times 22\mu F$ 16V X5R or X7R ceramic capacitors rated at $2A_{RMS}$ each.

The LTM4634 regulators are inherently current mode controlled devices, so the paralleling of V_{OUT1} and V_{OUT2} channels will have good current sharing. This will balance the thermals in the design. Tie the COMP, V_{FB}, TK/SS and RUN pins together for these two channels to share the current evenly. Figure 24 shows a schematic of the parallel design.

Minimum On-Time

Minimum on-time, t_{ON}, is the smallest time duration that any of the three regulator channels is capable of turning on the top MOSFET. It is determined by internal timing delays, and the gate charge required to turn on the top MOSFET.

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Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \bullet FREQ} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple and inductor ripple current will increase. The minimum on-time can be increased by lowering the switching frequency. A good rule of thumb is to use a 100ns on-time.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TK/SS pins. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4634 uses an accurate 60.4k resistor internally for the top feedback resistor for each channel. Figure 3 shows an example of coincident tracking for V_{OUT1} and V_{OUT2}. V_{OUT1} is the master and V_{OUT2} is the slave:

$$V_{SLAVE} = \left(1 + \frac{60.4k}{R_{TA}}\right) V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.8V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when V_{TRACK} is more than 0.8V. R_{TA} in Figure 3 will be equal to the R_{FB2} for coincident tracking.

The TK/SS pin of the master can be controlled by a capacitor placed on the master regulator TK/SS pin to ground. A 1.5µA current source will charge the TK/SS pin up to the

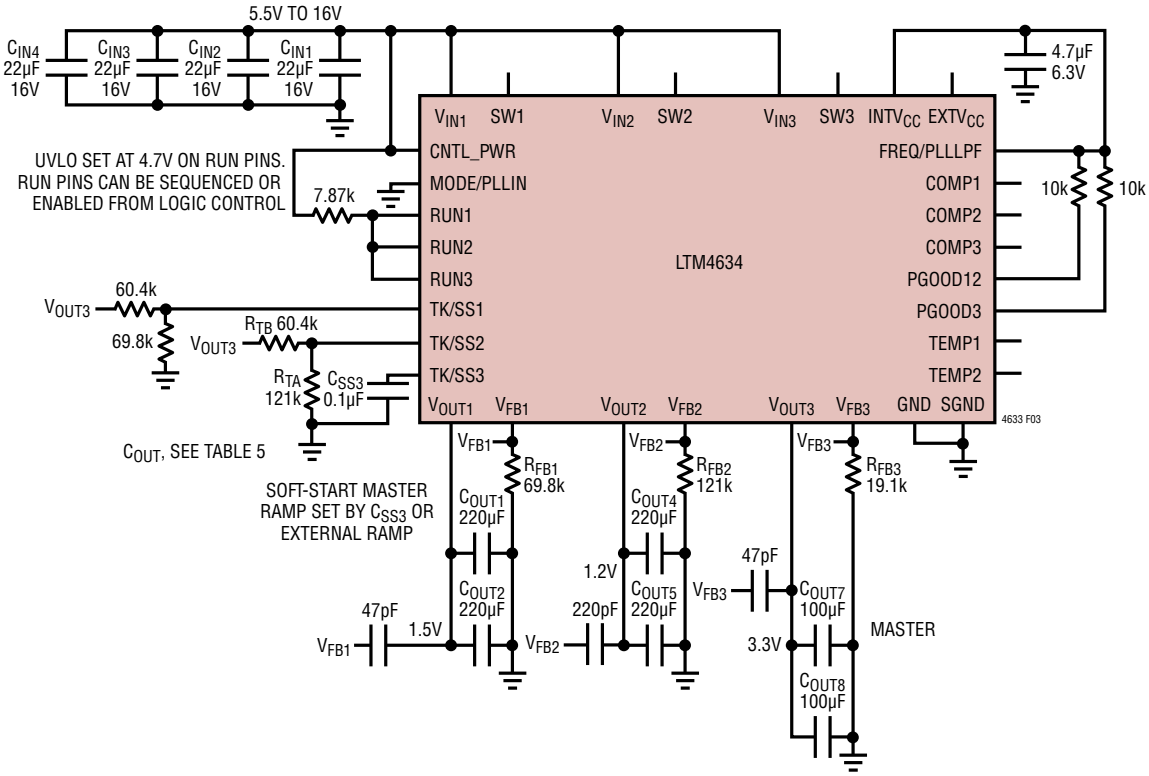

Figure 3. Triple Outputs (1.5V and 1.2V) with Tracking and 3.3V

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reference voltage and then proceed up to $INTV_{CC}$. After the 0.8V ramp, the TK/SS pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. Foldback current limit is disabled during this sequence of turn-on during tracking or soft-starting. The TK/SS pins are pulled low when the RUN pin is below 1.15V or $INTV_{CC}$ drops below 3.5V. The total soft-start time can be calculated as:

$$t_{SS} = \left(\frac{0.8V \bullet C_{SS}}{1.5\mu A} \right)$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator channels will always start in pulse-skipping mode up to TK/SS = 0.64V. Between TK/SS = 0.64V and 0.74V, it will operate in forced continuous mode and revert to the selected mode once TK/SS > 0.74V. The output ripple is minimized during the 100mV forced continuous mode window ensuring a clean PGOOD signal.

When the channel is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider value to be small enough to make this error negligible. In order to track down another channel or supply after the soft-start phase expires, the LTM4634 is forced into continuous mode of operation as soon as V_{FB} is below the undervoltage threshold of 0.74V regardless of the setting of the MODE/PLLIN pin. However, the LTM4634 should always be set in forced continuous mode tracking down when there is no load. After TK/SS drops below 0.1V, its channel will operate in discontinuous mode.

The master's TK/SS pin slew rate is directly equal to the master's output slew rate in Volts/Time. The equation:

$$R_{TB} = \left(\frac{MR}{SR} \right) \bullet 60.4k$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal the 60.4k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.8V}{\frac{V_{FB}}{60.4k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.8V. Since R_{TB} is equal to the 60.4k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB} with $V_{FB} = V_{TRACK}$. Therefore R_{TB} = 60.4k, and R_{TA} = 60.4k in Figure 3.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

Power Good

The PGOOD12 pin is an open-drain pin that can be used to monitor valid output voltage regulation for V_{OUT1} and V_{OUT2}, and PGOOD3 for monitoring V_{OUT3}. These pins monitor a ±7.5% window around the 0.8V feedback voltage on either $V_{FB1,2,3}$ from the output regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring. Any of the PGOOD pins are pulled low when the RUN pin of the corresponding channel is pulled low.

Overcurrent and Overvoltage Protection

Each of the regulator channels senses the peak inductor current on a cycle-by-cycle basis in current mode operation. When current limit is reached the output voltage will begin to fall and the internal current limit threshold will begin fold back as the output voltage falls below 50% of its value. Foldback current limit is disabled during start-up or track-up. Under short-circuit condition at low duty cycle operation, each of the regulator channels will begin to skip cycles to limit the short-circuit current.

Overvoltage protection is implemented by monitoring each one of the regulator's V_{FB} pins. When the V_{FB} voltage exceeds ~7.5% of the 0.8V reference value, then an

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internal comparator monitor will turn off the top power switch, and turn on the bottom power switch to protect the load. If the top power switch faults as a short, then a fuse or circuit breaker would be recommended to protect the system. This is due to the top switch being shorted while the bottom switch is turning on to protect the output from over voltage. High currents will flow and could damage the bottom switch.

Stability Compensation

The module has already been internally compensated for all output voltages. Table 4 is provided for most application requirements with verified stability. LTpowerCAD is available for other control loop optimization.

Run Enable

The RUN 1, 2, 3 pins have an enable threshold of 1.4V maximum, typically 1.3V with 175mV of hysteresis. They control the turn-on of their respective channel. There is a 10k resistor on each pin to ground. The RUN pins can be pulled up to V_{IN} for 5V operation, or a resistor can be placed on the pins and connected to V_{IN} for higher than 5V input. This resistor can be set along with the onboard 10k resistor such that an undervoltage lockout (UVLO) level can be programmed to shut down a particular regulator channel if V_{IN} falls below a set value. Use the equation:

$$R = \frac{10k(UVLO - 1.3V)}{1.3V}$$

where R is the resistor from the RUN pin to V_{IN} to set the UVLO trip point. For example, if the UVLO point is to be 6.25V while operating at 12V input:

$$R = \frac{10k(6.25V - 1.3V)}{1.3V} \approx 38k$$

See the Block Diagram in Figure 1. The RUN pins must never exceed 6V maximum voltage. The RUN pins have to be pulled up to enable the regulators.

SW Pins

The SW pins are generally for testing purposes by monitoring the pin. The SW pin can also be used to dampen out switch node ringing caused by LC parasitics in the switched current path. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor.

If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the PowerPath™ board inductance in combination with the MOSFET interconnect inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance, Z, can be calculated:

$$Z_{(L)} = 2\pi \bullet f \bullet L$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by:

$$Z_{(C)} = \frac{1}{2\pi \bullet f \bullet C}$$

these values are a good place to start with. Modification to these components should be made to attenuate the ringing without lowering the regulator's conversion efficiency.

$INTV_{CC}$ and $EXTV_{CC}$

The LTM4634 has an onboard linear regulator fed by CNTL_PWR which delivers a roughly 5V output at $INTV_{CC}$ to power the internal controller and MOSFET drivers for all three regulator channels. Apply a 4.7µF ceramic capacitor between $INTV_{CC}$ and ground for decoupling. CNTL_PWR requires a voltage between 4.75V to 28V. If the voltage supplied to CNTL_PWR is ≤ 5.8V, connect $INTV_{CC}$ to CNTL_PWR. Otherwise, $INTV_{CC}$ should be left floating. To eliminate power loss in the onboard linear regulator and improve efficiency connect a supply from 4.7V to 6V at $EXTV_{CC}$. Biasing $EXTV_{CC}$ at 5V will reduce the power loss in the internal LDO by (V_{CNTL_PWR} – 5V) • 90mA and is recommended for V_{CNTRL_POWER} ≥ 12V when all three channels are operating. If $EXTV_{CC}$ is used add a 1µF

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ceramic capacitor to ground at $EXTV_{CC}$ and ensure the voltage at CNTL_PWR is always greater than the voltage at $EXTV_{CC}$ at all times during start-up and shutdown. Connecting V_{OUT3} to $EXTV_{CC}$ may present a convenient way to meet the sequencing requirement. Otherwise float $EXTV_{CC}$ if not used.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12. These coefficients are quoted or paraphrased as follows:

1. θ_{JA}: The thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.
2. $\theta_{JCbottom}$: The thermal resistance from the junction to the bottom of the product case, is determined with all of the internal power dissipation flowing through the bottom of the package. In a typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}: The thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4. θ_{JB}: The thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule package and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured at a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 4; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through

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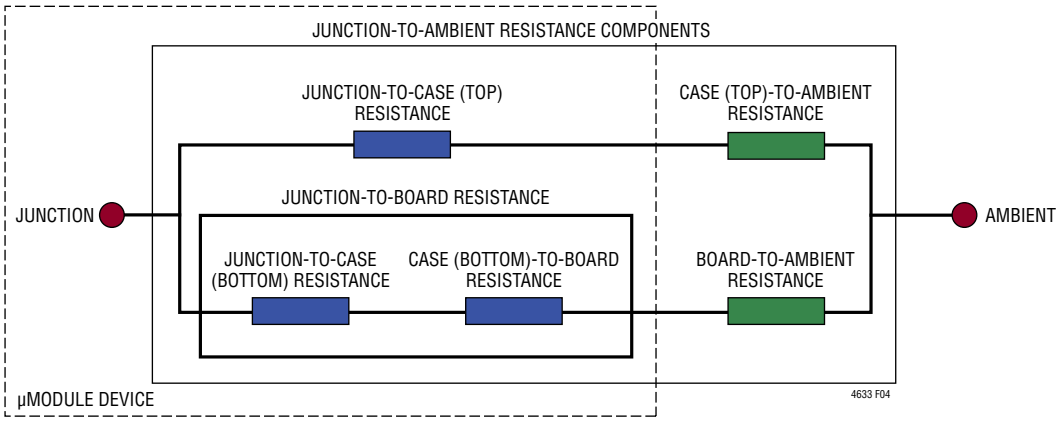

Figure 4. Graphical Representations of JESD51-12 Thermal Coefficients

bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow; a majority of the heat flow is into the board.

Within the LTM4634, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4634 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4634 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves shown in this data sheet.

After these laboratory tests have been performed and correlated to the LTM4634 model, then the θ_{JB} and θ_{BA} are summed together to correlate quite well with the device model conditions of no airflow or heat sinking in a properly define chamber. This θ_{JB} + θ_{BA} value should accurately equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no air-flow or top mounted heat sink.

LTM4634 Thermal Considerations and Output Current Derating

The power loss curves at 5V input, 12V input, and 24V input are shown in Figures 8 to 13. These power loss curves can be used in coordination with the load current derating curves in Figures 14 to 21 for calculating an approximate θ_{JA} thermal resistance for the LTM4634 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a multiplicative factor of 1.4 at 120°C junction.

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The derating curves are plotted with the output current starting at 15A (5A/CH) and the ambient temperature at ~40°C. The 15A comes from each of the three channels operating at 5A each. This simplifies the loading for this thermal testing. The output voltages are 3.3V, and 5V when all three channels are loaded together in parallel. Channel 1 and Channel 2 are designed to operate with outputs up to 5V, and Channel 3 is designed for 12V. The power loss curve values at a particular output voltage and output current for each output are taken and multiplied by 1.4 for increased power loss at 120°C junction. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 17 the 5.0V load current is derated to ~12.6A at ~71°C with no air and with no heat sink. In Figure 10, the 12V to 5.0V power loss at 4.2A per channel is 1.25W. The total loss would be 3 times 1.25W for 3.75W total power loss. The 3.75W is then multiplied by the 1.4 multiplier for 120°C junction. This 5.25W value is used with the total temperature rise of 120°C minus the 71°C ambient to calculate θ_{JA} thermal resistance. If the 71°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 49°C divided 5.25W equals a 9.3°C/W θ_{JA} thermal resistance. Table 2 specifies a 9.0°C/W value which is very close. Tables 2 and 3 provide equivalent thermal resistances for 3.3V and 5V outputs with and without air flow and heat sinking. The derived thermal resistances in Tables 2 and 3 for the various conditions can be multiplied by the calculated power loss as a function of the 120°C maximum junction temperature to determine if the temperature rise plus ambient is below the 120°C maximum junction temperature. Thermal measurements or infrared analysis should be performed to validate the values. Ambient temperature power loss can be derived from the power loss curves in Figures 8 to 13 and adjusted with the 1.4 multiplier. The printed circuit board is a 1.6mm thick four-layer board with two ounce copper for the two outer layers and 1 ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The BGA heat sinks are listed in Table 3.

Temperature Monitoring (TEMP1 and TEMP2)

Diode connected PNP transistors are used for the TEMP1, TEMP2 monitoring function since the diode forward voltage varies with temperature. The temperature dependence of the diodes can be understood in the equation:

$$V_D = nV_T \ln\left(\frac{I_D}{I_S}\right)$$

where V_T is the thermal voltage (kT/q), and n, the ideality factor, is 1 for the two diode connected PNPs being used in the LTM4634. I_S is expressed by the typical empirical equation:

$$I_S = I_0 \exp\left(\frac{-V_{G0}}{V_T}\right)$$

where I_0 is a process and geometry-dependent current (I_0 is typically around 20 orders of magnitude larger than I_S at room temperature), and V_{G0} is the band gap voltage of 1.2V extrapolated to absolute zero or –273°C.

If we take the I_S equation and substitute into the V_D equation, then we get:

$$V_D = V_{G0} - \left(\frac{kT}{q}\right)\ln\left(\frac{I_0}{I_D}\right),\ V_T = \frac{kT}{q}$$

The expression shows that the diode voltage decreases (linearly if I_0 were constant) with increasing temperature and constant diode current. Figure 5 shows a plot of V_D vs Temperature over the operating temperature range of the LTM4634.

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If we take this equation and differentiate it with respect to temperature T, then:

$$\frac{dV_D}{dT} = -\frac{V_{G0} - V_D}{T}$$

This dV_D/dT term is the temperature coefficient equal to about –2mV/K or –2mV/°C. The equation is simplified for the first order derivation.

Solving for T, $T = -(V_{G0} - V_D)/(dV_D/dT)$ provides the temperature.

1st Example: Figure 5 for 27°C, or 300K the diode voltage is 0.598V, thus, 300K = –(1200mV – 598mV)/–2.0 mV/K)

2nd Example: Figure 5 for 75°C, or 350K the diode voltage is 0.50V, thus, 350K = –(1200mV – 500mV)/–2.0mV/K)

Converting the Kelvin scale to Celsius is simply taking the Kelvin temp and subtracting 273 from it.

A typical forward voltage is given in the electrical characteristics section of the data sheet, and Figure 5 is the plot of this forward voltage. Measure this forward voltage at 27°C to establish a reference point. Then using the above expression while measuring the forward voltage over temperature will provide a general temperature monitor. Connect resistors between TEMP1, TEMP2 and V_{IN} to set the currents to 100µA each. See Figure 25 for an example.

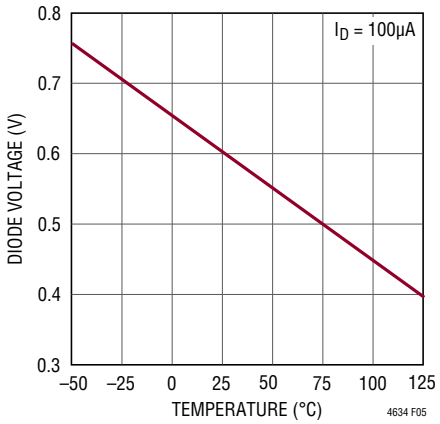

Figure 5. Diode Voltage V_D vs Temperature T(°C)

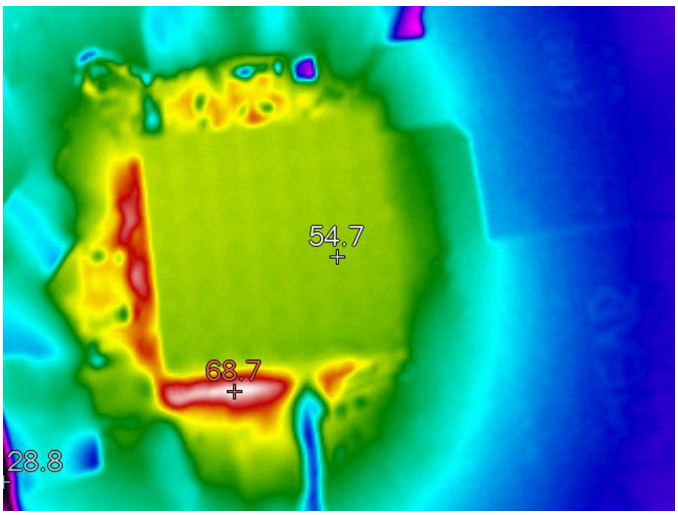

Figure 6. Thermal Plot 24V to 3.3V at 5A, 5V at 5A, and 12V at 4A, Airflow = 200LFM, Ambient = 25°C

Safety Considerations

The LTM4634 module does not provide galvanic isolation from V_{IN} to any of the three V_{OUT}s. There is no internal fuse. If required, a slow blow fuse with a rating higher than the maximum input current can be used to protect the unit in case of a catastrophic failure. An inline circuit breaker function can also be used instead of a fuse.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation.

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Layout Checklist/Example

The high integration of LTM4634 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1}, V_{OUT2}, and V_{OUT3}. It helps to minimize the PCB conduction loss and thermal stress. Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and the V_{OUT} pins to minimize high frequency noise.

Place a dedicated power ground layer underneath the unit. To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

Do not put vias directly on the pads, unless they are capped or plated over. Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit. Bring out test points on the signal pins for monitoring. Figure 7 gives a good example of the recommended layout.

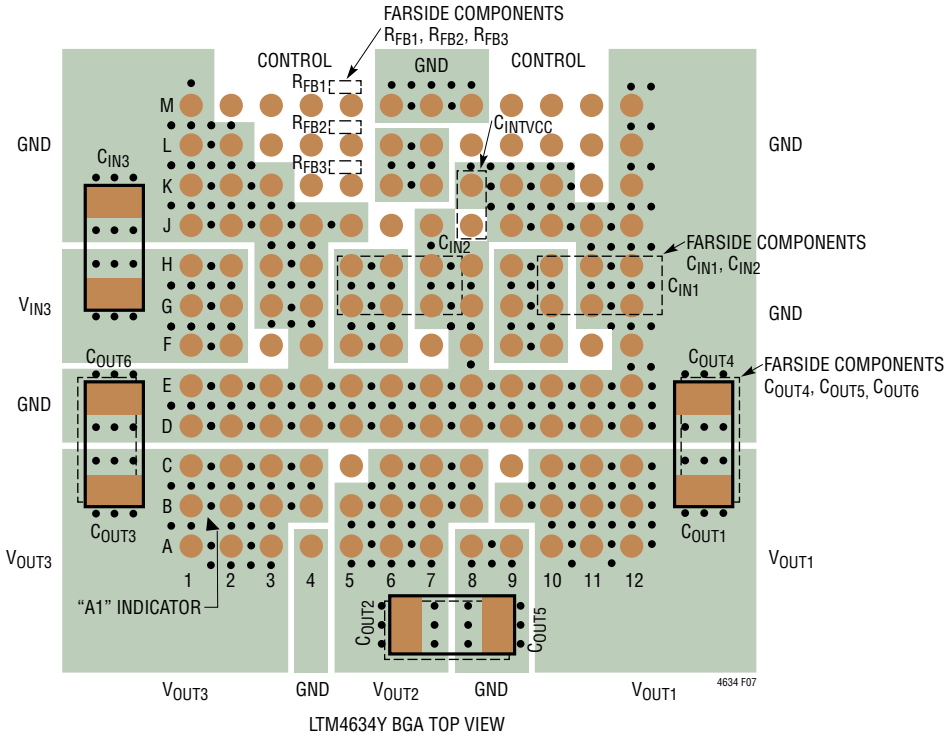

Figure 7. Recommended PCB Layout

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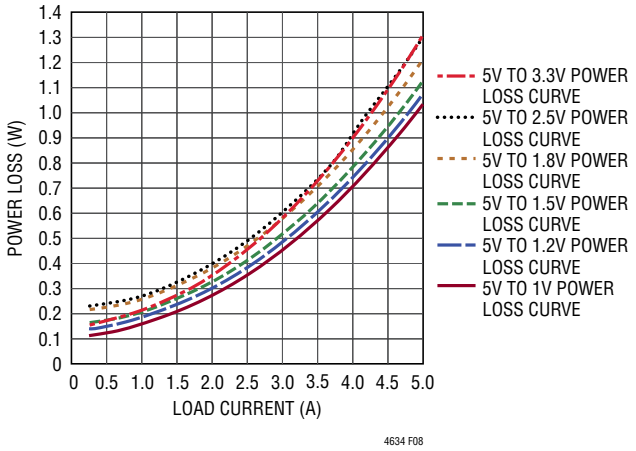

Figure 8. 5V Input Power Loss (Ch1 and Ch2)

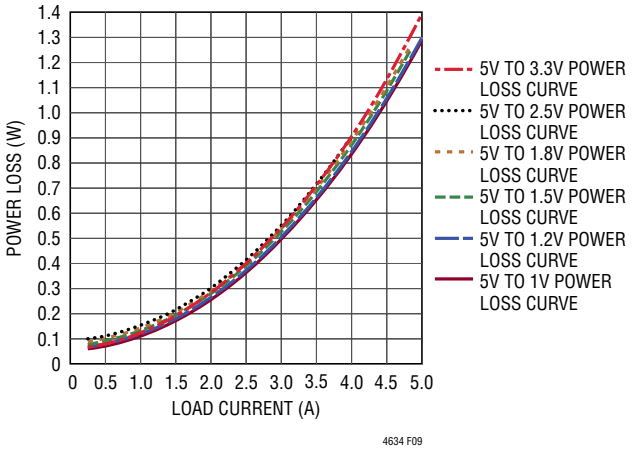

Figure 9. 5V Input Power Loss (Ch3)

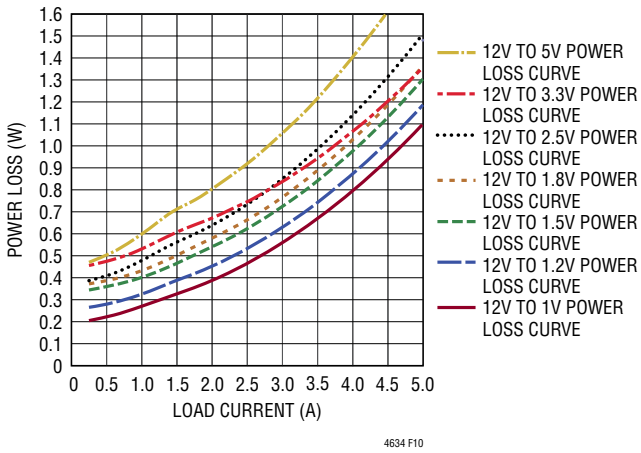

Figure 10. 12V Input Power Loss (Ch1 and Ch2)

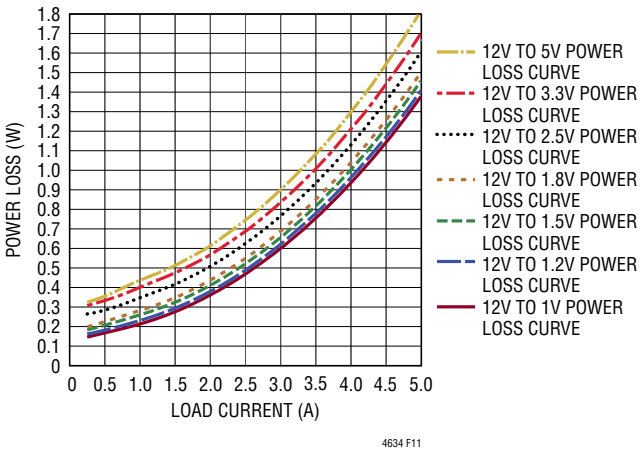

Figure 11. 12V Power Loss (Ch3)

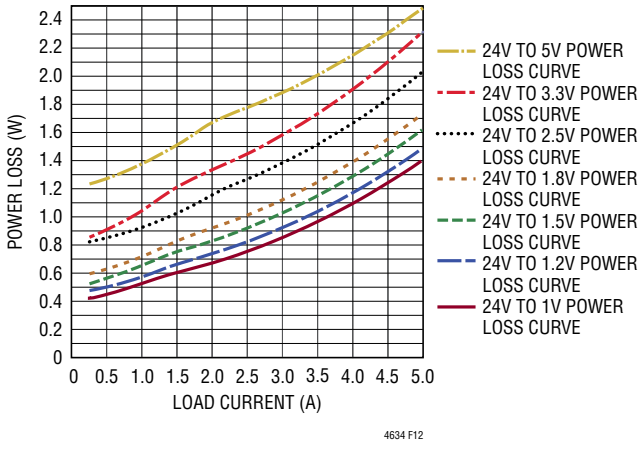

Figure 12. 24V Power Loss (Ch1 and Ch2)

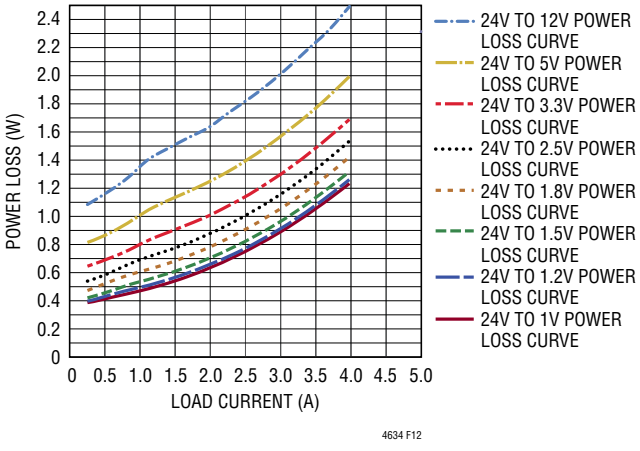

Figure 13. 24V Power Loss (Ch3)

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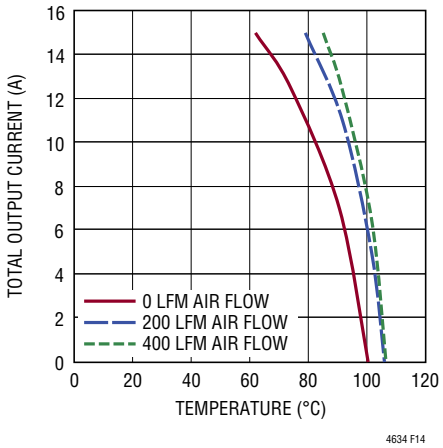

Figure 14. $12V_{IN}$, $3.3V_{OUT}$, with Heat Sink, All Channels at 5A Each

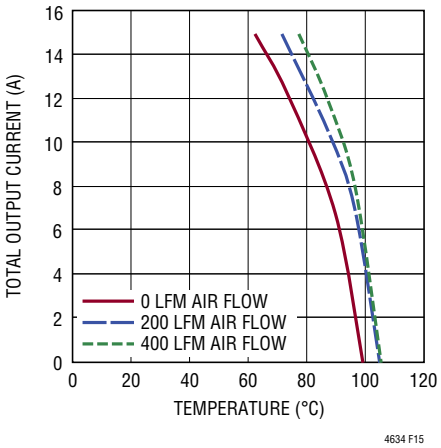

Figure 15. $12V_{IN}$, $3.3V_{OUT}$, without Heat Sink, All Channels at 5A Each

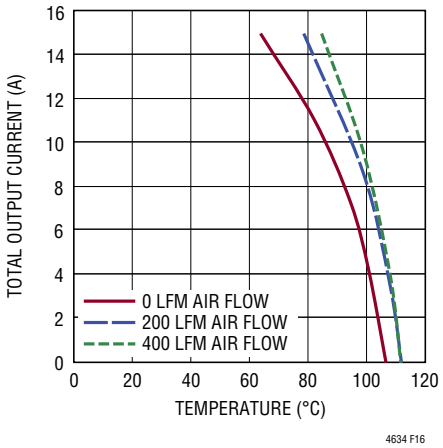

Figure 16. $12V_{IN}$, 5V, with Heat Sink, All Channels at 5A Each

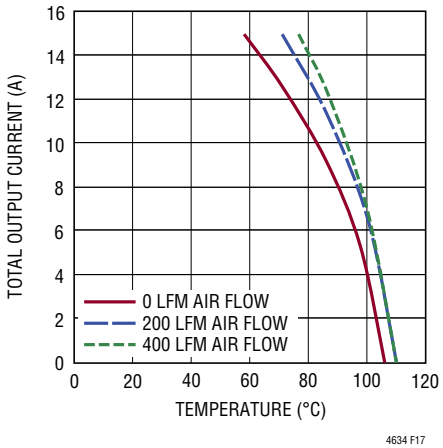

Figure 17. $12V_{IN}$, 5V, without Heat Sink, All Channels at 5A Each

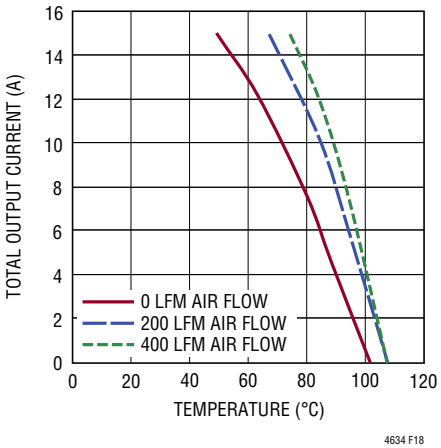

Figure 18. $24V_{IN}$, 3.3V, with Heat Sink, All Channels at 5A Each

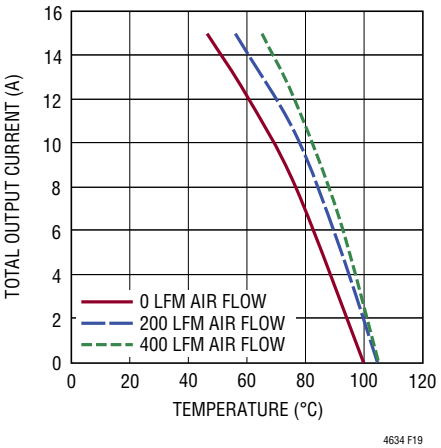

Figure 19. $24V_{IN}$, 3.3V, without Heat Sink, All Channels at 5A Each

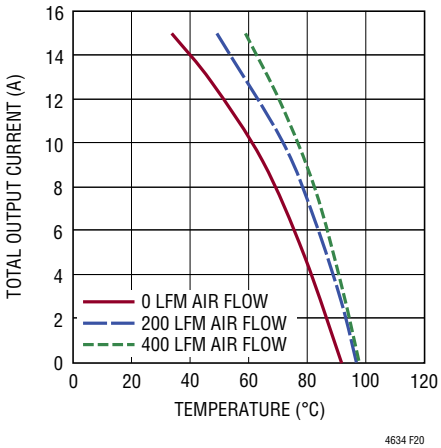

Figure 20. $24V_{IN}$, 5V, with Heat Sink, All Channels at 5A Each

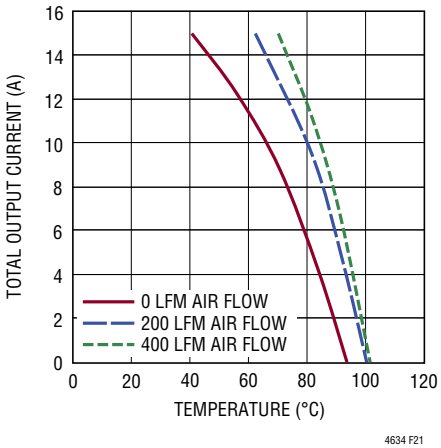

Figure 21. $24V_{IN}$, 5V, without Heat Sink, All Channels at 5A Each

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Table 2. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 15, 19	12, 24	Figures 8 to 13	0	None	9.0
Figures 15, 19	12, 24	Figures 8 to 13	200	None	7.5
Figures 15, 19	12, 24	Figures 8 to 13	400	None	6.5
Figures 14, 18	12, 24	Figures 8 to 13	0	BGA Heat Sink	9.0
Figures 14, 18	12, 24	Figures 8 to 13	200	BGA Heat Sink	6.5
Figures 14, 18	12, 24	Figures 8 to 13	400	BGA Heat Sink	6.0

Table 3. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 17, 20	12, 24	Figures 8 to 13	0	None	9.0
Figures 17, 20	12, 24	Figures 8 to 13	200	None	7.5
Figures 17, 20	12, 24	Figures 8 to 13	400	None	6.5
Figures 16, 21	12, 24	Figures 8 to 13	0	BGA Heat Sink	9.0
Figures 16, 21	12, 24	Figures 8 to 13	200	BGA Heat Sink	6.5
Figures 16, 21	12, 24	Figures 8 to 13	400	BGA Heat Sink	6.0

Heat Sink Manufacturer Part Number Website

Aavid Thermalloy	375424B00034G	www.aavid.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com

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Table 4. Output Voltage Response Versus Component Matrix (Refer to Figure 26) 0 to 2.5A Load Step Typical Measured Values

C_{OUT} CERAMIC VENDORS	VALUE	PART NUMBER
Murata	220µF, 4V, X5R 1206 Case Size	GRM31CR60G277M
TDK	100µF, 6.3V, X5R 1210 Case Size	C3225X5R0J107M
Murata	22µF, 25V, X7R, 1210 Case Size	GRM32ER71E226K
Panasonic Poscap	100µF, 16V, D2 Case Size	16TQC100M
	150µF, 16V, D3L Case Size	16TQC100M
Murata	4.7µF, 50V	GRU55ER71H475K
	10µF, 50V	GRM32ER71H06KA12L

V_{OUT1}, V_{OUT2}	C_{IN} (CERAMIC)	C_{IN} (BULK)*	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	C_{FF}	C_{BOT}	C_{COMP}	V_{IN}	DROP	PEAK-TO-PEAK DEVIATION AT 2.5A LOAD STEP	RECOVERY TIME	LOAD STEP	R_{FB}	FREQ
1V	22µF × 3	150µF	100µF × 2	None	47pF	None	None	12V	50mV	100mV	90µs	2.5A/µs	243kΩ	500kHz
1V	22µF × 3	150µF	220µF × 2	None	47pF	None	None	12V	40mV	80mV	90µs	2.5A/µs	243kΩ	500kHz
1.2V	22µF × 3	150µF	220µF × 2	None	47pF	None	None	12V	48mV	96mV	90µs	2.5A/µs	121kΩ	500kHz
1.5V	22µF × 3	150µF	220µF × 2	None	47pF	None	None	12V	50mV	100mV	100µs	2.5A/µs	69.8kΩ	500kHz
1.8V	22µF × 3	150µF	220µF × 2	None	47pF	None	None	12V	50mV	100mV	100µs	2.5A/µs	48.7kΩ	500kHz
2.5V	22µF × 3	150µF	220µF × 2	None	47pF	None	None	12V	75mV	150mV	100µs	2.5A/µs	28.7kΩ	500kHz
2.5V	22µF × 3	150µF	220µF × 3	None	47pF	None	None	12V	70mV	140mV	100µs	2.5A/µs	28.7kΩ	500kHz
3.3V	22µF × 3	150µF	220µF × 2	None	47pF	None	None	12V	100mV	200mV	120µs	2.5A/µs	19.1kΩ	500kHz
3.3V	22µF × 3	150µF	220µF × 2	None	47pF	None	None	12V	100mV	200mV	120µs	2.5A/µs	19.1kΩ	750kHz
3.3V	22µF × 3	150µF	220µF × 3	None	47pF	None	None	12V	90mV	180mV	120µs	2.5A/µs	19.1kΩ	500kHz
3.3V	22µF × 3	150µF	100µF × 2	None	47pF	None	None	12V	100mV	200mV	120µs	2.5A/µs	19.1kΩ	750kHz
5V	22µF × 3	150µF	100µF × 2	None	47pF	None	None	12V	170mV	340mV	100µs	2.5A/µs	11.5kΩ	750kHz
5V	22µF × 3	150µF	100µF × 3	None	47pF	None	None	12V	140mV	280mV	100µs	2.5A/µs	11.5kΩ	750kHz

V_{OUT3}	C_{IN}** (CERAMIC)	C_{IN} (BULK)*	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	C_{FF}	C_{BOT}	C_{COMP}	V_{IN}	DROP	PEAK-TO-PEAK DEVIATION AT 2.5A LOAD STEP	RECOVERY TIME	LOAD STEP	R_{FB}	FREQ
5	4.7µF × 3	150µF	100µF × 2	None	47pF	None	None	24V	170mV	340mV	120µs	2.5A/µs	11.5kΩ	600kHz
5	4.7µF × 3	150µF	100µF × 3	None	47pF	None	None	24V	140mV	280mV	120µs	2.5A/µs	11.5kΩ	600kHz
5	4.7µF × 3	150µF	100µF × 1	100µF × 1	47pF	None	None	24V	120mV	240mV	120µs	2.5A/µs	11.5kΩ	600kHz
5	4.7µF × 3	150µF	22µF × 1	100µF × 1	47pF	None	None	24V	120mV	240mV	120µs	2.5A/µs	11.5kΩ	600kHz
5	4.7µF × 3	150µF	22µF × 2	100µF × 1	47pF	None	None	24V	120mV	240mV	120µs	2.5A/µs	11.5kΩ	600kHz
5	4.7µF × 3	150µF	22µF × 1	100µF × 1	47pF	None	None	24V	110mV	220mV	120µs	2.5A/µs	11.5kΩ	600kHz
5	4.7µF × 3	150µF	22µF × 2	100µF × 1	47pF	None	None	24V	110mV	220mV	120µs	2.5A/µs	11.5kΩ	600kHz
12	4.7µF × 3	150µF	22µF × 2	None	47pF	None	None	24V	300mV	600mV	200µs	2.5A/µs	4.32kΩ	600kHz
12	4.7µF × 3	150µF	22µF × 3	None	47pF	None	None	24V	300mV	600mV	200µs	2.5A/µs	4.32kΩ	600kHz
12	4.7µF × 3	150µF	22µF × 1	100µF × 1	47pF	None	None	24V	250mV	500mV	200µs	2.5A/µs	4.32kΩ	600kHz
12	4.7µF × 3	150µF	22µF × 2	100µF × 1	47pF	None	None	24V	240mV	480mV	200µs	2.5A/µs	4.32kΩ	600kHz
12	4.7µF × 3	150µF	22µF × 1	100µF × 1	47pF	None	None	24V	230mV	460mV	200µs	2.5A/µs	4.32kΩ	600kHz
12	4.7µF × 3	150µF	22µF × 2	100µF × 1	47pF	None	None	24V	220mV	440mV	200µs	2.5A/µs	4.32kΩ	600kHz

*Bulk capacitor is optional if VIN has very low input impedance. Slew rate: 2.5A/µs. **50V

TYPICAL APPLICATIONS

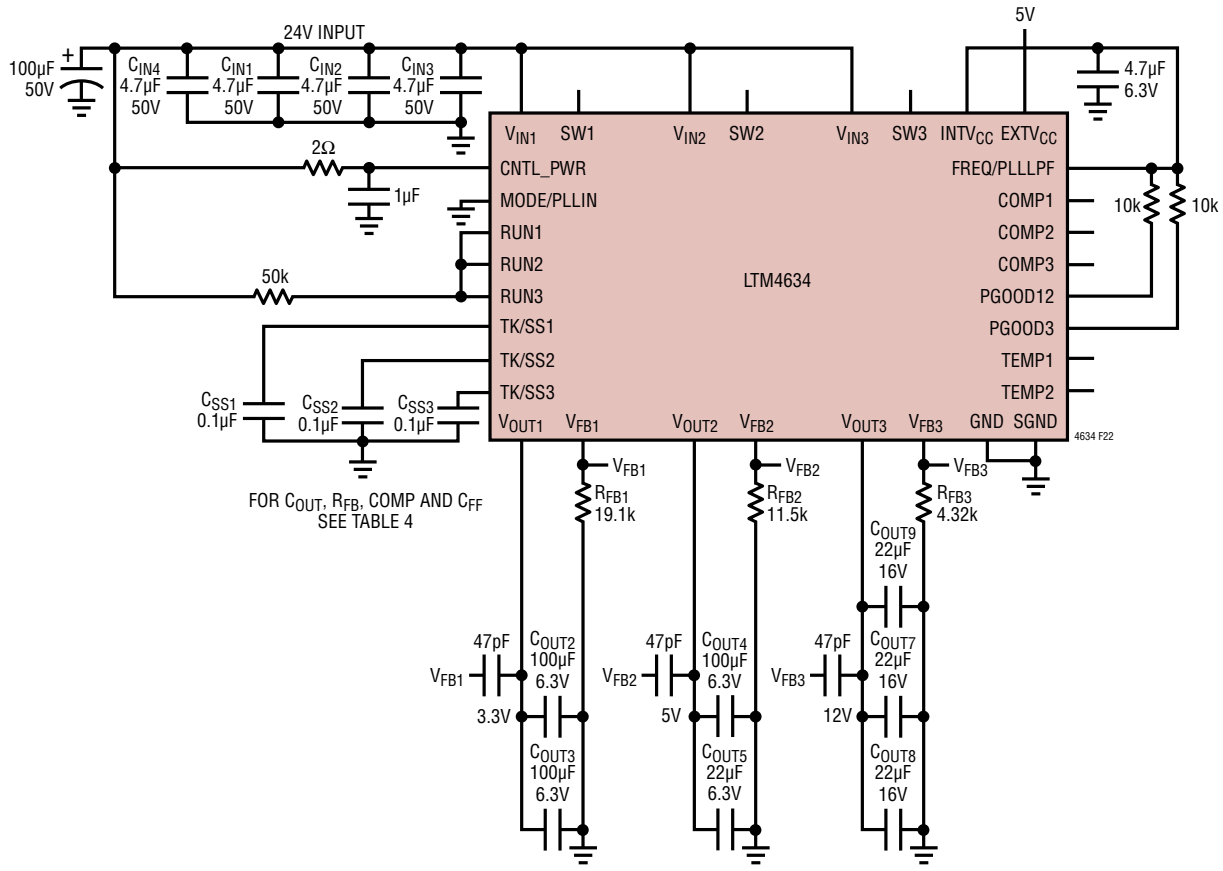


Figure 22. LTM4634 Typical 24V Input to 3.3V at 5A, 5V at 5A, 12V at 4A

TYPICAL APPLICATIONS

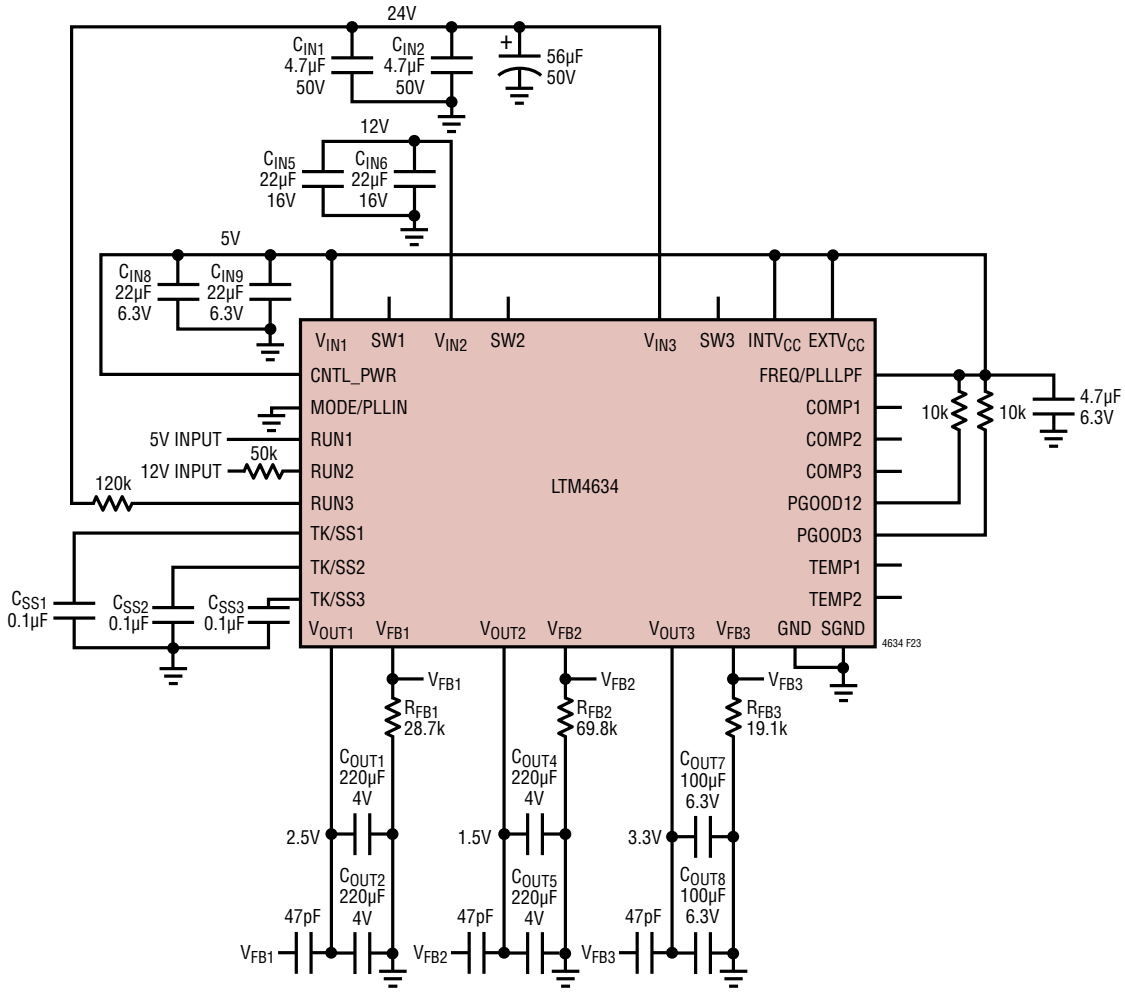


Figure 23. LTM4634 Triple Input and Triple Output (2.5V, 1.5V and 3.3V) at 5A, 5A and 4A

TYPICAL APPLICATIONS

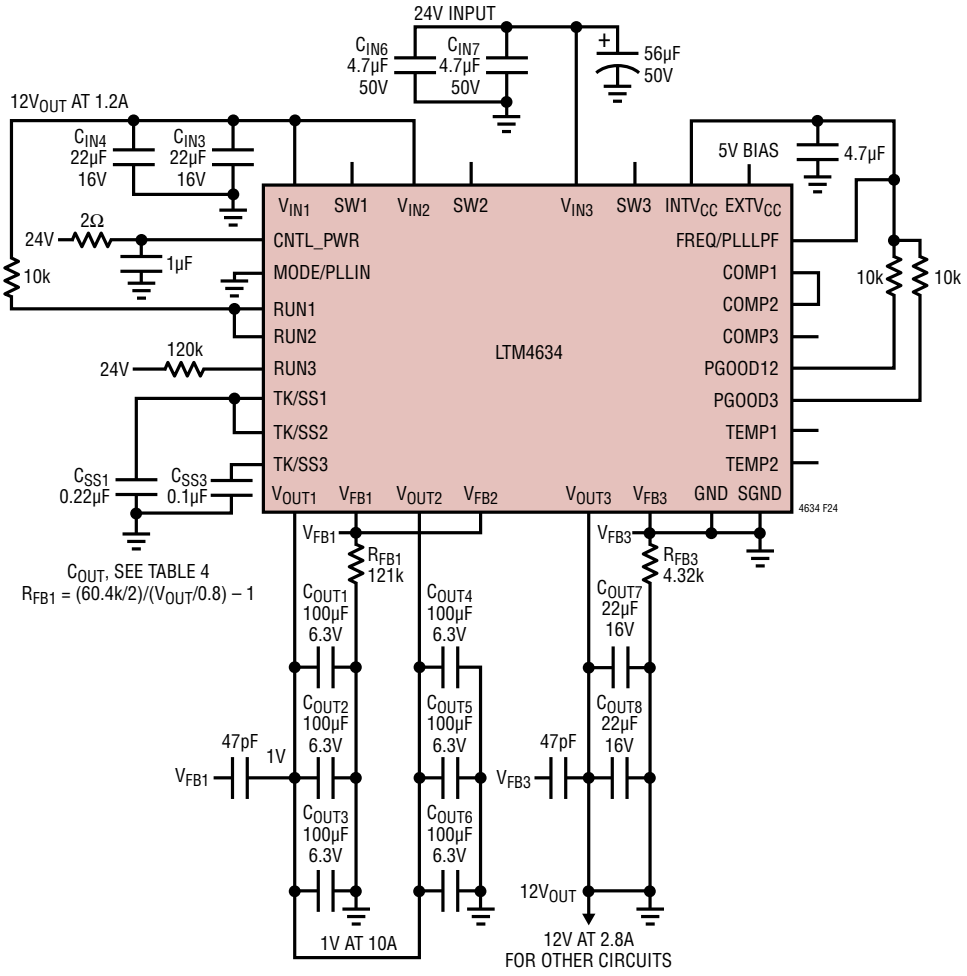


Figure 24. 24V to 12V at 2.8A, Then 12V to 1V at 10A

TYPICAL APPLICATIONS

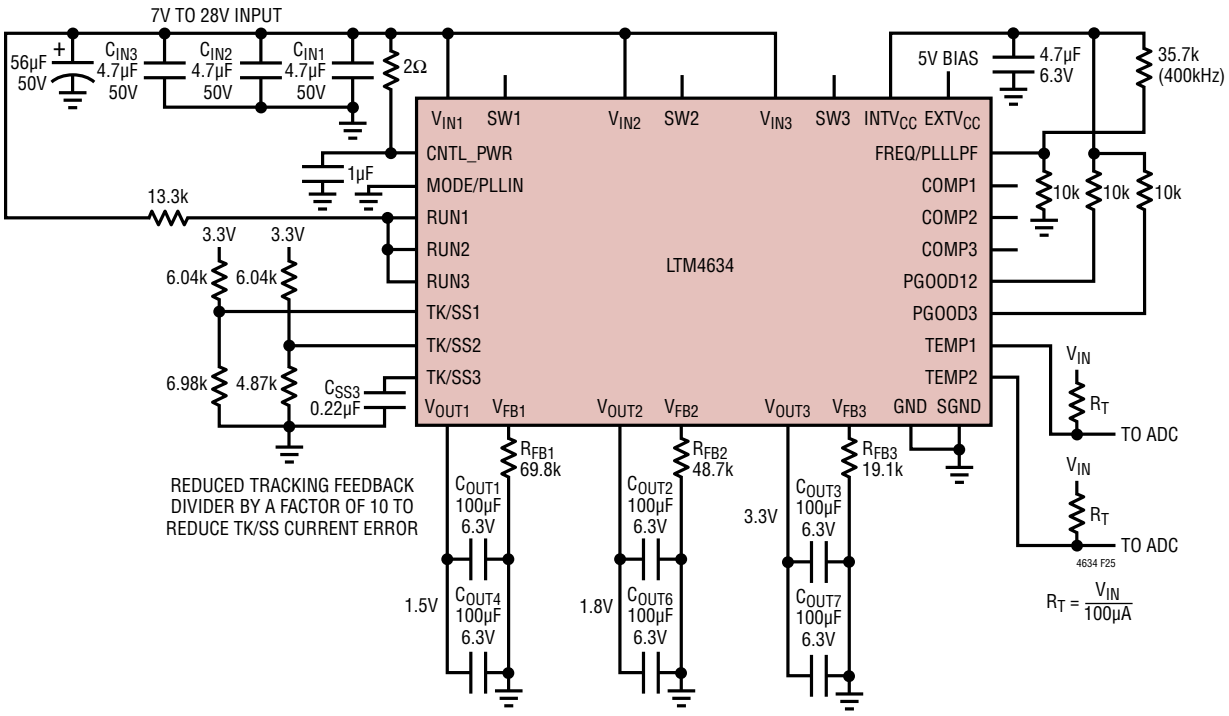


Figure 25. 7V to 28V Input, 1.5V, 1.8V and 3.3V at 5A,5A, 4A with Tracking

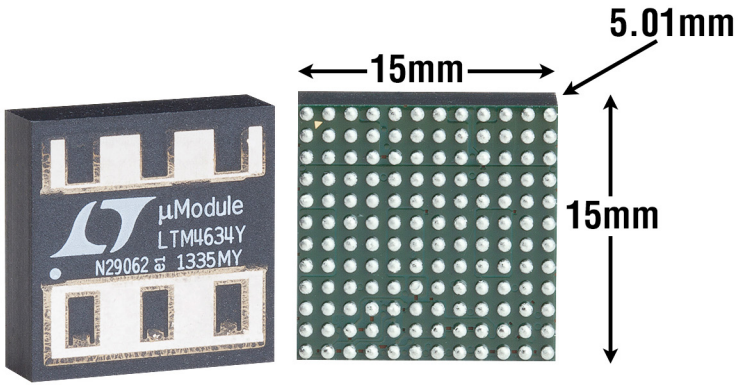
PACKAGE DESCRIPTION

LTM4634 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT3}	B1	V_{OUT3}	C1	V_{OUT3}	D1	GND	E1	GND	F1	V_{IN3}
A2	V_{OUT3}	B2	V_{OUT3}	C2	V_{OUT3}	D2	GND	E2	GND	F2	V_{IN3}
A3	V_{OUT3}	B3	V_{OUT3}	C3	V_{OUT3}	D3	GND	E3	GND	F3	SW3
A4	GND	B4	V_{OUT3}	C4	V_{OUT3}	D4	GND	E4	GND	F4	GND
A5	V_{OUT2}	B5	V_{OUT2}	C5	TEMP2	D5	GND	E5	GND	F5	V_{IN2}
A6	V_{OUT2}	B6	V_{OUT2}	C6	V_{OUT2}	D6	GND	E6	GND	F6	V_{IN2}
A7	V_{OUT2}	B7	V_{OUT2}	C7	V_{OUT2}	D7	GND	E7	GND	F7	SW2
A8	GND	B8	V_{OUT2}	C8	V_{OUT2}	D8	GND	E8	GND	F8	GND
A9	GND	B9	V_{OUT1}	C9	TEMP1	D9	GND	E9	GND	F9	V_{IN1}
A10	V_{OUT1}	B10	V_{OUT1}	C10	V_{OUT1}	D10	GND	E10	GND	F10	V_{IN1}
A11	V_{OUT1}	B11	V_{OUT1}	C11	V_{OUT1}	D11	GND	E11	GND	F11	SW1
A12	V_{OUT1}	B12	V_{OUT1}	C12	V_{OUT1}	D12	GND	E12	GND	F12	GND

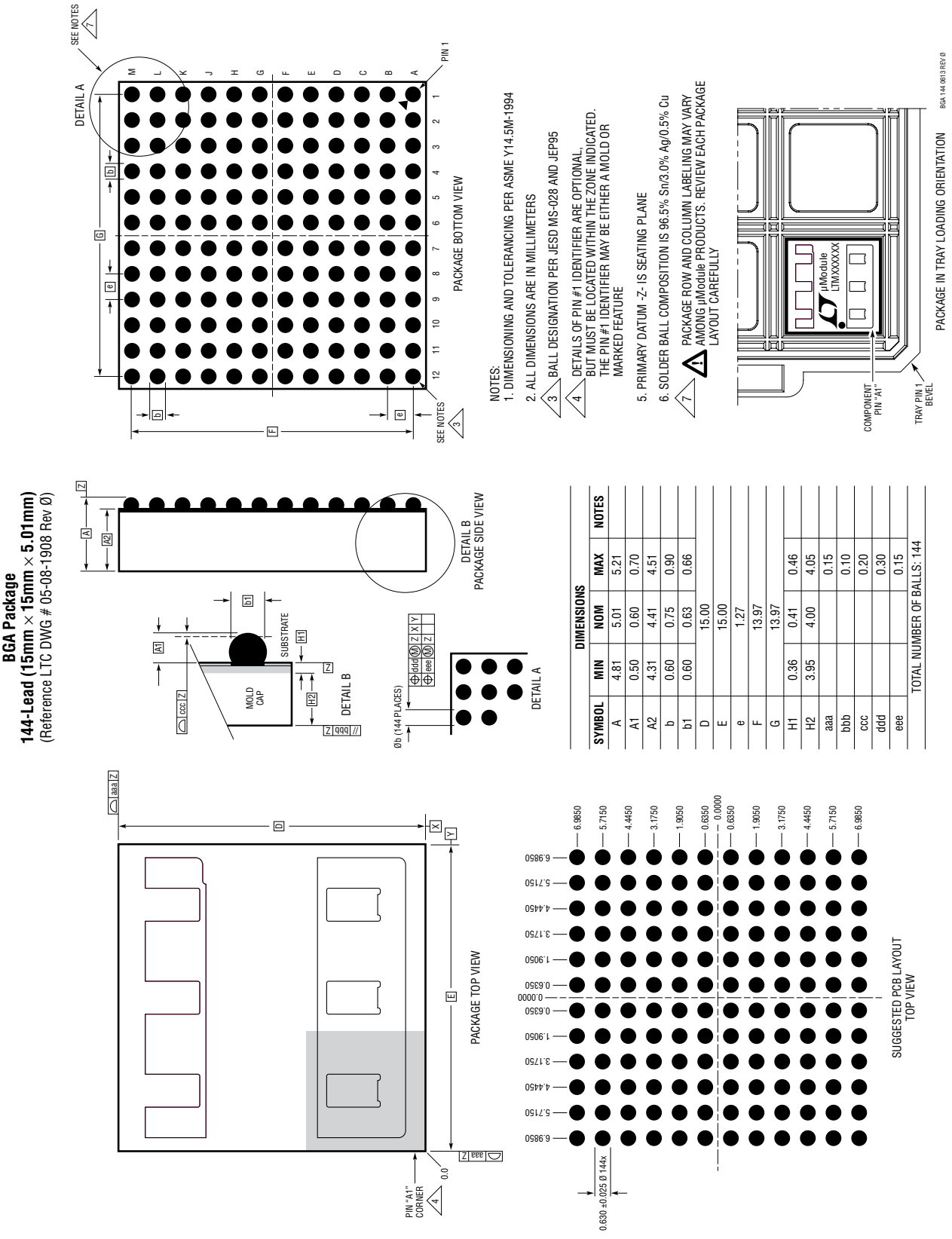
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	V_{IN3}	H1	V_{IN3}	J1	GND	K1	GND	L1	GND	M1	GND
G2	V_{IN3}	H2	V_{IN3}	J2	GND	K2	GND	L2	GND	M2	PGOOD12
G3	GND	H3	GND	J3	GND	K3	GND	L3	$EXTV_{CC}$	M3	PGOOD3
G4	GND	H4	GND	J4	GND	K4	COMP3	L4	COMP2	M4	COMP1
G5	V_{IN2}	H5	V_{IN2}	J5	GND	K5	V_{FB3}	L5	V_{FB2}	M5	V_{FB1}
G6	V_{IN2}	H6	V_{IN2}	J6	CNTL_PWR	K6	SGND	L6	SGND	M6	GND
G7	GND	H7	GND	J7	GND	K7	SGND	L7	SGND	M7	GND
G8	GND	H8	GND	J8	$INTV_{CC}$	K8	GND	L8	FREQ/PLLLPF	M8	GND
G9	V_{IN1}	H9	V_{IN1}	J9	GND	K9	GND	L9	MODE/PLLIN	M9	TK/SS1
G10	V_{IN1}	H10	V_{IN1}	J10	GND	K10	GND	L10	RUN1	M10	TK/SS2
G11	GND	H11	GND	J11	GND	K11	RUN3	L11	RUN2	M11	TK/SS3
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

PACKAGE PHOTO



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.36	0.41	0.46	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 144				

TYPICAL APPLICATION

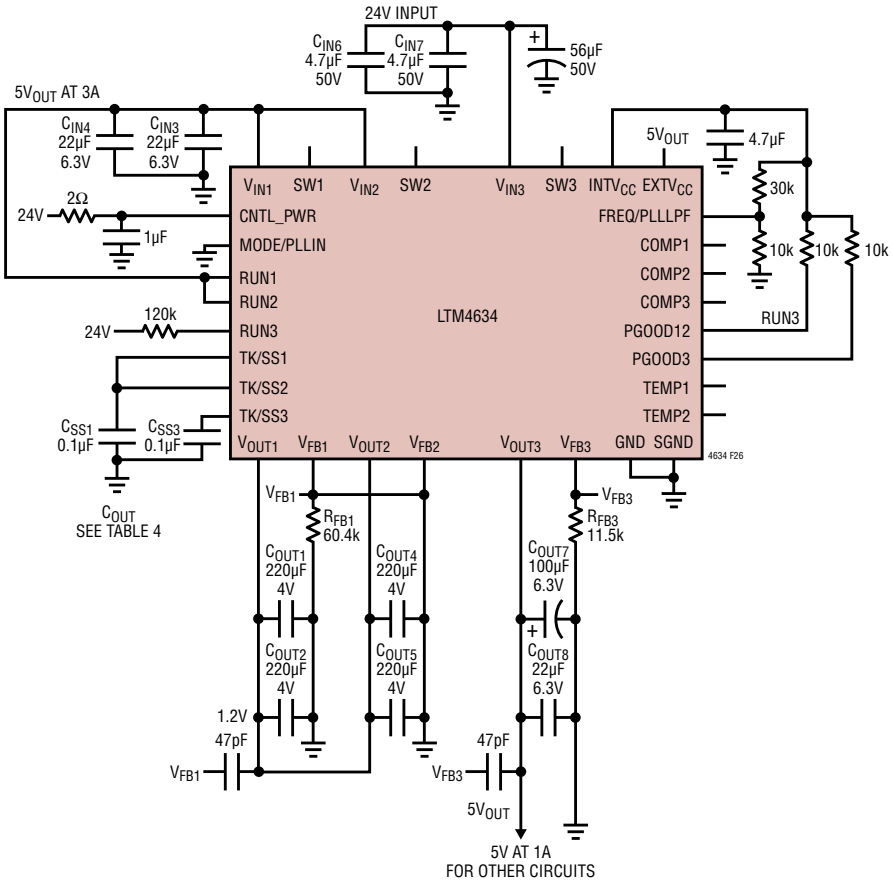


Figure 26. 24V to 5V at 1A, Then 5V Output to 1.2V at 10A

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4633	Triple 10A, 16V_{IN} Step-Down DC/DC µModule Regulator	4.7V ≤ V_{IN} ≤ 16V, 0.8V ≤ $V_{OUT1,2}$ ≤ 1.8V, 0.8V ≤ V_{OUT3} ≤ 5.5V, PLL Input, V_{OUT} Soft-Start and Tracking, PGOOD, Internal Temperature Monitor, 15mm × 15mm × 5.01mm BGA
LTM4630	Dual 15V_{IN}, 18A or Single 36A Step-Down µModule Regulator with V_{OUT} Up to 1.8V	4.5V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V, PLL Input, Remote Sense Amplifier, V_{OUT} Tracking, PGOOD, CLKOUT, Internal Temperature Monitor, 16mm × 16mm × 4.41mm LGA
LTM4644	Quad 4A, 14V Step-Down µModule Regulator with Configurable Output Array	4V ≤ V_{IN} ≤ 14V, 0.6V ≤ V_{OUT} ≤ 5.5V, CLK Input and Output, V_{OUT} Tracking, PGOOD, 9mm × 15mm × 5.01mm BGA
LTM4676	Dual 13A or Single 26A µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤ 26V, 0.5V ≤ V_{OUT0} ≤ 4.0V, 0.5V ≤ V_{OUT1} ≤ 5.4V, Digital I/F for Control and Monitoring, Integrated 16-Bit ADC, PMBus Compliant I^2C Interface, Remote Sense Amplifiers, 16mm × 16mm × 5.01mm BGA
LTM8028	36V_{IN}, UltraFast™, Low Output Noise 5A µModule Regulator	6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 1.8V Set Via 3-Pin Three-State Interface, <1mV V_{OUT} Ripple, 10% Accurate Current Limit, PGOOD, 15mm × 15mm × 4.9mm BGA
LTM4637	20V_{IN}, 20A DC/DC µModule Step-Down Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, PLL Input, V_{OUT} Tracking, Remote Sense Amplifier, PGOOD, 15mm × 15mm × 4.32mm LGA and 15mm × 15mm × 4.92mm BGA
LTM8045	Inverting or SEPIC _Module DC/DC Converter with Up to 700mA Output Current	2.8V ≤ V_{IN} ≤ 18V, ±2.5V ≤ V_{OUT} ≤ ±15V, Synchronizable, No Derating or Logic-Level Shift for Control Inputs When Inverting, 6.25mm × 11.25mm × 4.92mm BGA
LTC2977	8-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Temperature Monitoring and Supervision
LTC2974	4-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision

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