



**THE DATASHEET OF
NVJD5121NT1G**



MOSFET – Power, Dual, N-Channel With ESD Protection, SC-88 60 V, 295 mA NTJD5121N, NVJD5121N

Features

- Low $R_{DS(on)}$
- Low Gate Threshold
- Low Input Capacitance
- ESD Protected Gate
- NVJD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

Applications

- Low Side Load Switch
- DC-DC Converters (Buck and Boost Circuits)

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | | Symbol | Value | Unit | |
|---|-------------------------|--------------------------|------------|--------------------------|----|
| Drain-to-Source Voltage | | V_{DSS} | 60 | V | |
| Gate-to-Source Voltage | | V_{GS} | ± 20 | V | |
| Continuous Drain Current (Note 1) | Steady State | $T_A = 25^\circ\text{C}$ | I_D | 295 | mA |
| | | | | $T_A = 85^\circ\text{C}$ | |
| | $t \leq 5\text{ s}$ | $T_A = 25^\circ\text{C}$ | I_D | 304 | |
| | | | | $T_A = 85^\circ\text{C}$ | |
| Power Dissipation (Note 1) | Steady State | $T_A = 25^\circ\text{C}$ | P_D | 250 | mW |
| | | | | $t \leq 5\text{ s}$ | |
| Pulsed Drain Current | $t_p = 10\ \mu\text{s}$ | I_{DM} | 900 | mA | |
| Operating Junction and Storage Temperature | | T_J, T_{STG} | -55 to 150 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | | I_S | 210 | mA | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | T_L | 260 | $^\circ\text{C}$ | |
| Gate-Source ESD Rating (HBM) | | ESD_{HBM} | 2000 | V | |
| Gate-Source ESD Rating (MM) | | ESD_{MM} | 200 | V | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

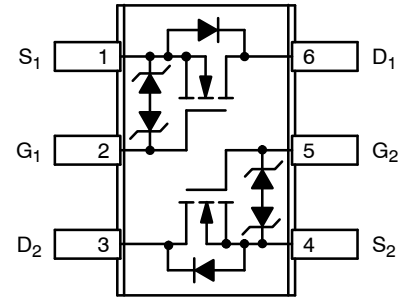
THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Ambient – Steady State | $R_{\theta JA}$ | 467 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – $t \leq 5\text{ s}$ | $R_{\theta JA}$ | 412 | |
| Junction-to-Lead – Steady State | $R_{\theta JL}$ | 252 | |

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

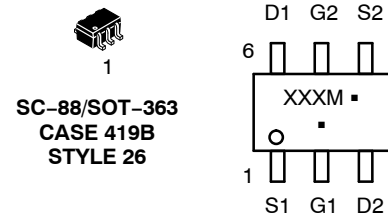
| $V_{(BR)DSS}$ | $R_{DS(on)}\text{ MAX}$ | $I_D\text{ Max}$ |
|---------------|-------------------------|------------------|
| 60 V | 1.6 Ω @ 10 V | 295 mA |
| | 2.5 Ω @ 4.5 V | |

SC-88 (SOT-363)



Top View

MARKING DIAGRAM & PIN ASSIGNMENT



SC-88/SOT-363
CASE 419B
STYLE 26

XXX = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NTJD5121N, NVJD5121N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------------------|--|------------------------|-----|-----|-------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | I _D = 250 μA, ref to 25°C | | 92 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 60 V | T _J = 25°C | | 1.0 | μA |
| | | | T _J = 125°C | | 500 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = ±20 V | | | ±10 | μA |

ON CHARACTERISTICS (Note 2)

| | | | | | | |
|--|-------------------------------------|---|-----|-----|-----|-------|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 250 μA | 1.0 | 1.7 | 2.5 | V |
| Negative Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | 4.0 | | mV/°C |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 500 mA | | 1.0 | 1.6 | Ω |
| | | V _{GS} = 4.5 V, I _D = 200 mA | | 1.2 | 2.5 | |
| Forward Transconductance | g _{FS} | V _{DS} = 5 V, I _D = 200 mA | | 80 | | S |
| Gate Resistance | R _G | | | 536 | | Ω |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|---------------------|--|--|------|--|----|
| Input Capacitance | C _{ISS} | V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 20 V | | 26 | | pF |
| Output Capacitance | C _{OSS} | | | 4.4 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | 2.5 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 25 V, I _D = 200 mA | | 0.9 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | | | 0.2 | | |
| Gate-to-Source Charge | Q _{GS} | | | 0.3 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 0.28 | | |

SWITCHING CHARACTERISTICS (Note 3)

| | | | | | | |
|---------------------|---------------------|---|--|----|--|----|
| Turn-On Delay Time | t _{d(on)} | V _{GS} = 4.5 V, V _{DD} = 25 V, I _D = 200 mA, R _G = 25 Ω | | 22 | | ns |
| Rise Time | t _r | | | 34 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 34 | | |
| Fall Time | t _f | | | 32 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-----------------------|-----------------|--|-----------------------|--|-----|-----|---|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 200 mA | T _J = 25°C | | 0.8 | 1.2 | V |
| | | | T _J = 85°C | | 0.7 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

NTJD5121N, NVJD5121N

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

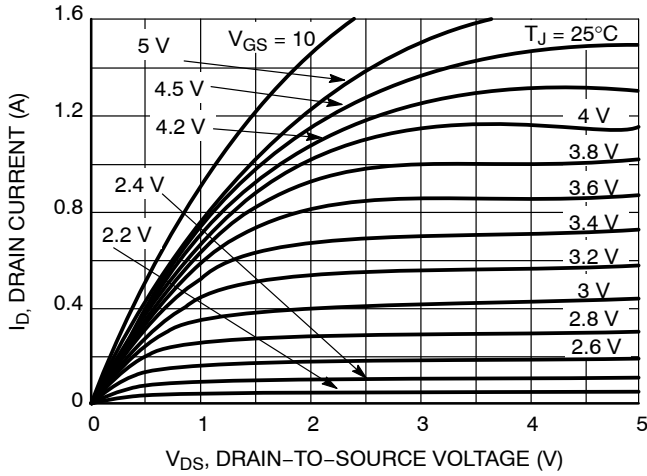


Figure 1. On-Region Characteristics

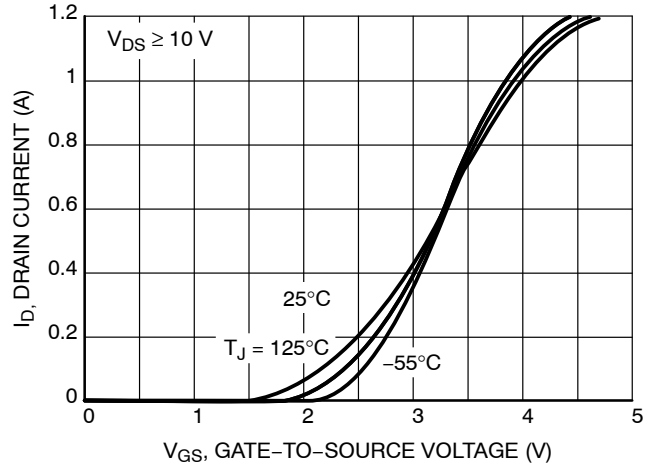


Figure 2. Transfer Characteristics

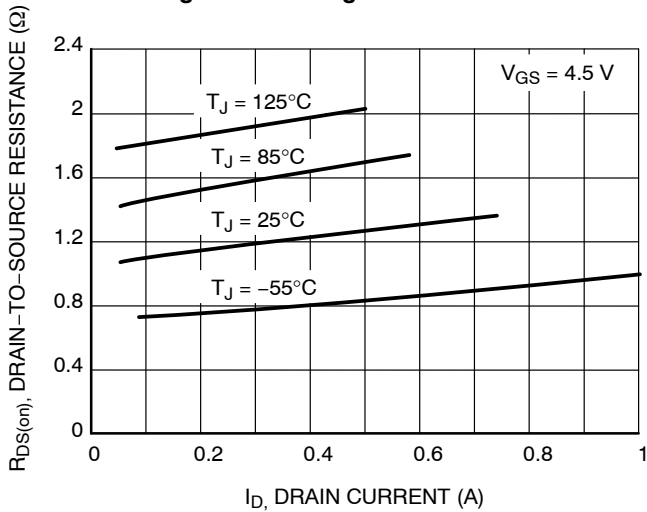


Figure 3. On-Resistance vs. Drain Current and Temperature

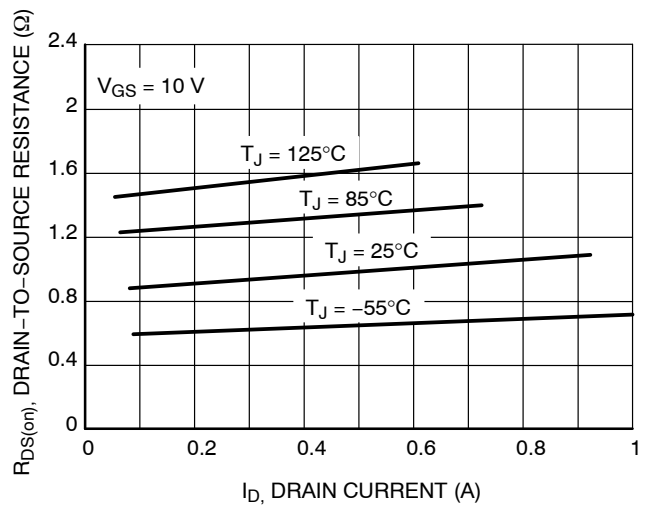


Figure 4. On-Resistance vs. Drain Current and Temperature

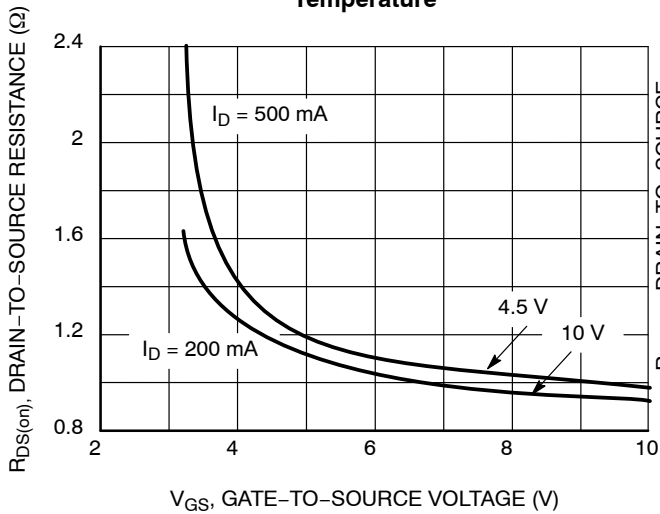


Figure 5. On-Resistance versus Gate-to-Source Voltage

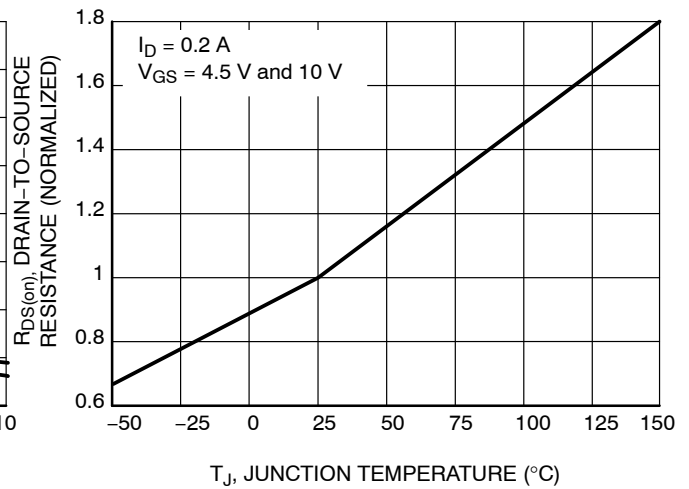


Figure 6. On-Resistance Variation with Temperature

NTJD5121N, NVJD5121N

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

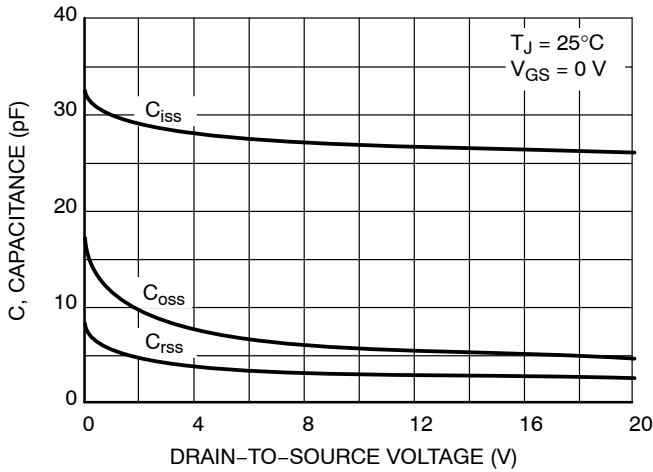


Figure 7. Capacitance Variation

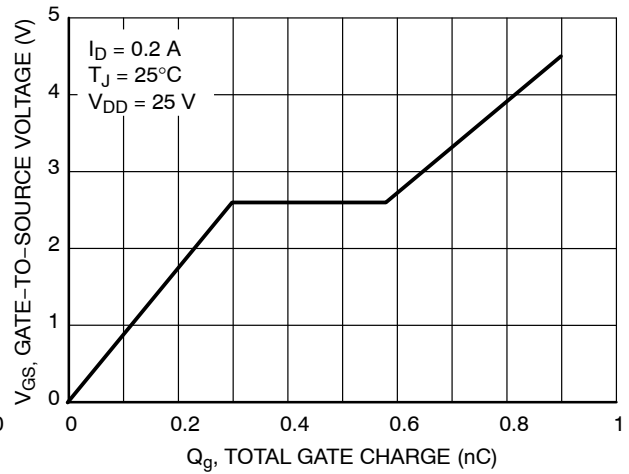


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

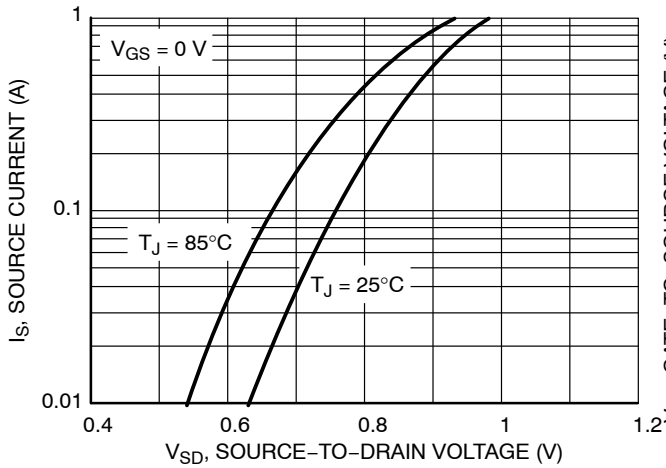


Figure 9. Diode Forward Voltage vs. Current

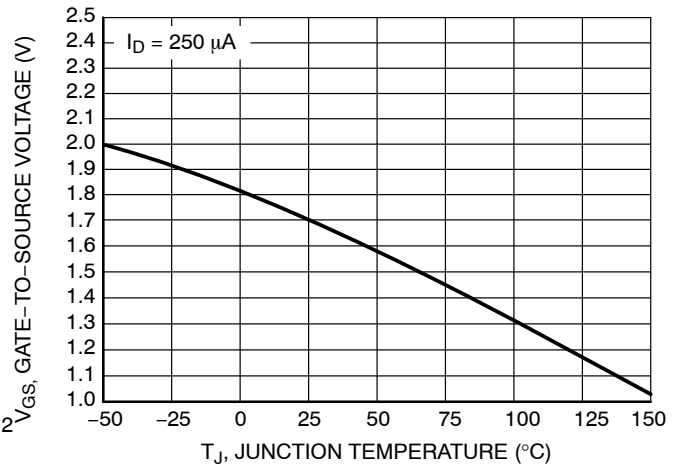


Figure 10. Threshold Voltage with Temperature

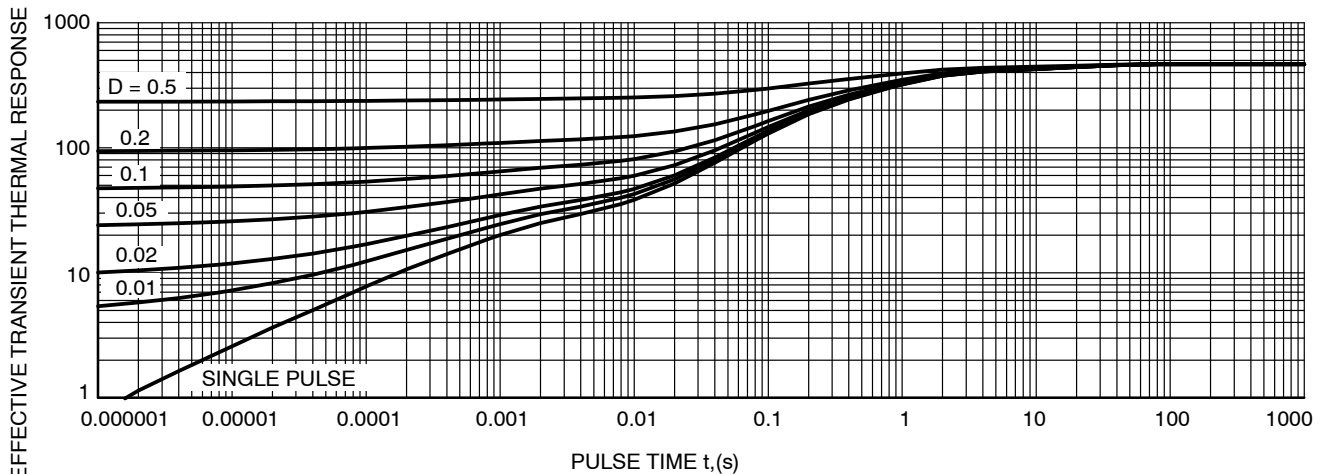


Figure 11. Thermal Response

NTJD5121N, NVJD5121N

Table 1. ORDERING INFORMATION

| Part Number | Marking | Package | Shipping† |
|--------------------|----------------|--------------------|--------------------|
| NTJD5121NT1G | TF | SC-88 (Pb-Free) | 3000 / Tape & Reel |
| NTJD5121NT2G | TF | SC-88 (Pb-Free) | 3000 / Tape & Reel |
| NVJD5121NT1G* | VTF | SC-88 (Pb-Free) | 3000 / Tape & Reel |
| NVJD5121NT1G-M06* | VTF | SC-88 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NVJD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

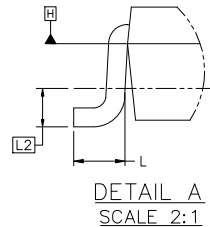
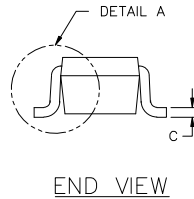
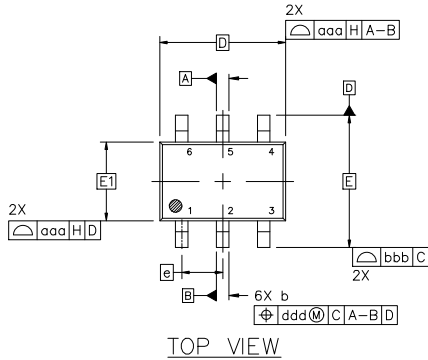


SC-88 2.00x1.25x0.90, 0.65P CASE 419B-02 ISSUE Z

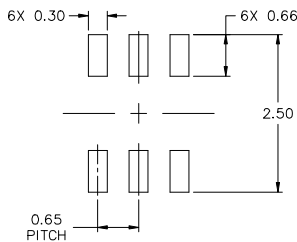
DATE 18 APR 2024

NOTES:

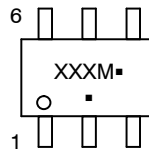
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.10 |
| A1 | 0.00 | --- | 0.10 |
| A2 | 0.70 | 0.90 | 1.00 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.08 | 0.15 | 0.22 |
| D | 2.00 BSC | | |
| E | 2.10 BSC | | |
| E1 | 1.25 BSC | | |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L2 | 0.15 BSC | | |
| aaa | 0.15 | | |
| bbb | 0.30 | | |
| ccc | 0.10 | | |
| ddd | 0.10 | | |



GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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CASE 419B-02
ISSUE Z

DATE 18 APR 2024

| | | | | | |
|---|---|--|--|--|--|
| STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2 | STYLE 2: CANCELLED | STYLE 3: CANCELLED | STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE | STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE | STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2 |
| STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2 | STYLE 8: CANCELLED | STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2 | STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2 | STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2 | STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2 |
| STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE | STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC | STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1 | STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1 | STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1 | STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1 |
| STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF | STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR | STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1 | STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c) | STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C | STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE |
| STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1 | STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1 | STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2 | STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN | STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE | STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1 |

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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