THE DATASHEET OF

MKL82Z128VLK7

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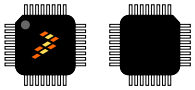
Kinetis KL82 Microcontroller

72 MHz ARM® Cortex®-M0+ with 128 KB Flash and 96 KB SRAM

MKL82Z128Vxx7(R)

121 & 64 MAPBGA
(MC&MP)
8x8x1.43 mm Pitch
0.65 mm 5x5x1.23 mm
Pitch 0.5 mm



100 & 80 & 64 LQFP
(LL&LK&LH)
14x14 x1.7 mm Pitch
0.5mm 12x12x1.6 mm
Pitch 0.5 mm
10x10x1.6 mm Pitch
0.5 mm

The KL82 MCU family's high performance, encryption features and ultra-low power capabilities extend its reach beyond traditional mPOS pin pads and terminals into more power-restricted payment applications, such as smartphone and tablet attach readers, as well as those embedded in wearable technology.

The product offers:

- Hardware asymmetric cryptography – high-speed, code- and power-efficient data authentication with support for latest encryption protocols
- EMV®-compatible with ISO7816-3 SIM interfaces – architected for EMV compliance and supported by an EMV Level 1 software stack
- QSPI interface to expand program memory
- Sleep mode power consumption from 2.5 µA with the SRAM content retained and RTC enabled
- Crystal-less USB OTG controller, 16-bit ADC and multiple serial communication interfaces can all function autonomously in low-power modes with minimal CPU intervention
- FlexIO to support any standard and customized serial peripheral emulation

Core Processor

- 72 MHz ARM® Cortex®-M0+ core (up to 96 MHz for high-speed run)

Memories

- 128 KB program flash memory
- 96 KB SRAM
- 32 KB ROM with built-in boot loader
- 32 B backup register
- QSPI to expand program code in external high-speed serial NOR flash memory

System

- 8-channel asynchronous enhanced DMA controller
- Watchdog
- Low-leakage wakeup unit
- Two-pin serial wire debug (SWD) programming and debugging interface
- Micro trace buffer
- Bit manipulation engine
- Interrupt controller

Peripherals

- USB full-speed 2.0 OTG controller supporting crystal-less operation and keeping connection alive under ultra-low power
- Three low-power UART modules supporting asynchronous operation in low-power modes
- Two I2C modules supporting up to 1 Mbps
- Two 16-bit SPI modules supporting up to 24Mbps
- One FlexIO module supporting emulation of additional UART, SPI, I2C, I2S, PWM and other serial modules, etc. up to 32 channels
- One 16-bit ADC module with high accurate internal voltage reference and up to 16 channels
- High-speed analog comparator containing a 6-bit DAC for programmable reference input
- One 12-bit DAC module
- Two EMVSIM modules supporting EMV L1 compatible interface
- Touch sensing interface up to 16 channels

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

- Memory protection unit
- SRAM bit-banding

Clocks

- 48 MHz high accuracy (up to 0.5%) internal reference clock for high-speed run
- 4 MHz high accuracy (up to 2%) internal reference clock for low-speed run
- 32 kHz internal reference clock
- 1 kHz internal reference clock
- 32–40 kHz and 3–32 MHz crystal oscillator
- PLL/FLL

Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- Two low-power timers
- 4-channel periodic interrupt timer
- Independent real time clock

Security

- 128-bit unique identification number per chip
- Advanced flash security and access control
- Hardware CRC module
- Low-power trusted crypto engine supporting AES128/256, DES, 3DES, SHA256, RSA and ECC, with hardware DPA
- True random number generator

I/O

- Up to 85 General-purpose input/output pins (GPIO)

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Low Power

- Down to 125 µA/MHz in Run mode
- Down to 272 nA in Stop mode (RAM and RTC retained)
- Six flexible static modes

Packages

- 121 MAPBGA 8mm x 8mm, 0.65mm pitch, 1.43mm max thickness
- 80 LQFP 12mm x 12mm, 0.5mm pitch, 1.6mm max thickness
- 100 LQFP 14mm x 14mm, 0.5mm pitch, 1.7mm max thickness (Package Your Way)
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm max thickness (Package Your Way)
- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm max thickness (Package Your Way)

NOTE

The 100-, 64-pin LQFP and 64-pin MAPBGA packages supporting MKL82Z128VLL7, MKL82Z128VLH7 and MKL82Z128VMP7 part numbers for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

Related resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL82P121M72SF0RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL82P121M72SF0[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	*x*N51R[2]
Package drawing	Package dimensions are provided in package drawings.	MAPBGA 121-pin: 98ASA00423D MAPBGA 64-pin: 98ASA00420D LQFP 100-pin: 98ASS23308W LQFP 80-pin: 98ASS23174W LQFP 64-pin: 98ASS23234W

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

2. To find the associated resource, go to http://www.nxp.com and perform a search using this term with the "x" replaced by the revision of the device you are using.

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1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product		Memory		Package		IO and ADC channel		
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels (SE/DP)
MKL82Z128VMC7(R)	MKL82 Z128VMC7	128	96	121	MAPBGA	85	85/0	16/2
MKL82Z128VLL7(R)	MKL82Z128VL L7	128	96	100	LQFP	66	66/0	14/1
MKL82Z128VLK7(R)	MKL82Z128 VLK7	128	96	80	LQFP	56	56/0	12/1
MKL82Z128VMP7(R)	M82N7V	128	96	64	MAPBGA	41	41/0	11/1
MKL82Z128VLH7(R)	MKL82Z128V LH7	128	96	64	LQFP	41	41/0	11/1

1. INT: interrupt pin numbers; HD: high drive pin numbers

NOTE

The 100-, 64-pin LQFP and 64-pin MAPBGA packages supporting MKL82Z128VLL7, MKL82Z128VLH7 and MKL82Z128VMP7 part numbers for this product are not yet available. However, these packages are included in Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

2 Overview

The following figure shows the system diagram of this device

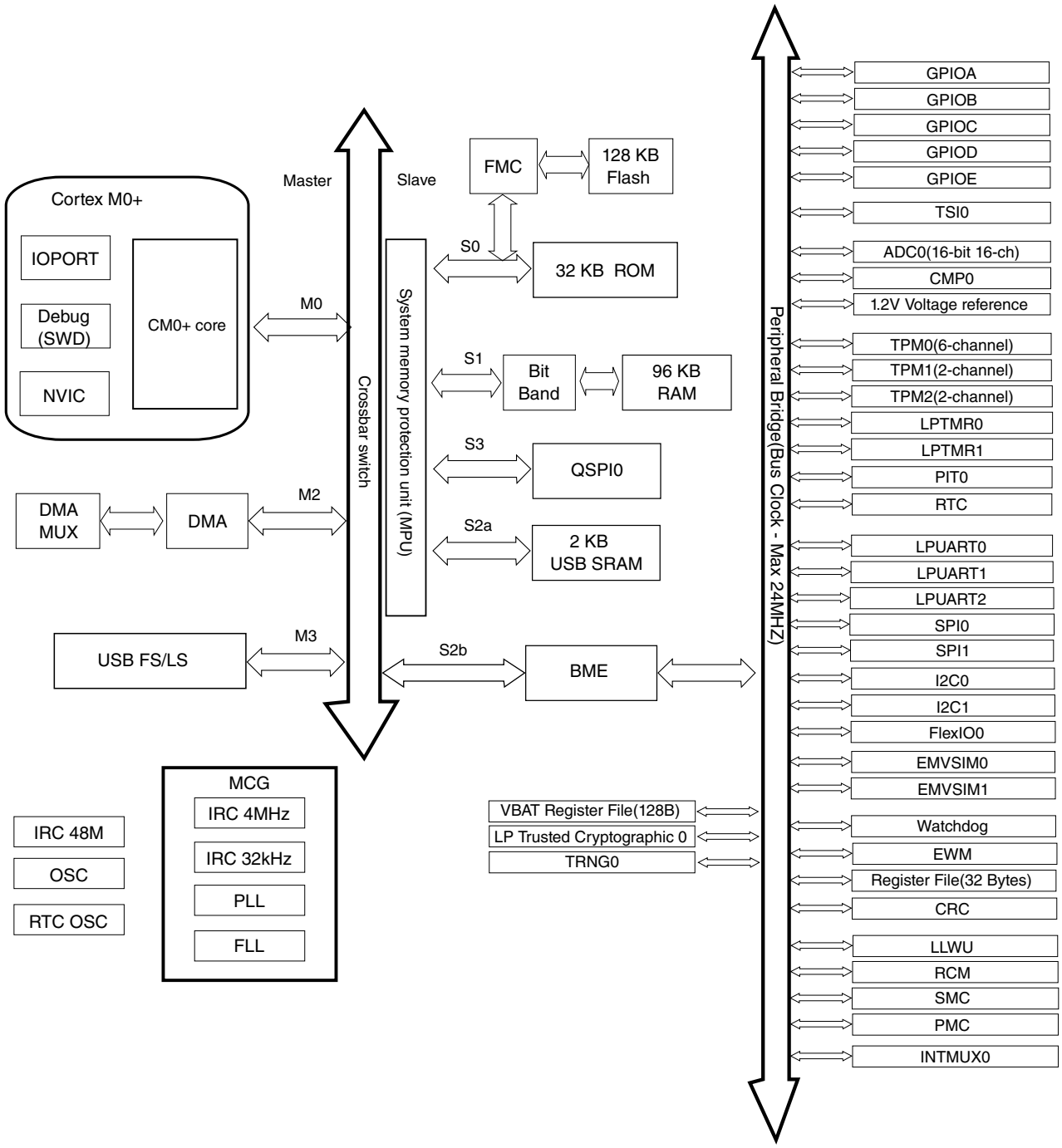


Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.1 ARM Cortex-M0+ core

The enhanced ARM Cortex M0+ is the member of the Cortex-M series of processors targeting microcontroller cores focused on very cost sensitive, low power applications. It has a single 32-bit AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality including support for simple program trace capability. The processor supports the ARMv6-M instruction set (Thumb) architecture including all but three 16-bit Thumb opcodes (52 total) plus seven 32-bit instructions. It is upward compatible with other Cortex-M profile processors.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 4 priority levels for interrupts. In the NVIC, each source in the IPR registers contains two bits. It also differs in number of interrupt sources and supports 32 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency to up to 15 clock cycles for Cortex-M0+. It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Stop and VLPS modes.

Wake-up sources are listed as below:

Table 2. AWIC Partial Stop, Stop and VLPS wake-up sources

Wake-up source	Description
Available system resets	RESET_b pin and WDOG when LPO is its clock source, and Debug
Low-voltage detect	Power mode controller
Low-voltage warning	Power mode controller
Pin interrupts	Port control module - any enabled pin interrupt is capable of waking the system
ADC0	The ADC is functional when using internal clock source
CMPx	Since no system clocks are available, functionality is limited, trigger mode provides wakeup functionality with periodic sampling
I2Cx	Address match wakeup
LPUARTx	Functional when using clock source which is active in Stop and VLPS modes
USB FS/LS Controller	Wakeup
FlexIO0	Functional when using clock source which is active in Stop and VLPS modes
LPTMR	Functional when using clock source which is active in Stop, VLPS and LLS/VLLS modes
RTC	Functional in Stop/VLPS modes
TPM	Functional when using clock source which is active in Stop and VLPS modes
TSI0	Wakeup
NMI	Non-maskable interrupt

2.1.4 Memory

This device has the following features:

- 96 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into two arrays
  - 128 KB of embedded program memory
  - 32 KB ROM (built-in bootloader to support UART, I2C, USB, and SPI interfaces)

  The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 1 KB.

  The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

  The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

This device contains a 32-byte register file that is powered in all power modes.

Also, it retains contents during low power modes and is reset only during a power-on reset.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules								
		PMC	SIM	SMC	RCM	LLWU	Reset pin is negated	RTC[1]	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	N	Y	Y
System reset	Low leakage wakeup (LLWU) reset	N	Y[2]	N	Y	N	Y[3]	N	N	Y
	External pin reset ($\overline{\text{RESET}}$)	Y	Y[2]	Y[4]	Y	Y	Y	N	N	Y
	Computer operating properly (COP) watchdog reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Software reset (SW)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	MDM DAP system reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
Debug reset	Debug reset	Y	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y

1. The VBAT POR asserts on a VBAT POR reset source. It affects only the modules withinthe VBAT power domain: RTC and VBAT Register File. These modules are notaffected by the other reset types.
2. Except SIM_SOPT1
3. Only if $\overline{\text{RESET}}$ is used to wake from VLLS mode.
4. Except SMC_PMCTRL, SMC_STOPCTRL, SMC_PMSTAT
5. Except RCM_RPFC, RCM_RPFW, RCM_FM

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- ROM

The Flash Option (FOPT) register in the Flash Memory module (FTFA_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. Below is boot flow chart for this device.

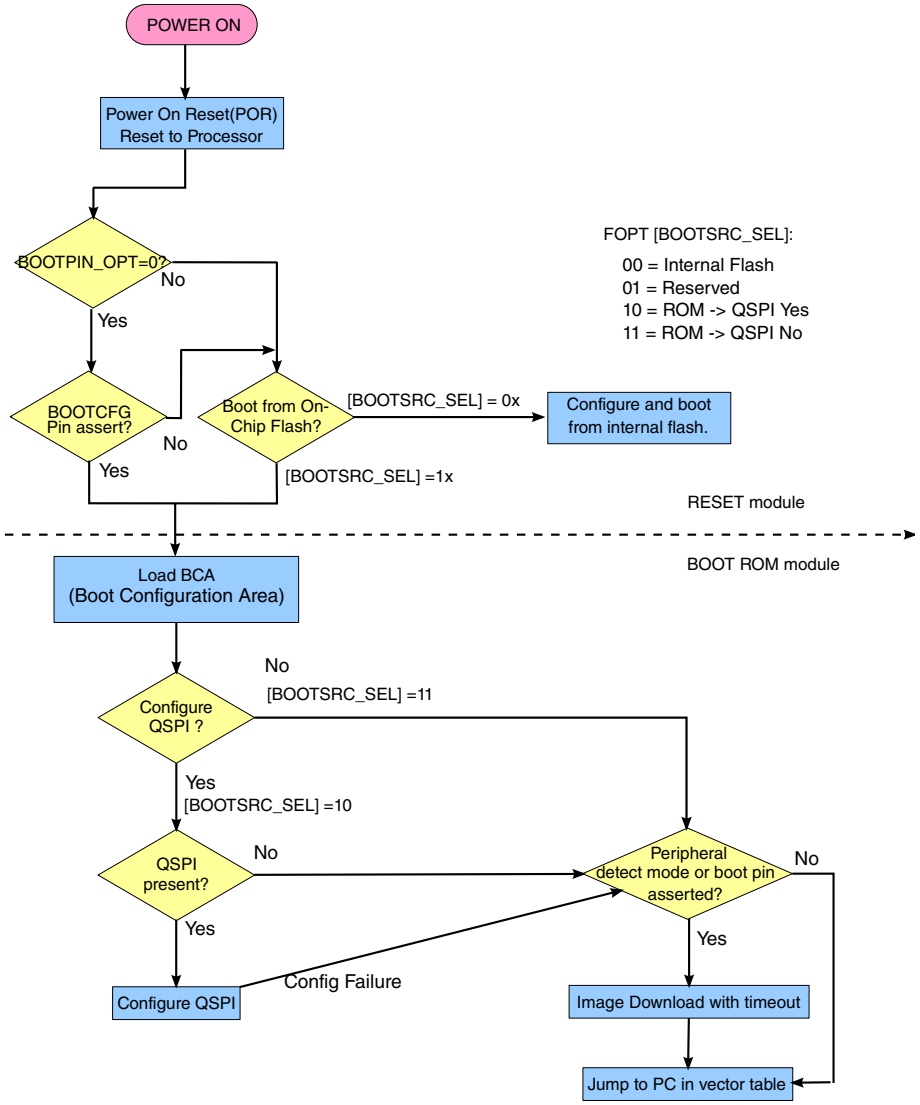


Figure 2. Boot Flow For Devices with QSPI

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

If booting from ROM, the device executes in boot loader mode or proceeds with a secondary boot to a QSPI device connected to QSPI0.

2.1.6 Clock options

This chip provides a wide range of sources to generate the internal clocks. These sources include internal resistor capacitor (IRC) oscillators, external oscillators, external clock sources, ceramic resonators, phase-locked loop (PLL) and frequency-locked loop (FLL). These sources can be configured to provide the required performance and optimize the power consumption.

The IRC oscillators include the 48 MHz internal resister capacitor (IRC48M) oscillator, the 4 MHz internal resister capacitor (4 MHz IRC) oscillator, the 32 kHz internal resister capacitor (32 kHz IRC) oscillator, and the low power oscillator (LPO).

The 48 MHz internal resister capacitor (IRC48M) oscillator generates a 48 MHz clock and synchronizes with the USB clock in full speed mode to achieve the required accuracy.

The 4 MHz internal resister capacitor (4 MHz IRC) oscillator generates a 4 MHz clock. It can serve as the low power, low speed system clock under very low power run (VLPR) mode or very low power wait (VLPW) mode. It can also be provided as clock source for other on-chip modules. The 4 MHz IRC cannot be used in any VLLS modes.

The 32 kHz internal resister capacitor (32 kHz IRC) oscillator generates a 32 kHz clock. It can be used as FLL internal reference clock or can be provided as low power clock source to other on-chip modules. The 32 kHz IRC cannot be used in any VLLS modes.

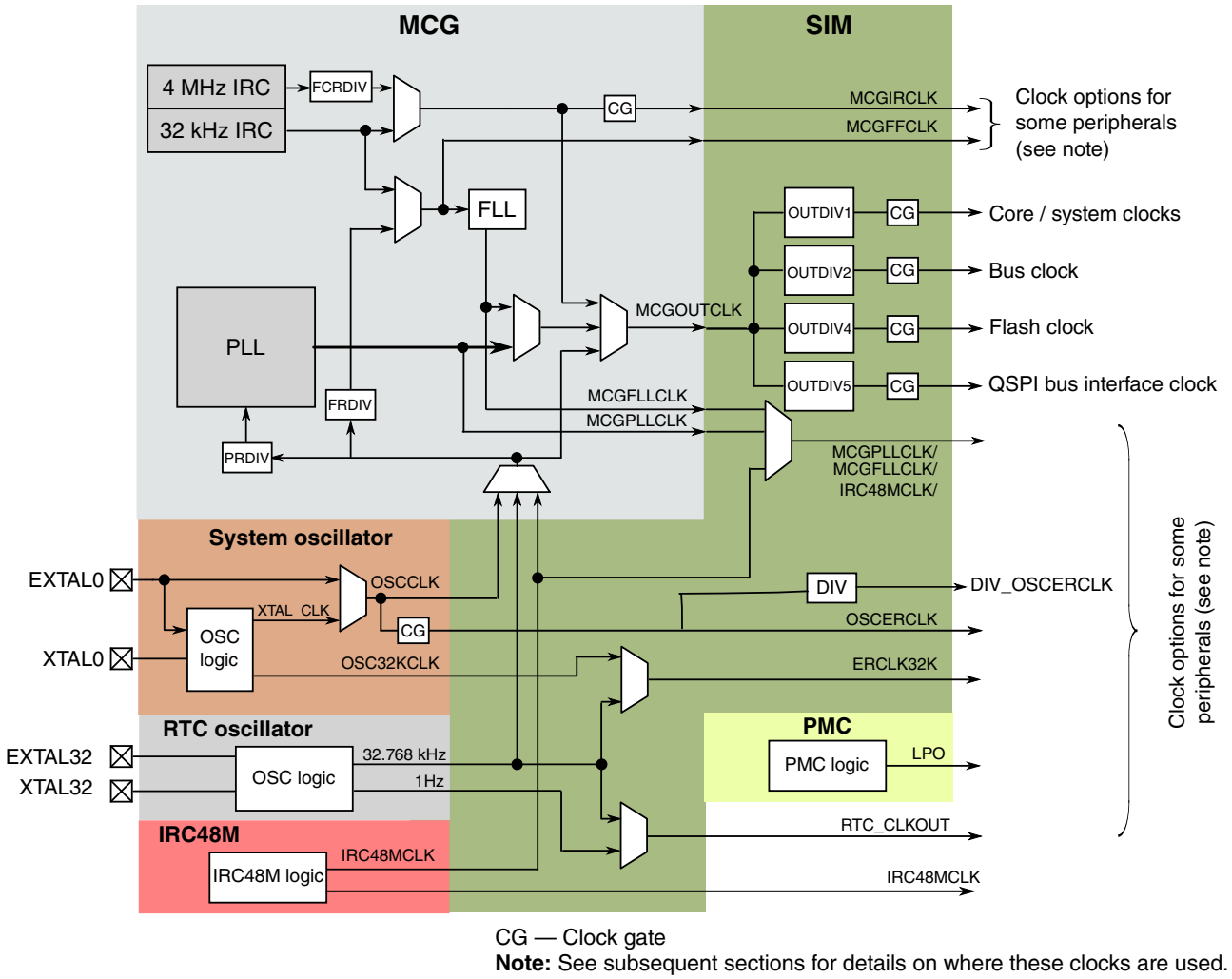
The LPO generates a 1 kHz clock and cannot be used in VLLS0 mode.

The system oscillator supports low frequency crystals (32 kHz to 40 kHz), high frequency crystals (1 MHz to 32 MHz), and ceramic resonators (1 MHz to 32 MHz). An external clock source, DC to 48 MHz, can be used as the system clock through the EXTAL0 pin. The external oscillator also supports a low speed external clock (32.768 kHz) on the RTC_CLKIN pin for use with the RTC.

The frequency-locked loop (FLL) can generate clock up to four programmable different frequency ranges (20–25 MHz, 40–50 MHz, 60–75 MHz or 80–100 MHz) with low speed (31.25–39.0625 kHz) internal or external reference clock. The FLL can be used as the system clock or clock source for other on-chip modules.

The phase-locked loop (PLL) can generate up to 144 MHz high speed, low jitter clock with 8–16 MHz internal or external reference clock. The PLL can be used as the system clock or clock source for other on-chip modules.

For more details on the clock operations and configurations, see Reference Manual.



CG — Clock gate
Note: See subsequent sections for details on where these clocks are used.

Figure 3. Clocking diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 4. Module clocks

Module	Bus interface clock	Internal clocks	I/O interface clocks
Core modules			
ARM Cortex-M0+ core	System clock	Core clock	—
NVIC	System clock	—	—
DAP	System clock	—	SWD_CLK
System modules			
DMA	System clock	—	—
DMAMUX	Bus clock	—	—
Port control	Bus clock	LPO	—
Crossbar Switch	System clock	—	—
Peripheral bridges	System clock	Bus clock	—
LLWU, PMC, SIM, RCM	Bus clock	LPO	—
Mode controller	Bus clock	—	—
INTMUX	Bus clock	—	—
MCM	System clock	—	—
EWM	Bus clock	LPO	—
Watchdog timer	Bus clock	LPO	—
Clocks			
MCG	Flash clock	MCGOUTCLK, MCGPLLCLK, MCGFLLCLK, MCGIRCLK, OSCERCLK	—
OSC	Bus clock	OSCERCLK	—
IRC48M	—	IRC48MCLK	—
Memory and memory interfaces			
Flash controller	System clock	Flash clock	—
Flash memory	Flash clock	—	—
QSPI controller	QSPI bus interface clock	QSPI clock	QSPIx_SCK
Security			
CRC	Bus clock	—	—
TRNG	Bus clock	—	—
LTC Encryption Engine	System clock	—	—
Analog			
ADC	Bus clock	OSCERCLK, IRC48MCLK	—
CMP	Bus clock	—	—
DAC	Bus clock	—	—
VREF	Flash clock	—	—
Timers			

Table continues on the next page...

Table 4. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
TPM	Bus clock	TPM clock	TPM_CLKIN0, TPM_CLKIN1
PDB	Bus clock	—	—
PIT	Bus clock	—	—
LPTMR	Bus clock	LPO, OSCERCLK, MCGIRCLK, ERCLK32K	—
RTC	Bus clock	EXTAL32	—
Communication interfaces			
USB FS OTG	System clock	USB FS clock	—
USB DCD	Bus clock	—	—
SPI	System clock	—	DSPI_SCK
I2C	Bus clock	—	I2C_SCL
LPUART	Bus clock	LPUART clock	—
EMVSIM	Bus clock	EMVSIM clock	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—
TSI	Bus clock	LPO, ERCLK32K, MCGIRCLK	—

2.1.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWD port	Cannot access memory source by SWD interface	The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command
ROM boot loader Interface (UART/I2C/SPI/USB)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key

This device features 128-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex User Guide.

The PMC provides High Speed Run (HSRUN), Run (Run), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLSx modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 6. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	High Speed Run	In HSRun mode, MCU is able to operate at a faster frequency, all device modules are operational.
	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, DAC, CMP, LPTimer, RTC, TPM, LPUART, TSI and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, TPM, FlexIO, LPUART, USB, TSI and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.
	Low Leakage Stop	In LLS mode, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), LLWU, LPTMR, and RTC are operational. The ADC, CRC, DMA, FlexIO, I2C, LPUART, MCG-Lite, NVIC, PIT, SPI, TPM, UART, USB, and WDOGCOP are static, but retain their programming. The DAC, GPIO, and VREF are static, retain their programming, and continue to drive their previous values.
	Very Low Leakage Stop	In VLLS modes, most peripherals are powered off and will resume operation from their reset state when the device wakes up. The LLWU, LPTMR, and RTC are operational in all VLLS modes. In VLLS3, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The DAC, GPIO, and VREF are not operational but continue driving. In VLLS1, the contents of the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The DAC, GPIO, and VREF are not operational but continue driving. In VLLS0, the contents of the 32-byte system register file are retained. The PMC is operational. The GPIO is not operational but continues driving. The POR detection circuit can be enabled or disabled.

2.1.9 LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

This device uses 25 external wakeup pin inputs and five internal modules as wakeup sources to the LLWU module.

The following is internal peripheral and external pin inputs as wakeup sources to the LLWU module.

Table 7. Wakeup sources for LLWU inputs

LLWU pins	Module sources or pin names
LLWU_P0	PTE1
LLWU_P1	PTE2
LLWU_P2	PTE4
LLWU_P3	PTA4
LLWU_P4	PTA13
LLWU_P5	PTB0
LLWU_P6	PTC1
LLWU_P7	PTC3
LLWU_P8	PTC4
LLWU_P9	PTC5
LLWU_P10	PTC6
LLWU_P11	PTC11
LLWU_P12	PTD0
LLWU_P13	PTD2
LLWU_P14	PTD4
LLWU_P15	PTD6
LLWU_P16	PTE6
LLWU_P17	PTE9
LLWU_P18	PTE10
LLWU_P19	Reserved
LLWU_P20	Reserved
LLWU_P21	Reserved
LLWU_P22	PTA10
LLWU_P23	PTA11
LLWU_P24	PTD8
LLWU_P25	PTD11
LLWU_P26	Reserved
LLWU_P27	USB0_DP
LLWU_P28	USB0_DM[1]
LLWU_P29	Reserved
LLWU_P30	Reserved
LLWU_P31	Reserved
LLWU_M0IF	LPTMR0 or LPTMR1[2]

Table continues on the next page...

Table 7. Wakeup sources for LLWU inputs (continued)

LLWU pins	Module sources or pin names
LLWU_M1IF	CMP0
LLWU_M2IF	Reserved
LLWU_M3IF	Reserved
LLWU_M4IF	TSI0[2]
LLWU_M5IF	RTC alarm
LLWU_M6IF	Reserved
LLWU_M7IF	RTC second

1. A wakeup source of LLWU, USB0_DP or USB0_DM is available only when the chip is in USB host mode.
2. Requires the peripheral and the peripheral interrupt to be enabled. The LLWU_ME[WUMEn] (n=0-7) bit enables the internal module flag a wakeup inputs. After wakeup, the flags are cleared based on the peripheral clearing mechanism.

2.1.10 Debug controller

This device supports standard ARM 2-pin SWD debug port. It provides register and memory accessibility from the external debugger interface, basic run/halt control plus 2 breakpoints and 2 watchpoints.

It also supports trace function with the Micro Trace Buffer (MTB), which provides a simple execution trace capability for the Cortex-M0+ processor.

2.1.11 INTMUX

The Interrupt Multiplexer (INTMUX) routes the interrupt sources to the interrupt outputs. It provides interrupt status registers to monitor interrupt pending status and vector numbers and implements the ability to logical AND or OR enabled interrupts on a given channel.

The INTMUX has the following features:

- Supports 4 multiplex channels
- Each channel receives 32 interrupt sources and has one interrupt output
- Each interrupt source can be enabled or disabled
- Each channel supports logic AND or logic OR of all enabled interrupt sources

2.1.12 Watch dog

The Watchdog Timer (WDOG) keeps a watch on the system functioning and resets it in case of its failure.

The WDOG has the following features:

- Clock source input independent from CPU/bus clock. Choice between low-power oscillator (LPO) and external system clock.
- Unlock sequence for allowing updates to write-once WDOG control/configuration bits.
- All WDOG control/configuration bits are writable once only within 256 bus clock cycles of being unlocked.
- Programmable time-out period specified in terms of number of WDOG clock cycles.
- Ability to test WDOG timer and reset with a flag indicating watchdog test.
- Windowed refresh option.
- Robust refresh mechanism.
- Count of WDOG resets as they occur.
- Configurable interrupt on time-out to provide debug breadcrumbs. This is followed by a reset after 256 bus clock cycles.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 BME

The Bit Manipulation Engine (BME) provides hardware support for atomic read-modify-write memory operations to the peripheral address space in Cortex-M0+ based microcontrollers. It reduces up to 30% of the code size and up to 9% of the cycles for bit-oriented operations to peripheral registers.

The BME supports unsigned bit field extract, load-and-set 1-bit, load-and-clear 1-bit, bit field insert, logical AND/OR/XOR operations with byte, halfword or word-sized data type.

2.2.2 eDMA and DMAMUX

The eDMA controller module enables fast transfers of data, which provides an efficient way to move blocks of data with minimal processor interaction. The eDMA controller in this device implements eight channels which can be routed from up to 63 DMA request sources through DMA MUX module. Some of the peripheral request sources have asynchronous eDMA capability which can be used to wake MCU from Stop mode. The peripherals which have such capability include FlexIO, LPUART0, LPUART1, LPUART2, TPM0, TPM1, TPM2, PORTA-PORTE, ADC0, and CMP0. The DMA channel 0 t0 3 can be periodically triggered by PIT via DMA MUX.

Main features are listed below:

- Dual-address transfers via 32-bit master connection to the system bus and data transfers in 8-, 16-, or 32-bit blocks
- 8-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Provide the selectable channel activation methods.
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

2.2.3 TPM

This device contains three low power TPM modules (TPM). All TPM modules are functional in Stop/VLPS mode if the clock source is enabled.

The TPM features include:

- TPM clock mode is selectable from external clock input or internal clock source, HIRC48M clock, external crystal input clock, MCGIRCLK, MCGPLLCLK, or MCGFLLCLK.
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter
- Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel or counter overflow

- Support selectable trigger input to optionally reset or cause the counter to start or stop incrementing
- Support the generation of hardware triggers when the counter overflows and per channel

2.2.4 ADC

this device contains one ADC module. This ADC module supports hardware triggers from TPM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 17 single-ended external analog inputs
- Support selectable 16-bit, 13-bit, 11-bit, and 9-bit differential output mode, or 16-bit, 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Selectable clock source up to four
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function up to 32x
- Selectable voltage reference: external or alternate
- Self-Calibration mode

2.2.5 VREF

The Voltage Reference (VREF) can supply an accurate voltage output (1.2V typically) trimmed in 0.5 mV steps. It can be used in applications to provide a reference voltage to external devices or used internally as a reference to analog peripherals such as the ADC, DAC or CMP.

The VREF supports the following programmable buffer modes:

- Bandgap on only, used for stabilization and startup
- High power buffer mode
- Low-power buffer mode
- Buffer disabled

A 100 nF capacitor must always be connected between VERF output (VREFO) pin and VSSA if the VREF is used. This capacitor must be as close to VREFO pin as possible.

2.2.6 CMP

The device contains one high-speed comparator and two 8-input multiplexers for both the inverting and non-inverting inputs of the comparator. Each CMP input channel connects to both muxes.

The CMP includes one 6-bit DAC, which provides a selectable voltage reference for various user application cases. Besides, the CMP also has several module-to-module interconnects in order to facilitate ADC triggering, TPM triggering, and interfaces.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: shorter propagation delay at the expense of higher power and Low power with longer propagation delay
- DMA transfer support
- Functional in all modes of operation except in VLLS0 mode
- The window and filter functions are not available in Stop, VLPS, LLS, or VLLSx modes
- Integrated 6-bit DAC with selectable supply reference source and can be power down to conserve power
- Two 8-to-1 channel mux

2.2.7 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers. During chip power-down, RTC is powered from the backup power supply (VBAT), electrically isolated from the rest of the chip, continues to increment the time counter (if enabled) and retain the state of the RTC registers. The RTC registers are not accessible.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt
- 64-bit monotonic counter with roll-over protection

2.2.8 PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has four independent channels and each channel has a 32-bit counter. Two channels can be chained together to form a 64-bit counter.

The PIT module can trigger a DMA transfer on the first four DMA channels. and also can be selected as ADC, TPM, and DAC trigger source.

The PIT module has the following features:

- Each 32-bit timers is able to generate DMA trigger
- Each 32-bit timers is able to generate timeout interrupts
- Two timers can be cascaded to form a 64-bit timer
- Each timer can be programmed as ADC/TPM trigger source
- Timer 0 is able to trigger DAC

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.11 LPUART

This product contains three Low-Power UART modules, both of their clock sources are selectable fromIRC48M, MCGFLLCLK, MCGPLLCLK, MCGIRCCLK or external crystal clock, and can work in Stop and VLPS modes. They also support 4x to 32x data oversampling rate to meet different applications.

The LPUART module has the following features:

- Full-duplex, standard non-return-to-zero (NRZ) format

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods: idle line wakeup, address mark wakeup, receive data match
- Automatic address matching to reduce ISR overhead
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width

2.2.12 SPI

This device contains two SPI modules. SPI modules support 8-bit and 16-bit modes. FIFO function is available only on SPI1 module.

The SPI modules have the following features:

- Full-duplex or single-wire bidirectional mode
- Programmable transmit bit rate
- Double-buffered transmit and receive data register
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8- or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed/large amounts of data transfers
- Support DMA

2.2.13 I2C

This device contains two I2C modules, which support up to 1 Mbits/s by dual buffer features, and address match to wake MCU from the low power mode.

I2C modules support DMA transfer, and the interrupt condition can trigger DMA request when DMA function is enabled.

The I2C modules have the following features:

- Support for system management bus (SMBus) Specification, version 2
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection
- Acknowledge bit generation and detection
- Bus busy detection
- General call recognition
- 10-bit address extension
- Programmable input glitch filter
- Low power mode wakeup on slave address match
- Range slave address support
- DMA support
- Double buffering support to achieve higher baud rate

2.2.14 USB

This device contains one USB module which implements a USB2.0 full-speed compliant peripheral and interfaces to the on-chip USBFS transceiver. It implements keep-alive feature to avoid re-enumerating when exiting from low power modes and enables HIRC48M to allow crystal-less USB operation.

The USBFS has the following features:

- USB 1.1 and 2.0 compatible FS device controller
- 16 bidirectional endpoints
- DMA or FIFO data stream interfaces
- Low-power consumption

- IRC48M with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.
- Keep-alive feature is supported to power down system bus and CPU. USB can respond to IN with NAK and wake up for SETUP/OUT.

2.2.15 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to LPUART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation. It also supports to work in VLPR, VLPW, Stop, and VLPS modes when clock source remains enabled.

The FlexIO module has the following features:

- Array of 32-bit shift registers with transmit, receive and data match modes
- Double buffered shifter operation for continuous data transfer
- Shifter concatenation to support large transfer sizes
- Automatic start/stop bit generation
- 1, 2, 4, 8, 16 or 32 multi-bit shift widths for parallel interface support
- Interrupt, DMA or polled transmit/receive operation
- Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during stop modes
- Highly flexible 16-bit timers with support for a variety of internal or external trigger, reset, enable and disable conditions
- Programmable logic mode for integrating external digital logic functions on-chip or combining pin/shifter/timer functions to generate complex outputs
- Programmable state machine for offloading basic system control functions from CPU with support for up to 8 states, 8 outputs and 3 selectable inputs per state

2.2.16 DAC

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, OPAMPS or ADC.

DAC module has the following features:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 V_{in} to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input voltage.

- V_{in} can be selected from two reference sources
- Static operation in Normal Stop mode
- 16-word data buffer supported with configurable watermark and multiple operation modes
- DMA support

2.2.17 EMV-SIM

The EMV_SIM (Euro/Mastercard/Visa/SIM Serial Interface Module) is designed to facilitate communication to Smart Cards compatible to the EMV ver4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 Standard.

EMV-SIM module has the following features:

- Supports Smart Cards based on the EMV Standard v4.3 and ISO 7816-3 standard
- Independent clock for SIM logic (transmitter + receiver) and independent clock for register read-write interface
- 16 byte deep FIFO for transmitter and receiver
- Automatic NACK generation on parity error and receiver FIFO overflow error
- Support for both Inverse and Direct conventions
- Re-transmission of byte upon Smart Card NACK request with programmable threshold of re-transmissions
- Auto detection of Initial Character in receiver and setting of data format (inverse or direct)
- NACK detection in receiver
- Independent timers to measure character wait time, block wait time and block guard time
- Two general purpose counters available for use by software application with programmable clock selection for the counters
- DMA support available to transfer data to/from FIFOs. Programmable option available to select interrupt or DMA feature
- Programmable Prescaler to generate the desired frequency for Card Clock and Baud Rate Divisor to generate the internal ETU clocks for transmitter and receiver for any F/D ratio
- Deep sleep wake-up via Smart Card presence detect interrupt
- Manual control of all Smart Card interface signals

- Automatic power down of port logic on Smart Card presence detect
- Support for 8-bit LRC and 16-bit CRC generation for bytes sent out from transmitter and checking incoming message checksum for receiver

2.2.18 LTC

LP Trusted Cryptography (LTC) is a hardware accelerate module dedicate for the popular encryption algorithm.

LTC module has the following features:
- Cryptographic authentication
- Authenticated encryption algorithms
  - AES-CCM (counter with CBC-MAC)
  - AES-GCM (Galois counter mode)
- Symmetric key block ciphers
- Public key cryptography
- Secure Scan

2.2.19 TRNG

The Standalone True Random Number Generator (SA-TRNG) is hardware accelerator module that generates a 512-bit entropy as needed by an entropy consuming module or by other post processing functions.

2.2.20 TSI

The touch sensing input (TSI) module provides capacitive touch sensing detection with high sensitivity and enhanced robustness.

TSI module has the following features:
- Support up to 16 external electrodes
- Automatic detection of electrode capacitance across all operational power modes
- Internal reference oscillator for high-accuracy measurement
- Configurable software or hardware scan trigger
- Fully support NXP touch sensing software (TSS) library, see www.nxp.com/touchsensing.
- Capability to wake MCU from low power modes
- Compensate for temperature and supply voltage variations

- High sensitivity change with 16-bit resolution register
- Configurable up to 4096 scan times.
- Support DMA data transfer

2.2.21 QuadSPI

The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to one single or two external serial flash devices, each with up to eight bidirectional data lines. This device contains one QSPI module, which supports singles, dual, quad or octal data lines in single (SDR) or double (DDR) data rate configurations. The QuadSPI clock frequencies support up to 96 MHz in SDR mode and up to 72 MHz in DDR mode.

The QuadSPI has the following features:

- Flexible sequence engine to support various flash vendor devices.
- Single, dual, quad and octal modes of operation.
- DDR/DTR mode wherein the data is generated on every edge of the serial flash clock.
- Support for flash data strobe signal for data sampling in DDR and SDR mode.
- Support for parallel writes via register mapped interface in single I/O mode.
- Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
- DMA support to read RX Buffer data via AMBA AHB bus (64-bit width interface) or IP registers space (32-bit access) and DMA support to fill TX Buffer via IPS register space (32-bit access).
- Multimaster accesses with priority
- Multiple interrupt conditions
- Memory mapped read access to connected flash devices.
- Programmable sequence engine to cater to future command/protocol changes and able to support all existing vendor commands and operations.

3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. The following figure shows the system memory and peripheral locations

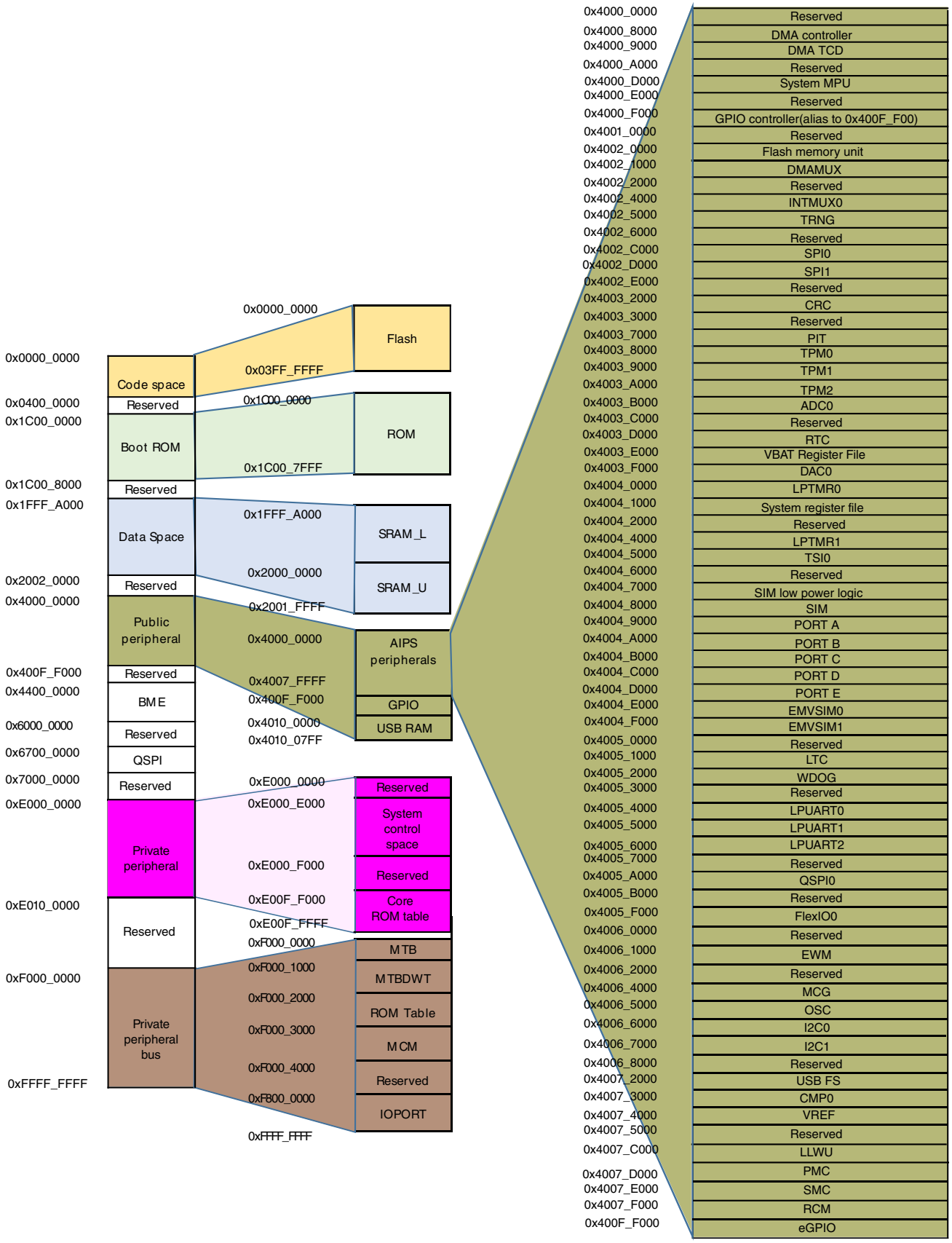


Figure 4. Memory map

4 Pinouts

4.1 KL82 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

121 MAP BGA	100 LQFP	80 LQFP	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
B1	1	1	A1	1	PTE0	DISABLED		PTE0	SPI1_PCS1	LPUART1_ TX		QSPI0A_ DATA3	I2C1_SDA	RTC_ CLKOUT
C2	2	2	B1	2	PTE1/ LLWU_P0	DISABLED		PTE1/ LLWU_P0	SPI1_SCK	LPUART1_ RX		QSPI0A_ SCLK	I2C1_SCL	SPI1_SIN
C1	3	3	C5	3	PTE2/ LLWU_P1	DISABLED		PTE2/ LLWU_P1	SPI1_SOUT	LPUART1_ CTS_b		QSPI0A_ DATA0		SPI1_SCK
D2	4	4	D2	4	PTE3	DISABLED		PTE3	SPI1_PCS2	LPUART1_ RTS_b		QSPI0A_ DATA2		SPI1_SOUT
F7	5	5	C4	5	VSS	VSS	VSS							
E5	6	6	D3	6	VDDIO_E	VDDIO_E	VDDIO_E							
D1	7	7	E2	7	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_SIN			QSPI0A_ DATA1		
E2	8	8	D1	8	PTE5	DISABLED		PTE5	SPI1_PCS0			QSPI0A_ SS0_B		USB0_ SOF_OUT
E1	9	—	—	—	PTE6/ LLWU_P16	DISABLED		PTE6/ LLWU_P16	SPI1_PCS3			QSPI0B_ DATA3		
F3	10	9	—	—	PTE7	DISABLED		PTE7				QSPI0B_ SCLK		QSPI0A_ SS1_B
F2	11	10	—	—	PTE8	DISABLED		PTE8				QSPI0B_ DATA0		
F1	12	—	—	—	PTE9/ LLWU_P17	DISABLED		PTE9/ LLWU_P17				QSPI0B_ DATA2		
G2	13	—	—	—	PTE10/ LLWU_P18	DISABLED		PTE10/ LLWU_P18				QSPI0B_ DATA1		
G1	14	11	—	—	PTE11	DISABLED		PTE11				QSPI0B_ SS0_B		QSPI0A_ DQS
—	15	12	—	—	VDDIO_E	VDDIO_E	VDDIO_E							
—	16	13	—	9	VSS	VSS	VSS							
H3	—	—	F3	—	VSS	VSS	VSS							
H2	17	14	E1	10	USB0_DP	USB0_DP	USB0_DP							
H1	18	15	F1	11	USB0_DM	USB0_DM	USB0_DM							

121 MAP BGA	100 LQFP	80 LQFP	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
J1	19	16	F2	12	USB_VDD	USB_VDD	USB_VDD							
J2	20	—	—	—	NC	NC	NC							
—	21	—	—	—	NC									
K2	—	—	—	—	ADC0_DP0	ADC0_DP0	ADC0_DP0							
K1	—	—	—	—	ADC0_DM0	ADC0_DM0	ADC0_DM0							
F5	22	17	G2	13	VDDA	VDDA	VDDA							
G5	23	18	H3	14	VREFH	VREFH	VREFH							
G6	24	19	H2	15	VREFL	VREFL	VREFL							
F6	25	20	G1	16	VSSA	VSSA	VSSA							
L2	26	21	H1	17	ADC0_DP1	ADC0_DP1	ADC0_DP1							
L1	27	22	G3	18	ADC0_DM1	ADC0_DM1	ADC0_DM1							
L3	28	23	F4	19	VREF_OUT/ CMP0_IN5/ ADC0_SE22	VREF_OUT/ CMP0_IN5/ ADC0_SE22	VREF_OUT/ CMP0_IN5/ ADC0_SE22							
K4	29	24	G4	20	DAC0_OUT/ ADC0_SE23	DAC0_OUT/ ADC0_SE23	DAC0_OUT/ ADC0_SE23							
H6	—	—	—	—	NC	NC	NC							
K5	30	25	F5	21	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B							
L4	31	26	H4	22	XTAL32	XTAL32	XTAL32							
L5	32	27	H5	23	EXTAL32	EXTAL32	EXTAL32							
K6	33	28	G5	24	VBAT	VBAT	VBAT							
—	34	—	—	—	VDD	VDD	VDD							
—	35	—	—	—	VSS	VSS	VSS							
L7	36	29	D4	25	PTA0	SWD_CLK	TSI0_CH1	PTA0	LPUART0_ CTS_b	TPM0_CH5		FXIO0_D10	EMVSIM0_ CLK	SWD_CLK
H8	37	30	D5	26	PTA1	TSI0_CH2	TSI0_CH2	PTA1	LPUART0_ RX			FXIO0_D11	EMVSIM0_ IO	
J7	38	31	E5	27	PTA2	TSI0_CH3	TSI0_CH3	PTA2	LPUART0_ TX			FXIO0_D12	EMVSIM0_ PD	
H9	39	32	H6	28	PTA3	SWD_DIO	TSI0_CH4	PTA3	LPUART0_ RTS_b	TPM0_CH0		FXIO0_D13	EMVSIM0_ RST	SWD_DIO
J8	40	33	G6	29	PTA4/ LLWU_P3	NMI_b	TSI0_CH5	PTA4/ LLWU_P3		TPM0_CH1		FXIO0_D14	EMVSIM0_ VCCEN	NMI_b
K7	41	—	—	—	PTA5	DISABLED		PTA5	USB0_ CLKIN	TPM0_CH2		FXIO0_D15		
L10	—	—	—	—	VDD	VDD	VDD							
K10	—	—	—	—	VSS	VSS	VSS							
J9	—	—	—	—	PTA10/ LLWU_P22	DISABLED		PTA10/ LLWU_P22		TPM2_CH0	EMVSIM1_ VCCEN	FXIO0_D16		
H7	—	—	—	—	PTA11/ LLWU_P23	DISABLED		PTA11/ LLWU_P23		TPM2_CH1		FXIO0_D17		

121 MAP BGA	100 LQFP	80 LQFP	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
K8	42	—	—	—	PTA12	DISABLED		PTA12		TPM1_CH0		FXIO0_D18		
L8	43	—	—	—	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		TPM1_CH1		FXIO0_D19		
K9	44	34	—	—	PTA14	DISABLED		PTA14	SPI0_PCS0	LPUART0_ TX		FXIO0_D20		
L9	45	35	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	LPUART0_ RX		FXIO0_D21		
J10	46	36	—	—	PTA16	DISABLED		PTA16	SPI0_SOUT	LPUART0_ CTS_b		FXIO0_D22		
H10	47	37	—	—	PTA17	DISABLED		PTA17	SPI0_SIN	LPUART0_ RTS_b		FXIO0_D23		
E6	48	38	H7	30	VDD	VDD	VDD							
G7	49	39	G7	31	VSS	VSS	VSS							
L11	50	40	H8	32	PTA18	EXTAL0	EXTAL0	PTA18			TPM_ CLKIN0			
K11	51	41	G8	33	PTA19	XTAL0	XTAL0	PTA19			TPM_ CLKIN1		LPTMR0_ ALT1/ LPTMR1_ ALT1	
J11	52	42	F8	34	RESET_b	RESET_b	RESET_b							
H11	—	—	—	—	PTA29	DISABLED		PTA29						
G11	53	43	E6	35	PTB0/ LLWU_P5	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				FXIO0_D0
G10	54	44	—	—	PTB1	ADC0_SE9/ TSI0_CH6	ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	TPM1_CH1				FXIO0_D1
G9	55	—	—	—	PTB2	ADC0_ SE12/ TSI0_CH7	ADC0_ SE12/ TSI0_CH7	PTB2	I2C0_SCL	LPUART0_ RTS_b				FXIO0_D2
G8	56	—	—	—	PTB3	ADC0_ SE13/ TSI0_CH8	ADC0_ SE13/ TSI0_CH8	PTB3	I2C0_SDA	LPUART0_ CTS_b				FXIO0_D3
B11	—	45	F7	36	PTB4	DISABLED		PTB4	EMVSIM1_ IO					
C11	—	46	F6	37	PTB5	DISABLED		PTB5	EMVSIM1_ CLK					
F11	—	47	E7	38	PTB6	DISABLED		PTB6	EMVSIM1_ VCCEN					
E11	—	48	E8	39	PTB7	DISABLED		PTB7	EMVSIM1_ PD					
D11	—	49	D7	40	PTB8	DISABLED		PTB8	EMVSIM1_ RST					
E10	57	—	—	—	PTB9	DISABLED		PTB9	SPI1_PCS1					
D10	58	—	—	—	PTB10	DISABLED		PTB10	SPI1_PCS0					FXIO0_D4
C10	59	50	—	—	PTB11	DISABLED		PTB11	SPI1_SCK					FXIO0_D5
L6	60	—	—	—	VSS	VSS	VSS							

121 MAP BGA	100 LQFP	80 LQFP	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E7	61	—	—	—	VDD	VDD	VDD							
B10	62	51	—	—	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	LPUART0_ RX	TPM_ CLKIN0		EWM_IN	
E9	63	52	—	—	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	LPUART0_ TX	TPM_ CLKIN1		EWM_OUT_ b	
D9	64	53	D6	41	PTB18	TSI0_CH11	TSI0_CH11	PTB18		TPM2_CH0				FXIO0_D6
C9	65	54	C7	42	PTB19	TSI0_CH12	TSI0_CH12	PTB19		TPM2_CH1				FXIO0_D7
F10	66	—	—	—	PTB20	DISABLED		PTB20					CMP0_OUT	FXIO0_D8
F9	67	—	—	—	PTB21	DISABLED		PTB21						FXIO0_D9
F8	68	—	—	—	PTB22	DISABLED		PTB22						FXIO0_D10
E8	69	—	—	—	PTB23	DISABLED		PTB23		SPI0_PCS5				FXIO0_D11
B9	70	55	D8	43	PTC0	ADC0_ SE14/ TSI0_CH13	ADC0_ SE14/ TSI0_CH13	PTC0	SPI0_PCS4	EXTRG_IN	USB0_ SOF_OUT			FXIO0_D12
D8	71	56	C6	44	PTC1/ LLWU_P6	ADC0_ SE15/ TSI0_CH14	ADC0_ SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	LPUART1_ RTS_b	TPM0_CH0			FXIO0_D13
C8	72	57	B7	45	PTC2	ADC0_ SE4b/ TSI0_CH15	ADC0_ SE4b/ TSI0_CH15	PTC2	SPI0_PCS2	LPUART1_ CTS_b	TPM0_CH1			
B8	73	58	C8	46	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7	SPI0_PCS1	LPUART1_ RX	TPM0_CH2	CLKOUT		
—	74	59	E3	47	VSS	VSS	VSS							
—	75	60	E4	48	VDD	VDD	VDD							
A8	76	61	B8	49	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	LPUART1_ TX	TPM0_CH3			
D7	77	62	A8	50	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2/ LPTMR1_ ALT2			CMP0_OUT	TPM0_CH2
C7	78	63	A7	51	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	EXTRG_IN				FXIO0_D14
B7	79	64	B6	52	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB0_ SOF_OUT				FXIO0_D15
A7	80	65	A6	53	PTC8	CMP0_IN2	CMP0_IN2	PTC8						FXIO0_D16
D6	81	66	B5	54	PTC9	CMP0_IN3	CMP0_IN3	PTC9						FXIO0_D17
C6	82	67	B4	55	PTC10	DISABLED		PTC10	I2C1_SCL					FXIO0_D18
C5	83	68	A5	56	PTC11/ LLWU_P11	DISABLED		PTC11/ LLWU_P11	I2C1_SDA					FXIO0_D19
B6	84	69	—	—	PTC12	DISABLED		PTC12			TPM_ CLKIN0			
A6	85	70	—	—	PTC13	DISABLED		PTC13			TPM_ CLKIN1			
A5	86	—	—	—	PTC14	DISABLED		PTC14						FXIO0_D20

121 MAP BGA	100 LQFP	80 LQFP	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
B5	87	—	—	—	PTC15	DISABLED		PTC15						FXIO0_D21
—	88	—	—	—	VSS	VSS	VSS							
—	89	—	—	—	VDD	VDD	VDD							
D5	—	71	—	—	PTC16	DISABLED		PTC16						
C4	90	72	—	—	PTC17	DISABLED		PTC17						
B4	—	—	—	—	PTC18	DISABLED		PTC18						
A4	—	—	—	—	PTC19	DISABLED		PTC19						
D4	91	73	C3	57	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	LPUART2_ RTS_b				FXIO0_D22
D3	92	74	A4	58	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	LPUART2_ CTS_b				FXIO0_D23
C3	93	75	C2	59	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	LPUART2_ RX				I2C0_SCL
B3	94	76	B3	60	PTD3	DISABLED		PTD3	SPI0_SIN	LPUART2_ TX				I2C0_SDA
A3	95	77	A3	61	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	LPUART0_ RTS_b	TPM0_CH4		EWM_IN	SPI1_PCS0
A2	96	78	C1	62	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	LPUART0_ CTS_b	TPM0_CH5		EWM_OUT_ b	SPI1_SCK
B2	97	79	B2	63	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	LPUART0_ RX				SPI1_SOUT
—	98	—	—	—	VSS	VSS	VSS							
—	99	—	—	—	VDD	VDD	VDD							
A1	100	80	A2	64	PTD7	DISABLED		PTD7		LPUART0_ TX				SPI1_SIN
A10	—	—	—	—	PTD8/ LLWU_P24	DISABLED		PTD8/ LLWU_P24	I2C0_SCL					FXIO0_D24
A9	—	—	—	—	PTD9	DISABLED		PTD9	I2C0_SDA					FXIO0_D25
E4	—	—	—	—	PTD10	DISABLED		PTD10						FXIO0_D26
E3	—	—	—	—	PTD11/ LLWU_P25	DISABLED		PTD11/ LLWU_P25						FXIO0_D27
F4	—	—	—	—	PTD12	DISABLED		PTD12						FXIO0_D28
G3	—	—	—	—	PTD13	DISABLED		PTD13						FXIO0_D29
G4	—	—	—	—	PTD14	DISABLED		PTD14						FXIO0_D30
H4	—	—	—	—	PTD15	DISABLED		PTD15						FXIO0_D31
A11	—	—	—	—	NC	NC	NC							
J6	—	—	—	—	NC	NC	NC							
J4	—	—	—	—	NC	NC	NC							
H5	—	—	—	—	NC	NC	NC							
J3	—	—	—	—	NC	NC	NC							
J5	—	—	—	—	NC	NC	NC							
K3	—	—	—	—	NC	NC	NC							

121 MAP BGA	100 LQFP	80 LQFP	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
121	100	80	64	64										

4.2 Pin properties

The following table lists the pin properties.

121 MAPBGA	100 LQFP	80 LQFP	64 LQFP	64 MAPBGA	Pin Name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
B1	1	1	1	A1	PTE0	ND	Hi-Z	—	FS	N	N	Y
C2	2	2	2	B1	PTE1/LLWU_P0	ND	Hi-Z	—	FS	N	N	Y
C1	3	3	3	C5	PTE2/LLWU_P1	ND	Hi-Z	—	FS	N	N	Y
D2	4	4	4	D2	PTE3	ND	Hi-Z	—	FS	N	N	Y
F7	5	5	5	C4	VFS	—	—	—	—	—	—	—
E5	6	6	6	D3	VDDIO_E	—	—	—	—	—	—	—
D1	7	7	7	E2	PTE4/LLWU_P2	ND	Hi-Z	—	FS	N	N	Y
E2	8	8	8	D1	PTE5	ND	Hi-Z	—	FS	N	N	Y
E1	9				PTE6/LLWU_P16	ND	Hi-Z	—	FS	N	N	Y
F3	10	9			PTE7	ND	Hi-Z	—	FS	N	N	Y
F2	11	10			PTE8	ND	Hi-Z	—	FS	N	N	Y
F1	12				PTE9/LLWU_P17	ND	Hi-Z	—	FS	N	N	Y
G2	13				PTE10/LLWU_P18	ND	Hi-Z	—	FS	N	N	Y
G1	14	11			PTE11	ND	Hi-Z	—	FS	N	N	Y
	15	12			VDDIO_E	—	—	—	—	—	—	—
	16	13	9		VFS	—	—	—	—	—	—	—
H3				F3	VFS	—	—	—	—	—	—	—
H2	17	14	10	E1	USB0_DP	—	—	—	—	—	—	—
H1	18	15	11	F1	USB0_DM	—	—	—	—	—	—	—
J1	19	16	12	F2	USB_VDD	—	—	—	—	—	—	—

Table continues on the next page...

121 MAPBGA	100 LQFP	80 LQFP	64 LQFP	64 MAPBGA	Pin Name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
J2	20				NC	—	—	—	—	—	—	—
	21				NC	—	—	—	—	—	—	—
K2					ADC0_DP0	ND	Hi-Z	—	FS	N	N	—
K1					ADC0_DM0	ND	Hi-Z	—	FS	N	N	—
F5	22	17	13	G2	VDDA	—	—	—	—	—	—	—
G5	23	18	14	H3	VREFH	—	—	—	—	—	—	—
G6	24	19	15	H2	VREFL	—	—	—	—	—	—	—
F6	25	20	16	G1	VFSA	—	—	—	—	—	—	—
L2	26	21	17	H1	ADC0_DP1	ND	Hi-Z	—	FS	N	N	—
L1	27	22	18	G3	ADC0_DM1	ND	Hi-Z	—	FS	N	N	—
L3	28	23	19	F4	VREF_OUT/ CMP0_IN5/ ADC0_SE22	ND	Hi-Z	—	FS	N	N	—
K4	29	24	20	G4	DAC0_OUT/ ADC0_SE23	ND	Hi-Z	—	FS	N	N	—
H6					NC	—	—	—	—	—	—	—
K5	30	25	21	F5	RTC_WAKEUP_B	ND	Hi-Z	—	FS	N	Y	—
L4	31	26	22	H4	XTAL32	ND	Hi-Z	—	FS	N	N	Y
L5	32	27	23	H5	EXTAL32	ND	Hi-Z	—	FS	N	N	Y
K6	33	28	24	G5	VBAT	—	—	—	—	—	—	—
	34				VDD	—	—	—	—	—	—	—
	35				VFS	—	—	—	—	—	—	—
L7	36	29	25	D4	PTA0	ND	L	PU	FS	N	N	Y
H8	37	30	26	D5	PTA1	ND	H	PU	FS	N	N	Y
J7	38	31	27	E5	PTA2	ND	H	PU	FS	N	N	Y
H9	39	32	28	H6	PTA3	ND	H	PU	FS	N	N	Y
J8	40	33	29	G6	PTA4/LLWU_P3	ND	H	PU	FS	Y	N	Y
K7	41				PTA5	ND	H	PU	FS	N	N	Y
L10					VDD	—	—	—	—	—	—	—
K10					VFS	—	—	—	—	—	—	—

Table continues on the next page...

121 MAPBGA	100 LQFP	80 LQFP	64 LQFP	64 MAPBGA	Pin Name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
J9					PTA10/LLWU_P22	ND	Hi-Z	—	FS	N	N	Y
H7					PTA11/LLWU_P23	ND	Hi-Z	—	FS	N	N	Y
K8	42				PTA12	ND	Hi-Z	—	FS	N	N	Y
L8	43				PTA13/LLWU_P4	ND	Hi-Z	—	FS	N	N	Y
K9	44	34			PTA14	ND	Hi-Z	—	FS	N	N	Y
L9	45	35			PTA15	ND	Hi-Z	—	FS	N	N	Y
J10	46	36			PTA16	ND	Hi-Z	—	FS	N	N	Y
H10	47	37			PTA17	ND	Hi-Z	—	FS	N	N	Y
E6	48	38	30	H7	VDD	—	—	—	—	—	—	—
G7	49	39	31	G7	VFS	—	—	—	—	—	—	—
L11	50	40	32	H8	PTA18	ND	Hi-Z	—	FS	N	N	Y
K11	51	41	33	G8	PTA19	ND	Hi-Z	—	FS	N	N	Y
J11	52	42	34	F8	RESET_b	ND	H	PU	FS	N	Y	N
H11					PTA29	ND	Hi-Z	—	FS	N	N	Y
G11	53	43	35	E6	PTB0/LLWU_P5	ND	Hi-Z	—	FS	N	N	Y
G10	54	44			PTB1	ND	Hi-Z	—	FS	N	N	Y
G9	55				PTB2	ND	Hi-Z	—	FS	N	N	Y
G8	56				PTB3	ND	Hi-Z	—	FS	N	N	Y
B11		45	36	F7	PTB4	ND	Hi-Z	—	FS	N	N	Y
C11		46	37	F6	PTB5	ND	Hi-Z	—	FS	N	N	Y
F11		47	38	E7	PTB6	ND	Hi-Z	—	FS	N	N	Y
E11		48	39	E8	PTB7	ND	Hi-Z	—	FS	N	N	Y
D11		49	40	D7	PTB8	ND	Hi-Z	—	FS	N	N	Y
E10	57				PTB9	ND	Hi-Z	—	FS	N	N	Y
D10	58				PTB10	ND	Hi-Z	—	FS	N	N	Y
C10	59	50			PTB11	ND	Hi-Z	—	FS	N	N	Y
L6	60				VFS	—	—	—	—	—	—	—
E7	61				VDD	—	—	—	—	—	—	—
B10	62	51			PTB16	ND	Hi-Z	—	FS	N	N	Y

Table continues on the next page...

121 MAPBGA	100 LQFP	80 LQFP	64 LQFP	64 MAPBGA	Pin Name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
E9	63	52			PTB17	ND	Hi-Z	—	FS	N	N	Y
D9	64	53	41	D6	PTB18	ND	Hi-Z	—	FS	N	N	Y
C9	65	54	42	C7	PTB19	ND	Hi-Z	—	FS	N	N	Y
F10	66				PTB20	ND	Hi-Z	—	FS	N	N	Y
F9	67				PTB21	ND	Hi-Z	—	FS	N	N	Y
F8	68				PTB22	ND	Hi-Z	—	FS	N	N	Y
E8	69				PTB23	ND	Hi-Z	—	FS	N	N	Y
B9	70	55	43	D8	PTC0	ND	Hi-Z	—	FS	N	N	Y
D8	71	56	44	C6	PTC1/LLWU_P6	ND	Hi-Z	—	FS	N	N	Y
C8	72	57	45	B7	PTC2	ND	Hi-Z	—	FS	N	N	Y
B8	73	58	46	C8	PTC3/LLWU_P7	ND	Hi-Z	—	FS	N	N	Y
	74	59	47	E3	VFS	—	—	—	—	—	—	—
	75	60	48	E4	VDD	—	—	—	—	—	—	—
A8	76	61	49	B8	PTC4/LLWU_P8	ND	Hi-Z	—	FS	N	N	Y
D7	77	62	50	A8	PTC5/LLWU_P9	ND	Hi-Z	—	FS	N	N	Y
C7	78	63	51	A7	PTC6/LLWU_P10	ND	Hi-Z	—	FS	N	N	Y
B7	79	64	52	B6	PTC7	ND	Hi-Z	—	FS	N	N	Y
A7	80	65	53	A6	PTC8	ND	Hi-Z	—	FS	N	N	Y
D6	81	66	54	B5	PTC9	ND	Hi-Z	—	FS	N	N	Y
C6	82	67	55	B4	PTC10	ND	Hi-Z	—	FS	N	N	Y
C5	83	68	56	A5	PTC11/LLWU_P11	ND	Hi-Z	—	FS	N	N	Y
B6	84	69			PTC12	ND	Hi-Z	—	FS	N	N	Y
A6	85	70			PTC13	ND	Hi-Z	—	FS	N	N	Y
A5	86				PTC14	ND	Hi-Z	—	FS	N	N	Y
B5	87				PTC15	ND	Hi-Z	—	FS	N	N	Y
	88				VFS	—	—	—	—	—	—	—
	89				VDD	—	—	—	—	—	—	—
D5		71			PTC16	ND	Hi-Z	—	FS	N	N	Y
C4	90	72			PTC17	ND	Hi-Z	—	FS	N	N	Y

Table continues on the next page...

121 MAPBGA	100 LQFP	80 LQFP	64 LQFP	64 MAPBGA	Pin Name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
B4					PTC18	ND	Hi-Z	—	FS	N	N	Y
A4					PTC19	ND	Hi-Z	—	FS	N	N	Y
D4	91	73	57	C3	PTD0/LLWU_P12	ND	Hi-Z	—	FS	N	N	Y
D3	92	74	58	A4	PTD1	ND	Hi-Z	—	FS	N	N	Y
C3	93	75	59	C2	PTD2/LLWU_P13	ND	Hi-Z	—	FS	N	N	Y
B3	94	76	60	B3	PTD3	ND	Hi-Z	—	FS	N	N	Y
A3	95	77	61	A3	PTD4/LLWU_P14	ND	Hi-Z	—	FS	N	N	Y
A2	96	78	62	C1	PTD5	ND	Hi-Z	—	FS	N	N	Y
B2	97	79	63	B2	PTD6/LLWU_P15	ND	Hi-Z	—	FS	N	N	Y
	98				VFS	—	—	—	—	—	—	—
	99				VDD	—	—	—	—	—	—	—
A1	100	80	64	A2	PTD7	ND	Hi-Z	—	FS	N	N	Y
A10					PTD8/LLWU_P24	ND	Hi-Z	—	FS	N	N	Y
A9					PTD9	ND	Hi-Z	—	FS	N	N	Y
E4					PTD10	ND	Hi-Z	—	FS	N	N	Y
E3					PTD11/LLWU_P25	ND	Hi-Z	—	FS	N	N	Y
F4					PTD12	ND	Hi-Z	—	FS	N	N	Y
G3					PTD13	ND	Hi-Z	—	FS	N	N	Y
G4					PTD14	ND	Hi-Z	—	FS	N	N	Y
H4					PTD15	ND	Hi-Z	—	FS	N	N	Y
A11					NC	—	—	—	—	—	—	—
J6					NC	—	—	—	—	—	—	—
J4					NC	—	—	—	—	—	—	—
H5					NC	—	—	—	—	—	—	—
J3					NC	—	—	—	—	—	—	—
J5					NC	—	—	—	—	—	—	—
K3					NC	—	—	—	—	—	—	—

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impendence
	H	High level
	L	Low level
Pullup/ pulldown setting after POR	PD	Pulldown
	PU	Pullup
Slew rate after POR	FS	Fast slew rate
	SS	Slow slew rate
Passive Pin Filter after POR	N	Disabled
	Y	Enabled
Open drain	N	Disabled[1]
	Y	Enabled[2]
Pin interrupt	Y	Yes

1. When I2C module is enabled and a pin is functional for I2C, this pin is (pseudo-) open drain enabled. When UART or LPUART module is enabled and a pin is functional for UART or LPUART, this pin is (pseudo-) open drain configurable.
2. PTA20 is a true open drain pin that must never be pulled above VDD.

4.3 Module signal description tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

4.3.1 Core Modules

Table 9. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_DIO	SWD_DIO	Serial Wire Data	I/O
SWD_CLK	SWD_CLK	Serial Wire Clock	I

4.3.2 System modules

Table 10. System signal descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt **NOTE:** Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin.	I
RESET_b	—	Reset bi-directional signal	I/O
VDD	—	MCU power	I
VDDIO_E	PTE	MCU power for IOs on PTE	I
VDDA	—	MCU analog power	I
VSS	—	MCU ground	I
VREFH	—	MCU analog voltage reference-high	I
VREFL	—	MCU analog voltage reference--low	I

Table 11. EWM signal descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_ b	$\overline{\text{EWM_out}}$	EWM reset out signal	O

Table 12. LLWU signal descriptions

Chip signal name	Module signal name	Description	I/O
LLWU_Pn	LLWU_Pn	Wakeup inputs	I

Table 13. EMVSIM0 signal descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM0_CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM0_IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O
EMVSIM0_PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I
EMVSIM0_RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM0_VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O

Table 14. EMVSIM1 signal descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM1_CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM1_IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O
EMVSIM1_PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I
EMVSIM1_RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM1_VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O

4.3.3 Clock Modules

Table 15. OSC signal descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL0	EXTAL	External clock/Oscillator input	I
XTAL0	XTAL	Oscillator output	O

Table 16. RTC OSC signal descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	Analog input of the RTC oscillator	I
XTAL32	XTAL32	Analog output of the RTC oscillator module	O

4.3.4 Memories and memory interfaces

Table 17. QSPI signal description

Chip signal name	Module signal Name	Description	I/O
QSPI0A_SS0_B	PCSFA1	Peripheral Chip Select Flash A1. This signal is the chip select for the serial flash device A1. A1 represents the first device in a dual-die package flash A or the first of the two flash devices that share IOFA.	O
QSPI0A_SS1_B	PCSFA2	Peripheral Chip Select Flash A2. This signal is the chip select for the serial flash device A2. A2 represents the	O

Table continues on the next page...

Table 17. QSPI signal description (continued)

Chip signal name	Module signal Name	Description	I/O
		second device in a dual-die package flash A or the second of the two flash devices that share IOFA.	
QSPI0B_SS0_B	PCSFB1	Peripheral Chip Select Flash B1. This signal is the chip select for the serial flash device B1. B1 represents the first device in a dual-die package flash B or the first of the two flash devices that share IOFB.	O
QSPI0A_SCLK	SCKFA	Serial Clock Flash A. This signal is the serial clock output to the serial flash device A.	O
QSPI0B_SCLK	SCKFB	Serial Clock Flash B. This signal is the serial clock output to the serial flash device B.	O
QSPI0B_DATA3 QSPI0B_DATA2 QSPI0B_DATA1 QSPI0B_DATA0 QSPI0A_DATA3 QSPI0A_DATA2 QSPI0A_DATA1 QSPI0A_DATA0	IOFA[7:0]	Serial I/O Flash A. These signals are the data I/O lines to/from the serial flash device A. Note that the signal pins of the serial flash device may change their function according to the SFM Command executed, leaving them as control inputs when Single and Dual Instructions are executed. The module supports driving these inputs to dedicated values.	I/O
QSPI0B_DATA3 QSPI0B_DATA2 QSPI0B_DATA1 QSPI0B_DATA0	IOFB[3:0]	Serial I/O Flash B. These signals are the data I/O lines to/from the serial flash device B. Note that the signal pins of the serial flash device may change their function according to the SFM Command executed, leaving them as control inputs when Single and Dual Instructions are executed. The module supports driving these inputs to dedicated values.	I/O
QSPI0A_DQS	DQSFA	Data Strobe signal Flash A. Data strobe signal for port A. Some flash vendors provide the DQS signal to which the read data is aligned in DDR mode.	I

4.3.5 Analog

Table 18. ADC0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC0_DP[1:0]	DADP1–DADP0	Differential analog channel inputs	I
ADC0_DM[1:0]	DADM1–DADM0	Differential Analog Channel Inputs	I
ADC0_SEn	ADn	Single-Ended Analog Channel Inputs[1]	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog power supply	I
VSSA	V_{SSA}	Analog ground	I

1. See ADC channel assignment for the n.

Table 19. CMP0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CMP0_INn, n=[5,3:0]	INn, n=[5,3:0]	Analog voltage inputs, see CMP input connection for more details about the n.	I
CMP0_OUT	CMPO	Comparator output	O

NOTE

There is no CMP0_IN[4] coming from pad.

Table 20. DAC0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
DAC0_OUT	—	DAC output	O

Table 21. VREF Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VREF_OUT	VREF_OUT	Internally-generated Voltage Reference output	O

4.3.6 Timer Modules

Table 22. LPTMR0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[2:1]	LPTMR_ALTn	Pulse Counter Input	I

Table 23. LPTMR1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR1_ALT[2:1]	LPTMR_ALTn	Pulse Counter Input	I

Table 24. RTC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VBAT	—	Backup battery supply for RTC and VBAT register file	I
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output or OSCERCLK	O
RTC_WAKEUP_B	$\overline{\text{RTC_WAKEUP}}$	Wakeup for external device	I/O

Table 25. TPM0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM0_CH[5:0]	TPM_CHn	A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 26. TPM1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM1_CH[1:0]	TPM_CHn	A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 27. TPM2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM1_CH[1:0]	TPM_CHn	A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

4.3.7 Communication interfaces

Table 28. USB FS OTG signal descriptions

Chip signal name	Module signal name	Description	I/O
USB0_DM	usb_dm	USB D- analog data signal on the USB bus.	I/O
USB0_DP	usb_dp	USB D+ analog data signal on the USB bus.	I/O
USB0_CLKIN	—	Alternate USB clock input	I
USB_VDD	—	USB domain power supply, 3.3 V.	I
USB0_SOF_OUT	—	USB start of frame signal. Can be used to make the USB start of frame available for external synchronization.	O

Table 29. SPI0 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_PCS0	PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O) in the master mode and Slave Select (I) in the slave mode	I/O
SPI0_PCS[1:3]	PCS[1:3]	Peripheral Chip Selects 1–3 in the master mode	O
SPI0_PCS4	PCS4	Peripheral Chip Select 4 in the master mode	O
SPI0_PCS5	PCS5	Peripheral Chip Select 5 /Peripheral Chip Select Strobe in the master mode	O
SPI0_SIN	SIN	Serial Data In	I
SPI0_SOUT	SOUT	Serial Data Out	O
SPI0_SCK	SCK	Serial Clock (O) in the master mode and Serial Clock (I) in the slave mode	I/O

Table 30. SPI1 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI1_PCS0	PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O) in the master mode and Slave Select (I) in the slave mode	I/O
SPI1_PCS[1:3]	PCS[1:3]	Peripheral Chip Selects 1–3 in the master mode	O
SPI1_SIN	SIN	Serial Data In	I
SPI1_SOUT	SOUT	Serial Data Out	O
SPI1_SCK	SCK	Serial Clock (O) in the master mode and Serial Clock (I) in the slave mode	I/O

Table 31. I2C0 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C0_SCL	SCL	Bidirectional serial clock line of the I2C system.	I/O
I2C0_SDA	SDA	Bidirectional serial data line of the I2C system.	I/O

Table 32. I2C1 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C1_SCL	SCL	Bidirectional serial clock line of the I2C system.	I/O
I2C1_SDA	SDA	Bidirectional serial data line of the I2C system.	I/O

Table 33. LPUART0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART0_CTS_b	LPUART_CTS	Clear to Send	I
LPUART0_RTS_b	LPUART_RTS	Request to send	O
LPUART0_TX	LPUART_TX	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART0_RX	LPUART_RX	Receive Data	I

Table 34. LPUART1 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART1_CTS_b	LPUART_CTS	Clear to Send	I
LPUART1_RTS_b	LPUART_RTS	Request to send	O

Table continues on the next page...

Table 34. LPUART1 signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
LPUART1_TX	LPUART_TX	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART1_RX	LPUART_RX	Receive Data	I

Table 35. LPUART2 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART2_CTS_b	LPUART_CTS	Clear to Send	I
LPUART2_RTS_b	LPUART_RTS	Request to send	O
LPUART2_TX	LPUART_TX	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART2_RX	LPUART_RX	Receive Data	I

Table 36. FlexIO signal descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dn(n=0-31)	FXIO_Dn (n=0...31)	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

Table 37. EMVSIM0 signal descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM0_ CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM0_ IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O
EMVSIM0_ PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I
EMVSIM0_ RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM0_ VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O

Table 38. EMVSIM1 signal descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM1_ CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM1_ IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O

Table continues on the next page...

Table 38. EMVSIM1 signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
EMVSIM1_ PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I
EMVSIM1_ RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM1_ VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O

4.3.8 Human-machine interfaces (HMI)

Table 39. GPIO signal descriptions

Chip signal name	Module signal name	Description	I/O
PTA[31:0][1]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0][1]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[31:0][1]	PORTC31–PORTC0	General-purpose input/output	I/O
PTD[31:0][1]	PORTD31–PORTD0	General-purpose input/output	I/O
PTE[31:0][1]	PORTE31–PORTE0	General-purpose input/output	I/O

1. The available GPIO pins depends on the specific package. See the signal multiplexing section for which exact GPIO signals are available.

Table 40. TSI0 signal descriptions

Chip signal name	Module signal name	Description	I/O
TSI0_CH[15:0]	TSI[15:0]	TSI capacitive pins. Switches driver that connects directly to the electrode pins TSI[15:0] can operate as GPIO pins.	I/O

4.4 KL82 Pinouts

The below figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	PTD9	PTD8/ LLWU_P24	NC	A
B	PTE0	PTD6/ LLWU_P15	PTD3	PTC18	PTC15	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	PTB4	B
C	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	PTB5	C
D	PTE4/ LLWU_P2	PTE3	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	PTE6/ LLWU_P16	PTE5	PTD11/ LLWU_P25	PTD10	VDDIO_E	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	PTE9/ LLWU_P17	PTE8	PTE7	PTD12	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	PTB6	F
G	PTE11	PTE10/ LLWU_P18	PTD13	PTD14	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	USB0_DM	USB0_DP	VSS	PTD15	NC	NC	PTA11/ LLWU_P23	PTA1	PTA3	PTA17	PTA29	H
J	USB_VDD	NC	NC	NC	NC	NC	PTA2	PTA4/ LLWU_P3	PTA10/ LLWU_P22	PTA16	RESET_b	J
K	ADC0_DM0	ADC0_DP0	NC	DAC0_OUT/ ADC0_SE23	RTC_WAK EUP_B	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	ADC0_DM1	ADC0_DP1	VREF_OUT/ CMP0_IN5/ ADC0_SE22	XTAL32	EXTAL32	VSS	PTA0	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 5. KL82 121-pin MAPBGA pinout diagram

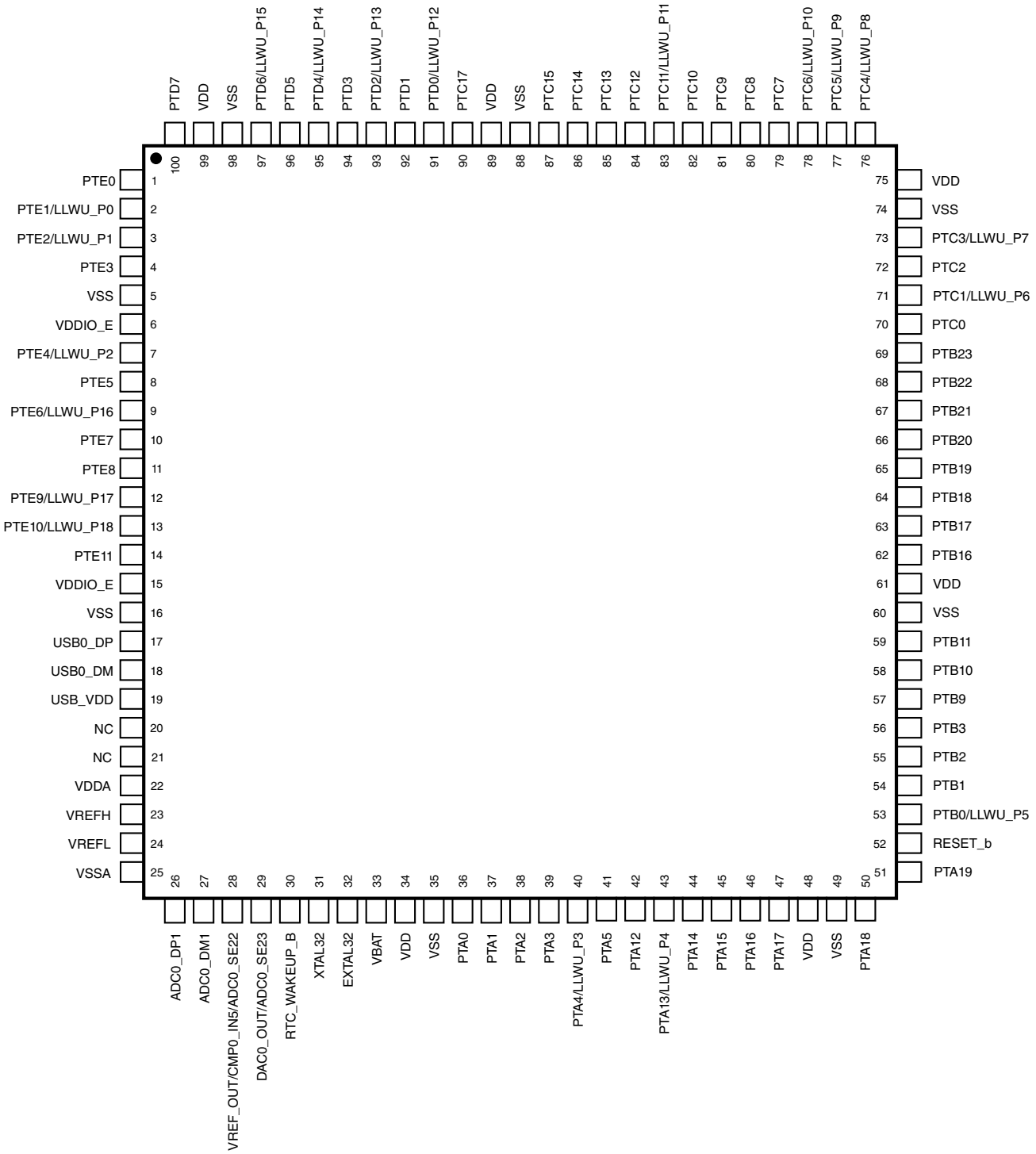


Figure 6. KL82 100-pin LQFP pinout diagram

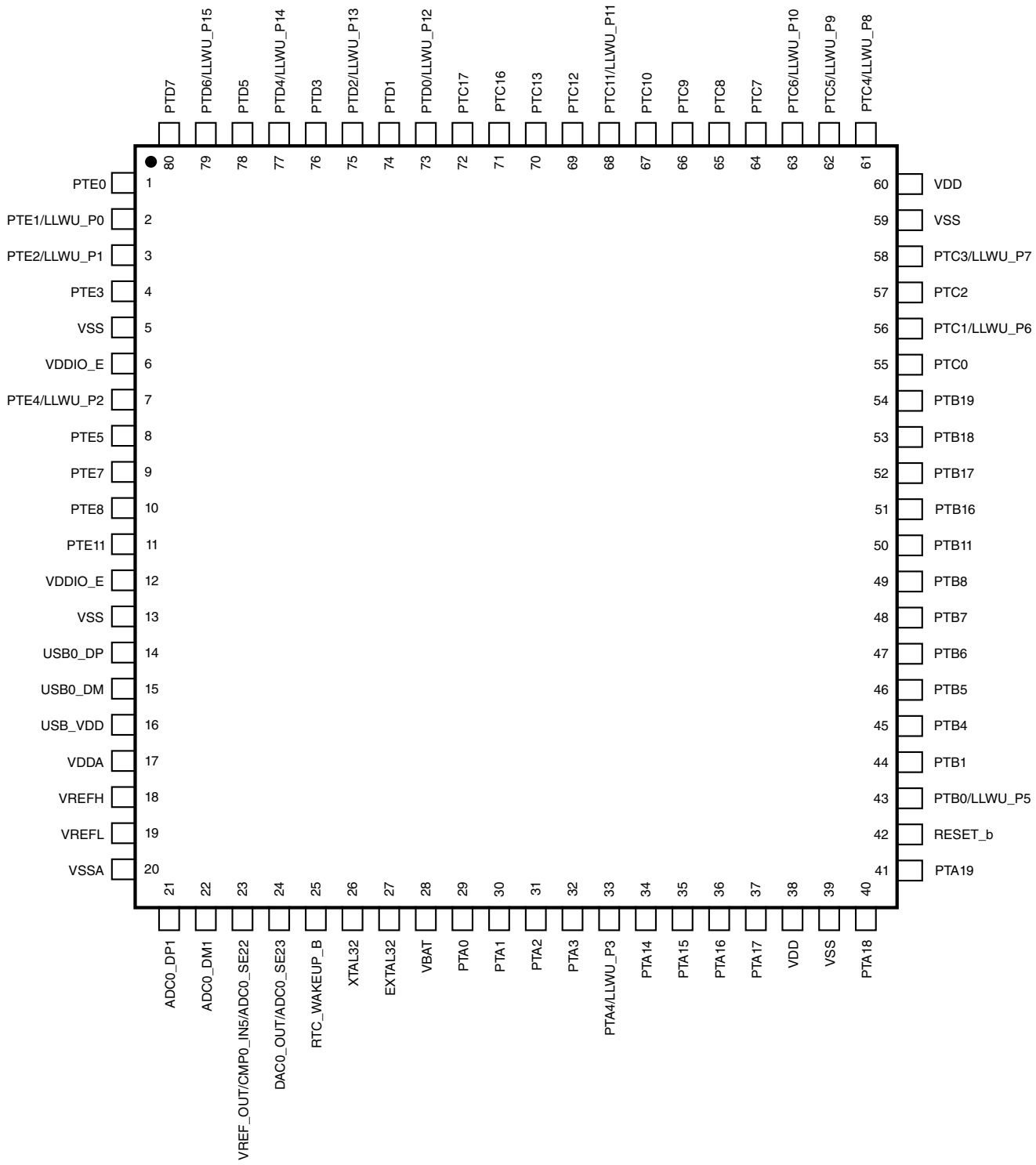


Figure 7. KL82 80-pin LQFP pinout diagram

	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	PTC11/ LLWU_P11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1/ LLWU_P0	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2/ LLWU_P13	PTD0/ LLWU_P12	VSS	PTE2/ LLWU_P1	PTC1/ LLWU_P6	PTB19	PTC3/ LLWU_P7	C
D	PTE5	PTE3	VDDIO_E	PTA0	PTA1	PTB18	PTB8	PTC0	D
E	USB0_DP	PTE4/ LLWU_P2	VSS	VDD	PTA2	PTB0/ LLWU_P5	PTB6	PTB7	E
F	USB0_DM	USB_VDD	VSS	VREF_OUT/ CMP0_IN5/ ADC0_SE22	RTC_WAK EUP_B	PTB5	PTB4	RESET_b	F
G	VSSA	VDDA	ADC0_DM1	DAC0_OUT/ ADC0_SE23	VBAT	PTA4/ LLWU_P3	VSS	PTA19	G
H	ADC0_DP1	VREFL	VREFH	XTAL32	EXTAL32	PTA3	VDD	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 8. KL82 64-pin MAPBGA pinout diagram

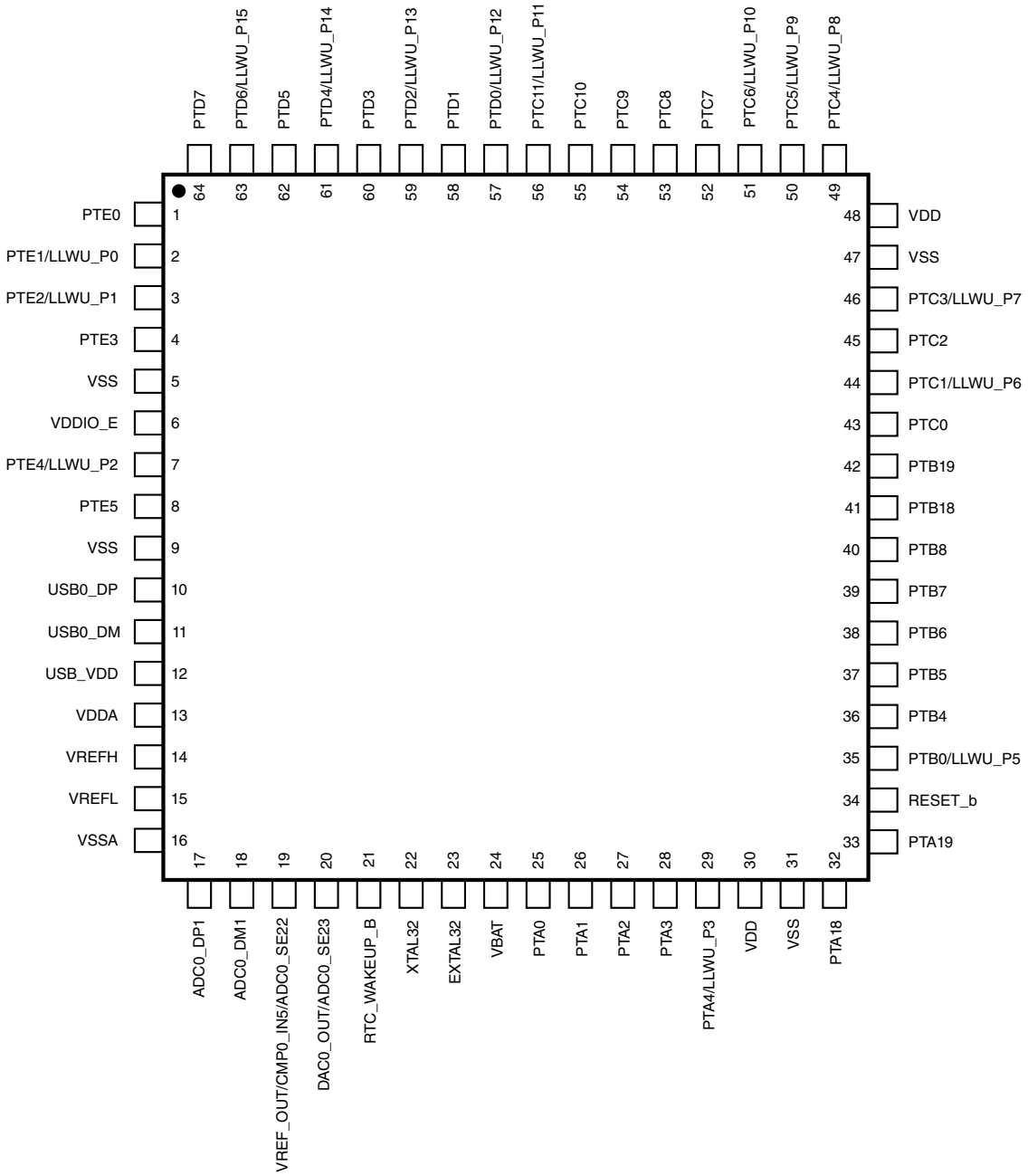


Figure 9. KL82 64-pin LQFP pinout diagram

NOTE

The 100-, 64-pin LQFP and 64-pin MAPBGA packages for this product are not yet available, however they are included in a Package Your Way program for KL MCUs. Please visit nxp.com/KPYW for more details.

4.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.

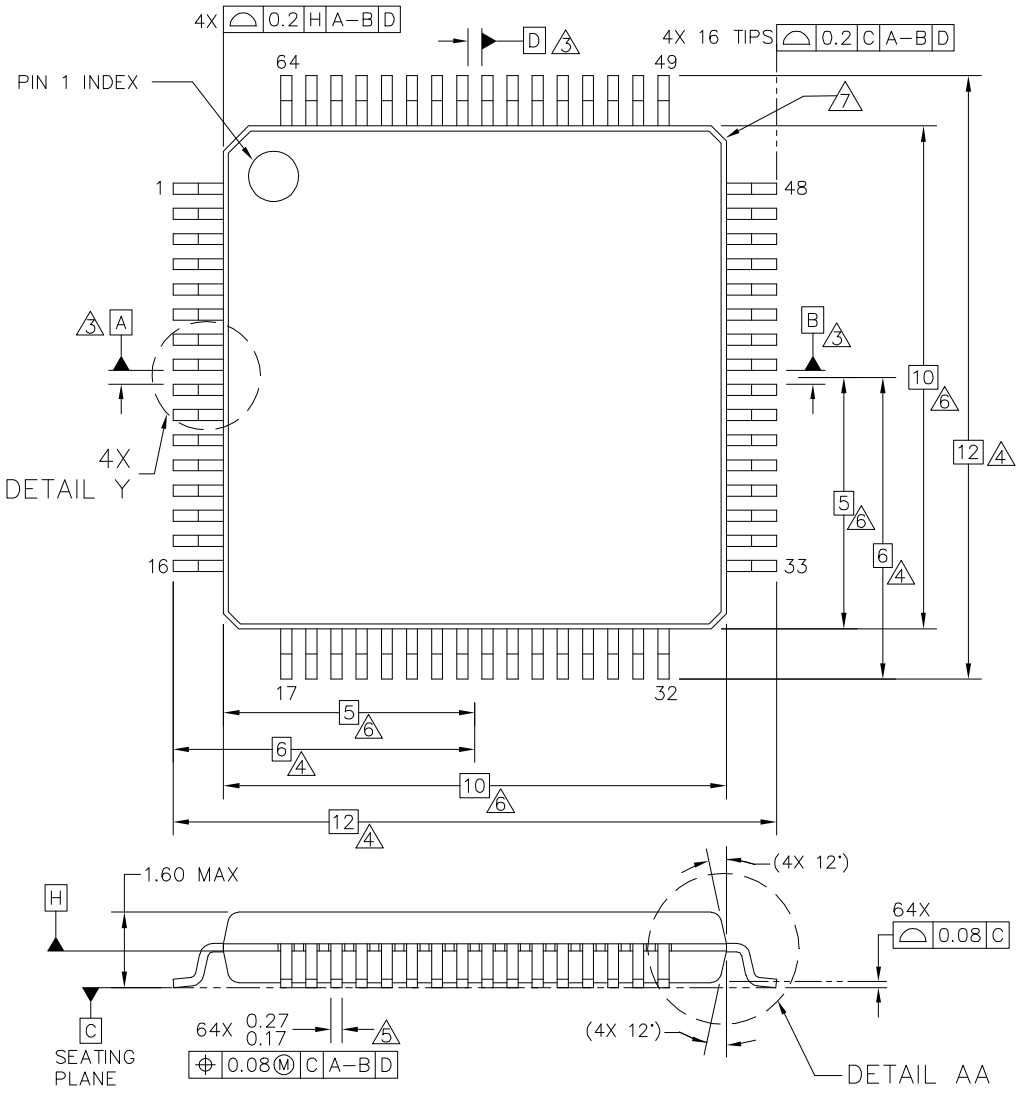
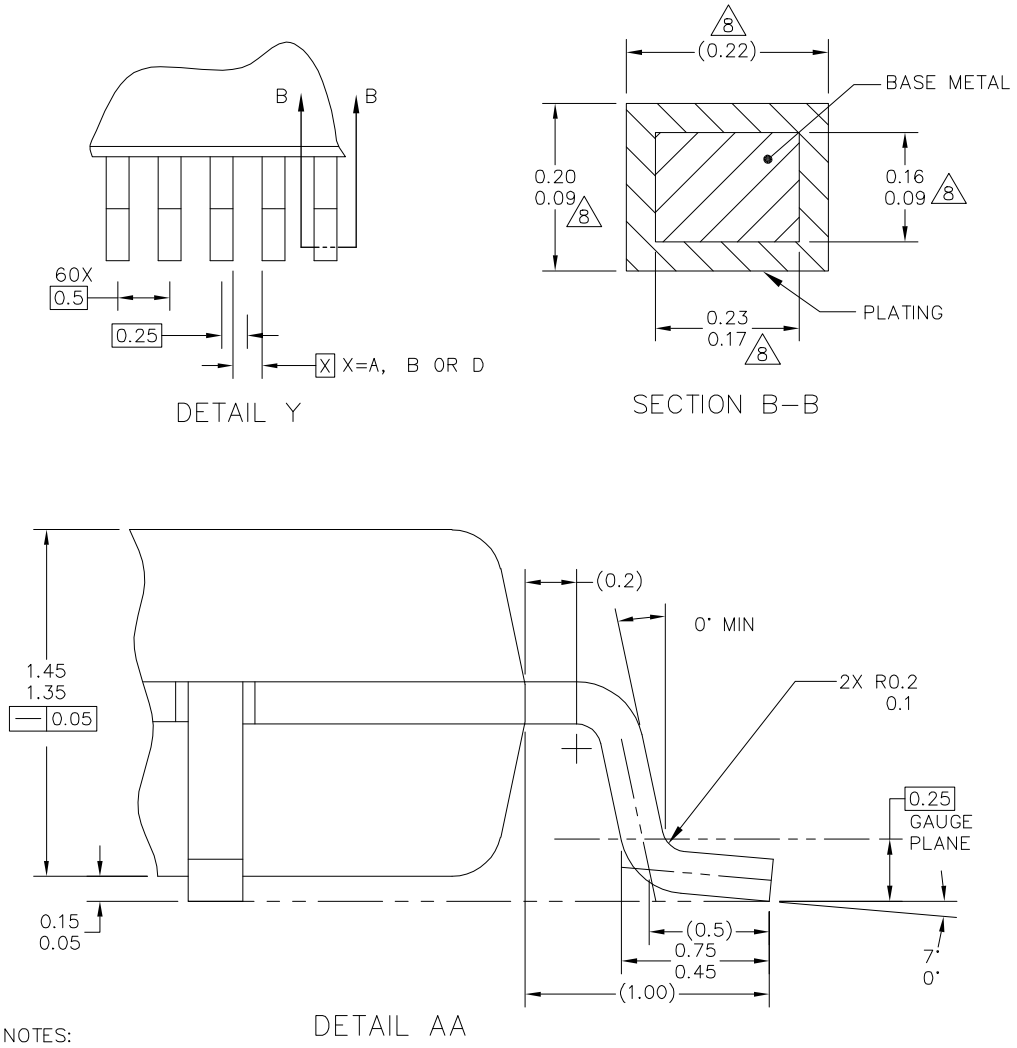


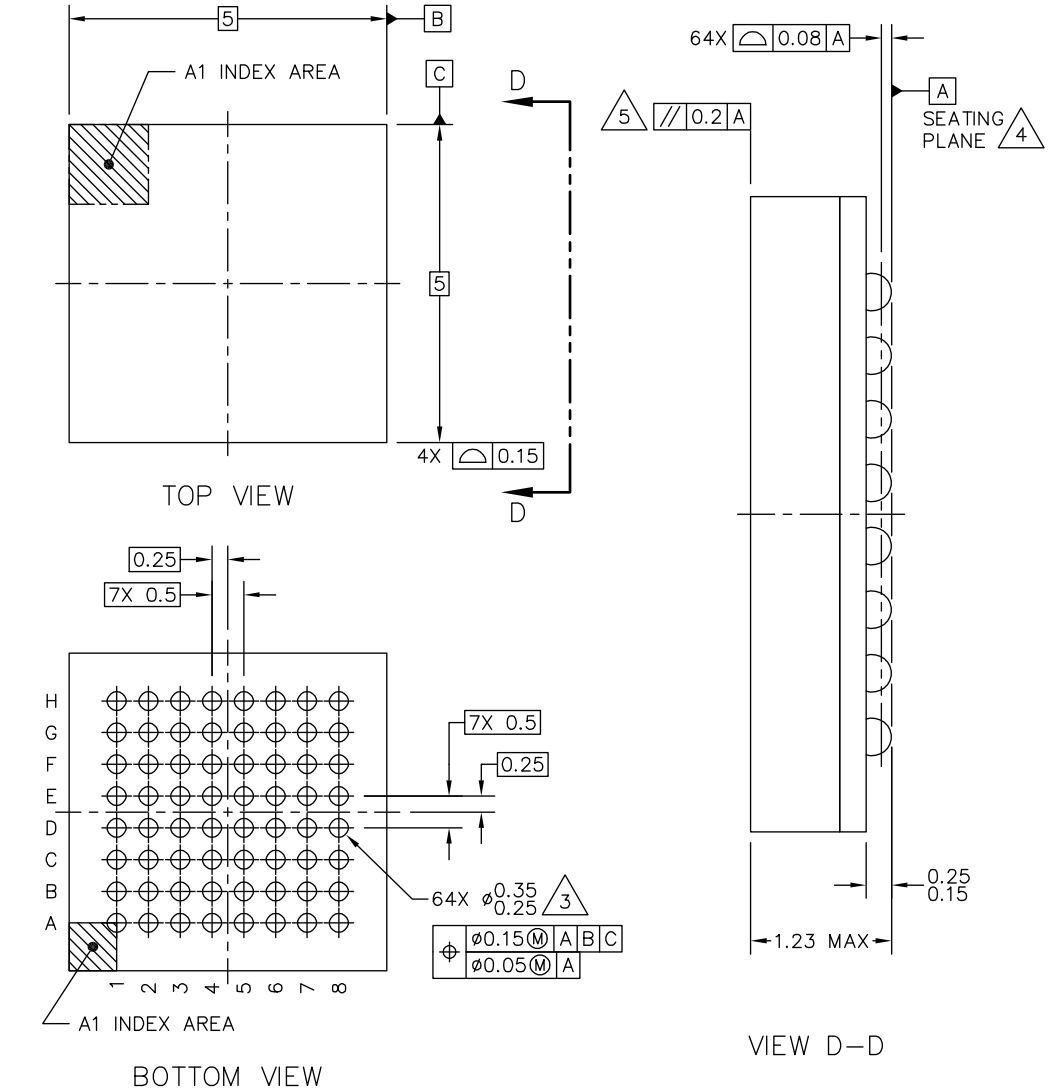
Figure 10. 64-pin LQFP package dimensions 1



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 11. 64-pin LQFP package dimensions 2



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 12. 64-pin MAPBGA package dimension

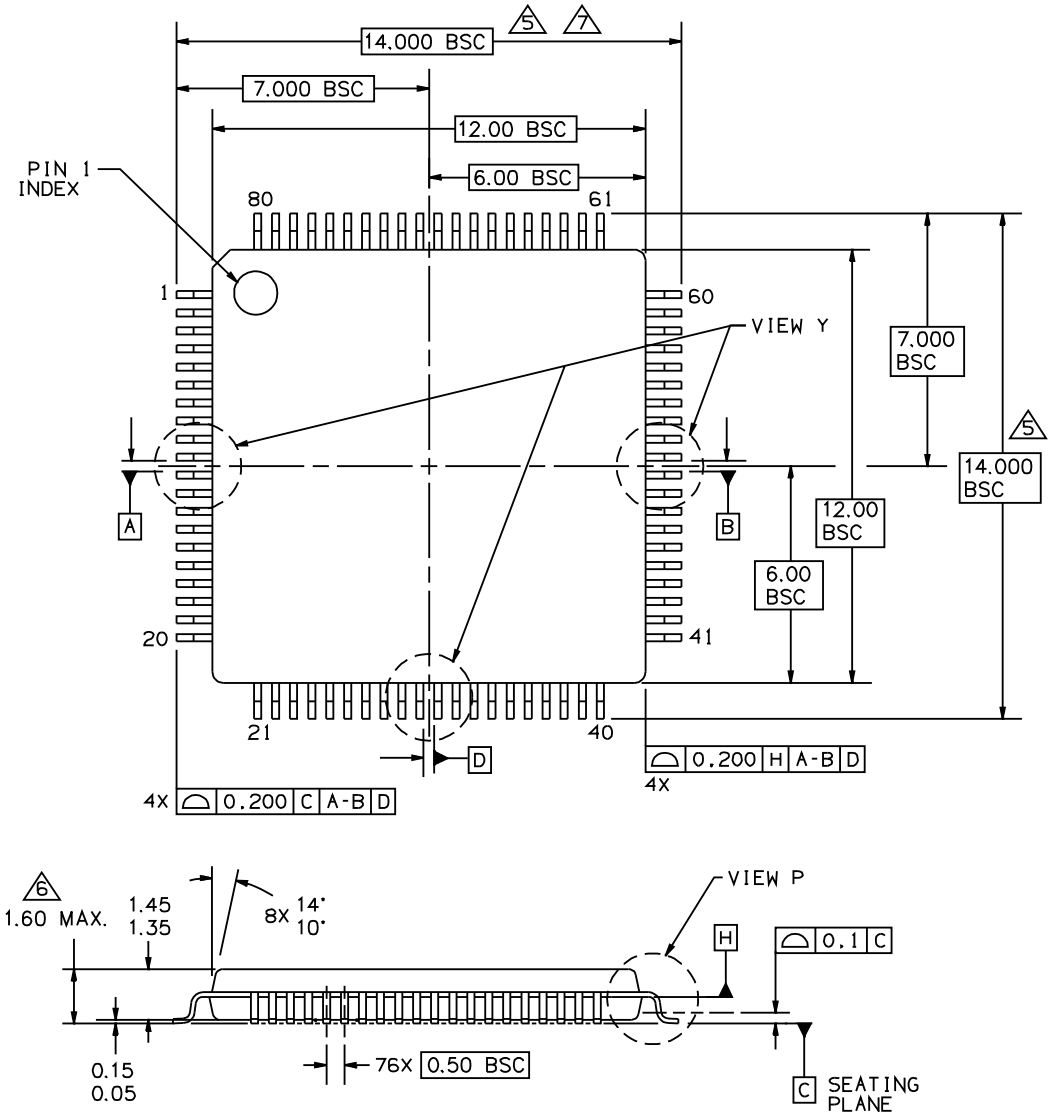
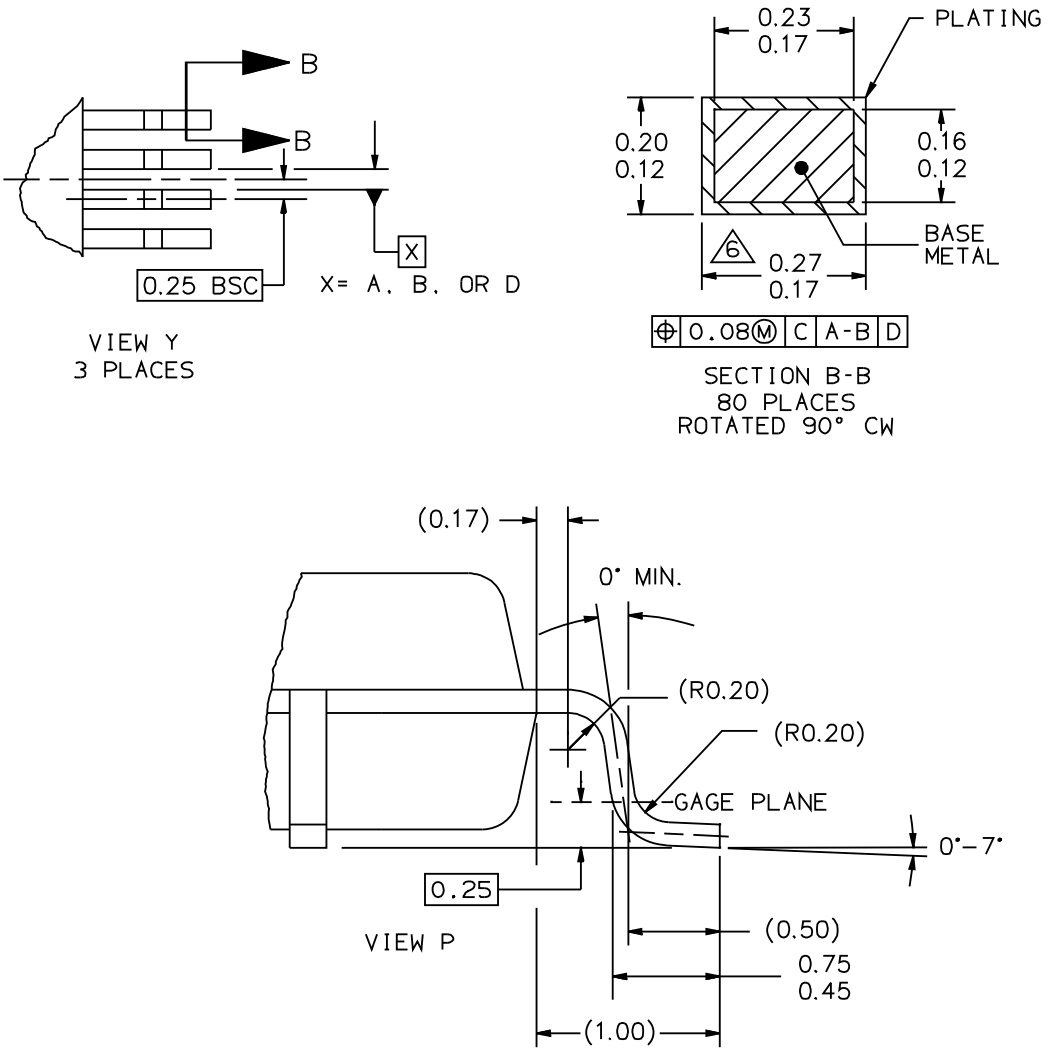


Figure 13. 80-pin LQFP package dimension 1



NOTES
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

2. CONTROLLING DIMENSIONS: MILLIMETER.

3. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35.

Figure 14. 80-pin LQFP package dimension 2

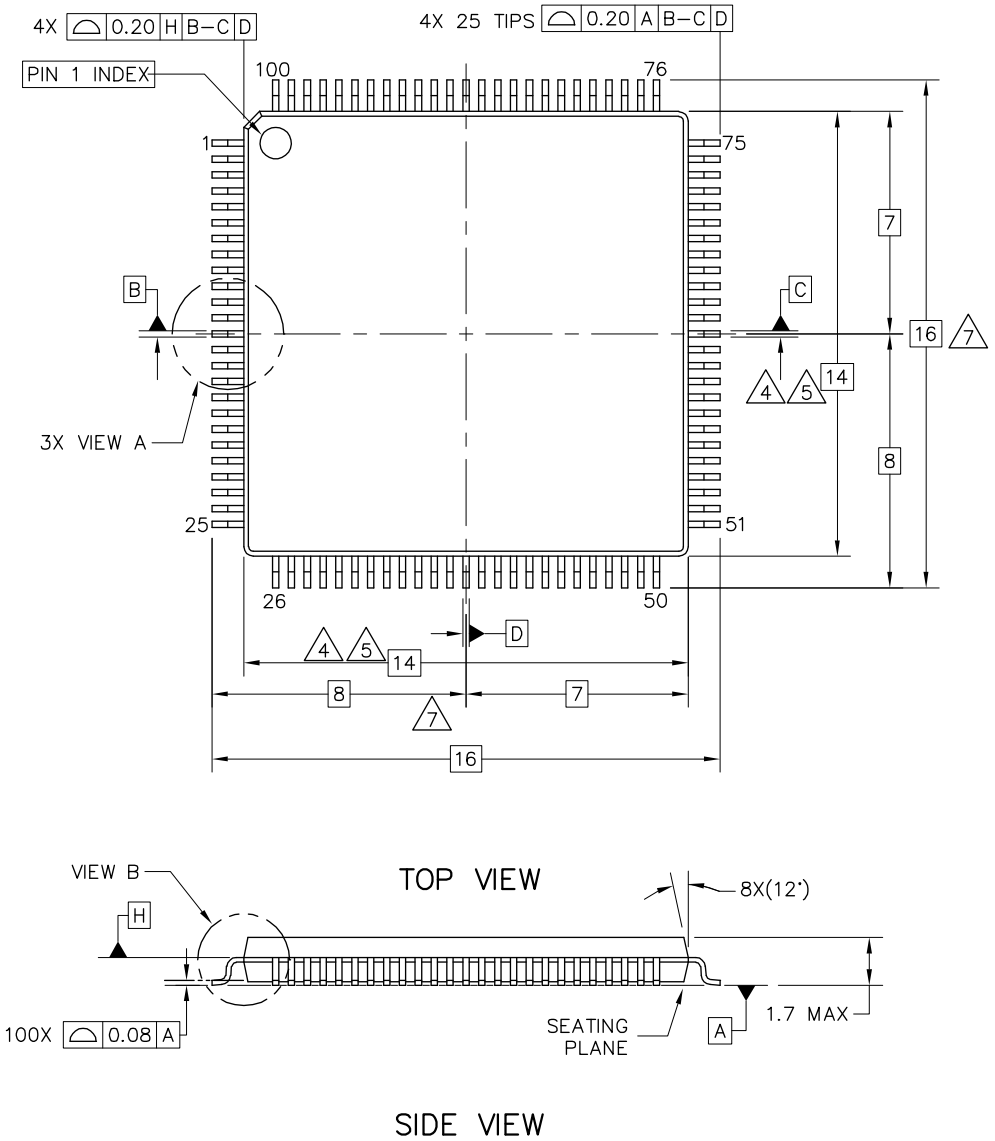
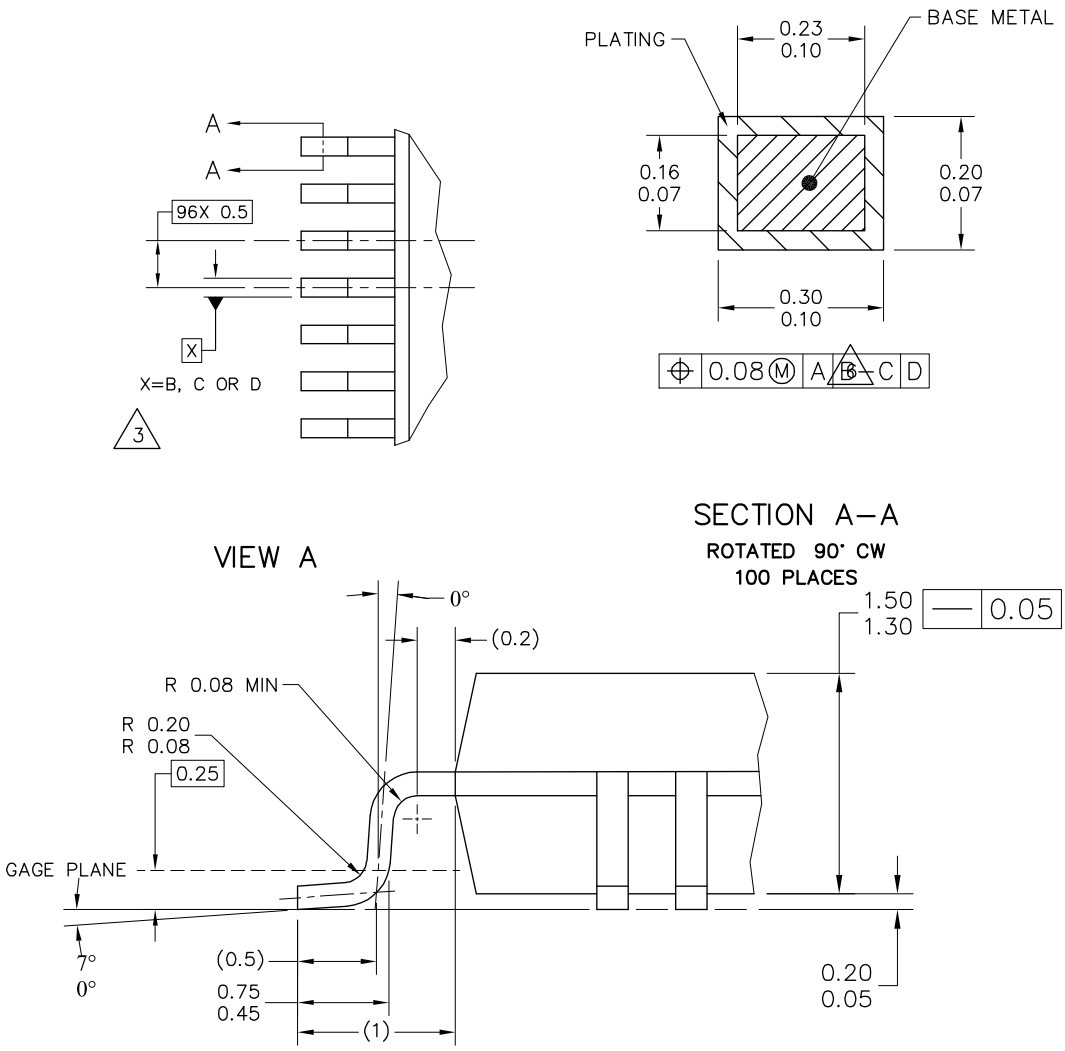


Figure 15. 100-pin LQFP package dimension 1



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

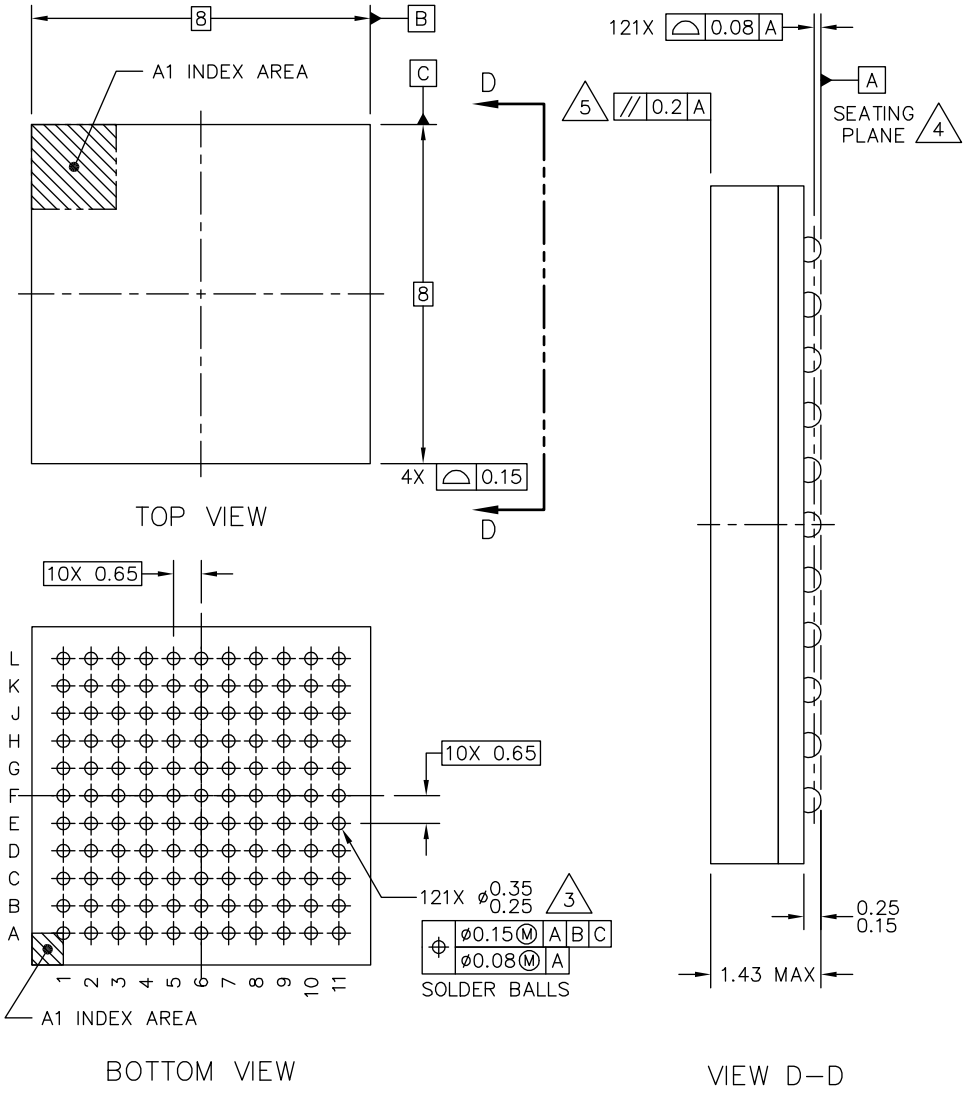
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.

5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 16. 100-pin LQFP package dimension 2



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 17. 121-pin MAPBGA package dimension

5 Electrical characteristics

5.1 Terminology and guidelines

5.1.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

5.1.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

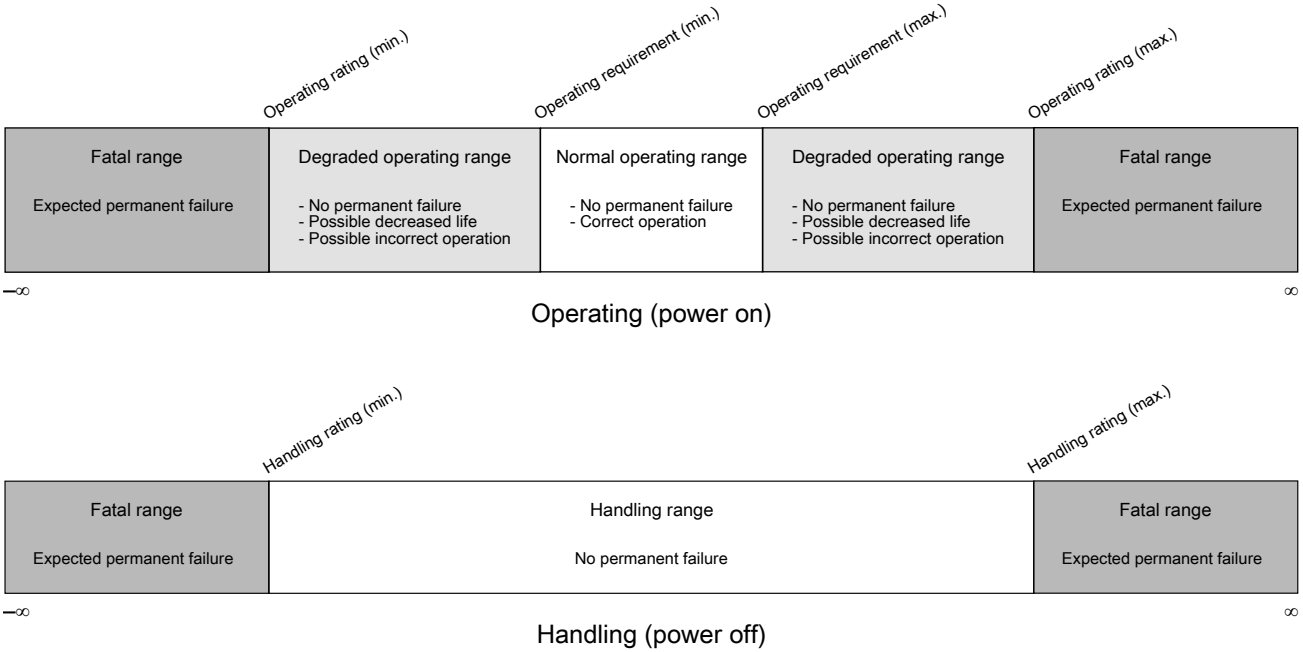
EXAMPLE

5.1.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

5.1.4 Relationship between ratings and operating requirements



5.1.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.2 Ratings

5.2.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.2.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage [1]	–0.3	3.8	V
V_{DDIO}	V_{DDIO} is an independent voltage supply for PORTE [2]	–0.3	3.8	V
I_{DD}	Digital supply current	—	300	mA
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[3], $\overline{RESET}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

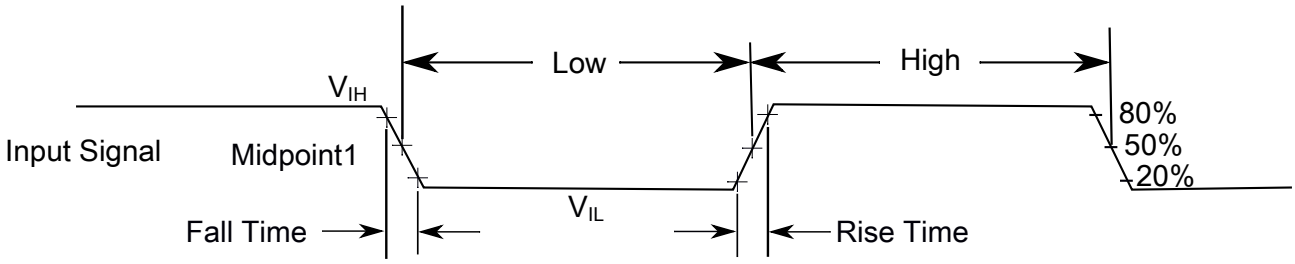
1. It applies for all port pins.
2. V_{DDIO} is independent of V_{DD} domain and can operate at a voltage independent of V_{DD}. However, it is required that V_{DD} domain be powered up first prior to V_{DDIO}. V_{DDIO} must never be higher than V_{DD} during power ramp up, or power down. V_{DD} and V_{DDIO} may ramp together if tied to the same power supply.

3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5.3 General

5.3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 18. Input signal measurement reference

5.3.2 Nonswitching electrical specifications

5.3.2.1 Voltage and current operating requirements

Table 41. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
USB_V_{DD}	Supply voltage	3.0	3.6	V	1
V_{DDIO_E}	Supply voltage	V_{DD}	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • $2.7 V \le V_{DD} \le 3.6 V$ • $1.7 V \le V_{DD} \le 2.7 V$	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
V_{IL}	Input low voltage	—	$0.35 \times V_{DD}$	V	

Table continues on the next page...

Table 41. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	—	0.3 × V_{DD}	V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	 mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. The ripple limit for USB_V_{DD} is 100 mV.

5.3.2.2 LVD and POR operating requirements

Table 42. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	60	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	40	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 43. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.3.2.3 Voltage and current operating behaviors

Table 44. Voltage and current operating behaviors

Symbol	Description		Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Standard IO	3.3 V, I_{load} = -5 mA	V_{DD} – 0.5	—	V	1
		1.71 V, I_{load} = -2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports		—	100	mA	
$V_{OH_RTC_WAKEUP}$	Output high voltage — normal drive pad	2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -5 mA	V_{BAT} – 0.5	—	V	
		1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{BAT} – 0.5	—	V	
$I_{OH_RTC_WAKEUP}$	Output high current total for RTC_WAKEUP pins		—	100	mA	
V_{OL}	Output low voltage — Standard IO	3.3 V, I_{load} = 5 mA	—	0.5	V	1
		1.71 V, I_{load} = 2.5 mA	—	0.5		
V_{OL}	Output low voltage — RESET_b	3.3 V, I_{load} = 5 mA	—	0.5	V	1
		1.71 V, I_{load} = 2.5 mA	—	0.5		
I_{OLT}	Output low current total for all ports		—	100	mA	
$V_{OL_RTC_WAKEUP}$	Output low voltage— normal drive pad	2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
		1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 2.5 mA	—	0.5		
V_{OH}	Output high voltage — Standard fast IO	3.3 V, I_{load} = 15 mA	V_{DD} – 0.5	—	V	2
		1.71V, I_{load} = 7.5 mA	V_{DD} – 0.5	—		
V_{OL}	Output high voltage — Standard fast IO	3.3 V, I_{load} = 15 mA	—	0.5	V	2
		1.71 V, I_{load} =7.5 mA	—	0.5		
$I_{OL_RTC_WAKEUP}$	Output low current total for RTC_WAKEUP pins		—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range		—	0.5	μA	3
I_{IN}	Input leakage current (per pin) at 25 °C		—	0.002	μA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)		—	0.25	μA	
$I_{OZ_RTC_WAKEUP}$	Hi-Z (off-state) leakage current (per RTC_WAKEUP pin)		—	0.25	μA	
R_{PU}	Internal pullup resistors		20	50	kΩ	4
R_{PD}	Internal pulldown resistors		20	50	kΩ	5

1. This is applicanble for all GPIO pins except PTE
2. This is applicable for PTE pins only.
3. Measured at VDD=3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
5. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

5.3.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx –> RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 24 MHz
- Flash clock = 24 MHz
- MCG mode=FEI

Table 45. Power mode transition operating behaviors

Symbol	Description		Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	V_{DD} slew rate ≥ 5.7 kV/s	—	300	µs	1
		V_{DD} slew rate < 5.7 kV/s	—	1.7 V/ (V_{DD} slew rate)		
	• VLLS0 –> RUN		—	138	µs	
	• VLLS1 –> RUN		—	138	µs	
	• VLLS2 –> RUN		—	76	µs	
	• VLLS3 –> RUN		—	76	µs	
	• LLS2 –> RUN		—	6.1	µs	
	• LLS3 –> RUN		—	6.1	µs	
	• VLPS –> RUN		—	5.6	µs	
	• STOP –> RUN		—	5.6	µs	

1. Normal boot (FTFA_FOPT[LPBOOT]=1)

Table 46. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105[1]	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA

Table continues on the next page...

Table 46. Low power mode peripheral adders — typical value (continued)

Symbol	Description		Temperature (°C)						Unit
			-40	25	50	70	85	105[1]	
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.		206	228	237	245	251	258	μA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	VLLS1	440	490	540	560	570	580	nA
		VLLS3	440	490	540	560	570	580	
		LLS2	490	490	540	560	570	680	
		LLS3	490	490	540	560	570	680	
		VLPS	510	560	560	560	610	680	
		STOP	510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.		22	22	22	22	22	22	μA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.		432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
		OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	μA
		OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.		45	45	45	45	45	45	μA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is		366	366	366	366	366	366	μA

Table 46. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105[1]	
	configured for low power mode using the internal clock and continuous conversions.							

1. Only LQFP and MAPBGA packages support the data in this column.

5.3.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The data at 105 °C is for MAPBGA and LQFP packages only.

Table 47. Power consumption operating behaviors

Symbol	Description		Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current		—	See note	mA	1
I_{DD_HSRUN}	Running CoreMark in Flash in Compute Operation mode, Core at 96 MHz, bus at 24 MHz, flash at 24 MHz, VDD = 3 V	25 °C	14.21	17.32	mA	2, 3
I_{DD_HSRUN}	Running CoreMark in Flash, all peripheral clock disabled, Core at 96 MHz, bus at 24 MHz, flash at 24 MHz, VDD = 3 V	25 °C	15.43	18.54	mA	2, 3
I_{DD_HSRUN}	Running CoreMark in Flash, all peripheral clock enabled, Core at 96 MHz, bus at 24 MHz, flash at 24 MHz, VDD = 3 V	25 °C	20.01	23.12	mA	2, 3
I_{DD_RUN}	Running CoreMark in Flash in Compute Operation mode, Core at 72 MHz, bus at 24 MHz, flash at 24 MHz, VDD = 3 V	25 °C	8.99	10.59	mA	2, 4
		105 °C	9.43	10.88		
I_{DD_RUN}	Running CoreMark in Flash all peripheral clock disabled, Core at 72 MHz, bus at 24 MHz,flash at 24 MHz , VDD = 3 V	25 °C	10.1	11.70	mA	2, 4
		105 °C	10.55	12.00		
I_{DD_RUN}	Running CoreMark in Flash all peripheral clock disabled, Core at 48 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V	25 °C	9.1	10.70	mA	2, 5
		105 °C	9.54	10.99		
I_{DD_RUN}	Running CoreMark in Flash all peripheral clock disabled, Core at 24 MHz, bus at 12 MHz, flash at 12 MHz , VDD = 3 V	25 °C	5.57	7.17	mA	2, 5
		105 °C	6.02	7.47		

Table continues on the next page...

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
I_{DD_RUN}	Running CoreMark in Flash all peripheral clock disabled, Core at 12 MHz, bus at 6 MHz, flash at 6 MHz , VDD = 3 V	25 °C	2.8	4.40	mA	2, 5
		105 °C	3.22	4.67		
I_{DD_RUN}	Running CoreMark in Flash all peripheral clock enabled, Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V	25 °C	12.94	14.54	mA	2, 4
		105 °C	13.35	14.80		
I_{DD_RUN}	Running While(1) loop in Flash, all peripheral clock disabled Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V	25 °C	7.6	9.20	mA	4
		105 °C	8.08	9.53		
I_{DD_RUN}	Running While(1) loop in Flash, all peripheral clock disabled Core at 48 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V	25 °C	6.3	7.90	mA	5
		105 °C	6.79	8.24		
I_{DD_RUN}	Running While(1) loop in Flash, all peripheral clock disabled Core at 24 MHz, bus at 12 MHz, flash at 12 MHz , VDD = 3 V	25 °C	4.08	5.68	mA	5
		105 °C	4.53	5.98		
I_{DD_RUN}	Running While(1) loop in Flash, all peripheral clock disabled Core at 12 MHz, bus at 6 MHz, flash at 6 MHz , VDD = 3 V	25 °C	3.03	4.63	mA	5
		105 °C	3.46	4.91		
I_{DD_RUN}	Running While(1) loop in Flash, all peripheral clock enabled Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V	25 °C	10.93	12.53	mA	4
		105 °C	11.45	12.90		
I_{DD_RUN}	Running CoreMark loop in SRAM all peripheral clock disabled, Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V	25 °C	11.64	13.24	mA	2, 4
		105 °C	12.17	13.62		
I_{DD_RUN}	Running CoreMark loop in SRAM in Compute Operation mode, Core at 72 MHz, bus at 24 MHz, flash at 24 MHz , VDD = 3 V	25 °C	10.52	12.12	mA	2, 4
		105 °C	11.03	12.48		
I_{DD_WAIT}	Core disabled, system at 72 MHz, bus at 24 MHz, flash disabled (flash doze enabled), VDD = 3 V, all peripheral clocks disabled	25 °C	5.11	6.47	mA	4
I_{DD_WAIT}	Core disabled, system at 48 MHz, bus at 24 MHz, flash disabled (flash doze enabled), VDD = 3 V, all peripheral clocks disabled	25 °C	4.33	5.69	mA	5
I_{DD_WAIT}	Core disabled, system at 24 MHz, bus at 12 MHz, flash disabled (flash doze enabled), VDD = 3 V, all peripheral clocks disabled	25 °C	2.76	4.12	mA	5

Table continues on the next page...

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
I_{DD_WAIT}	Core disabled, system at 12 MHz, bus at 6 MHz, flash disabled (flash doze enabled), VDD = 3 V, all peripheral clocks disabled	25 °C	1.98	3.34	mA	5
I_{DD_VLPR}	Very Low Power Run Core Mark in Flash in Compute Operation mode: Core at 4 MHz, bus at 1 MHz, flash at 1 MHz, VDD = 3 V	25 °C	845	936.88	μA	2, 6
I_{DD_VLPR}	Very Low Power Run Core Mark in Flash all peripheral clock enabled: Core at 4 MHz, bus at 1 MHz, flash at 1 MHz, VDD = 3 V	25 °C	1033	1145.32	μA	2, 6
I_{DD_VLPR}	Very Low Power Run Core Mark in Flash all peripheral clock disabled: Core at 4 MHz, bus at 1 MHz, flash at 1 MHz, VDD = 3 V	25 °C	898	995.64	μA	2, 6
I_{DD_VLPR}	Very Low Power Run While(1) loop in Flash all peripheral clock disabled mode: Core at 4 MHz, bus at 1 MHz, flash at 1 MHz, VDD = 3 V	25 °C	328	380.03	μA	6
I_{DD_VLPR}	Very Low Power Run While(1) loop in Flash all peripheral clock enabled: Core at 4 MHz, bus at 1 MHz, flash at 1 MHz, VDD = 3 V	25 °C	460	512.03	μA	6
I_{DD_VLPR}	Very Low Power Run While(1) loop in Flash all peripheral clock disabled mode: Core at 2 MHz, bus at 0.5 MHz, flash at 0.5 MHz, VDD = 3 V	25 °C	256	308.03	μA	6
I_{DD_VLPR}	Very Low Power Run While(1) loop in Flash all peripheral clock disabled mode: Core at 125 kHz, bus at 31.25 kHz, flash at 31.25 kHz, VDD = 3 V	25 °C	34	64.00	μA	6
I_{DD_VLPR}	Very Low Power Run Core Mark in SRAM in Compute Operation mode: Core at 4 MHz, bus at 1 MHz, flash at 1 MHz, VDD = 3 V	25 °C	591	655.26	μA	2, 6
I_{DD_VLPR}	Very Low Power Run Core Mark in SRAM all peripheral clock enable: Core at 4 MHz, bus at 1 MHz, flash at 1 MHz, VDD = 3 V	25 °C	777	861.48	μA	2, 6
I_{DD_VLPR}	Very Low Power Run Core Mark in SRAM all peripheral clock disable: Core at 4 MHz, bus at 1 MHz, flash at 1 MHz, VDD = 3 V	25 °C	643	712.91	μA	2, 6
I_{DD_VLPW}	Very Low Power Run Wait current, core disabled, system at 4 MHz, bus and flash at 1 MHz, all peripheral clocks disabled, VDD = 3 V	25 °C	297	349.03	μA	6

Table continues on the next page...

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
I_{DD_VLPW}	Very Low Power Run Wait current, core disabled, system at 2 MHz, bus and flash at 0.5 MHz, all peripheral clocks disabled, VDD = 3 V	25 °C	225	277.03	μA	6
I_{DD_VLPW}	Very Low Power Run Wait current, core disabled, system at 125 kHz, bus and flash at 31.25 kHz, all peripheral clocks disabled, VDD = 3 V	25 °C	31	61.00	μA	6
I_{IDD_PSTOP2}	Partial stop 2, core and system clock disabled, bus and flash at 12 MHz, VDD = 3 V	25 °C	2.9	4.26	mA	7
I_{DD_STOP}	Stop mode current at 3.0 V	25 °C and below	273	304.31	μA	
		50°C	306	384.47		
		85 °C	440	589.29		
		105 °C	625	925.33		
I_{DD_VLPS}	VLPS current, VDD= 3 V	25 °C and below	5.82	15.42	μA	
		50 °C	14.41	29.41		
		85 °C	56.47	99.67		
		105°C	121.54	223.54		
I_{DD_VLPS}	VLPS current, VDD= 1.8 V	25 °C and below	5.61	15.21	μA	
		50 °C	14.01	29.01		
		85 °C	55.8	99.00		
		105 °C	120.14	222.14		
I_{DD_LLS3}	LLS3 current, all peripheral disabled, VDD = 3 V	25 °C and below	3.68	7.88	μA	
		50 °C	8.28	15.48		
		70 °C	13.52	22.52		
		85 °C	20.91	39.55		
		105 °C	40.27	67.79		
I_{DD_LLS3}	LLS3 with RTC current, VDD = 3 V	25 °C and below	5.08	9.28	μA	
		50 °C	10.31	17.51		
		70 °C	15.76	24.76		
		85 °C	22.8	41.44		
		105 °C	43.5	71.02		
I_{DD_LLS3}	LLS3 with RTC current, VDD = 1.8 V	25 °C and below	5.02	9.22	μA	
		50 °C	10.06	17.26		

Table continues on the next page...

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
		70 °C	15.15	24.15		
		85 °C	21.88	40.52		
		105 °C	41.82	69.34		
I_{DD_LLS2}	LLS2 current, all peripheral disabled, VDD = 3 V	25 °C and below	3.37	6.67	μA	
		50 °C	6.82	13.42		
		70 °C	11.13	20.73		
		85 °C	16.84	31.46		
		105 °C	32.93	48.89		
I_{DD_LLS2}	LLS2 with RTC current, VDD = 3 V	25 °C and below	4.49	7.79	μA	
		50 °C	9.07	16.27		
		70 °C	12.98	22.58		
		85 °C	17.88	32.50		
		105 °C	35.98	51.94		
I_{DD_LLS2}	LLS2 with RTC current, VDD = 1.8 V	25 °C and below	4.47	7.77	μA	
		50 °C	8.79	15.99		
		70 °C	12.27	21.87		
		85 °C	17.77	32.39		
		105 °C	34.31	50.27		
I_{DD_VLLS3}	VLLS3 current, all peripheral disable, VDD = 3 V	25 °C and below	2	3.80	μA	
		50 °C	3.76	7.36		
		70 °C	7.19	12.82		
		85 °C	12.62	21.10		
		105 °C	27.61	42.33		
I_{DD_VLLS3}	VLLS3 with RTC current, VDD = 3 V	25 °C and below	2.83	4.63	μA	
		50 °C	4.62	8.22		
		70 °C	8.38	14.01		
		85 °C	14.06	21.54		
		105 °C	29.81	44.53		
I_{DD_VLLS3}	VLLS3 with RTC current, VDD = 1.8 V	25 °C and below	2.59	4.39	μA	
		50 °C	4.28	7.88		
		70 °C	7.89	13.52		
		85 °C	13.33	20.81		
		105 °C	28.34	43.06		

Table continues on the next page...

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
I_{DD_VLLS2}	VLLS2 current, all peripheral disable, VDD = 3 V	25 °C and below	1.98	3.78	μA	
		50 °C	2.95	5.71		
		70 °C	4.83	9.33		
		85 °C	7.95	13.80		
		105 °C	16.92	24.26		
I_{DD_VLLS2}	VLLS2 with RTC current, VDD = 3 V	25 °C and below	2.8	4.60	μA	
		50 °C	3.74	6.50		
		70 °C	5.96	10.46		
		85 °C	9.35	15.20		
		105 °C	19.37	26.71		
I_{DD_VLLS2}	VLLS2 with RTC current, VDD = 1.8 V	25 °C and below	2.56	4.36	μA	
		50 °C	3.43	6.19		
		70 °C	5.51	10.01		
		85 °C	8.61	14.46		
		105 °C	18.87	26.21		
I_{DD_VLLS1}	VLLS1 current, all peripheral disable, VDD = 3 V	25 °C and below	0.718	1.11	μA	
		50 °C	1.28	2.48		
		70 °C	2.4	4.56		
		85 °C	4.38	7.62		
		105 °C	10.28	15.68		
I_{DD_VLLS1}	VLLS1 with RTC current, VDD = 3 V	25 °C and below	1.51	1.90	μA	
		50 °C	2.13	3.63		
		70 °C	3.65	6.29		
		85 °C	5.76	9.00		
		105 °C	12.89	18.29		
I_{DD_VLLS1}	VLLS1 with RTC current, VDD = 1.8 V	25 °C and below	1.26	1.65	μA	
		50 °C	1.73	3.23		
		70 °C	2.93	5.57		
		85 °C	4.98	8.22		
		105 °C	11.21	16.61		
I_{DD_VLLS0}	VLLS0 current, all peripheral disabled, (SMC_STOPCTRL[PORPO] = 0), VDD = 3 V	25 °C and below	432	835	nA	
		50 °C	986	1723		
		70 °C	2030	3270		

Table continues on the next page...

Table 47. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max.	Unit	Notes
		85 °C	4000	5546		
		105 °C	9760	12709		
I_{DD_VLLS0}	VLLS0 current, all peripheral disabled, (SMC_STOPCTRL[PORPO] = 1), VDD = 3 V	25 °C and below	272	520	nA	
		50 °C	743	1398		
		70 °C	1700	2927		
		85 °C	3650	5177		
		105 °C	9300	12191		
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3 V	25 °C and below	160	218.10	nA	
		50 °C	269	366.96		
		70 °C	483	714.32		
		85 °C	851	1211.88		
		105 °C	1870	2715.16		
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 1.8 V	25 °C and below	137	195.10	nA	
		50 °C	230	327.96		
		70 °C	422	653.32		
		85 °C	746	1106.88		
		105 °C	1660	2505.16		
I_{DD_VBAT}	Average current when CPU is not accessing RTC register at 3.0 V including 32 kHz	25 °C and below	676	784.00	nA	
		50 °C	809	1013.00		
		70 °C	1040	1538.08		
		85 °C	1420	2022.17		
		105 °C	2460	3571.81		
I_{DD_VBAT}	Average current when CPU is not accessing RTC register at 1.8 V including 32 kHz	25 °C and below	556	664.00	nA	
		50 °C	674	878.00		
		70 °C	880	1378.08		
		85 °C	1220	1822.17		
		105 °C	2160	3271.81		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. CoreMark benchmark compiled using IAR 7.40 with optimization level high, optimized for balanced.
3. MCG configured for PEE mode.
4. MCG configured for FEE mode.
5. MCG configured for PBE mode.
6. MCG configured for BLPE mode.
7. MCG configured for FEI mode.

5.3.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

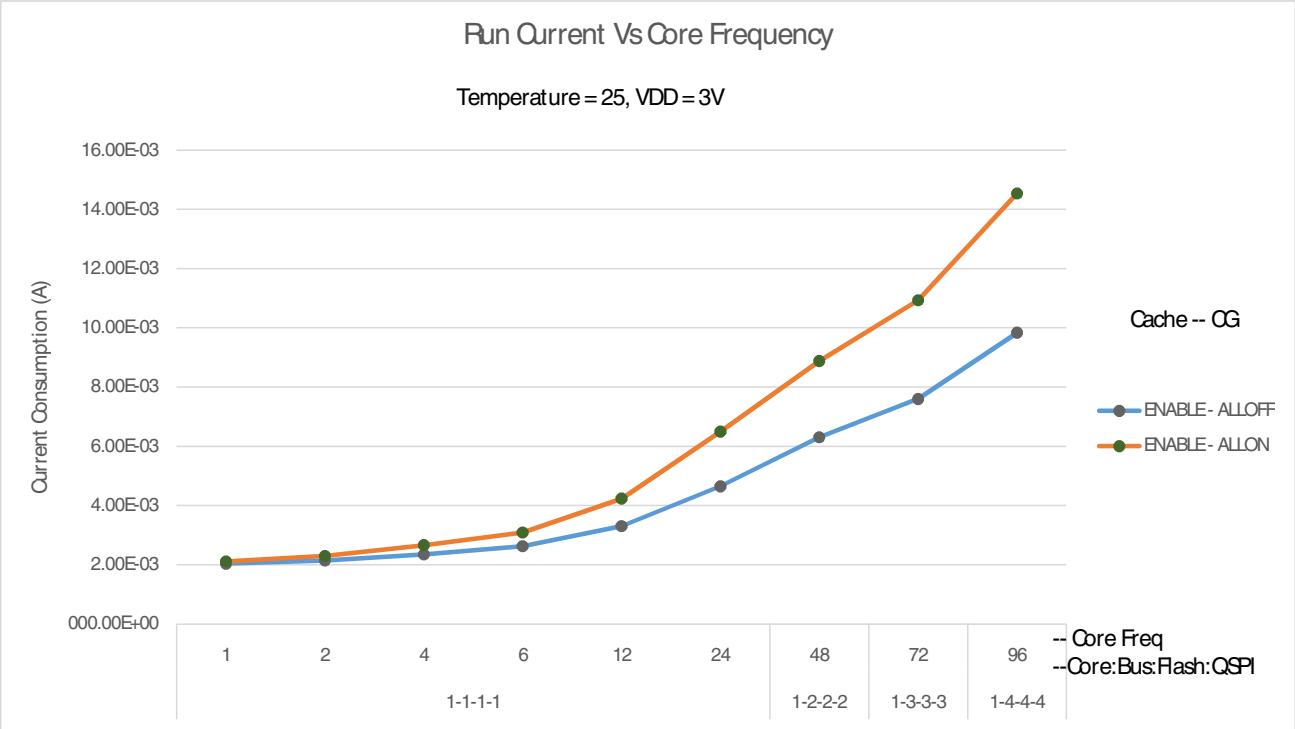


Figure 19. Run mode supply current vs. core frequency

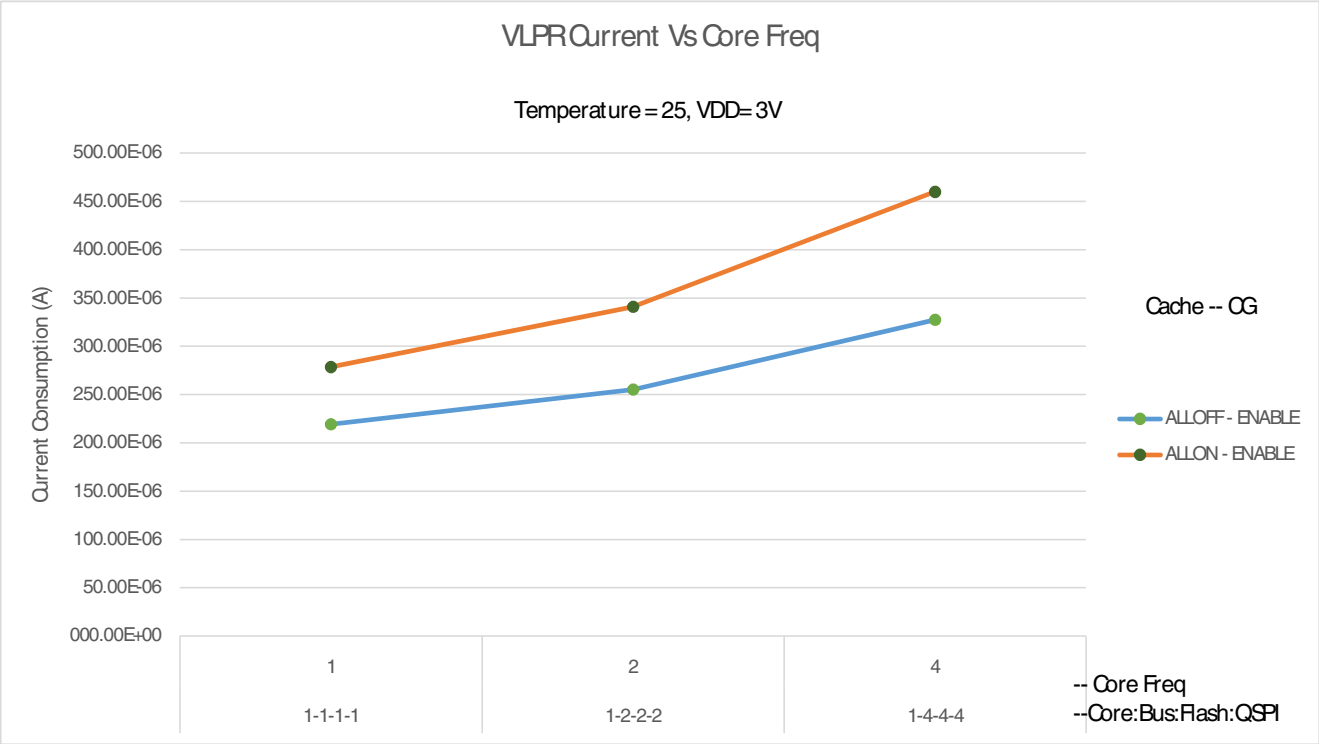


Figure 20. VLPR mode supply current vs. core frequency

5.3.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following applications notes, available on nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems
- KL-QRUG (Kinetis L-series Quick Reference).

5.3.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for "EMC design"

5.3.2.8 Capacitance attributes

Table 48. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3.3 Switching specifications

5.3.3.1 Device clock specifications

Table 49. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	96	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	72	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FBUS}	Bus interface clock for QSPI	36	—	MHz	
f_{FLASH}	Flash clock	—	24	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FBUS}	Bus interface clock for QSPI	2	—	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	16	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, LPUART, timers, and I^2C signals.

Table 50. General switching specifications

Description		Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path		1.5	—	Bus clock cycles	1
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path		16 [2]	—	ns	3
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path		50	—	ns	3
External reset pulse width (digital glitch filter disabled)		100	—	ns	3
Port rise and fall time (high drive) — slew enabled	1.71 V < V_{DDIO_E} < 2.7 V	—	34	ns	4, 5
	2.7 V < V_{DDIO_E} ≤ 3.6 V	—	16		
Port rise and fall time (high drive) — slew disabled	1.71 V < V_{DDIO_E} < 2.7 V	—	4.5	ns	4, 5
	2.7 V < V_{DDIO_E} ≤ 3.6V	—	3		
Port rise and fall time (low drive) — slew enabled	1.71 V < V_{DDIO_E} < 2.7 V	—	25	ns	6, 5
	2.7 V < V_{DDIO_E} ≤ 3.6 V	—	16		
Port rise and fall time (high drive) — slew disabled	1.71 V < V_{DDIO_E} < 2.7 V	—	4.2	ns	6, 5
	2.7 V < V_{DDIO_E} ≤ 3.6V	—	2.5		
Port rise and fall time (low drive) — slew enabled	1.71 < V_{DDIO_E} < 2.7V	—	25	ns	6, 7
	2.7 < V_{DDIO_E} ≤ 3.6V	—	13		
Port rise and fall time (low drive) — slew disabled	1.71 < V_{DDIO_E} < 2.7V	—	5.5	ns	6, 7
	2.7 < V_{DDIO_E} ≤ 3.6V	—	3.5		

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. This is applicable for Port E pins
6. 25 pF load
7. This is applicable for Ports A, B, C, and D.

5.3.4 Thermal specifications

5.3.4.1 Thermal operating requirements

Table 51. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A[1]	Ambient temperature	–40	105	°C

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + \theta_{JA}$ x chip power dissipation

5.3.4.2 Thermal attributes

Board type	Symbol	Description	121 MAPBGA	80 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	75.5	55	92.2	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	43.5	40	45.4	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	60.0	44	72.9	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	38.3	34	40.1	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	23.1	24	20.4	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.2	12	19.4	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter,	0.5	2	0.7	°C/W	4

Table continues on the next page...

Board type	Symbol	Description	121 MAPBGA	80 LQFP	64 MAPBGA	Unit	Notes
		junction to package top outside center (natural convection)					
—	$R_{\theta JB_CSB}$	Thermal characterization parameter, junction to package top outside center (natural convection)	14.6	—	19.5	°C/W	5

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
5. Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

5.4 Peripheral operating requirements and behaviors

5.4.1 Core modules

5.4.1.1 Debug trace timing specifications

Table 52. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

5.4.1.2 SWD electricals

Table 53. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

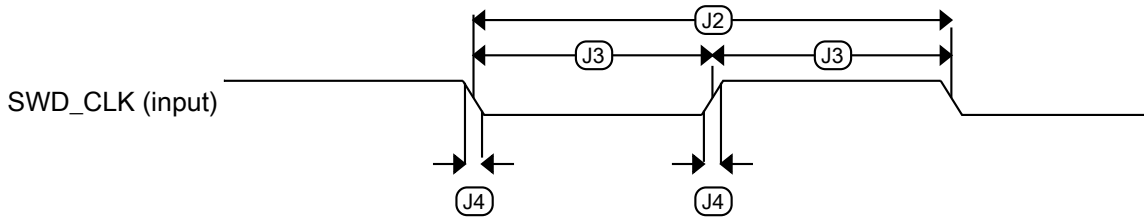


Figure 21. Serial wire clock input timing

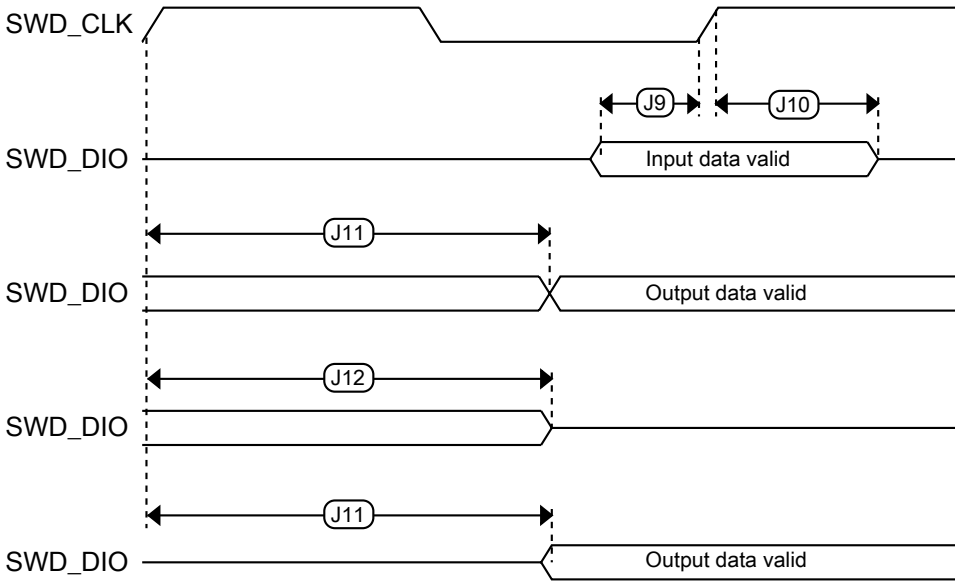


Figure 22. Serial wire data timing

5.4.2 Clock modules

5.4.2.1 MCG specifications

Table 54. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	20	—	μA	
$t_{irefsts}$	[O:] Internal reference (slow clock) startup time	—	32	—	μs	
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 1	± 2	$\%f_{dco}$	1

Table continues on the next page...

Table 54. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.5	± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current		—	25	—	μA	
$t_{irefsts}$	[L:] Internal reference startup time (fast clock)		—	10	15	μs	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00 ext clk freq: above $(3/5)f_{int}$ never reset ext clk freq: between (2/5)fint and $(3/5)f_{int}$ maybe reset (phase dependency) ext clk freq: below $(2/5)f_{int}$ always reset		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11 ext clk freq: above $(16/5)f_{int}$ never reset ext clk freq: between $(15/5)f_{int}$ and $(16/5)f_{int}$ maybe reset (phase dependency) ext clk freq: below $(15/5)f_{int}$ always reset		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco_ut}	DCO output frequency range — untrimmed	Low range (DRS=00, DMX32=0) $640 \times f_{ints_ut}$	16.0	23.04	26.66	MHz	2
		Mid range (DRS=01, DMX32=0) $1280 \times f_{ints_ut}$	32.0	46.08	53.32		
		Mid-high range (DRS=10, DMX32=0) $1920 \times f_{ints_ut}$	48.0	69.12	79.99		
		High range (DRS=11, DMX32=0) $2560 \times f_{ints_ut}$	64.0	92.16	106.65		
		Low range (DRS=00, DMX32=1) $732 \times f_{ints_ut}$	18.3	26.35	30.50		
		Mid range	36.6	52.70	60.99		

Table continues on the next page...

Table 54. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
		(DRS=01, DMX32=1) 1464 × f_{ints_ut}					
		Mid-high range (DRS=10, DMX32=1) 2197 × f_{ints_ut}	54.93	79.09	91.53		
		High range (DRS=11, DMX32=1) 2929 × f_{ints_ut}	73.23	105.44	122.02		
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco_t_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f_{pll_ref}	PLL reference frequency range		8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency		180	—	360	MHz	
f_{vcoclk}	PLL output frequency		90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency		90	—	180	MHz	
I_{pll}	PLL operating current • VCO at 184 MHz ($f_{osc_hi_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 23)		—	2.8	—	mA	8
I_{pll}	PLL operating current • VCO at 360 MHz ($f_{osc_hi_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	3.6	—	mA	8

Table continues on the next page...

Table 54. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 180 MHz • f_{vco} = 360 MHz	 — —	 120 75	 — —	 ps ps	9
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 180 MHz • f_{vco} = 360 MHz	 — —	 1350 600	 — —	 ps ps	9
D_{unl}	Lock exit frequency tolerance	±4.47	—	±5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. This applies when SCTRIM at value (0x80) and SCFTRIM control bit at value (0x0).
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5.4.2.2 IRC48M specifications

Table 55. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	520	—	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m_ol_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature • Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	 — —	 ± 0.5 ± 0.5	 ± 1.5 ± 1.5	$\%f_{irc48m}$	
$\Delta f_{irc48m_ol_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	—	± 0.5	± 1.5	$\%f_{irc48m}$	

Table continues on the next page...

Table 55. IRC48M specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)					
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	1
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	μs	2

1. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
   - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1, or
   - MCG_C7[OSCSEL]=10, or
   - SIM_SOPT2[PLLFLLSEL]=11

5.4.2.3 Oscillator electrical specifications

5.4.2.3.1 Oscillator DC electrical specifications

Table 56. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	600	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	7.5	—	μA	
	• 4 MHz	—	500	—	μA	
	• 8 MHz (RANGE=01)	—	650	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3.25	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3

Table continues on the next page...

Table 56. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C, Internal capacitance = 20 pf
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

5.4.2.3.2 Oscillator frequency specifications

Table 57. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	

Table continues on the next page...

Table 57. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	1, 2
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Proper PC board layout procedures must be followed to achieve specifications.
2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

5.4.2.4 32 kHz oscillator electrical characteristics

5.4.2.4.1 32 kHz oscillator DC electrical specifications

Table 58. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

5.4.2.4.2 32 kHz oscillator frequency specifications

Table 59. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

5.4.3 Memories and memory interfaces

5.4.3.1 QuadSPI AC specifications

- All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing diagrams in this section.
- Measurements are with a load of 15pf (1.8V) and 35pf (3V) on output pins. Input slew: 1ns
- Timings assume a setting of 0x0000_000x for QuadSPI _SMPR register (see the reference manual for details).

The following table lists the QuadSPI delay chain read/write settings. Please see the device reference manual for register and bit descriptions.

Table 60. QuadSPI delay chain read/write settings

Mode	QuadSPI registers				Notes
	QuadSPI_MCR[DQS_EN]	QuadSPI_SOCCR[SOCCFG]	QuadSPI_MCR[SCLKCFG]	QuadSPI_FLSHCR[TDH]	
SDR	Yes	3Fh	5	No	Delay of 63 buffer and 64 mux
DDR	Yes	3Fh	1	2	Delay of 63 buffer and 64 mux
Hyperflash	RDS driven from Flash	0h	No	2	Delay of 1 mux

SDR mode

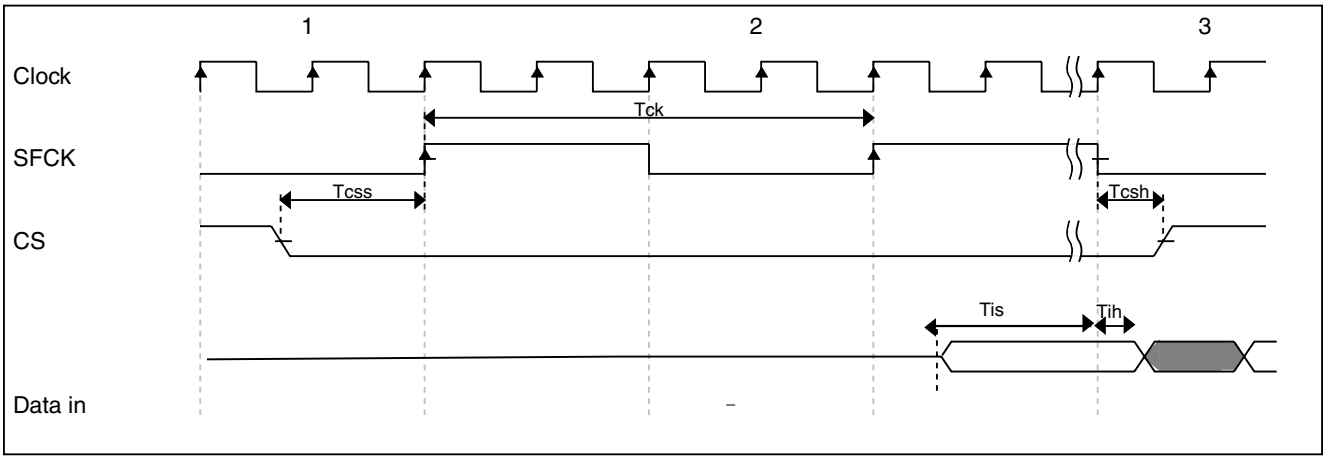


Figure 23. QuadSPI input timing (SDR mode) diagram

NOTE

- The below timing values are with default settings for sampling registers like QuadSPI_SMPR.
- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- The below timing are for a load of 15pf (1.8V) and 35pf (3V) or output pads
- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 61. QuadSPI input timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4	—	ns
T_{ih}	Hold time requirement for incoming data	1.5	—	ns

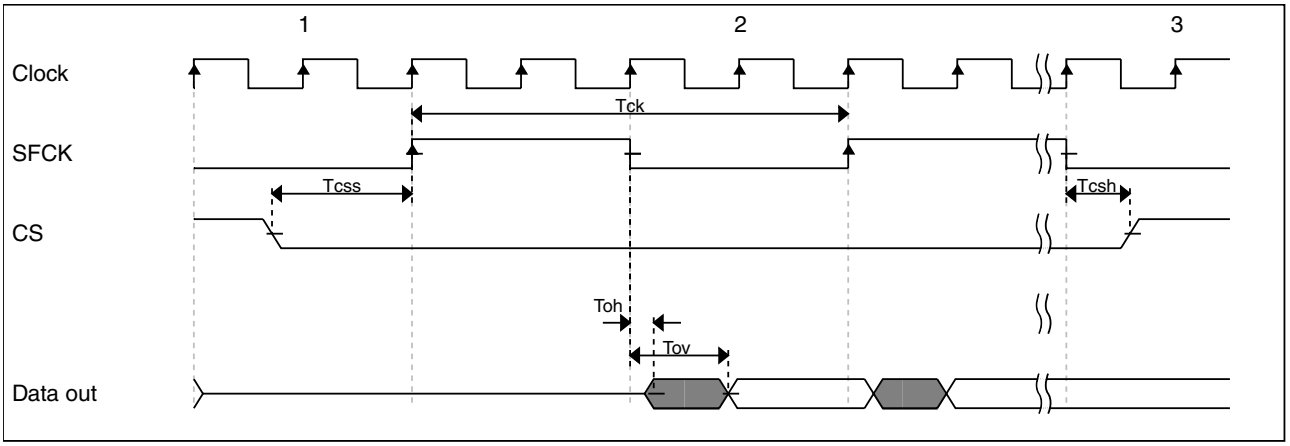


Figure 24. QuadSPI output timing (SDR mode) diagram

Table 62. QuadSPI output timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	—	2.8	ns
T_{oh}	Output Data Hold	-1.4	—	ns
T_{ck}	SCK clock period	—	96	MHz
T_{css}	Chip select output setup time	2	—	ns
T_{csh}	Chip select output hold time	-1	—	ns

NOTE

For any frequency setup and hold specifications of the memory should be met.

DDR Mode

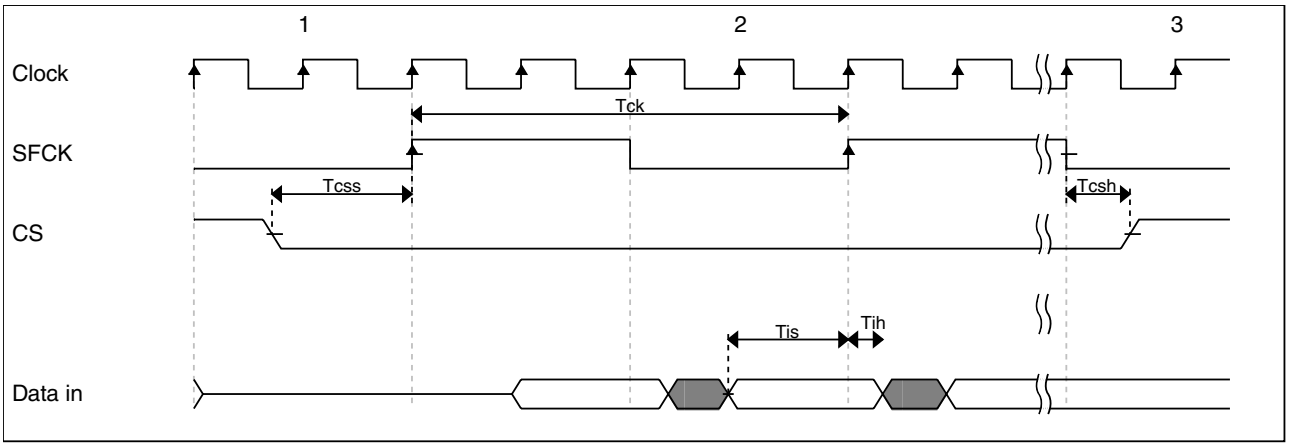


Figure 25. QuadSPI input timing (DDR mode) diagram

NOTE

- Numbers are for a load of 15pf (1.8V) and 35pf (3V)
- The numbers are for setting of hold condition in register QuadSPI_SMPR[DDRSNP]

Table 63. QuadSPI input timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4 (Without learning)	—	ns
		1 (With learning)	—	
T_{ih}	Hold time requirement for incoming data	1.5	—	ns

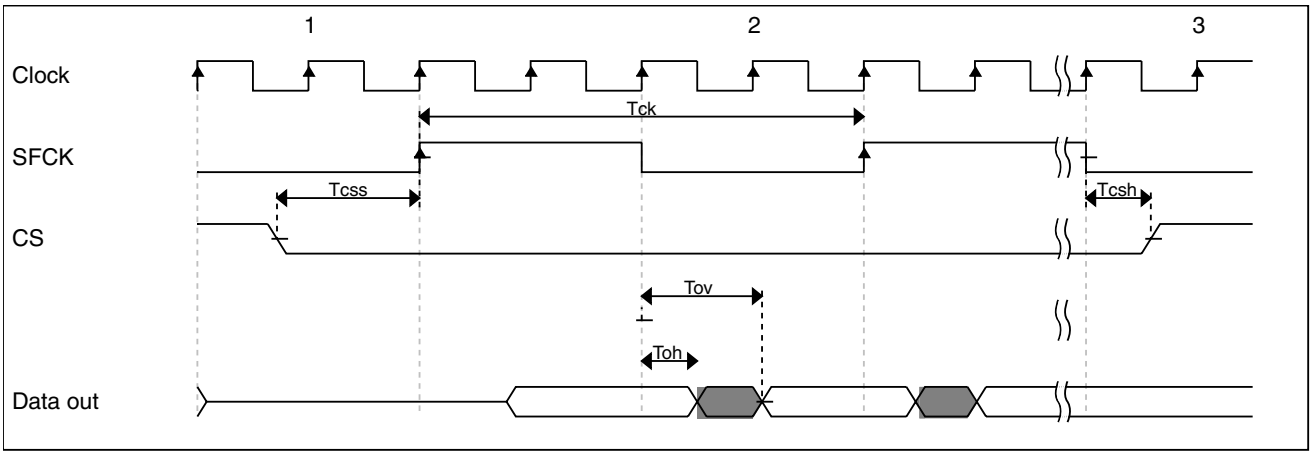


Figure 26. QuadSPI output timing (DDR mode) diagram

Table 64. QuadSPI output timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	—	4.5	ns
T_{oh}	Output Data Hold	1.5	—	ns
T_{ck}	SCK clock period	—	72 (with learning)	MHz
		—	45 (without learning)	
T_{css}	Chip select output setup time	2	—	Clk(sck)
T_{csh}	Chip select output hold time	-1	—	Clk(sck)

Hyperflash mode

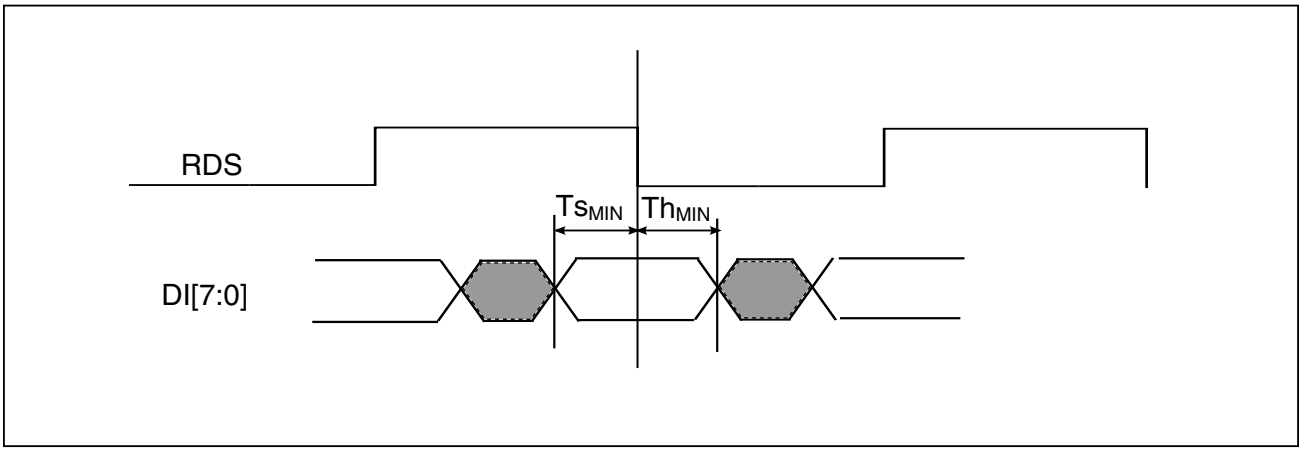


Figure 27. QuadSPI input timing (Hyperflash mode) diagram

Table 65. QuadSPI input timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Ts_{MIN}	Setup time for incoming data	2	—	ns
Th_{MIN}	Hold time requirement for incoming data	2	—	ns

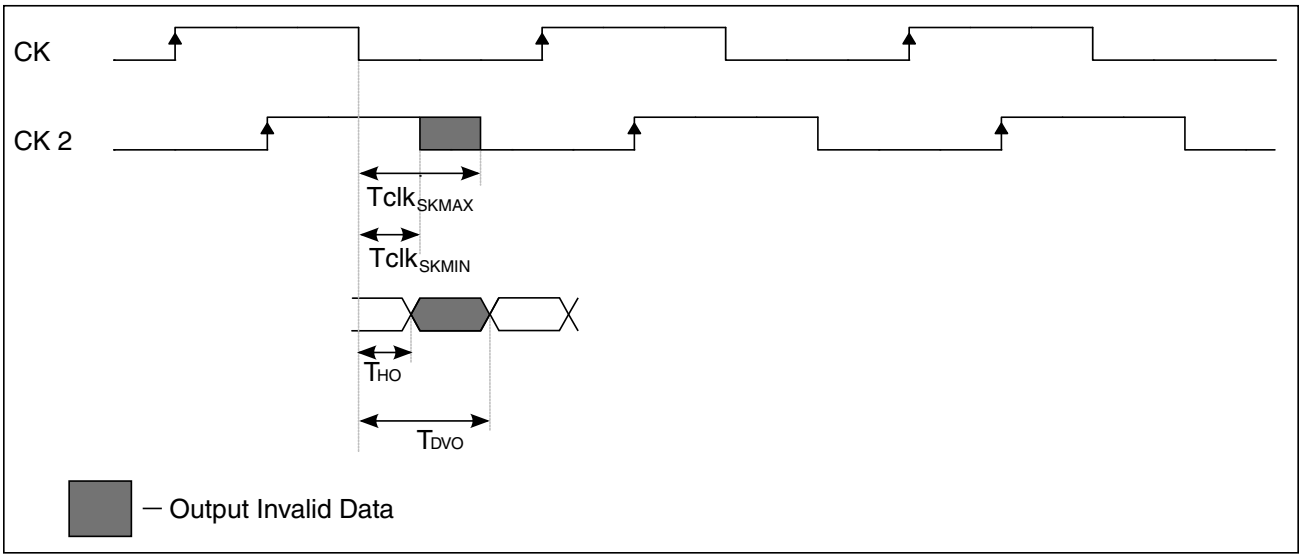


Figure 28. QuadSPI output timing (Hyperflash mode) diagram

Table 66. QuadSPI output timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Tdv_{MAX}	Output Data Valid	—	4.3	ns

Table continues on the next page...

Table 66. QuadSPI output timing (Hyperflash mode) specifications (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Tho	Output Data Hold	1.3	—	ns
$Tclk_{SKMAX}$	Ck to Ck2 skew max	—	T/4 + 0.5	ns
$Tclk_{SKMIN}$	Ck to Ck2 skew min	T/4 - 0.5	—	ns

NOTE

Maximum clock frequency = 72 MHz.

5.4.3.2 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

5.4.3.2.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 67. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

5.4.3.2.2 Flash timing specifications — commands

Table 68. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	30	μs	1
$t_{pgmonce}$	Program Once execution time	—	100	—	μs	—
t_{ersall}	Erase All Blocks execution time	—	140	1150	ms	2

Table continues on the next page...

Table 68. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.4.3.2.3 Flash high voltage current behaviors

Table 69. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.4.3.2.4 Reliability specifications

Table 70. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

5.4.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.4.5 Analog

5.4.5.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 1 and Table 72 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

5.4.5.1.1 16-bit ADC operating conditions

Table 71. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} – V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} – V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.

4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

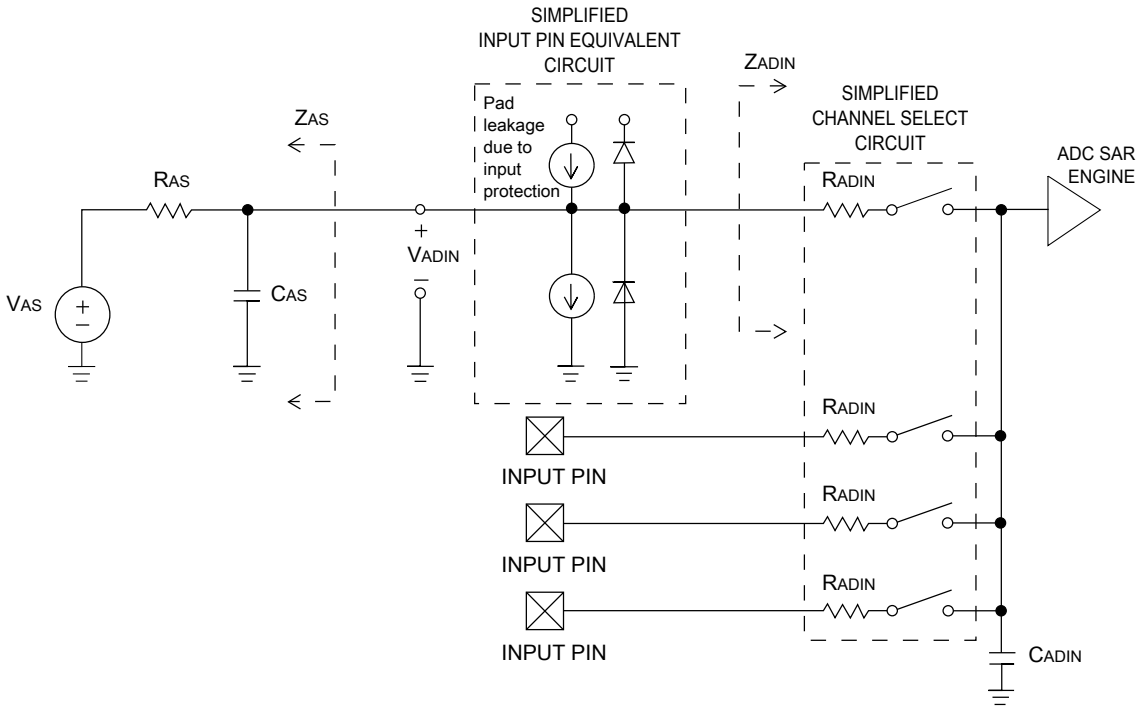


Figure 29. ADC input impedance equivalency diagram

5.4.5.1.2 16-bit ADC electrical characteristics

Table 72. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5

Table continues on the next page...

Table 72. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	 dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$

2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

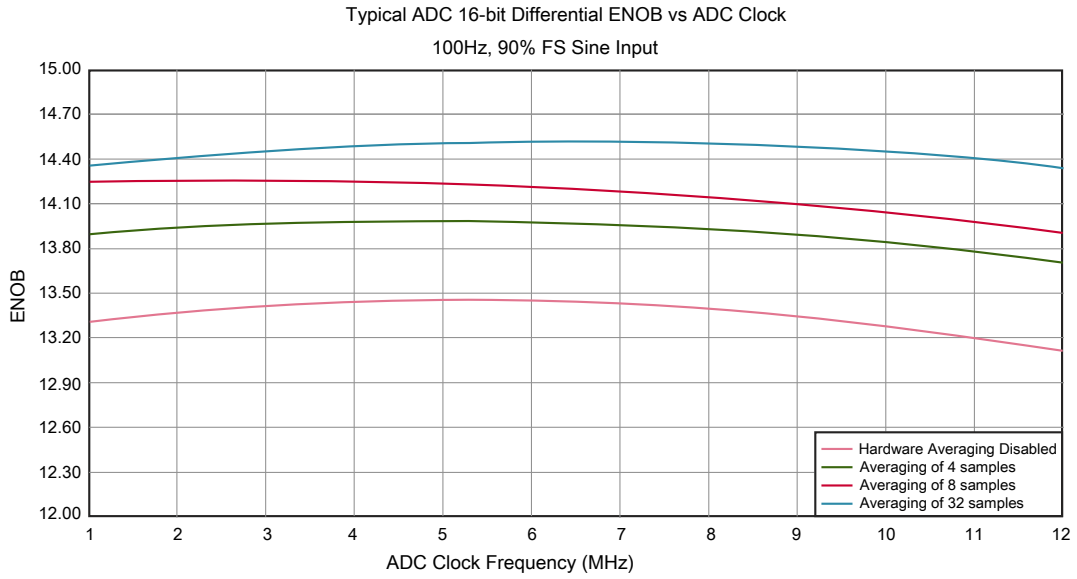


Figure 30. Typical ENOB vs. ADC_CLK for 16-bit differential mode

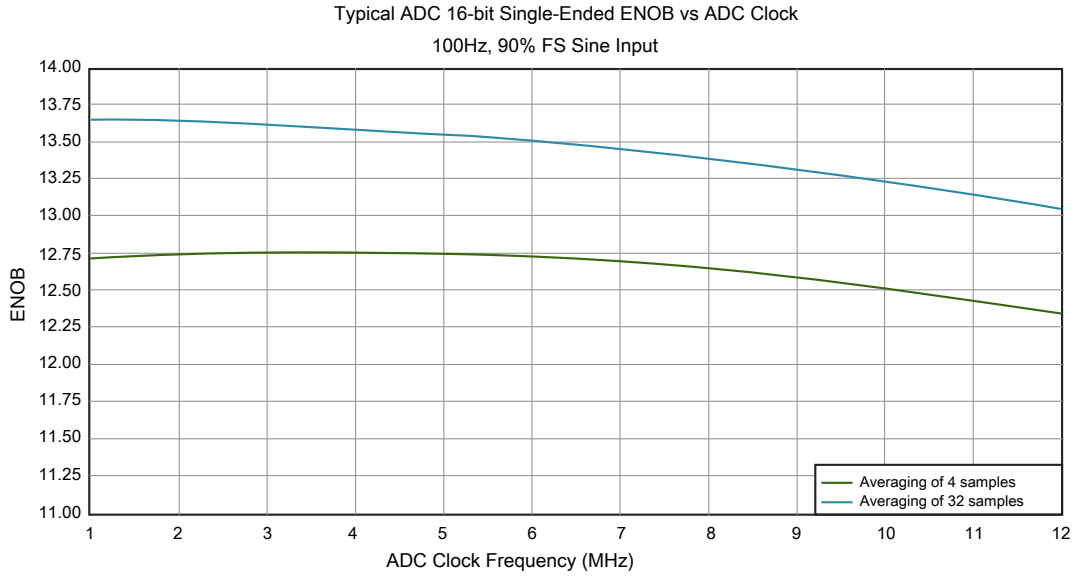


Figure 31. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

5.4.5.2 CMP and 6-bit DAC electrical specifications

Table 73. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

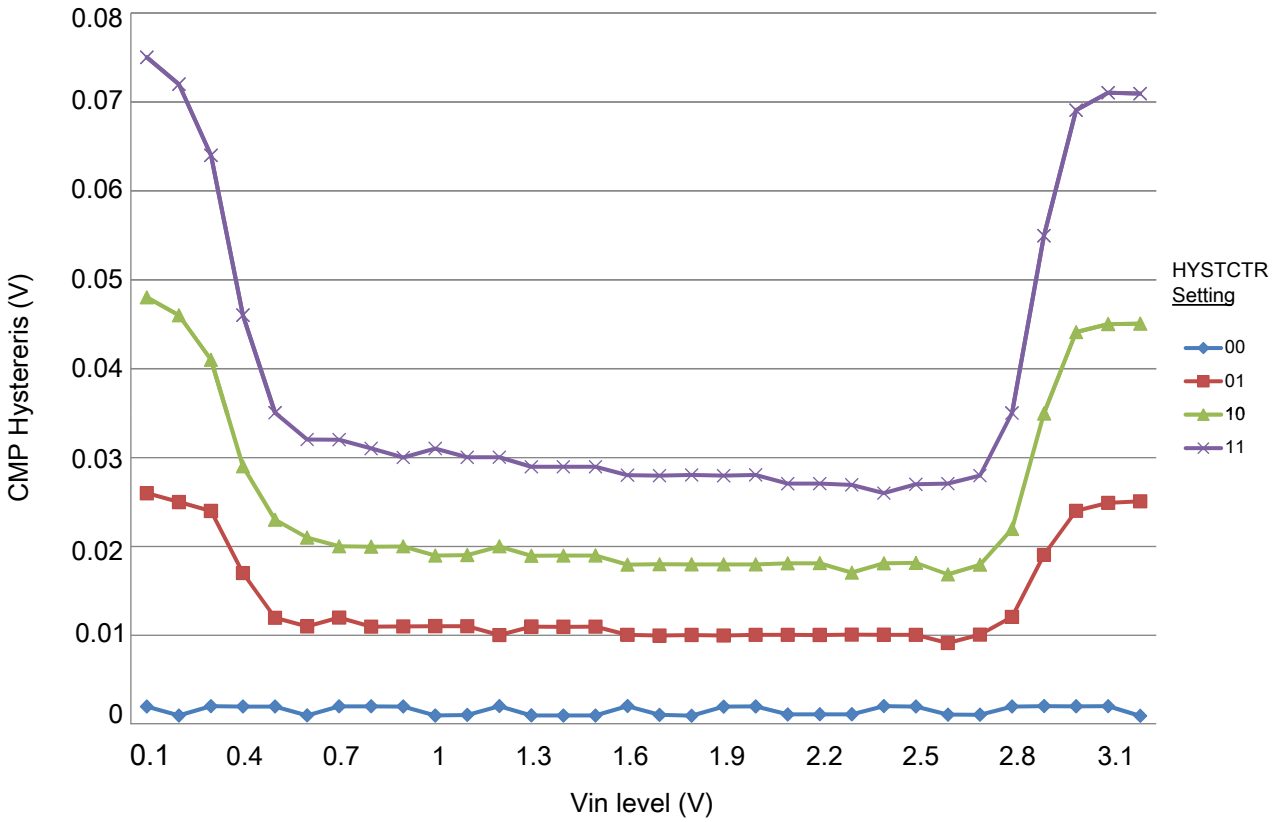


Figure 32. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

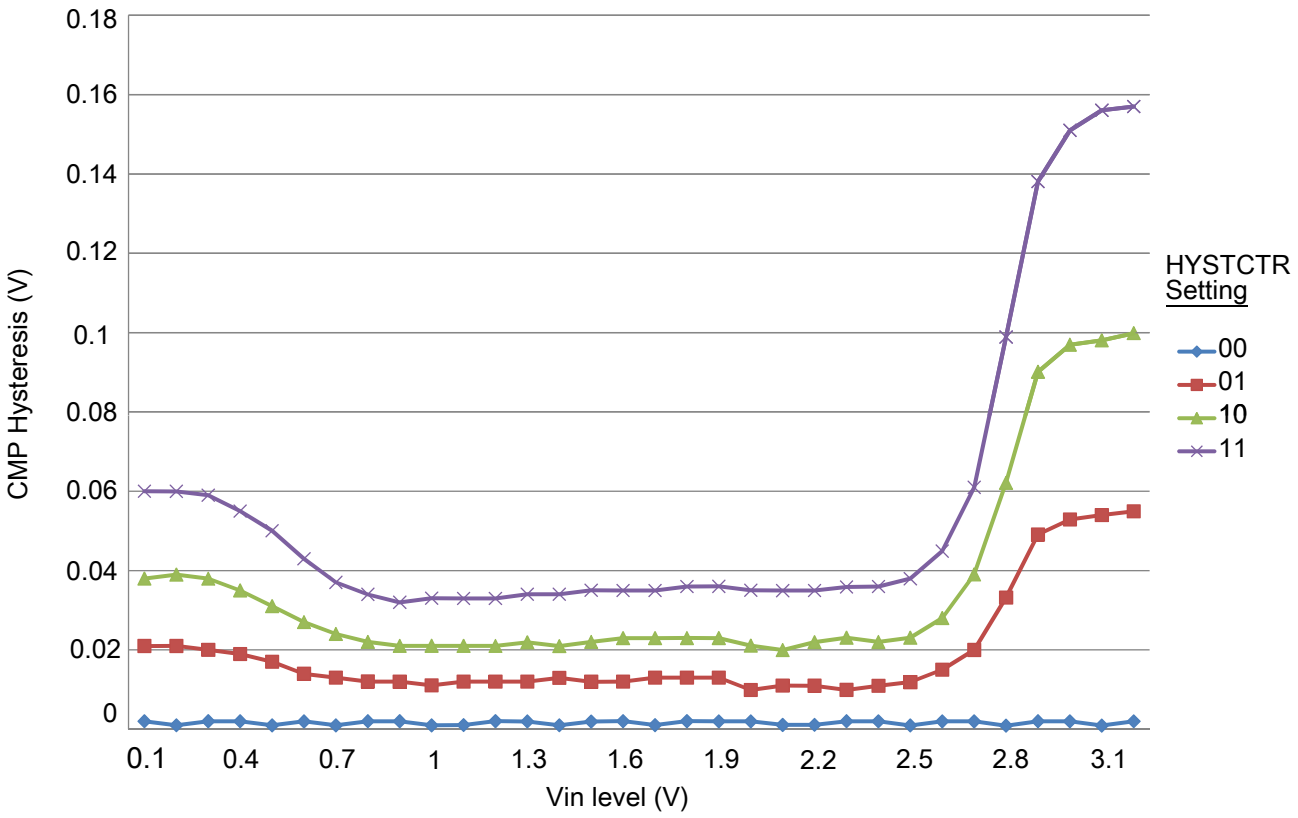


Figure 33. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

5.4.5.3 12-bit DAC electrical characteristics

5.4.5.3.1 12-bit DAC operating requirements

Table 74. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

5.4.5.3.2 12-bit DAC operating behaviors

Table 75. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
A_C	Offset aging coefficient	—	—	100	μV/yr	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

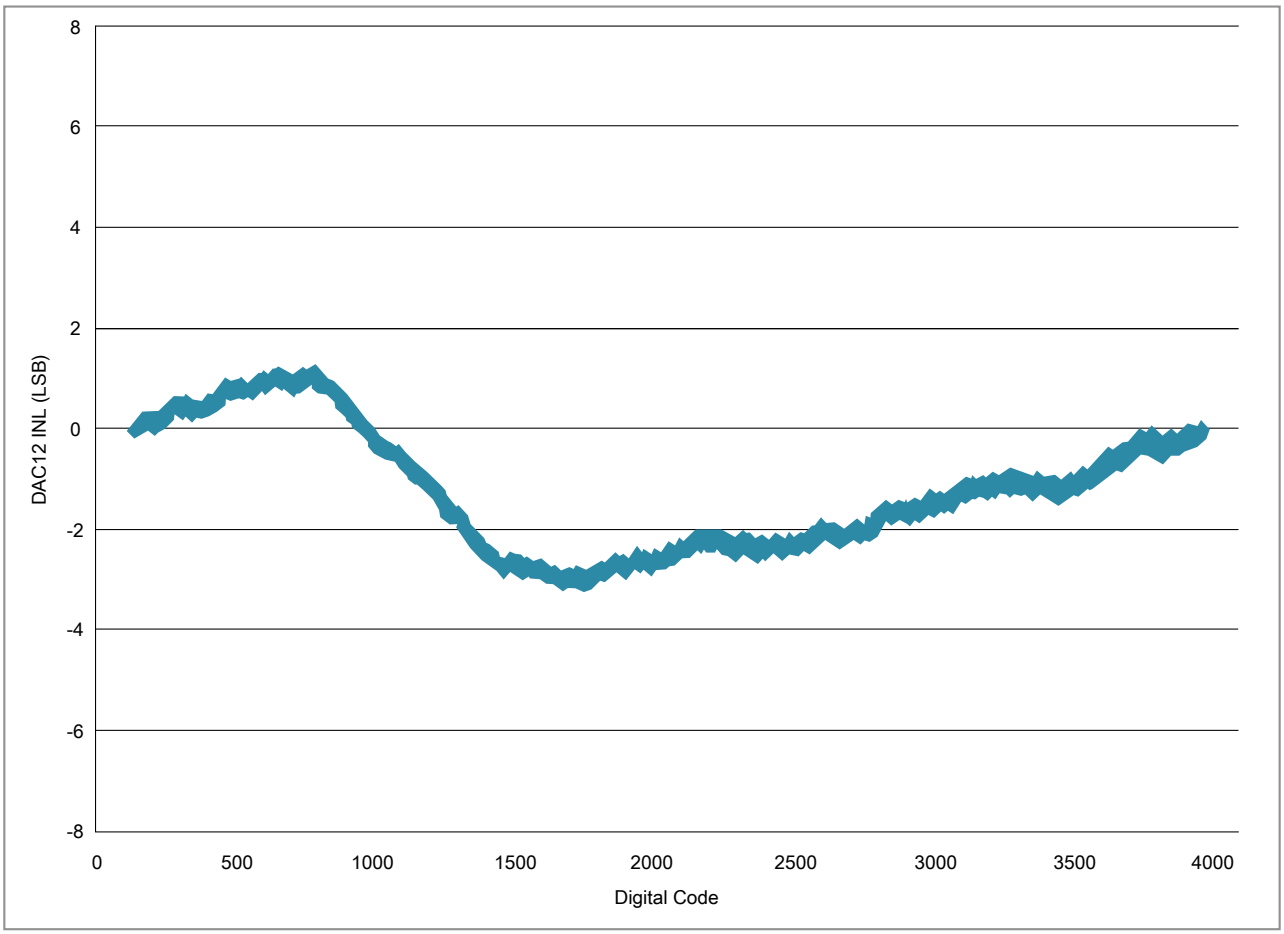


Figure 34. Typical INL error vs. digital code

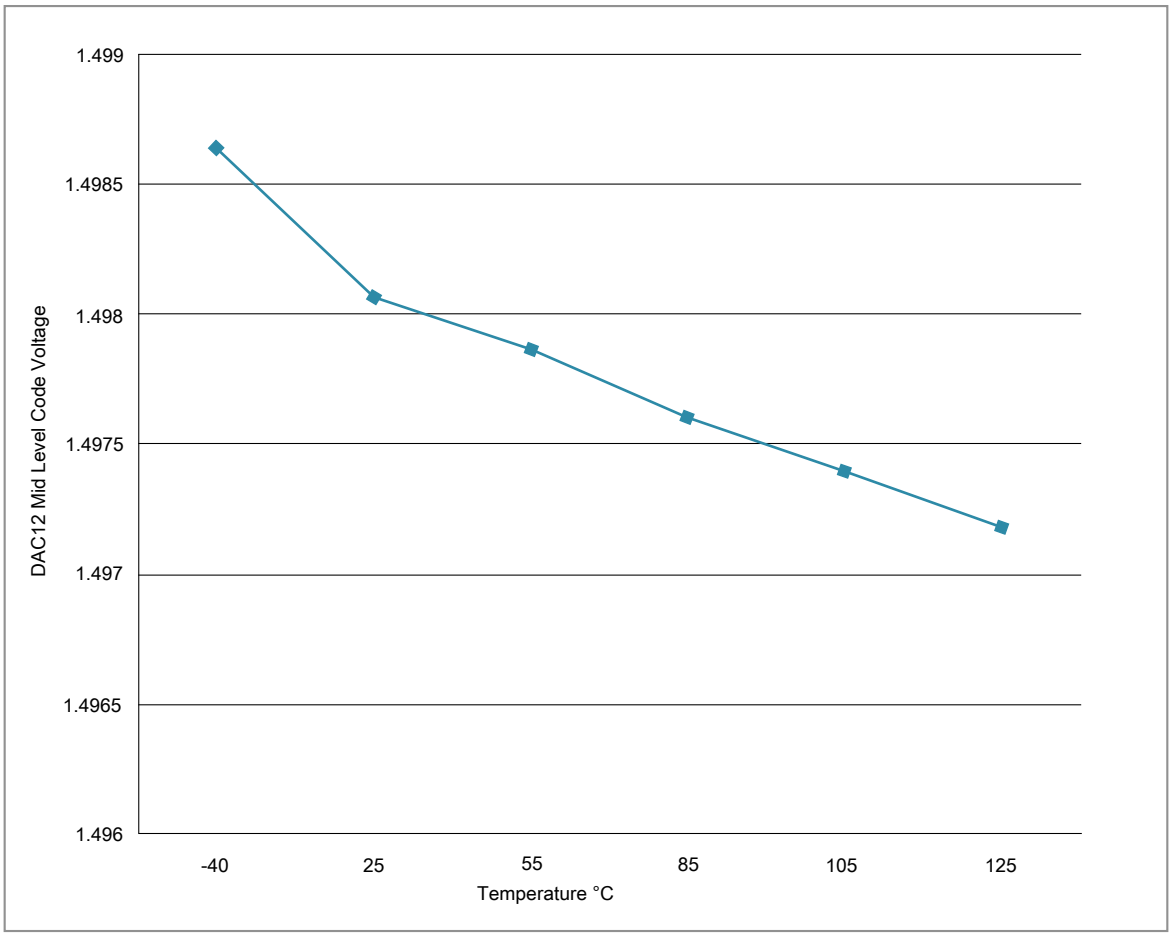


Figure 35. Offset at half scale vs. temperature

5.4.5.4 Voltage reference electrical specifications

Table 76. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 77. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	1
I_{bg}	Bandgap only current	—	—	80	μA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	— —	 200	 —	μV	1, 2
T_{stup}	Buffer startup time	—	—	100	μs	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 78. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 79. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

5.4.6 Timers

See General switching specifications.

5.4.7 Communication interfaces

5.4.7.1 EMV SIM specifications

Each EMV SIM module interface consists of a total of five pins.

The interface is designed to be used with synchronous Smart cards, meaning the EMV SIM module provides the clock used by the Smart card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the EMV SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the EMV SIM module provides to the Smart card is used by the Smart card to recover the clock from the data in the same manner as standard UART data exchanges. All five signals of the EMV SIM module are asynchronous with each other.

There are no required timing relationships between signals in normal mode. The smart card is initiated by the interface device; the Smart card responds with Answer to Reset. Although the EMV SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

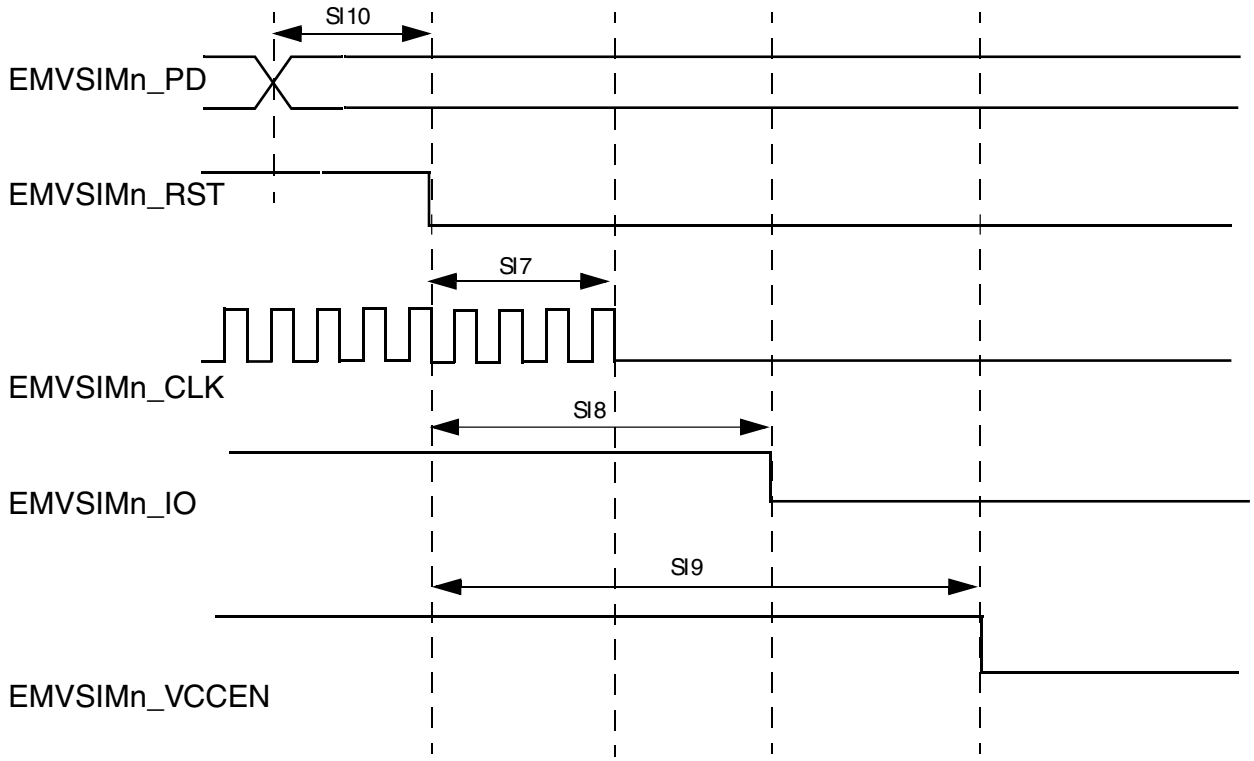


Figure 36. EMV SIM Clock Timing Diagram

The following table defines the general timing requirements for the EMV SIM interface.

Table 80. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min	Max	Unit
SI 1	EMV SIM clock frequency (EMVSIMn_CLK)[1]	S_{freq}	0.01	25	MHz
SI 2	EMV SIM clock rise time (EMVSIMn_CLK)[2]	S_{rise}	—	0.09 × (1/Sfreq)	ns
SI 3	EMV SIM clock fall time (EMVSIMn_CLK)[2]	S_{fall}	—	0.09 × (1/Sfreq)	ns
SI 4	EMV SIM input transition time (EMVSIMn_IO, EMVSIMn_PD)	S_{tran}	20	25	ns
Si 5	EMV SIM I/O rise time / fall time (EMVSIMn_IO)[3]	Tr/Tf	—	1	ns
Si 6	EMV SIM RST rise time / fall time (EMVSIMn_RST)[4]	Tr/Tf	—	1	ns

1. 50% duty cycle clock,
2. With C = 50 pF
3. With Cin = 30 pF, Cout = 30 pF,
4. With Cin = 30 pF,

5.4.7.1.1 EMV SIM Reset Sequences

Smart cards may have internal reset, or active low reset. The following subset describes the reset sequences in these two cases.

5.4.7.1.1.1 Smart Cards with Internal Reset

Following figure shows the reset sequence for Smart cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- The card must send a response on EMVSIMn_IO acknowledging the reset between 400–40000 clock cycles after T0.

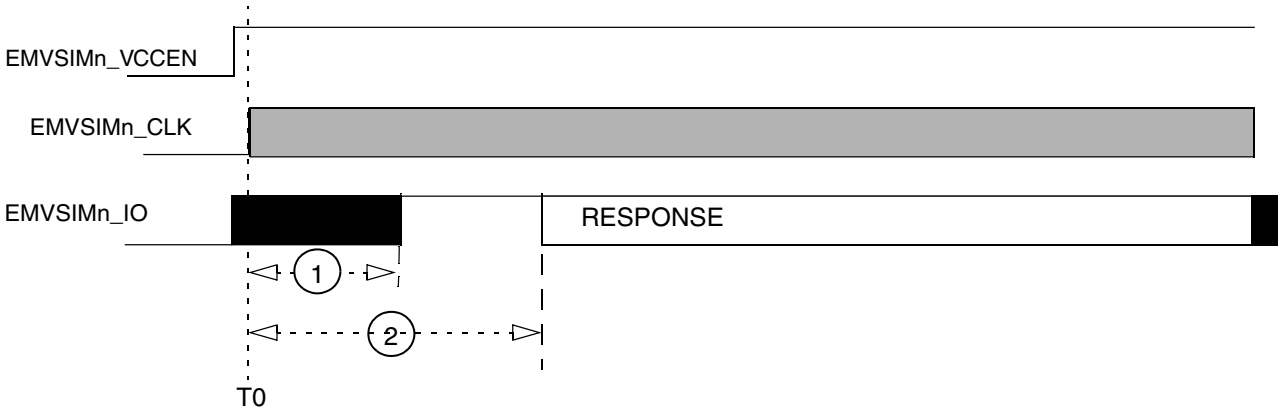


Figure 37. Internal Reset Card Reset Sequence

The following table defines the general timing requirements for the SIM interface.

Table 81. Timing Specifications, Internal Reset Card Reset Sequence

Ref	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles

5.4.7.1.1.2 Smart Cards with Active Low Reset

Following figure shows the reset sequence for Smart cards with active low reset. The reset sequence comprises the following steps::

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- EMVSIMn_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- EMVSIMn_RST is asserted (at time T1)
- EMVSIMn_RST must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on EMVSIMn_IO between 400 and 40,000 clock cycles after T1.

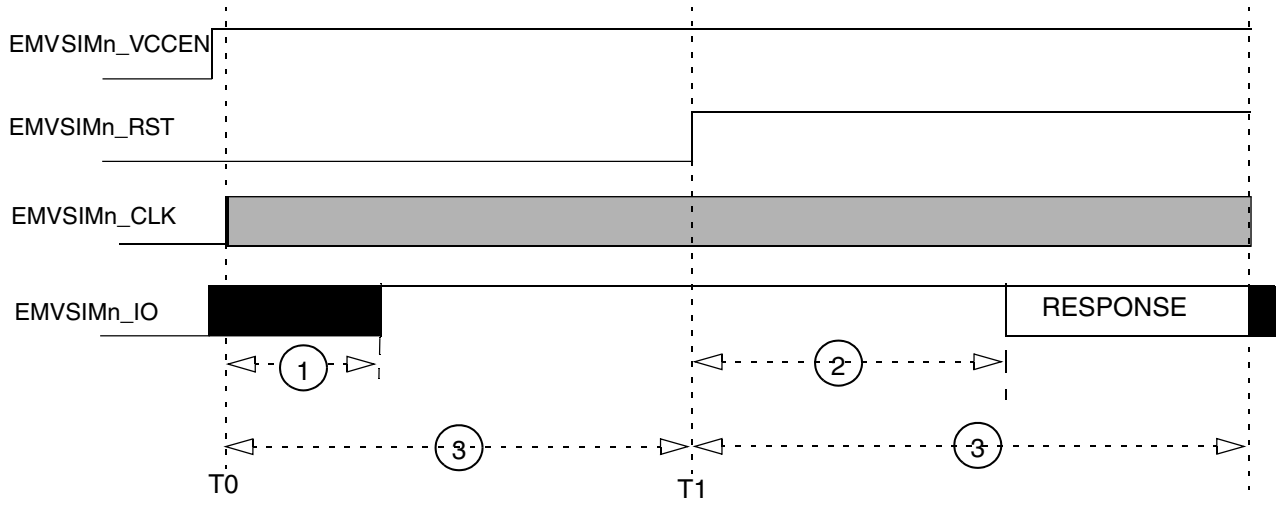


Figure 38. Active-Low-Reset Smart Card Reset Sequence

The following table defines the general timing requirements for the EMVSIM interface..

Table 82. Timing Specifications, Internal Reset Card Reset Sequence

Ref No	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles
3	40,000	—	EMVSIMx_CLK clock cycles

5.4.7.1.2 EMVSIM Power-Down Sequence

Following figure shows the EMV SIM interface power-down AC timing diagram.Table 83 table shows the timing requirements for parameters (SI7–SI10) shown in the figure. The power-down sequence for the EMV SIM interface is as follows:

- EMVSIMn_SIMPD port detects the removal of the Smart Card
- EMVSIMn_RST is negated
- EMVSIMn_CLK is negated
- EMVSIM_IO is negated
- EMVSIMx_VCCENy is negated

Each of the above steps requires one RTC CLK period (usually 32 kHz). Power-down may be initiated by a Smart card removal detection; or it may be launched by the processor.

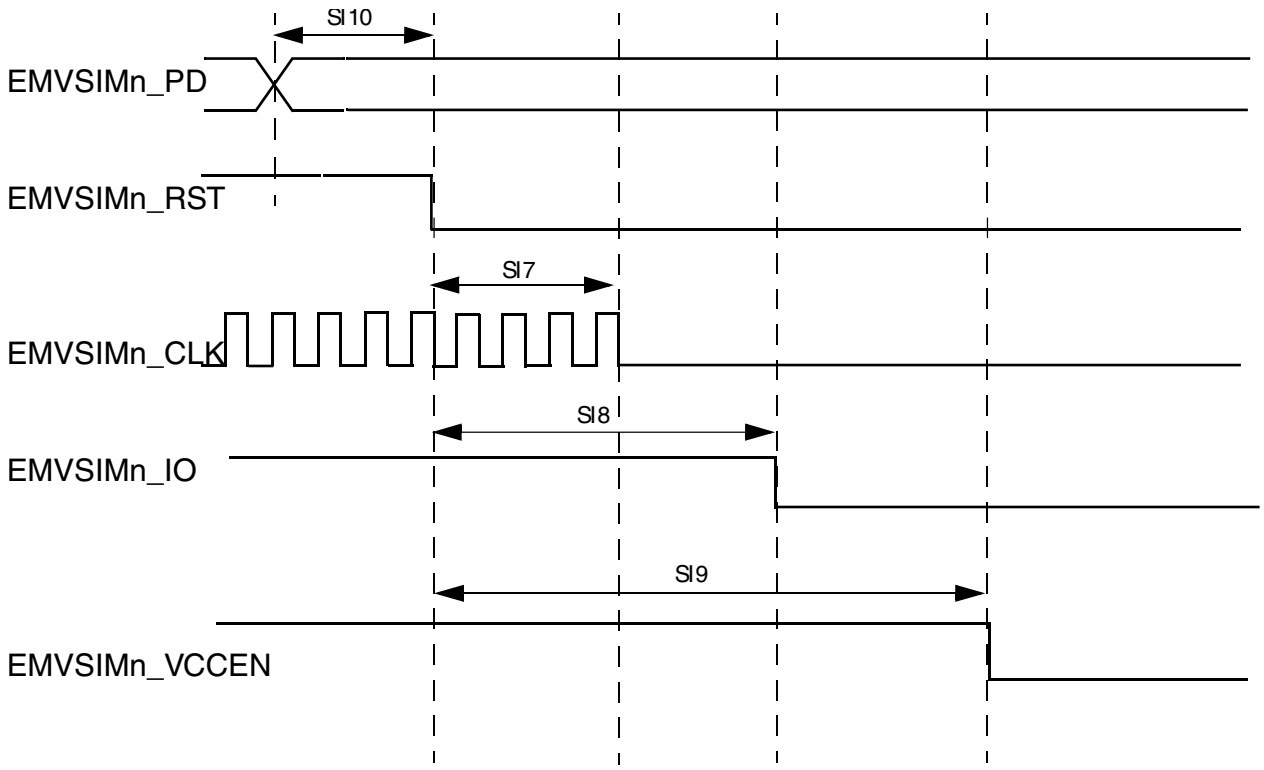


Figure 39. Smart Card Interface Power Down AC Timing

Table 83. Timing Requirements for Power-down Sequence

Ref No	Parameter	Symbol	Min	Max	Units
SI7	EMVSIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/ Frtcclk	1.1 × 1/Frtcclk	ns
SI8	EMVSIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/ Frtcclk	2.2 × 1/Frtcclk	ns
SI9	EMVSIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/ Frtcclk	3.3 × 1/Frtcclk	ns
SI10	EMVSIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/ Frtcclk	1.1 × 1/Frtcclk	ns

NOTE

Same timing is also followed when auto power down is initiated. See Reference Manual for reference.

5.4.7.2 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

NOTE

The MCGPLLCLK meets the USB jitter and signaling rate specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The IRC48M meets the USB jitter and signaling rate specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB signaling rate specifications for certification in Host mode operation.

5.4.7.3 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 84. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	24	MHz	1
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	15.0	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	1.0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15.8	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The SPI can run at a maximum frequency of 24 MHz serial clocks on PORTE interface, and up to 18 MHz on other PORT interfaces
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

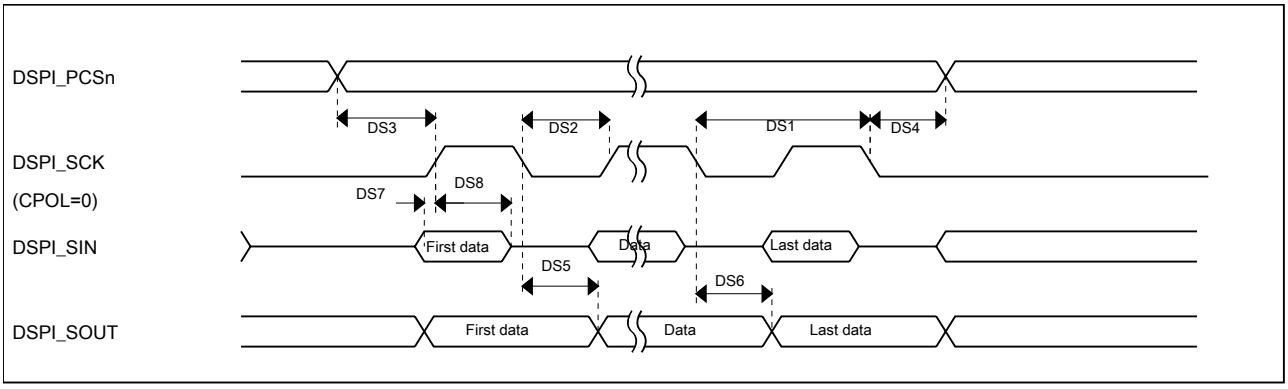


Figure 40. DSPI classic SPI timing — master mode

Table 85. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation	—	15 [1]	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.0	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.7	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven	—	13	ns
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	13	ns

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of system clock, for example, when system clock is 60MHz, SPI clock should not be greater than 10MHz.

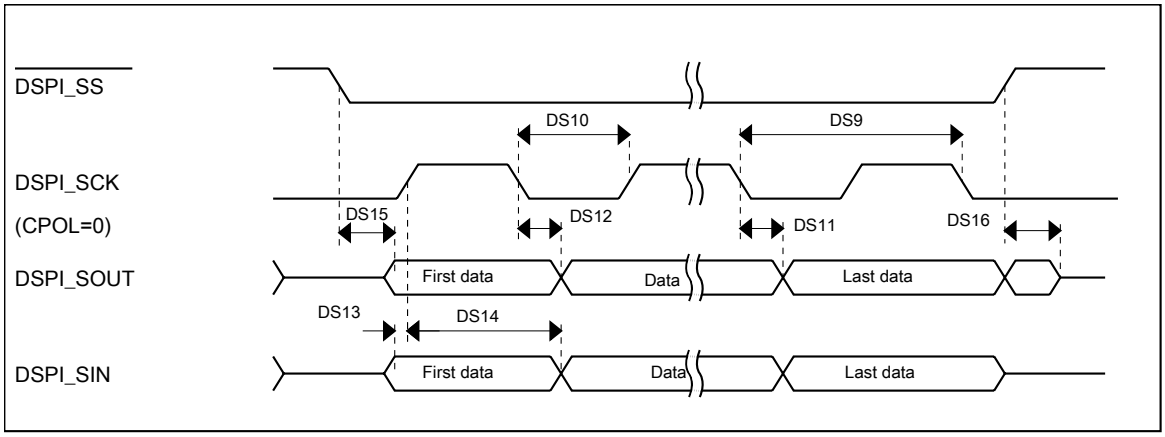


Figure 41. DSPI classic SPI timing — slave mode

5.4.7.4 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 86. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	16	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	1.0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

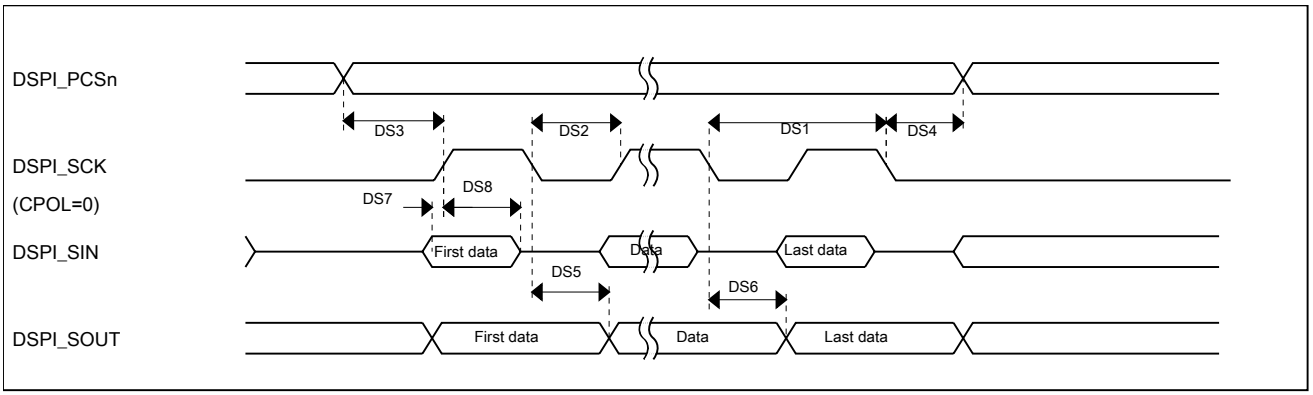


Figure 42. DSPI classic SPI timing — master mode

Table 87. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.1	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven	—	13.0	ns
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	13.0	ns

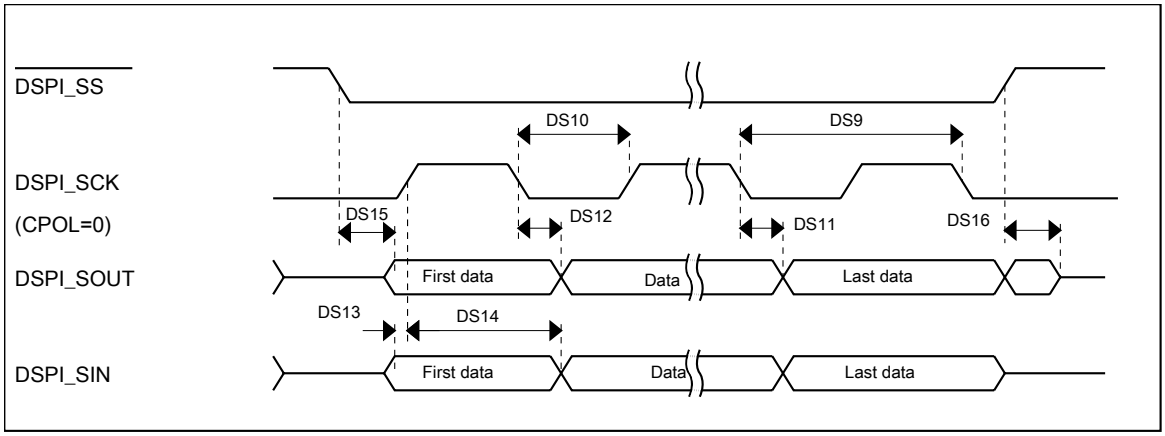


Figure 43. DSPI classic SPI timing — slave mode

5.4.7.5 Inter-Integrated Circuit Interface (I2C) timing

Table 88. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	μs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	μs

Table continues on the next page...

Table 88. I2C timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Data set-up time	t_{SU}; DAT	250[5]	—	100[3], [6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the normal drive pins and VDD ≥ 2.7 V.
2. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + $t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

To achieve 1MHz I2C clock rates, consider the following recommendations:

- To counter the effects of clock stretching, the I2C baud Rate select bits can be configured for faster than desired baud rate.
- Use high drive pad and DSE bit should be set in PORTx_PCRn register.
- Minimize loading on the I2C SDA and SCL pins to ensure fastest rise times for the SCL line to avoid clock stretching.
- Use smaller pull up resistors on SDA and SCL to reduce the RC time constant.

Table 89. I^2C 1Mbit/s timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f_{SCL}	0	1	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0	—	µs
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_r	20 +0.1C_b	120	ns

Table continues on the next page...

Table 89. I ^{2}C 1Mbit/s timing (continued)

Characteristic	Symbol	Minimum	Maximum	Unit
Fall time of SDA and SCL signals	t_f	20 +0.1C_b[1]	120	ns
Set-up time for STOP condition	t_{SU}; STO	0.26	—	μs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. C_b = total capacitance of the one bus line in pF.

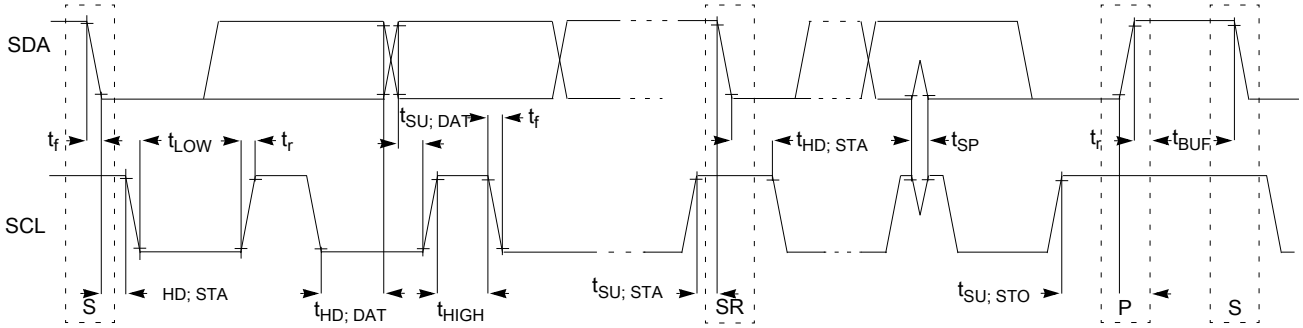


Figure 44. Timing definition for devices on the I^{2}C bus

5.4.7.6 LPUART switching specifications

See General switching specifications.

5.4.8 Human-machine interfaces (HMI)

5.4.8.1 TSI electrical specifications

Table 90. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V

6 Design considerations

6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

6.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

6.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 µF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.
- The USB_VDD voltage range is 3.0 V to 3.6 V. It is recommended to include a filter circuit with one bulk capacitor (no less than 2.2 µF) and one 0.1 µF capacitor at the USB_VDD pin to improve USB performance.

- Take special care to minimize noise levels on the VREFH/VREFL inputs. An option is to use the internal reference voltage (output 1.2 V typically) as the ADC reference.
- VDDIO_E, which is dedicated to powering PORTE, must be powered after VDD and must be greater than or equal to VDD voltage.

6.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

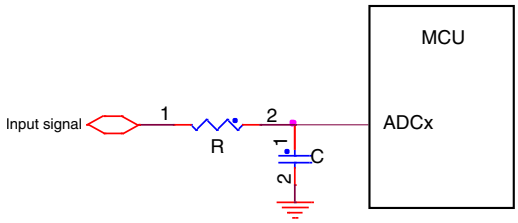


Figure 45. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

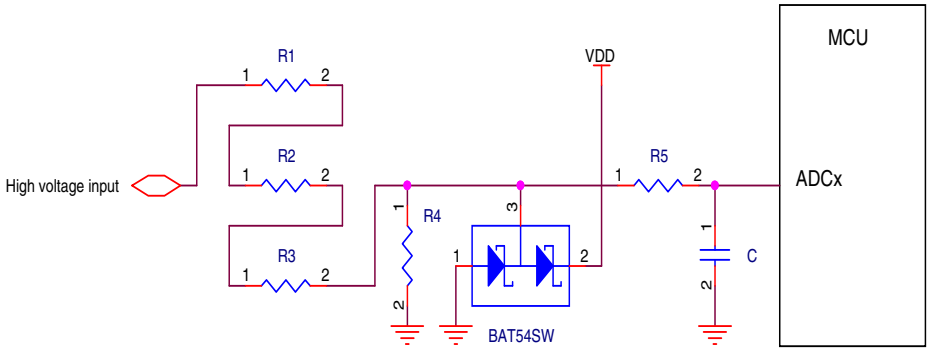


Figure 46. High voltage measurement with an ADC input

6.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 μF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

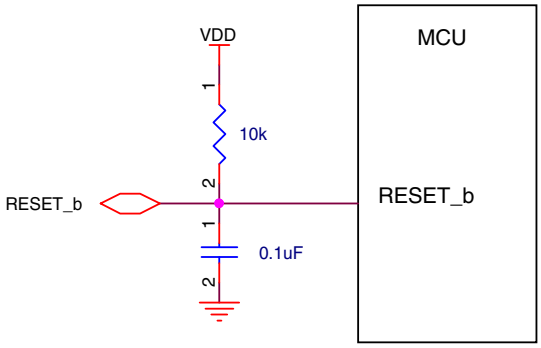


Figure 47. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

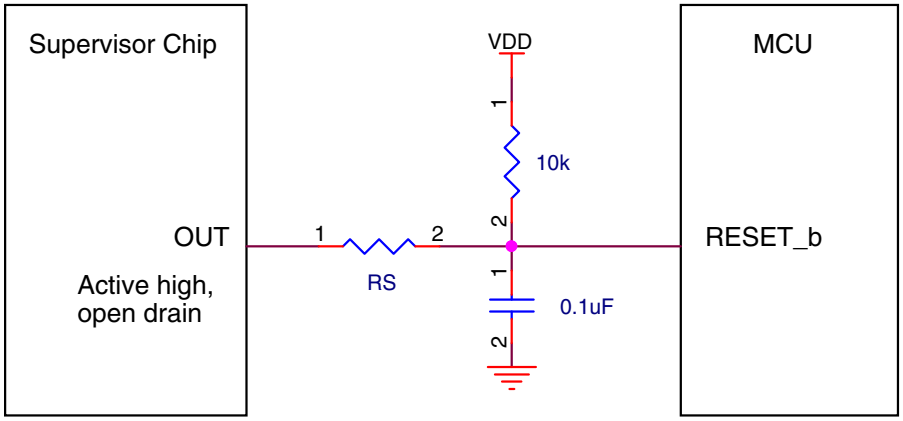


Figure 48. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

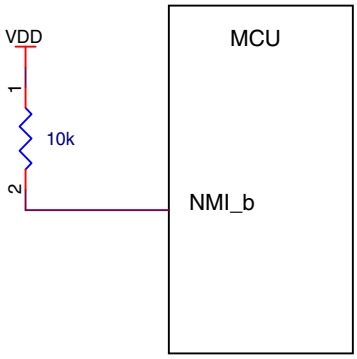


Figure 49. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

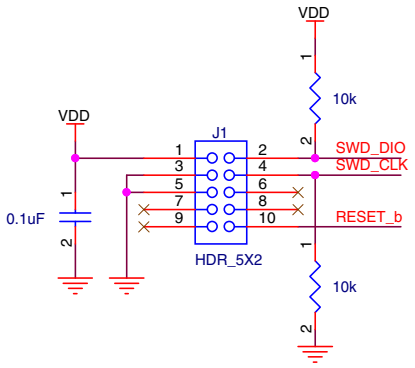


Figure 50. SWD debug interface

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See for pin selection.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

  If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect USB_VDD to ground through a 10 kΩ resistor if the USB module is not used.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16pF are sufficient for 32.768kHz crystals that have a 12.5pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

Table 91. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768kHz), low power	Diagram 1
Low frequency (32.768kHz), high gain	Diagram 2, Diagram 4
High frequency (3-32MHz), low power	Diagram 3
High frequency (3-32MHz), high gain	Diagram 4

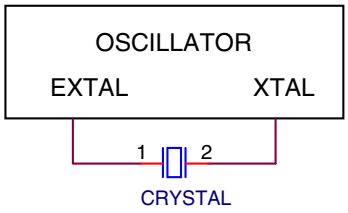


Figure 51. Crystal connection – Diagram 1

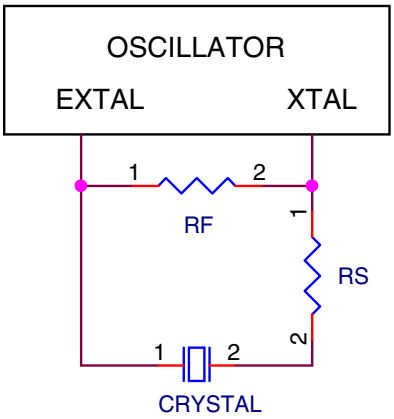


Figure 52. Crystal connection – Diagram 2

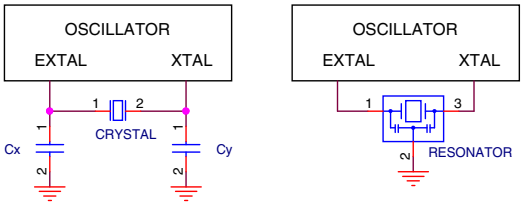


Figure 53. Crystal connection – Diagram 3

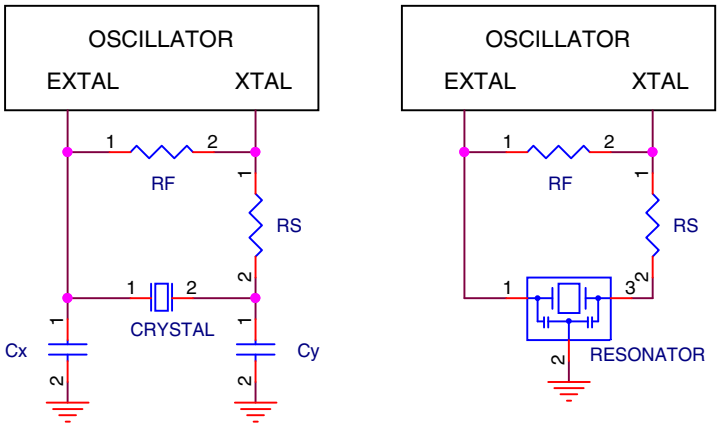


Figure 54. Crystal connection – Diagram 4

6.2 Software considerations

All Kinetis MCUs are supported by comprehensive NXP and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.nxp.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- NXP Freedom Development Platform: http://www.nxp.com/freedom
- Tower System Development Platform: http://www.nxp.com/tower

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.nxp.com/kds
- Partner IDEs: http://www.nxp.com/kide

Development Tools

- PEG Graphics Software: http://www.nxp.com/peg
- Processor Expert Software and Embedded Components: http://www.nxp.com/processorexpert)

Run-time Software

- Kinetis SDK: http://www.nxp.com/ksdk
- Kinetis Bootloader: http://www.nxp.com/kboot
- ARM mbed Development Platform: http://www.nxp.com/mbed
- MQX RTOS: http://www.nxp.com/mqx

For all other partner-developed software and tools, visit http://www.nxp.com/partners.

6.3 Soldering temperature

Base on JEDEC/IPC J-STD-020 Industry Standard, refer to AN3298: Solder Joint Temperature and Package Peak Temperature for soldering guideline of different packages.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KL##	Kinetis KL family	• KL82
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 128 = 128 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm)

Table continues on the next page...

Field	Description	Values
		• MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm)
CC	Maximum CPU frequency (MHz)	• 7 = 72 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKL82Z128VMC7

8 Revision history

The following table provides a revision history for this document.

Table 92. Revision history

Rev. No.	Date	Substantial Changes
2	11/2015	Initial public release
3	08/2016	• Updated the specification of frequency of operation in DSPI switching specifications (limited voltage range). • Updated USB electrical specifications
4	12/2016	• Updated the Pin properties. • Added a note to the T_A in the Thermal operating requirements • Updated the description of R_{PU} and R_{PD} in the Voltage and current operating behaviors

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