



**THE DATASHEET OF
AD8418ABRMZ-RL**



FEATURES

- Typical 0.1 $\mu\text{V}/^\circ\text{C}$ offset drift
- Maximum $\pm 200 \mu\text{V}$ voltage offset over full temperature range
- 2.7 V to 5.5 V power supply operating range
- Electromagnetic interference (EMI) filters included
- High common-mode input voltage range
 - 2 V to +70 V, continuous operation
 - 3 V to +80 V, continuous survival
- Minimum DC common-mode rejection ratio (CMRR): 90 dB
- Initial gain = 20 V/V
- Wide operating temperature range
 - AD8418AWB** and **AD8418AB**: -40°C to $+125^\circ\text{C}$
 - AD8418AWH**: -40°C to $+150^\circ\text{C}$
- Bidirectional operation
- Available in 8-lead SOIC_N, 8-lead MSOP, and FMEA tolerant 10-lead MSOP pinout
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- High-side current sensing in
 - Motor controls
 - Solenoid controls
 - Power management
- Low-side current sensing
- Diagnostic protection

GENERAL DESCRIPTION

The **AD8418A** is a high voltage, high resolution current shunt amplifier. It features an initial gain of 20 V/V, with a maximum $\pm 0.15\%$ gain error over the entire temperature range. The buffered output voltage directly interfaces with any typical converter. The **AD8418A** offers excellent input common-mode rejection from -2 V to $+70 \text{ V}$. The **AD8418A** performs bidirectional current measurements across a shunt resistor in a variety of automotive and industrial applications, including motor control, power management, and solenoid control.

The **AD8418A** offers breakthrough performance throughout the -40°C to $+150^\circ\text{C}$ temperature range. It features a zero drift core, which leads to a typical offset drift of $0.1 \mu\text{V}/^\circ\text{C}$ throughout the operating temperature range and the common-mode voltage range. The **AD8418A** is qualified for automotive applications. The device includes EMI filters and patented circuitry to enable output accuracy with pulse-width modulation (PWM) type input common-mode voltages. The typical input offset voltage is $\pm 100 \mu\text{V}$. The **AD8418A** is offered in an 8-lead MSOP and an 8-lead SOIC_N package with a 10-lead MSOP pinout option engineered for failure mode and effects analysis (FMEA).

Table 1. Related Devices

| Part No. | Description |
|------------------------|--|
| AD8205 | Current sense amplifier, gain = 50 |
| AD8206 | Current sense amplifier, gain = 20 |
| AD8207 | High accuracy current sense amplifier, gain = 20 |
| AD8210 | High speed current sense amplifier, gain = 20 |
| AD8417 | High accuracy current sense amplifier, gain = 60 |

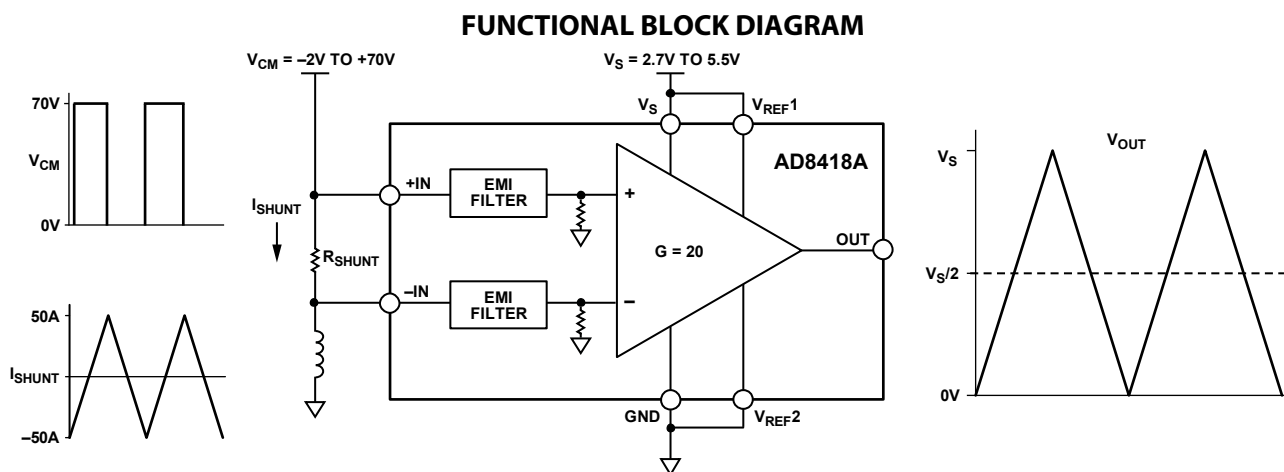


Figure 1.

Rev. E

[Document Feedback](#)

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TABLE OF CONTENTS

| | | | |
|---|----|---|----|
| Features | 1 | Bidirectional Operation | 12 |
| Applications | 1 | External Referenced Output | 13 |
| General Description | 1 | Splitting the Supply | 13 |
| Functional Block Diagram | 1 | Splitting an External Reference | 13 |
| Revision History | 2 | Applications Information | 14 |
| Specifications | 3 | Motor Control | 14 |
| Absolute Maximum Ratings | 4 | Solenoid Control | 15 |
| ESD Caution | 4 | Pinout Option Engineered for FMEA | 16 |
| Pin Configuration and Function Descriptions | 5 | Outline Dimensions | 17 |
| Typical Performance Characteristics | 6 | Ordering Guide | 18 |
| Theory of Operation | 11 | Automotive Products | 18 |
| Output Offset Adjustment | 12 | | |
| Unidirectional Operation | 12 | | |

REVISION HISTORY

6/2020—Rev. D to Rev. E

| | |
|---|----|
| Changes to Features Section and General Description Section | 1 |
| Changes to Figure 2 Caption and Table 4 Title | 6 |
| Added Figure 3 and Table 5; Renumbered Sequentially | 6 |
| Added Pinout Option Engineered for FMEA Section, Table 6, and Table 7 | 17 |
| Updated Outline Dimensions | 19 |
| Changes to Ordering Guide | 19 |

12/2018—Rev. C to Rev. D

| | |
|-----------------------------------|---|
| Changes to Features Section | 1 |
| Changes to Table 3 | 4 |

5/2018—Rev. B to Rev. C

| | |
|--|---|
| Changes to Input Bias Current Parameter, Table 2 | 3 |
| Changes to Figure 20 | 8 |

4/2017—Rev. A to Rev. B

| | |
|---|---|
| Changes to Features Section and General Description Section | 1 |
| Changes to Table 2 | 3 |
| Changes to Table 3 | 4 |
| Change to Figure 18 | 8 |
| Added Figure 19 and Figure 20; Renumbered Sequentially | 8 |

12/2014—Rev. 0 to Rev. A

| | |
|---|-----------|
| Added AD8418AWH | Universal |
| Changes to Features Section and General Description Section | 1 |
| Changes to Specifications Section and Table 2 | 3 |
| Changes to Table 3 | 4 |
| Changes to Ordering Guide | 16 |

11/2013—Revision 0: Initial Version

SPECIFICATIONS

$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (operating temperature range) for the [AD8418AWB](#), $T_A = -40^\circ\text{C}$ to $+150^\circ\text{C}$ for the [AD8418AWH](#), $V_S = 5\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|---|--------|-----------|---------------|------------------------------|
| GAIN | | | | | |
| Initial | | | 20 | | V/V |
| Error Over Temperature | Specified temperature range | | | ± 0.15 | % |
| Gain vs. Temperature | | -5 | | +5 | ppm/ $^\circ\text{C}$ |
| VOLTAGE OFFSET | | | | | |
| Offset Voltage, Referred to the Input, RTI | 25 $^\circ\text{C}$ | | ± 100 | | μV |
| Over Temperature, RTI | Specified temperature range | | | ± 200 | μV |
| Offset Drift | | -0.4 | +0.1 | +0.4 | $\mu\text{V}/^\circ\text{C}$ |
| INPUT | | | | | |
| Input Bias Current | | | 130 | | μA |
| | +IN = -IN = 12 V, $V_{\text{REF}1} = V_{\text{REF}2} = 2.5\text{ V}$, AD8418AWB | | | 260 | μA |
| Input Voltage Range | Common mode, continuous | -2 | | +70 | V |
| Common-Mode Rejection Ratio (CMRR) | Specified temperature range, $f = \text{dc}$ $f = \text{dc}$ to 10 kHz | 90 | 100 | | dB |
| | | | 86 | | dB |
| OUTPUT | | | | | |
| Output Voltage Range | $R_L = 25\text{ k}\Omega$ | 0.032 | | $V_S - 0.032$ | V |
| Output Resistance | | | 2 | | Ω |
| Maximum Capacitive Load | No continuous oscillation | 0 | | 500 | pF |
| DYNAMIC RESPONSE | | | | | |
| Small Signal -3 dB Bandwidth | | | 250 | | kHz |
| Slew Rate | | | 1 | | V/ μs |
| NOISE | | | | | |
| 0.1 Hz to 10 Hz (RTI) | | | 2.3 | | $\mu\text{V p-p}$ |
| Spectral Density, 1 kHz, RTI | | | 110 | | nV/ $\sqrt{\text{Hz}}$ |
| OFFSET ADJUSTMENT | | | | | |
| Ratiometric Accuracy ¹ | Divider to supplies | 0.4985 | | 0.5015 | V/V |
| Accuracy, Referred to the Output (RTO) | Voltage applied to $V_{\text{REF}1}$ and $V_{\text{REF}2}$ in parallel | | | ± 1 | mV/V |
| Output Offset Adjustment Range | $V_S = 5\text{ V}$ | 0.032 | | $V_S - 0.032$ | V |
| POWER SUPPLY | | | | | |
| Operating Range | | 2.7 | | 5.5 | V |
| Quiescent Current Over Temperature | $V_{\text{OUT}} = 0.1\text{ V dc}$ AD8418AWB and AD8418AB AD8418AWH | | | 4.1 | mA |
| | | | | 4.2 | mA |
| Power Supply Rejection Ratio | | 80 | | | dB |
| TEMPERATURE RANGE | | | | | |
| For Specified Performance | Operating temperature range AD8418AWB and AD8418AB AD8418AWH | -40 | | +125 | $^\circ\text{C}$ |
| | | -40 | | +150 | $^\circ\text{C}$ |

¹ The offset adjustment is ratiometric to the power supply when $V_{\text{REF}1}$ and $V_{\text{REF}2}$ are used as a divider between the supplies.

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|----------------------------------|-------------------|
| Supply Voltage | 6 V |
| Input Voltage Range | |
| Common-Mode | −3 V to +80 V |
| Differential | 5.5 V (magnitude) |
| Reverse Supply Voltage | 0.3 V |
| ESD Human Body Model (HBM) | ±2000 V |
| Operating Temperature Range | |
| AD8418AWB and AD8418AB | −40°C to +125°C |
| AD8418AWH | −40°C to +150°C |
| Storage Temperature Range | −65°C to +150°C |
| Output Short-Circuit Duration | Indefinite |
| SOIC Package | |
| θ_{JA} Thermal Resistance | 127.4°C/W |
| MSOP Package | |
| θ_{JA} Thermal Resistance | 134.5°C/W |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

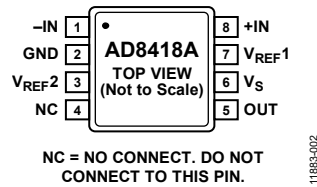


Figure 2. 8-lead MSOP and 8-lead SOIC Pin Configuration

Table 4. 8-lead MSOP and 8-lead SOIC Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-------------------|---|
| 1 | -IN | Negative Input. |
| 2 | GND | Ground. |
| 3 | V _{REF2} | Reference Input 2. |
| 4 | NC | No Connect. Do not connect to this pin. |
| 5 | OUT | Output. |
| 6 | V _S | Supply. |
| 7 | V _{REF1} | Reference Input 1. |
| 8 | +IN | Positive Input. |

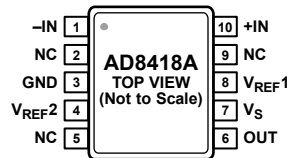


Figure 3. 10-lead MSOP Pin Configuration

Table 5. 10-lead MSOP Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-------------------|---|
| 1 | -IN | Negative Input. |
| 2, 5, 9 | NC | No Connect. Do not connect to this pin. |
| 3 | GND | Ground. |
| 4 | V _{REF2} | Reference Input 2. |
| 6 | OUT | Output. |
| 7 | V _S | Supply. |
| 8 | V _{REF1} | Reference Input 1. |
| 10 | +IN | Positive Input. |

TYPICAL PERFORMANCE CHARACTERISTICS

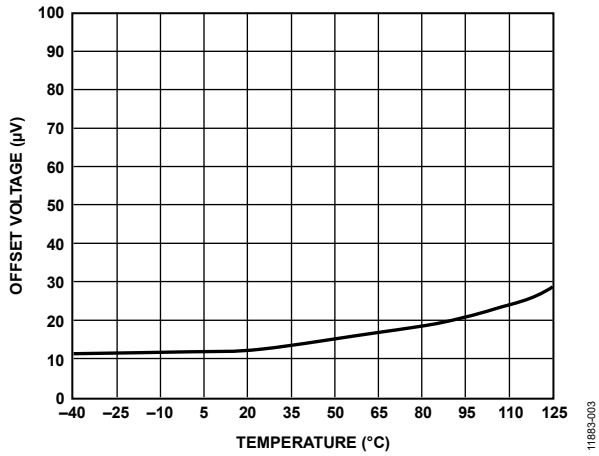


Figure 4. Typical Offset Drift vs. Temperature

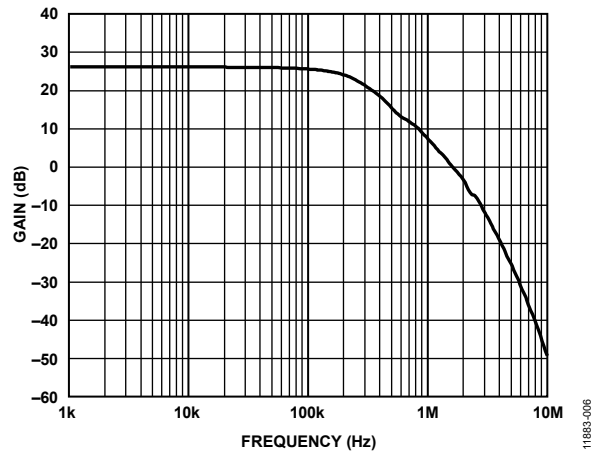


Figure 7. Typical Small Signal Bandwidth ($V_{OUT} = 200\text{ mV p-p}$)

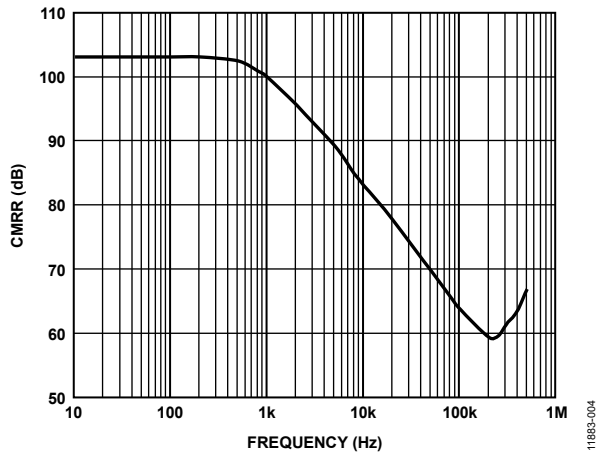


Figure 5. Typical CMRR vs. Frequency

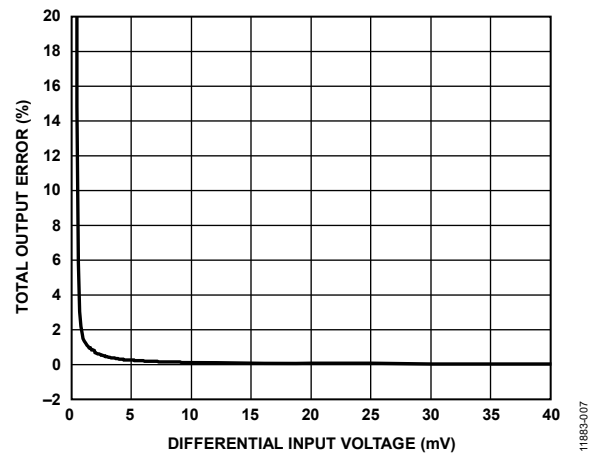


Figure 8. Total Output Error vs. Differential Input Voltage

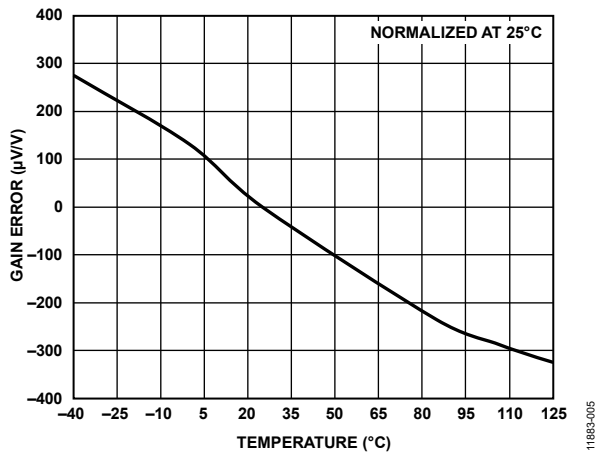


Figure 6. Typical Gain Error vs. Temperature

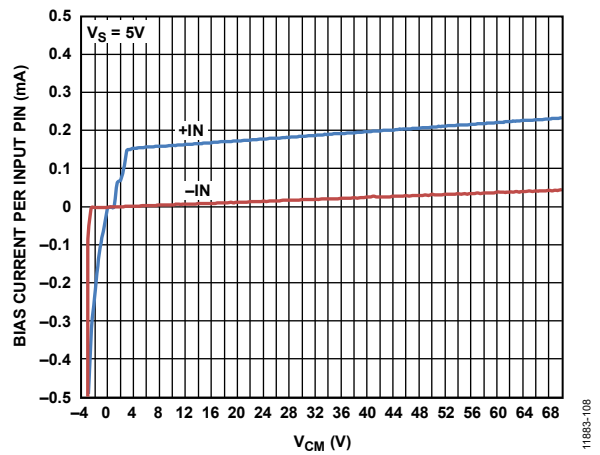


Figure 9. Bias Current per Input Pin vs. Common-Mode Voltage (V_{CM})

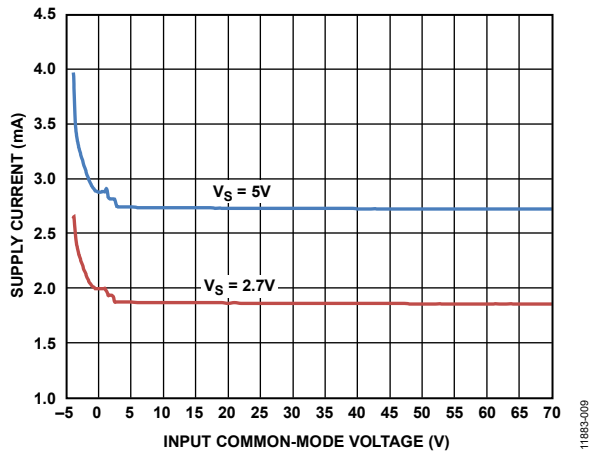


Figure 10. Supply Current vs. Input Common-Mode Voltage

11883-009

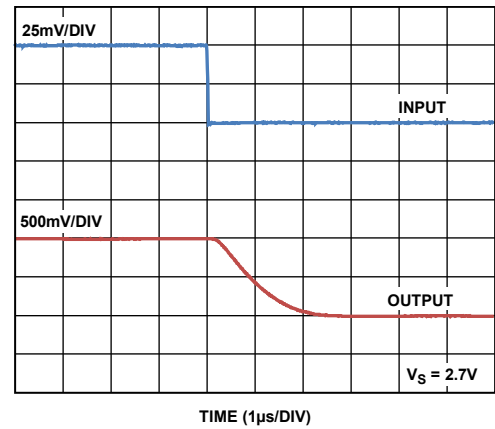


Figure 13. Fall Time ($V_S = 2.7V$)

11883-012

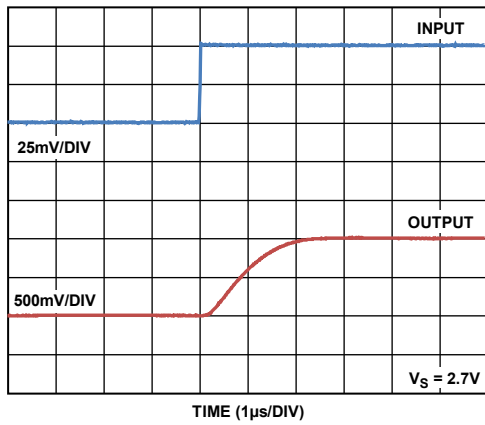


Figure 11. Rise Time ($V_S = 2.7V$)

11883-010

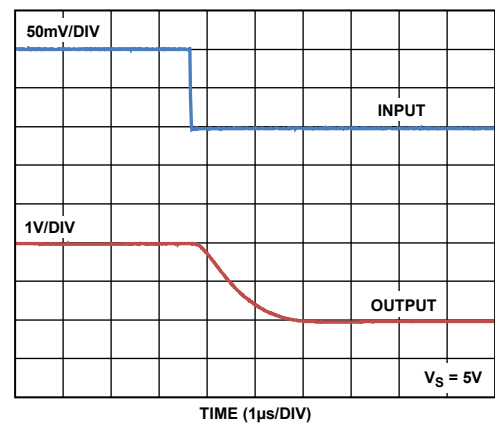


Figure 14. Fall Time ($V_S = 5V$)

11883-013

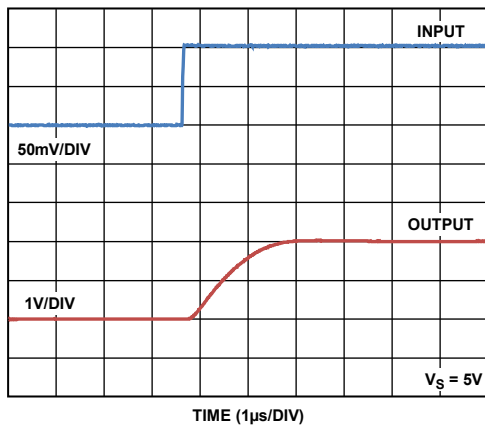


Figure 12. Rise Time ($V_S = 5V$)

11883-011

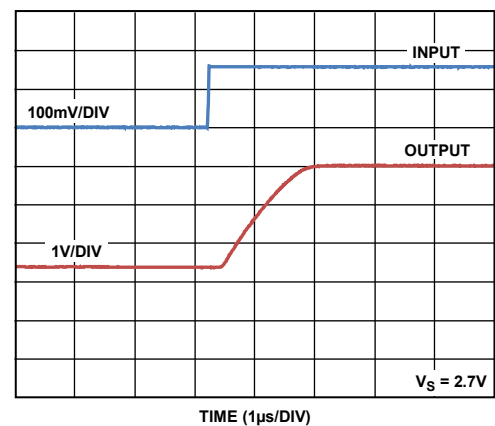


Figure 15. Differential Overload Recovery, Rising ($V_S = 2.7V$)

11883-014

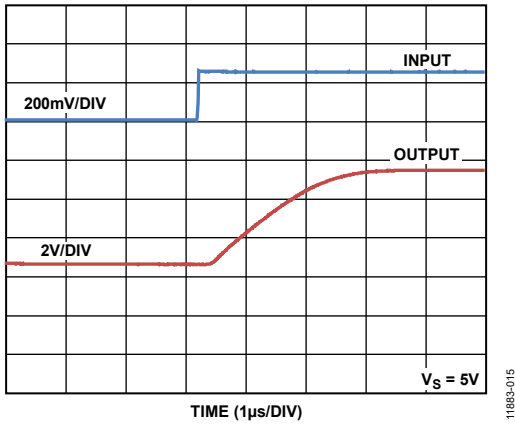


Figure 16. Differential Overload Recovery, Rising ($V_S = 5\text{ V}$)

11883-015

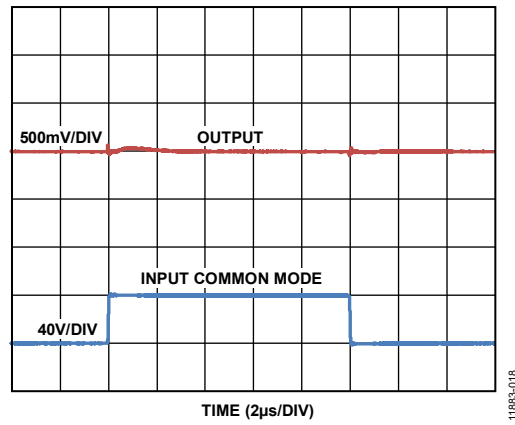


Figure 19. Input Common-Mode Step Response Large Scale ($V_S = 5\text{ V}$, Inputs Shorted)

11883-018

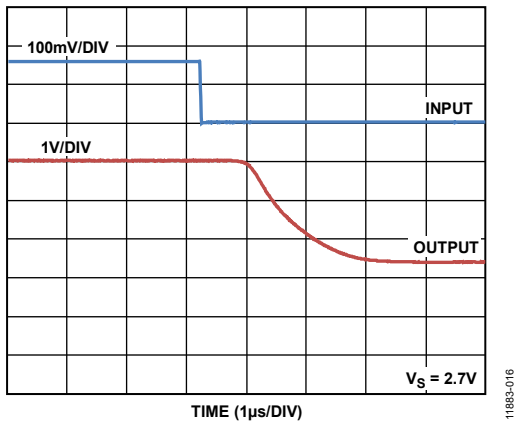


Figure 17. Differential Overload Recovery, Falling ($V_S = 2.7\text{ V}$)

11883-016

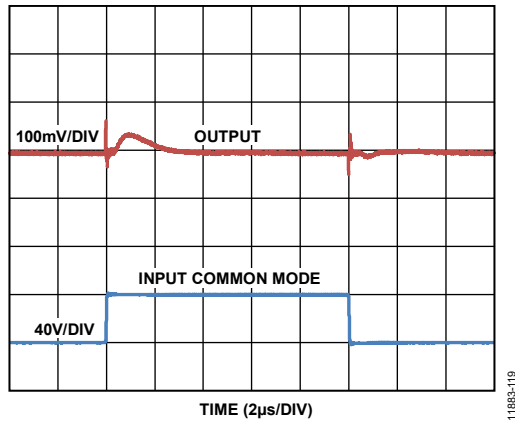


Figure 20. Input Common-Mode Step Response Small Scale ($V_S = 5\text{ V}$, Inputs Shorted)

11883-019

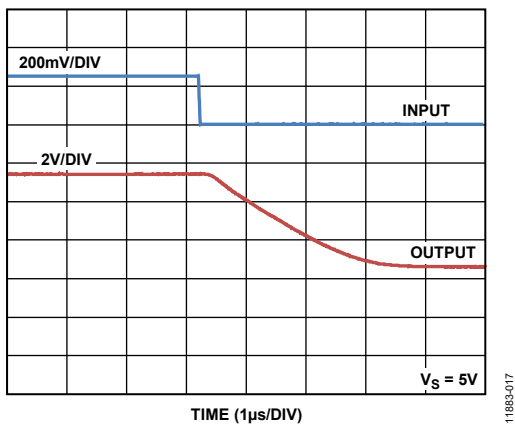


Figure 18. Differential Overload Recovery, Falling ($V_S = 5\text{ V}$)

11883-017

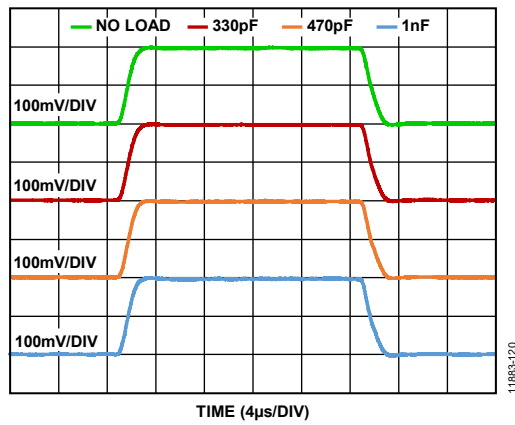


Figure 21. Small Signal Response for Various Capacitive Loads

11883-020

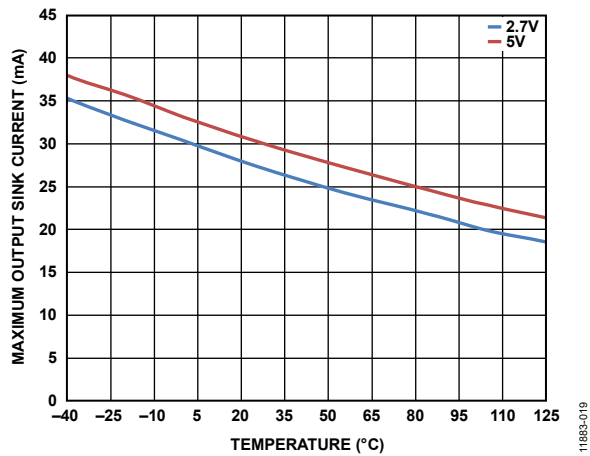


Figure 22. Maximum Output Sink Current vs. Temperature

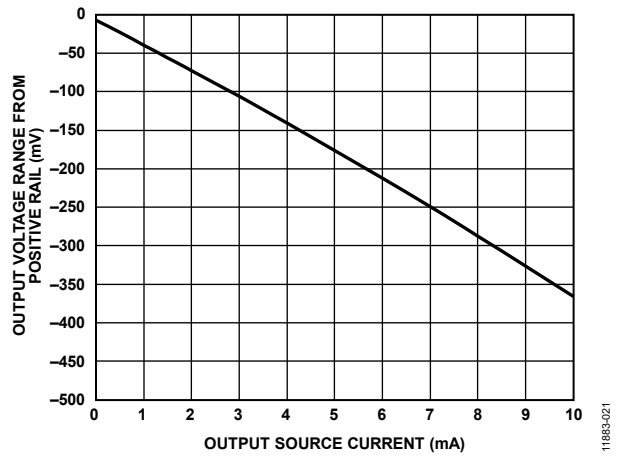


Figure 24. Output Voltage Range from Positive Rail vs. Output Source Current

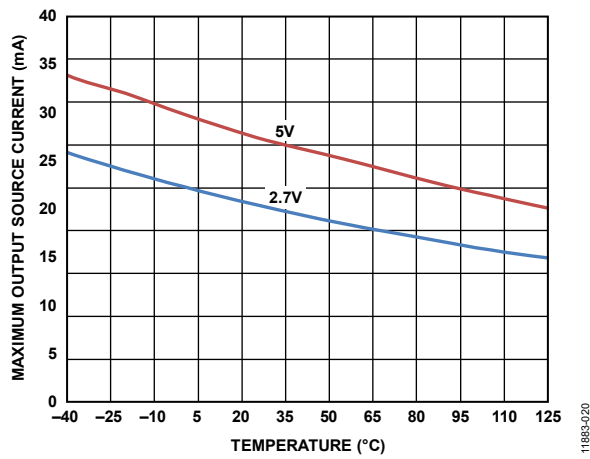


Figure 23. Maximum Output Source Current vs. Temperature

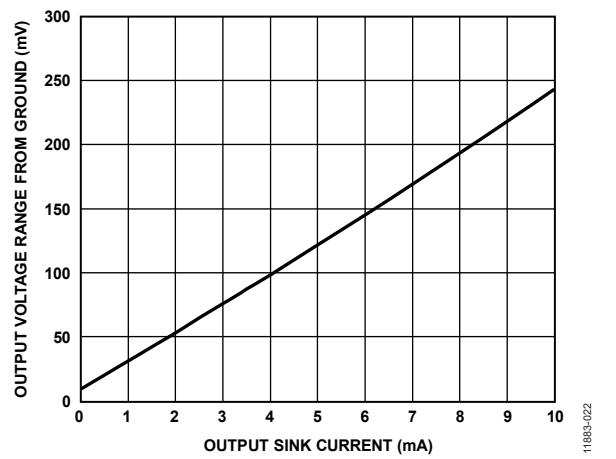


Figure 25. Output Voltage Range from Ground vs. Output Sink Current

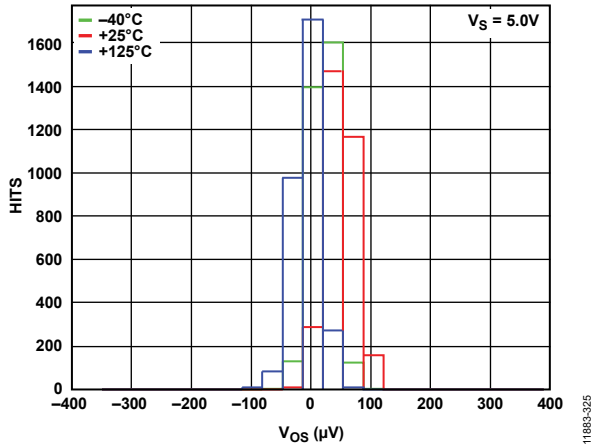


Figure 26. Offset Voltage Distribution

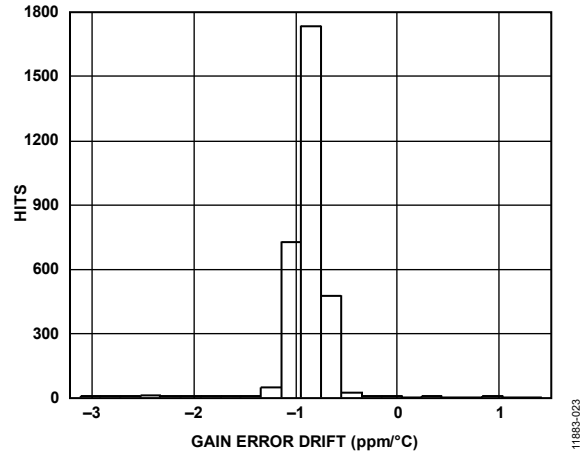


Figure 28. Gain Error Drift Distribution

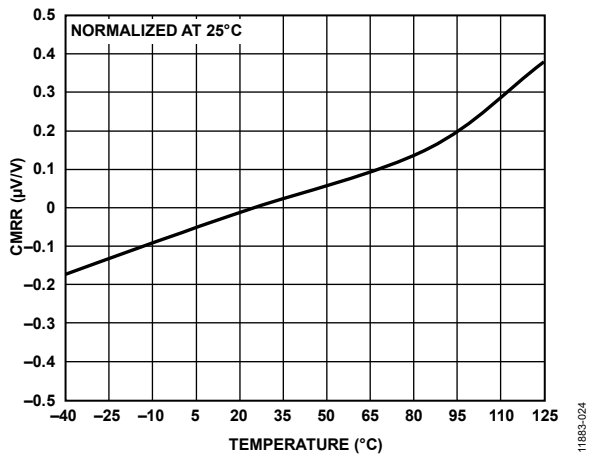


Figure 27. CMRR vs. Temperature

11883-025

11883-023

11883-024

THEORY OF OPERATION

The AD8418A is a single-supply, zero drift, difference amplifier that uses a unique architecture to accurately amplify small differential current shunt voltages in the presence of rapidly changing common-mode voltages.

In typical applications, the AD8418A measures current by amplifying the voltage across a shunt resistor connected to its inputs by a gain of 20 V/V (see Figure 29).

The AD8418A design provides excellent common-mode rejection, even with PWM common-mode inputs that can change at very fast rates, for example, 1 V/ns. The AD8418A contains proprietary technology to eliminate the negative effects of such fast changing external common-mode variations.

The AD8418A features an input offset drift of less than 400 nV/°C. This performance is achieved through a novel zero drift architecture that does not compromise bandwidth, which is typically rated at 250 kHz.

The reference inputs, V_{REF1} and V_{REF2} , are tied through 100 k Ω resistors to the positive input of the main amplifier, which allows the output offset to be adjusted anywhere in the output operating range. The gain is 1 V/V from the reference pins to the output when the reference pins are used in parallel. When the pins are used to divide the supply, the gain is 0.5 V/V.

The AD8418A offers breakthrough performance without compromising any of the robust application needs typical of solenoid or motor control. The ability to reject PWM input common-mode voltages and the zero drift architecture providing low offset and offset drift allows the AD8418A to deliver total accuracy for these demanding applications.

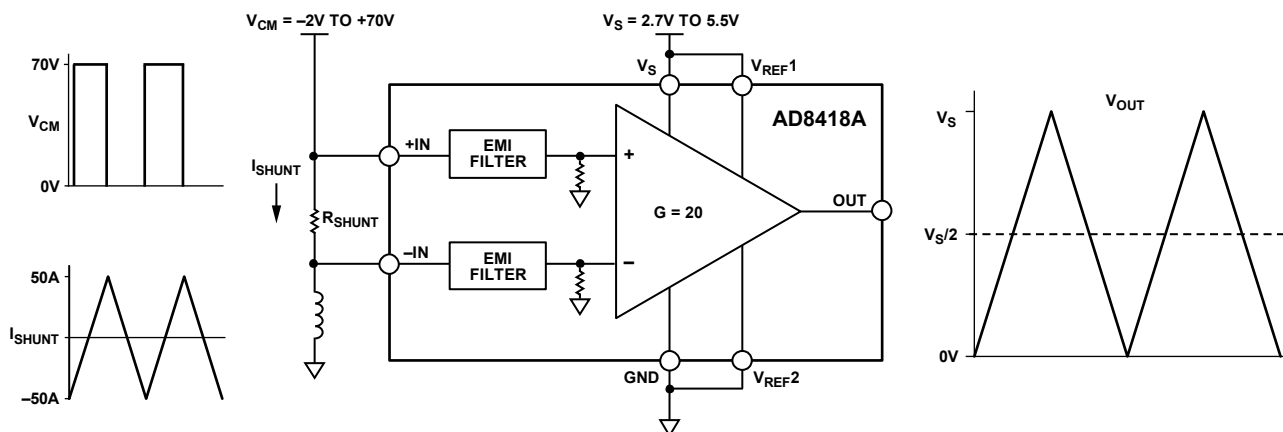


Figure 29. Typical Application

11889-225

OUTPUT OFFSET ADJUSTMENT

The output of the AD8418A can be adjusted for unidirectional or bidirectional operation.

UNIDIRECTIONAL OPERATION

Unidirectional operation allows the AD8418A to measure currents through a resistive shunt in one direction. The basic modes for unidirectional operation are ground referenced output mode and V_S referenced output mode.

For unidirectional operation, the output can be set at the negative rail (near ground) or at the positive rail (near V_S) when the differential input is 0 V. The output moves to the opposite rail when a correct polarity differential input voltage is applied. The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity needs to be negative to decrease the output. If the output is set at ground, the polarity must be positive to increase the output.

Ground Referenced Output Mode

When using the AD8418A in ground referenced output mode, both referenced inputs are tied to ground, which causes the output to sit at the negative rail when there are zero differential volts at the input (see Figure 30).

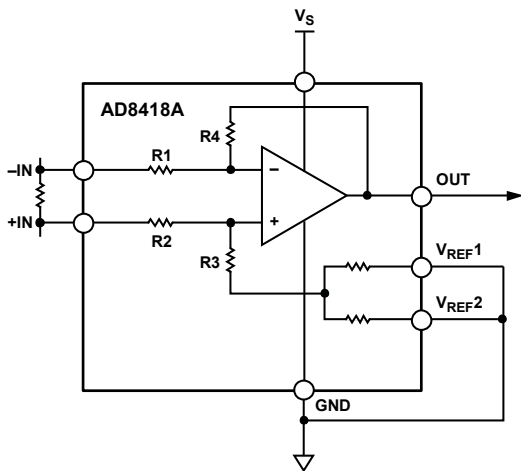


Figure 30. Ground Referenced Output

11883-025

V_S Referenced Output Mode

V_S referenced output mode is set when both reference pins are tied to the positive supply. It is typically used when the diagnostic scheme requires detection of the amplifier and the wiring before power is applied to the load (see Figure 31).

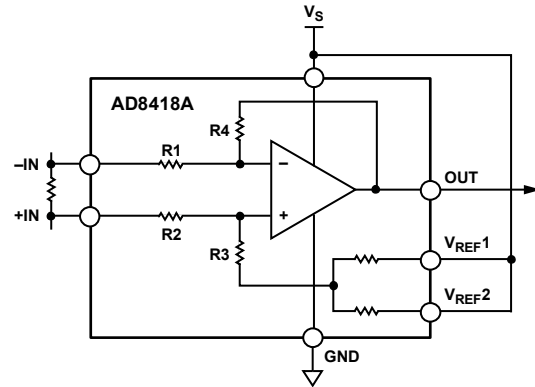


Figure 31. V_S Referenced Output

11883-026

BIDIRECTIONAL OPERATION

Bidirectional operation allows the AD8418A to measure currents through a resistive shunt in two directions.

In this case, the output is set anywhere within the output range. Typically, it is set at half-scale for equal range in both directions. In some cases, however, it is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

Adjusting the output is accomplished by applying voltage(s) to the referenced inputs. V_{REF1} and V_{REF2} are tied to internal resistors that connect to an internal offset node. There is no operational difference between the pins.

EXTERNAL REFERENCED OUTPUT

Tying V_{REF1} and V_{REF2} together and to a reference produces an output equal to the reference voltage when there is no differential input (see Figure 32). The output decreases with respect to the reference voltage when the input is negative, relative to the $-IN$ pin, and increases when the input is positive, relative to the $-IN$ pin.

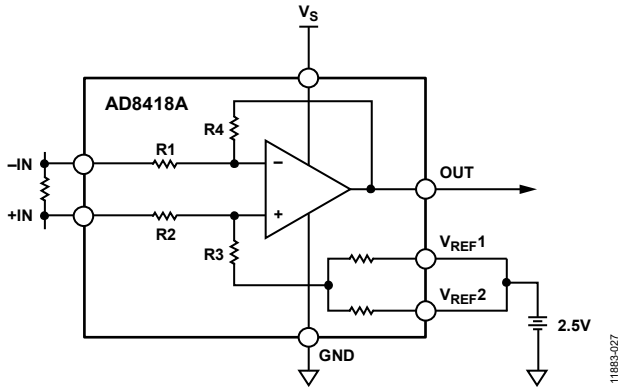


Figure 32. External Referenced Output

SPLITTING THE SUPPLY

By tying one reference pin to V_s and the other to the ground pin, the output is set at half of the supply when there is no differential input (see Figure 33). The benefit of this configuration is that an external reference is not required to offset the output for bidirectional current measurement. Tying one reference pin to V_s and the other to the ground pin creates a midscale offset that is ratiometric to the supply, which means that if the supply increases or decreases, the output remains at half the supply. For example, if the supply is 5.0 V, the output is at half scale or 2.5 V. If the supply increases by 10% (to 5.5 V), the output increases to 2.75 V.

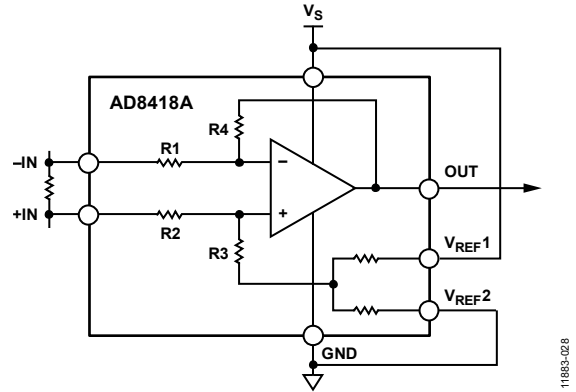


Figure 33. Split Supply

SPLITTING AN EXTERNAL REFERENCE

Use the internal reference resistors to divide an external reference by 2 with an accuracy of approximately 0.5%. Split an external reference by connecting one V_{REFX} pin to ground and the other V_{REFX} pin to the reference (see Figure 34).

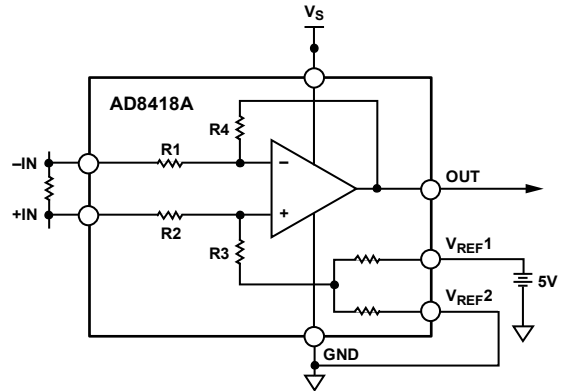


Figure 34. Split External Reference

SOLENOID CONTROL

High-Side Current Sense with a Low-Side Switch

In the case of a high-side current sense with a low-side switch, the PWM control switch is ground referenced. Tie an inductive load (solenoid) to a power supply and place a resistive shunt between the switch and the load (see Figure 37). An advantage of placing the shunt on the high side is that the entire current, including the recirculation current, is measurable because the shunt remains in the loop when the switch is off. In addition, diagnostics are enhanced because shorts to ground are detected with the shunt on the high side.

In this circuit configuration, when the switch is closed, the common-mode voltage decreases to near the negative rail. When the switch is open, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop above the battery by the clamp diode.

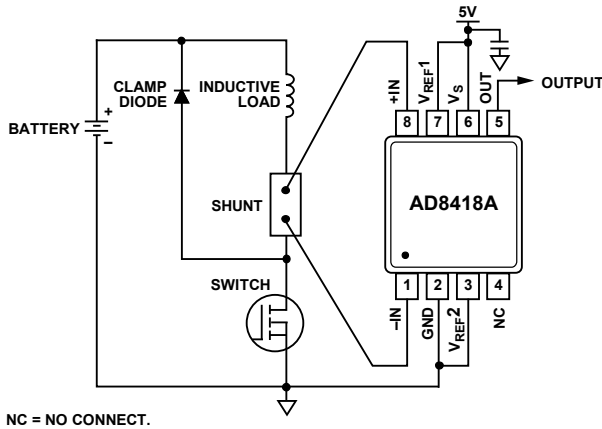
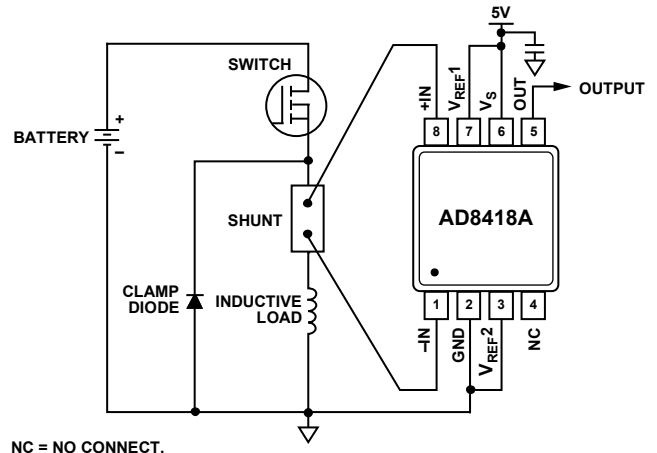


Figure 37. Low-Side Switch

High-Side Current Sense with a High-Side Switch

The high-side current sense with a high-side switch configuration minimizes the possibility of unexpected solenoid activation and excessive corrosion (see Figure 38). In this case, both the switch and the shunt are on the high side. When the switch is off, the battery is removed from the load, which prevents damage from potential shorts to ground while still allowing the recirculating current to be measured and to provide diagnostics. Removing the power supply from the load for the majority of the time that the switch is open minimizes the corrosive effects that can be caused by the differential voltage between the load and ground.

When using a high-side switch, the battery voltage is connected to the load when the switch is closed, causing the common-mode voltage to increase to the battery voltage. In this case, when the switch is open, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop below ground by the clamp diode.

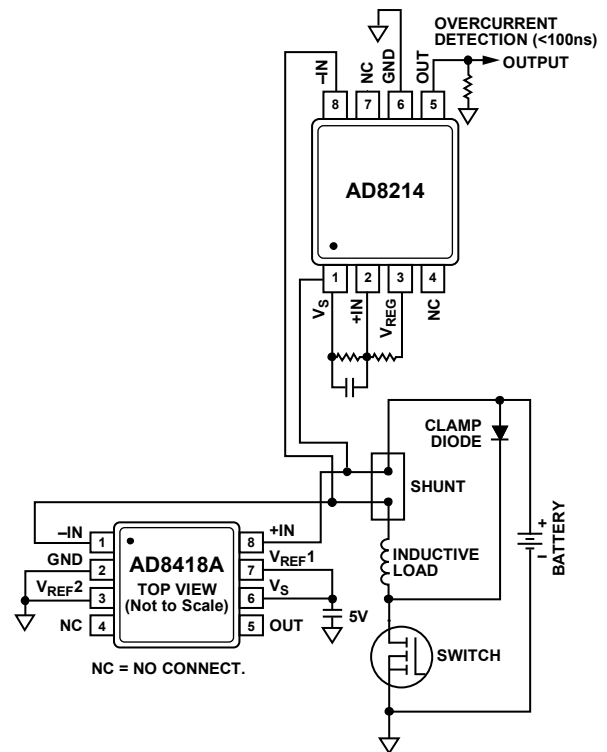


NC = NO CONNECT.

Figure 38. High-Side Switch

High Rail Current Sensing

In the high rail, current sensing configuration, the shunt resistor is referenced to the battery. High voltage is present at the inputs of the current sense amplifier. When the shunt is battery referenced, the AD8418A produces a linear ground referenced analog output. Additionally, the AD8214 provides an overcurrent detection signal in as little as 100 ns (see Figure 39). This feature is useful in high current systems where fast shutdown in overcurrent conditions is essential.



NC = NO CONNECT.

Figure 39. High Rail Current Sensing

PINOUT OPTION ENGINEERED FOR FMEA

The AD8418A is available in a 10-lead MSOP pinout option engineered for FMEA. This FMEA tolerant pinout is designed to meet stringent automotive requirements and to conditionally survive single faults that are a result of common printed circuit board (PCB) defects, as described in Table 6 and Table 7.

NC pins are inserted between $-IN$ and GND, as well as between $+IN$ and V_{REF1} . These NC pins effectively isolate the voltages at the input pins, which may range from -2 V to $+70\text{ V}$, from adjacent pins that prevent the occurrence of unrecoverable faults.

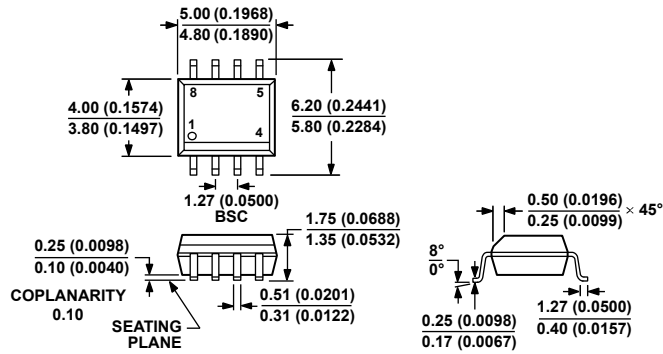
Table 6. Behavior as a Result of Adjacent Pin to Pin Shorts

| Pin Number | Adjacent Pins Shorted | Behavior |
|------------|-----------------------|--|
| 1, 2 | $-IN$ and NC | The circuit behaves normally. |
| 2, 3 | NC and GND | The circuit behaves normally. |
| 3, 4 | GND and V_{REF2} | The operating range of V_{REF2} is from GND to V_S . Therefore, shorting V_{REF2} to GND does not represent a fault. For example, if the AD8418A references are configured to split the supply with V_{REF2} tied to GND, the circuit behaves normally. A system error occurs, however, if V_{REF2} is tied either to V_S or to a different external reference because GND is shorted to V_S or to the external reference voltage on the PCB. |
| 4, 5 | V_{REF2} and NC | The circuit behaves normally. |
| 6, 7 | OUT and V_S | OUT approaches V_S voltage. |
| 7, 8 | V_S and V_{REF1} | The operating range of V_{REF1} is from GND to V_S . Therefore, shorting V_{REF1} to V_S does not represent a fault. For example, if the AD8418A references are configured to split the supply with V_{REF1} tied to V_S , the circuit behaves normally. A system error occurs, however, if V_{REF1} is tied either to GND or to a different external reference because V_S is shorted to GND or to the external reference voltage on the PCB. |
| 8, 9 | V_{REF1} and NC | The circuit behaves normally. |
| 9, 10 | NC and $+IN$ | The circuit behaves normally. |

Table 7. Behavior as a Result of Open Pin, Split Supply Setup (V_{REF1} to V_S and V_{REF2} to GND), $V_S = 5\text{ V}$, $-IN = +IN = 12\text{ V}$

| Pin Number | Pin Opened | Behavior |
|------------|------------|---|
| 1 | $-IN$ | OUT is undetermined but is limited between GND and V_S . |
| 2 | NC | The circuit behaves normally. |
| 3 | GND | The output voltage range is limited to 0.7 V to V_S and the device receives the ground through an ESD diode on V_{REF2} . |
| 4 | V_{REF2} | OUT approaches V_S . |
| 5 | NC | The circuit behaves normally. |
| 6 | OUT | No OUT signal. |
| 7 | V_S | The device is powered through an ESD diode between the V_{REF1} pin and V_S pin. The output voltage range is limited to GND to $V_S - 0.7\text{ V}$. |
| 8 | V_{REF1} | OUT approaches GND. |
| 9 | NC | The circuit behaves normally. |
| 10 | $+IN$ | OUT is undetermined but is limited between GND and V_S . |

OUTLINE DIMENSIONS

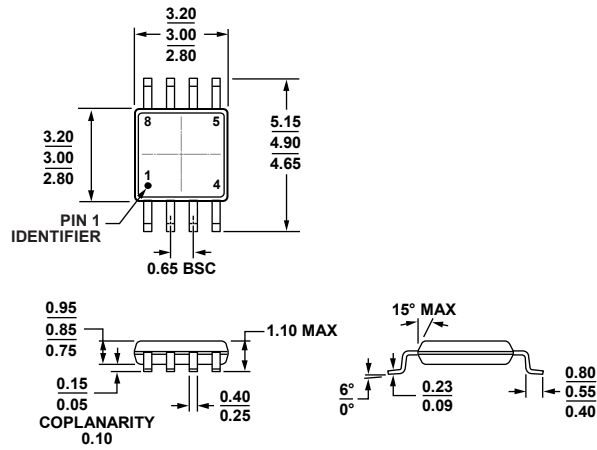


COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 40. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)

012407-A

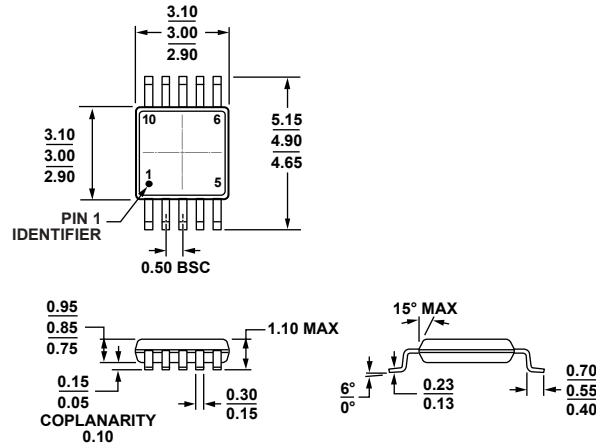


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 41. 8-Lead Mini Small Outline Package [MSOP]
 (RM-8)

Dimensions shown in millimeters

10-07-2009-B



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 42. 10-Lead Mini Small Outline Package [MSOP] (RM-10)

Dimensions shown in millimeters

081708-A

ORDERING GUIDE

| Model ^{1,2} | Temperature Range | Package Description | Package Option | Marking Code |
|----------------------|-------------------|----------------------------------|----------------|--------------|
| AD8418ABRMZ | -40°C to +125°C | 8-Lead MSOP | RM-8 | Y5J |
| AD8418ABRMZ-RL | -40°C to +125°C | 8-Lead MSOP, 13" Tape and Reel | RM-8 | Y5J |
| AD8418AWBRMZ | -40°C to +125°C | 8-Lead MSOP | RM-8 | Y5G |
| AD8418AWBRMZ-RL | -40°C to +125°C | 8-Lead MSOP, 13" Tape and Reel | RM-8 | Y5G |
| AD8418AWBRZ | -40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| AD8418AWBRZ-RL | -40°C to +125°C | 8-Lead SOIC_N, 13" Tape and Reel | R-8 | |
| AD8418AWHRZ | -40°C to +150°C | 8-Lead SOIC_N | R-8 | |
| AD8418AWHRZ-RL | -40°C to +150°C | 8-Lead SOIC_N, 13" Tape and Reel | R-8 | |
| AD8418AWHRMZ | -40°C to +150°C | 8-Lead MSOP | RM-8 | Y5H |
| AD8418AWHRMZ-RL | -40°C to +150°C | 8-Lead MSOP, 13" Tape and Reel | RM-8 | Y5H |
| AD8418AWBRMZ-10 | -40°C to +125°C | 10-lead MSOP | RM-10 | A3Z |
| AD8418AWBRMZ-10RL | -40°C to +125°C | 10-lead MSOP, 13" Tape and Reel | RM-10 | A3Z |
| AD8418AR-EVALZ | | 8-Lead SOIC_N Evaluation Board | | |
| AD8418ARM-EVALZ | | 8-Lead MSOP Evaluation Board | | |

¹ Z = RoHS Compliant Part.

² W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The AD8418AW models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View AD8418ABRMZ-RL on WIN SOURCE](#)
- ⊖ [Analog Devices Inc. Information](#)

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