THE DATASHEET OF

74LVC1T45W6-7

SINGLE BIT DUAL POWER SUPPLY TRANSLATING TRANSCEIVER WITH 3 STATE OUTPUTS

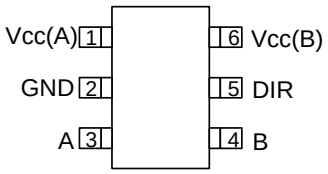
Description

The 74LVC1T45 is a single-bit, dual-supply transceiver with tri-state outputs suitable for transmitting a single logic bit across different voltage domains. The A input/output pin is designed to track V_{CCA} while the B input/output tracks V_{CCB}. This arrangement allows for universal low-voltage translation between any voltages from 1.65V to 5.5V. The Direction pin (DIR) controls the direction of the transceiver and in a logic voltage related to V_{CCA}. When a high logic level is applied to DIR, the A pin becomes an input, and the B pin becomes the output. Conversely, the roles of A and B are reversed when DIR is asserted low.

The tri-state feature occurs when either of the power supply voltages are zero. This is also an Ioff feature and allows for the output to remain in a high impedance state with both power supplies at 0V, which prevents and damages backflow currents and provides power-down electrical isolation up to 5.5V as not to interfere with any logic activity on pin A or B.

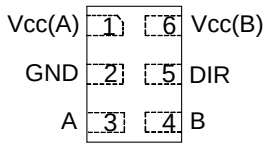
Pin Assignments

(Top View)



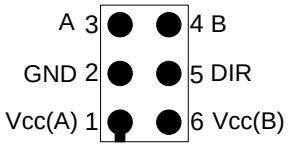
SOT26 SOT363 SOT563

(Top View)



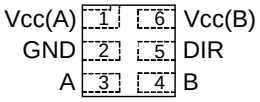
X2-DFN1410-6

(Bottom View)



X2-DFN1409-6
Chip Scale
Alternative

(Top View)



X2-DFN1010-6

Features

- Wide Supply Voltage Range:
  - V_{CC}(A): from 1.65V to 5.5V
  - V_{CC}(B): from 1.65V to 5.5V
- ± 24mA Output Drive at 3.3V
- CMOS Low Power Consumption 16µA Maximum I_{CC}
- High Noise Immunity—(100mV Hysteresis Typical)
- I_{OFF} Supports Partial-Power-Down Mode Operation
- I_{OFF} Controlled by Either V_{CC} Being at 0 V
- Inputs Accept up to 5.5V
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115)
  - 2000-V Human Body Model (A114)
  - 1000 V Charged Device Model (C101)
- Latch-up Exceeds 100mA per JESD 78, Class I
- X2-DFN1409-6 Package Designed as a Direct Replacement for Chip Scale Packaging.
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

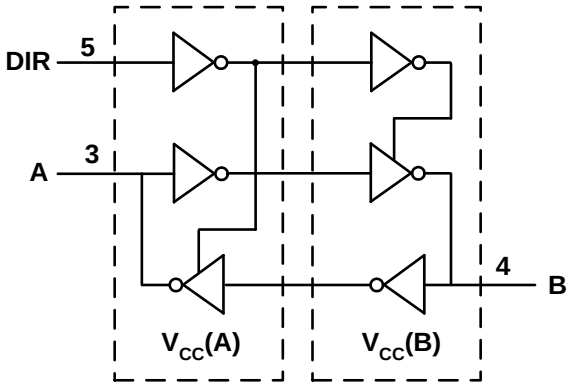
- Voltage Level Translation
  Well-Suited to Join Logic Types Operating at Different Voltages
- Power-Down Signal Isolation
  If Either Voltage Domain is Turned Off the Signal is Isolated and There is No Loading on Signal Lines
- Wide Array of Products, such as:
  - Cell Phones, Tablets, E-Readers
  - PCs, Notebooks, Netbooks, Ultrabooks
  - Networking, Routers, Gateways
  - Computer Peripherals, Hard Drives, CD/DVD ROM
  - TV, DVD, DVR, Set-Top Box
  - Personal Navigation / GPS
  - MP3 Players, Cameras, Video Recorders

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Descriptions

Pin Name	Pin	Function
VCC(A)	1	Supply for I/O Pin A; Reference for DIR
GND	2	Ground
A	3	Data Input/Output
B	4	Data Input/Output
DIR	5	Direction Control
VCC(B)	6	Supply for I/O Pin B

Logic Diagram



Function Tables

Input DIR (Direction Pin)	Operation
L	B Data to A Output
H	A Data to B Output

Inputs			Outputs	
A	B	DIR	A	B
Note 4	L	L	L	Note 4
Note 4	H	L	H	Note 4
L	Note 4	H	Note 4	L
H	Note 4	H	Note 4	H

Note: 4. Pin condition not applicable as defined by DIR.

Absolute Maximum Ratings (Note 5) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Rating	Unit
ESD HBM	Human Body Model ESD Protection		2	KV
ESD CDM	Charged Device Model ESD Protection		1	KV
ESD MM	Machine Model ESD Protection		200	V
V_{CC}(A), V_{CC}(B)	Supply Voltage Range		-0.5 to +6.5	V
V_I	Input Voltage Range		-0.5 to +6.5	V
V_O	Voltage Applied to Output in High Impedance or I_{OFF} State		-0.5 to +6.5	V
V_O	Voltage Applied to Output in High or Low State	A Pin	-0.3 to V_{CC}(A) +0.5	V
		B Pin	-0.3 to V_{CC}(B) +0.5	V
I_{IK}	Input Clamp Current V_I<0		-50	mA
I_{OK}	Output Clamp Current		-50	mA
I_O	Continuous Output Current		±50	mA
—	Continuous Current Through V_{cc} or GND		±100	mA
T_J	Operating Junction Temperature		-40 to +150	°C
T_{STG}	Storage Temperature		-65 to +150	°C

Note: 5. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 6) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		V_{CC} Inputs	V_{CC} Outputs	Min	Max	Units
$V_{CC}(A)$	Operating Voltage		—	—	1.65	5.5	V
$V_{CC}(B)$			—	—	1.65	5.5	V
V_{IH}	High-Level Input Voltage Pin A or DIR Referenced to $V_{CC}(A)$		V_{CC} = 1.65V to 1.95V	—	0.65 X $V_{CC(A)}$	—	V
			V_{CC} = 2.3V to 2.7V	—	1.7	—	
			V_{CC} = 3V to 3.6V	—	2	—	
			V_{CC} = 4.5V to 5.5V	—	0.7 X $V_{CC(A)}$	—	
V_{IL}	Low-Level Input Voltage Pin A or DIR Referenced to $V_{CC}(A)$		V_{CC} = 1.65V to 1.95V	—	—	0.35 X $V_{CC(A)}$	V
			V_{CC} = 2.3V to 2.7V	—	—	0.7	
			V_{CC} = 3V to 3.6V	—	—	0.8	
			V_{CC} = 4.5V to 5.5V	—	—	0.3 X $V_{CC(A)}$	
V_{IH}	High-Level Input Voltage Pin B Referenced to $V_{CC}(B)$		V_{CC} = 1.65V to 1.95V	—	0.65 X $V_{CC(B)}$	—	V
			V_{CC} = 2.3V to 2.7V	—	1.7	—	
			V_{CC} = 3V to 3.6V	—	2	—	
			V_{CC} = 4.5V to 5.5V	—	0.7 X $V_{CC(B)}$	—	
V_{IL}	Low-Level Input Voltage Pin B Referenced to $V_{CC}(B)$		V_{CC} = 1.65V to 1.95V	—	—	0.35 X $V_{CC(B)}$	V
			V_{CC} = 2.3V to 2.7V	—	—	0.7	
			V_{CC} = 3V to 3.6V	—	—	0.8	
			V_{CC} = 4.5V to 5.5V	—	—	0.3 X $V_{CC(B)}$	
V_I	Input Voltage		—	—	0	5.5	V
V_O	Output Voltage		—	—	0	V_{CC}	V
I_{OH}	High-Level Output Current		—	V_{CC} = 1.65V to 1.95V	—	-4	mA
			—	V_{CC} = 2.3V to 2.7V	—	-8	
			—	V_{CC} = 3V to 3.6V	—	-24	
			—	V_{CC} = 4.5V to 5.5V	—	-32	
I_{OL}	Low-Level Output Current		—	V_{CC} = 1.65V to 1.95V	—	4	mA
			—	V_{CC} = 2.3V to 2.7V	—	8	
			—	V_{CC} = 3V to 3.6V	—	24	
			—	V_{CC} = 4.5V to 5.5V	—	32	
Δt/ΔV	Input Transition Rise or Fall Rate	Data Inputs	V_{CC} = 1.65V to 1.95V	—	–	20	ns/V
			V_{CC} = 2.3V to 2.7V	—	–	20	
			V_{CC} = 3V to 3.6V	—	–	10	
			V_{CC} = 4.5V to 5.5V	—	–	5	
		Control Inputs	V_{CC} = 1.65V to 5.5V	—	—	5	
T_A	Operating Free-Air Temperature		—	—	-40	+125	°C

Note: 6. Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics (@T_A = +40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		V_{CC} (A)	V_{CC} (B)	T_A = +25°C			T_A = -40°C to +85°C		Unit
						Min	Typ	Max	Min	Max	
V_{OH}	High Level Output Voltage	I_{OH} = -100μA		1.65V to 5.5V	1.65V to 5.5V	—	—	—	V_{CC} – 0.1	—	V
		I_{OH} = -4mA		1.65V	1.65V	—	—	—	1.2	—	
		I_{OH} = -8mA		2.3V	2.3V	—	—	—	1.9	—	
		I_{OH} = -24mA		3V	3V	—	—	—	2.4	—	
		I_{OH} = -32mA		4.5V	4.5V	—	—	—	3.8	—	
V_{OL}	Low-Level Output Voltage	I_{OL} = 100μA		1.65V to 5.5V	1.65V to 5.5V	—	—	—	—	0.1	V
		I_{OL} = 4mA		1.65V	1.65V	—	—	—	—	0.45	
		I_{OL} = 8mA		2.3V	2.3V	—	—	—	—	0.3	
		I_{OL} = 24mA		3V	3V	—	—	—	—	0.55	
		I_{OL} = 32mA		4.5V	4.5V	—	—	—	—	0.55	
I_I	Input Current	DIR	V_I = V_{CC}(A) or GND	0 to 5.5V	0 to 5.5V	—	—	± 1	—	±2	μA
I_{OFF}	Power Down Leakage Current	A Pin	V_I or V_O = 0 to 5.5V	0	0V to 5.5V	—	—	± 1	—	±2	μA
		B Pin		0 to 5.5V	0	—	—	± 1	—	±2	
I_{OZ}	3-State Leakage Current	A Pin	V_O = V_{CC}(A)	1.65V to 5.5V	1.65V to 5.5V	—	—	± 1	—	±2	μA
		B Pin	V_O = V_{CC}(B)	1.65V to 5.5V	1.65V to 5.5V	—	—	± 1	—	±2	
I_{CCA}	Supply Current	V_I = 5.5V or GND I_O = 0		1.65V to 5.5V	1.65V to 5.5V	—	—	—	—	3	μA
				5.5V	0	—	—	—	—	2	
				0	5.5V	—	—	—	—	-2	
I_{CCB}	Supply Current	V_I = 5.5V or GND I_O = 0		1.65V to 5.5V	1.65V to 5.5V	—	—	—	—	3	μA
				0V	5.5V	—	—	—	—	2	
				5.5V	0V	—	—	—	—	-2	
I_{CCA} + I_{CCB}	Supply Current	V_I = 5.5V or GND I_O = 0		1.65V to 5.5V	1.65V to 5.5V	—	—	—	—	4	μA
ΔI_{CCA}	Additional Supply Current	A Pin	A = V_{CC}(A) -0.6V DIR = V_{CC}(A) B = Open	3V to 5.5V	3V to 5.5V	—	—	—	—	50	μA
		DIR	DIR= V_{CC}(A) -0.6V A= V_{CC}(A) or GND B = Open							50	
ΔI_{CCB}	Additional Supply Current	B Pin	B = V_{CC}(B) -0.6V DIR = GND A = Open	3V to 5.5V	3V to 5.5V	—	—	—	—	50	μA
C_I	Input Capacitance	DIR	V_I= V_{CC}(A) or GND	3.3V	3.3V	—	2.5	—	—	—	pF
C_{IO}	Input/Output Capacitance	A or B Pin	V_I= V_{CC}(A)/(B) or GND	3.3V	3.3V	—	6.0	—	—	—	pF

Electrical Characteristics (@T_A = +40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		V_{CC}(A)	V_{CC}(B)	T_A = -40°C to +125°C		Unit
						Min	Max	
V_{OH}	High Level Output Voltage	I_{OH} = -100µA		1.65V to 5.5V	1.65V to 5.5V	V_{CC} – 0.1	—	V
		I_{OH} = -4mA		1.65V	1.65V	1.2	—	
		I_{OH} = -8mA		2.3V	2.3V	1.9	—	
		I_{OH} = -24mA		3V	3V	2.4	—	
		I_{OH} = -32mA		4.5V	4.5V	3.8	—	
V_{OL}	High-Level Input Voltage	I_{OL} = 100µA		1.65V to 5.5V	1.65V to 5.5V	—	0.1	V
		I_{OL} = 4mA		1.65V	1.65V	—	0.45	
		I_{OL} = 8mA		2.3V	2.3V	—	0.3	
		I_{OL} = 24mA		3V	3V	—	0.55	
		I_{OL} = 32mA		4.5V	4.5V	—	0.55	
I_I	Input Current	DIR	V_I = V_{CC}(A) or GND	0 to 5.5V	0 to 5.5V	—	± 2	µA
I_{OFF}	Power Down Leakage Current	A Pin	V_I or V_O = 0 to 5.5V	0	1.65V to 5.5V	—	± 2	µA
		B Pin		1.65V to 5.5V	0V	—	± 2	
I_{OZ}	3-State Leakage Current	B Pin V_O =V_{CC} (B) DIR = 0 V	V_I = 0 to 5.5V	1.65V to 5.5V	1.65V to 5.5V	—	± 2	µA
		A Pin V_O = V_{CC}(A) DIR= V_{cc}(A)		1.65V to 5.5V	1.65V to 5.5V	—	± 2	
I_{CCA}	Supply Current	V_I = 5.5V or GND I_O = 0		1.65V to 5.5V	1.65V to 5.5V	—	3	µA
				5.5V	0	—	2	
				0	5.5V	—	-2	
I_{CCB}	Supply Current	V_I = 5.5V or GND I_O = 0		1.65V to 5.5V	1.65V to 5.5V	—	3	µA
				5.5V	0	—	2	
				0	5.5V	—	-2	
I_{CCA} + I_{CCB}	Supply Current	V_I = 5.5V or GND I_O = 0		1.65V to 5.5V	1.65V to 5.5V	—	4	µA
ΔI_{CCA}	Additional Supply Current	A Pin	A = V_{CC} (A) -0.6V DIR = V_{CC} (A) B = Open	3V to 5.5V	3V to 5.5V	—	50	µA
		DIR	DIR= V_{CC} (A) -0.6V A= V_{CC} (A) or GND B = Open				50	
ΔI_{CCB}	Additional Supply Current	B Pin	B = V_{CC} (B) -0.6V DIR = GND A = Open	3V to 5.5V	3V to 5.5V	—	50	µA

Package Characteristics (V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
Θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT26	Note 7	—	166	—	°C/W
		SOT363		—	371	—	
		SOT563		—	290	—	
		DFN1410		—	430	—	
		DFN1409		—	450	—	
		DFN1010		—	510	—	
Θ_{JC}	Thermal Resistance Junction-to-Case	SOT26	Note 7	—	46	—	°C/W
		SOT363		—	143	—	
		SOT563		—	96	—	
		DFN1410		—	190	—	
		DFN1409		—	200	—	
		DFN1010		—	250	—	

Note: 7. Test condition for SOT26, SOT363, DFN1410, DFN1409 and DFN1010: Device mounted on FR-4 substrate PCB, 2oz copper with minimum recommended pad layout.

Switching Characteristics (V_{CC} (A) = 1.8V ± 0.15V, T_A = -40°C to +85°C, see Figure 1)

Parameter	From (Input)	To (Output)	V_{CC}(B) = 1.8V ±0.15V		V_{CC}(B) = 2.5V ±0.2V		V_{CC}(B) = 3.3V ±0.3V		V_{CC}(B)= 5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pLH}	A	B	3	17.7	2.2	10.3	1.7	8.3	1.4	7.5	ns
t_{pHL}			2.8	14.3	2.2	8.5	1.8	8.1	1.7	7.5	
t_{pLH}	B	A	3	17.7	2.3	16	2.1	15.5	1.9	15.1	ns
t_{pHL}			2.8	14.3	2.1	12.9	2	12.6	1.8	12.2	
t_{pHZ}	DIR	A	5.2	19.4	4.8	18.5	4.7	18.4	5.1	17.1	ns
t_{pLZ}			2.3	10.5	2.1	10.5	2.4	10.7	3.1	10.9	
t_{pHZ}	DIR	B	6.4	21.9	4.9	11.5	4.6	10.3	2.8	8.2	ns
t_{pLZ}			4.2	17	3.7	9.6	3.3	8.8	2.4	8.0	
t_{pZH}	DIR	A	—	33.7	—	25.2	—	23.9	—	21.5	ns
t_{pZL}			—	36.2	—	24.4	—	22.9	—	20.4	
t_{pZH}	DIR	B	—	28.2	—	20.8	—	19	—	18.1	ns
t_{pZL}			—	33.7	—	27	—	25.5	—	24.1	

Switching Characteristics (continued) (V_{CC} (A) = 2.5V ± 0.2V, T_A = -40°C to +85°C, see Figure 1)

Parameter	From (Input)	To (Output)	V_{CC}(B) = 1.8V ±0.15V		V_{CC}(B) = 2.5V ±0.2V		V_{CC}(B) = 3.3V ±0.3V		V_{CC}(B) = 5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pLH}	A	B	2.3	16	1.5	8.5	1.3	6.4	1.1	5.1	ns
t_{pHL}			2.1	12.9	1.4	7.5	1.3	5.4	0.9	4.6	
t_{pLH}	B	A	2.2	10.3	1.5	8.5	1.4	8	1	7.5	ns
t_{pHL}			2.2	8.5	1.4	7.5	1.3	7	0.9	6.2	
t_{pHZ}	DIR	A	3	8.1	3.1	8.1	2.8	8.1	3.2	8.1	ns
t_{pLZ}			1.3	5.9	1.3	5.9	1.3	5.9	1	5.8	
t_{pHZ}	DIR	B	5.5	23.7	3.6	11.4	3.5	10.2	2.4	7.1	ns
t_{pLZ}			3.9	18.9	3.2	9.6	2.8	8.4	1.8	5.3	
t_{pZH}	DIR	A	—	29.2	—	18.1	—	16.4	—	12.8	ns
t_{pZL}			—	32.2	—	18.9	—	17.2	—	13.3	
t_{pZH}	DIR	B	—	21.9	—	14.4	—	12.3	—	10.9	ns

Switching Characteristics (continued) (V_{CC} (A) = 3.3V ± 0.3V, T_A = -40°C to +85°C, see Figure 1)

Parameter	From (Input)	To (Output)	V_{CC}(B) = 1.8V ±0.15V		V_{CC}(B) = 2.5V ±0.2V		V_{CC}(B) = 3.3V ±0.3V		V_{CC}(B) = 5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pLH}	A	B	2.1	15.5	1.4	8	0.7	5.8	0.7	4.4	ns
t_{pHL}			2	12.6	1.3	7	0.8	5	0.7	4	
t_{pLH}	B	A	1.7	8.3	1.3	6.4	0.7	5.8	0.6	5.4	ns
t_{pHL}			1.8	7.1	1.3	5.4	0.8	5	0.7	4.5	
t_{pHZ}	DIR	A	2.9	7.3	3	7.3	2.8	7.3	3.4	7.3	ns
t_{pLZ}			1.8	5.6	1.6	5.6	2.2	5.7	2.2	5.7	
t_{pHZ}	DIR	B	4.0	20.5	3.5	10.1	2.9	8.8	2.4	6.8	ns
t_{pLZ}			3.3	14.5	2.9	7.8	2.4	7.1	1.7	4.9	
t_{pZH}	DIR	A	—	22.8	—	14.2	—	12.9	—	10.3	ns
t_{pZL}			—	27.6	—	15.5	—	13.8	—	11.3	
t_{pZH}	DIR	B	—	21.1	—	13.6	—	11.5	—	10.1	ns
t_{pZL}			—	19.9	—	14.3	—	12.3	—	11.3	

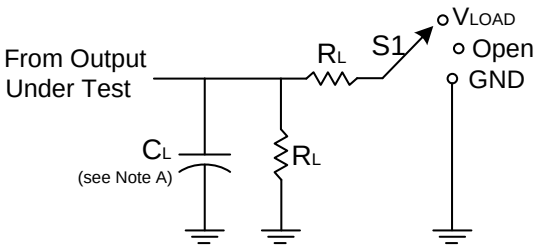
Switching Characteristics (continued) (V_{CC} (A) = 5V ± 0.5V, T_A = -40°C to +85°C, see Figure 1)

Parameter	From (Input)	To (Output)	V_{CC}(B) = 1.8V ±0.15V		V_{CC}(B) = 2.5V ±0.2V		V_{CC}(B) = 3.3V ±0.3V		V_{CC}(B)= 5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pLH}	A	B	1.9	15.1	1	7.5	0.6	5.4	0.5	3.9	ns
t_{pHL}			1.8	12.2	0.9	6.2	0.7	4.5	0.5	3.5	
t_{pLH}	B	A	1.4	8.5	1	5.1	0.7	4.4	0.5	3.9	ns
t_{pHL}			1.7	8.5	0.9	4.6	0.7	4	0.5	3.5	
t_{pHZ}	DIR	A	2.1	5.4	2.2	5.4	2.2	5.5	2.2	5.4	ns
t_{pLZ}			0.9	3.8	1	3.8	1	3.7	0.9	3.7	
t_{pHZ}	DIR	B	4.8	20.2	2.5	9.8	1	8.5	2.2	6.5	ns
t_{pLZ}			4.2	14.8	2.5	7.4	2.5	7	1.6	4.5	
t_{pZH}	DIR	A	—	22	—	12.5	—	11.4	—	8.4	ns
t_{pZL}			—	27.2	—	14.4	—	12.5	—	10	
t_{pZH}	DIR	B	—	18.9	—	11.3	—	9.1	—	7.6	ns

Operating Characteristics (T_A = +25°C, unless otherwise specified.)

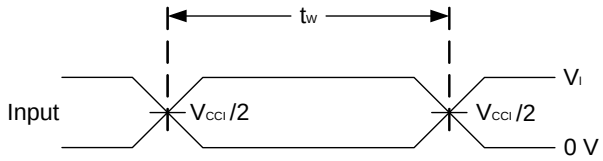
Parameter Power Dissipation Capacitance		Test Conditions	V_{CC}(A) = V_{CC}(B) = 1.8V	V_{CC}(A) = V_{CC}(B) = 2.5V	V_{CC}(A) = V_{CC}(B) = 3.3V	V_{CC}(A) = V_{CC}(B) = 5V	Unit
			Typ	Typ	Typ	Typ	
C_{pd} (A)	A- Input, B- Output	C_L = 0 pF f = 10 MHz tr = tf = 1 ns	3	4	4	4	pF
	B- Input, A- Output		18	19	20	21	
C_{pd} (B)	A- Input, B- Output	C_L = 0 pF f = 10 MHz tr = tf = 1 ns	18	19	20	21	pF
	B- Input, A- Output		3	4	4	4	

Parameter Measurement Information

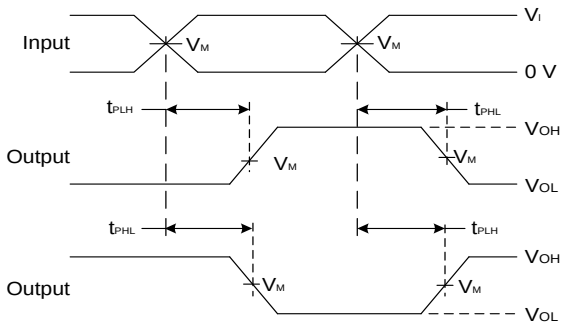


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	Vload
t_{PHZ}/t_{PZH}	GND

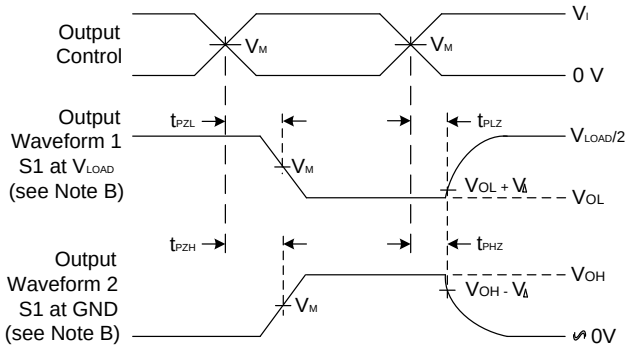
V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	$V\Delta$
	V_I	t_r/t_f					
1.8V±0.15V	V_{CCI}	≤2ns	$V_{CCO}/2$	2 X V_{CCO}	15pF	2KΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CCO}/2$	2 X V_{CCO}	15pF	2KΩ	0.15V
3.3V±0.3V	3V	≤2.5ns	$V_{CCO}/2$	2 X V_{CCO}	15pF	2KΩ	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CCO}/2$	2 X V_{CCO}	15pF	2KΩ	0.3V



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs

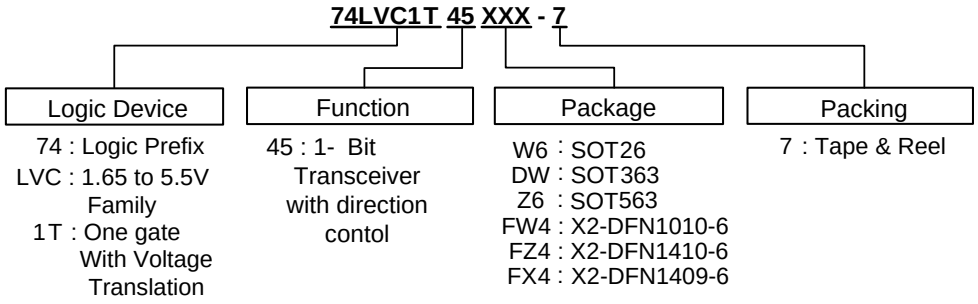


Voltage Waveform Enable and Disable Times
Low and High Level Enabling

Figure 1 Load Circuit and Voltage Waveforms

Notes:
8. Includes test lead and test apparatus capacitance.
9. Waveform 1 is for an output with input set up as a low and device coming out or into 3-state via DIR control.
   Waveform 2 is for an output with input set up as a high and device coming out or into 3-state via DIR control.
10. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
11. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
12. t_{PZL} and t_{PZH} are the same as t_{EN}.
13. t_{PLH} and t_{PHL} are the same as t_{PD}.
14. V_{CCI} is the V_{CC} associated with the input.
15. V_{CCO} is the V_{CC} associated with the output.

Ordering Information

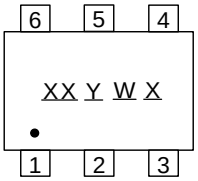


Part Number	Package Code	Packaging	7" Tape and Reel (Note 7)	
			Quantity	Part Number Suffix
74LVC1T45W6-7	W6	SOT26	3000/Tape & Reel	-7
74LVC1T45DW-7	DW	SOT363	3000/Tape & Reel	-7
74LVC1T45Z6-7	Z6	SOT563	4000/Tape & Reel	-7
74LVC1T45FW4-7	FW4	X2-DFN1010-6	5000/Tape & Reel	-7
74LVC1T45FZ4-7	FZ4	X2-DFN1410-6	5000/Tape & Reel	-7
74LVC1T45FX4-7	FX4	X2-DFN1409-6	5000/Tape & Reel	-7

Note: 16. The taping orientation is located on our website at http://www.diodes.com/package-outlines.html.

Marking Information

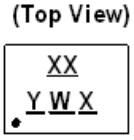
(1) SOT363, SOT563



XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Internal Code

Part Number	Package	Identification Code
74LVC1T45W6	SOT26	TT
74LVC1T45DW	SOT363	TR
74LVC1T45Z6	SOT563	TS

(2) X2-DFN1010-6, X2-DFN1410-6, and X2-DFN1409-6



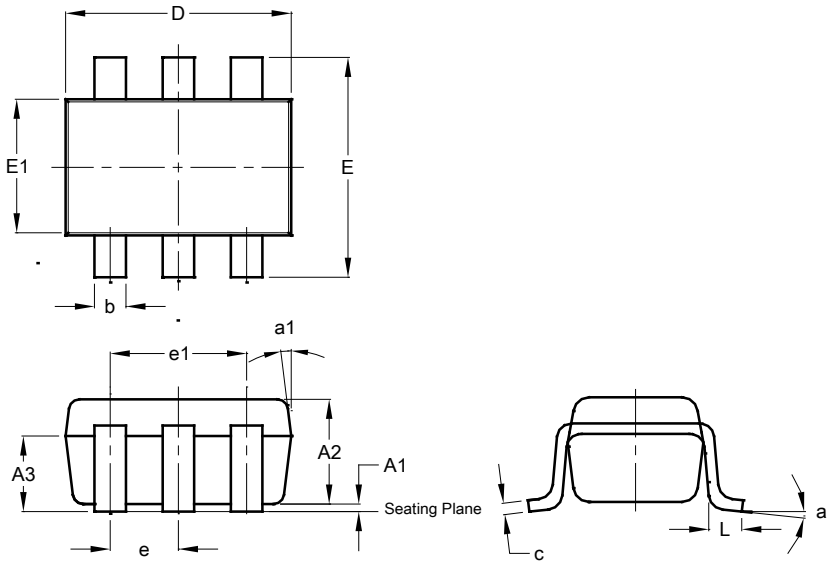
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Internal code

Part Number	Package	Identification Code
74LVC1T45FW4	X2-DFN1010-6	TR
74LVC1T45FX4	X2-DFN1409-6	TT
74LVC1T45FZ4	X2-DFN1410-6	TS

Package Outline Dimensions (All dimensions in mm.)

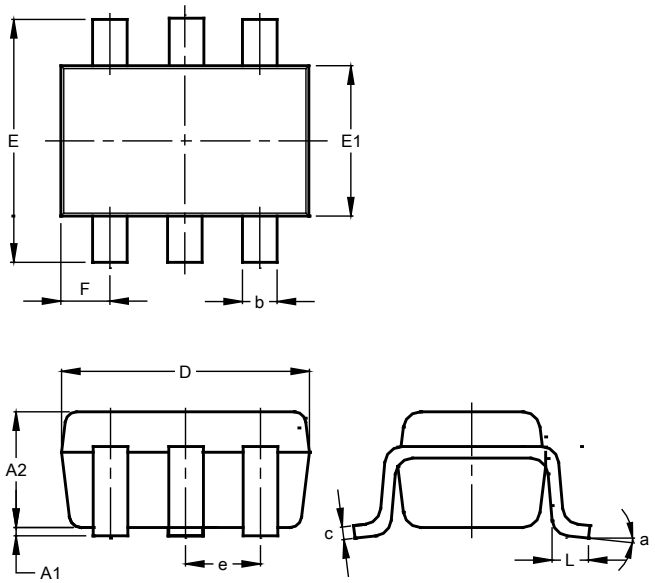
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SOT26



SOT26 (SC74R)			
Dim	**Min**	**Max**	**Typ**
A1	0.013	0.10	0.05
A2	1.00	1.30	1.10
A3	0.70	0.80	0.75
b	0.35	0.50	0.38
c	0.10	0.20	0.15
D	2.90	3.10	3.00
e	—	—	0.95
e1	—	—	1.90
E	2.70	3.00	2.80
E1	1.50	1.70	1.60
L	0.35	0.55	0.40
a	—	—	8°
a1	—	—	7°
All Dimensions in mm			

(2) Package Type: SOT363

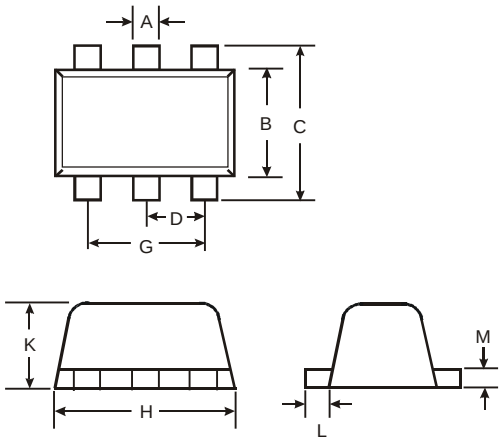


SOT363			
Dim	**Min**	**Max**	**Typ**
A1	0.00	0.10	0.05
A2	0.90	1.00	0.95
b	0.10	0.30	0.25
c	0.10	0.22	0.11
D	1.80	2.20	2.15
E	2.00	2.20	2.10
E1	1.15	1.35	1.30
e	0.650 BSC		
F	0.40	0.45	0.425
L	0.25	0.40	0.30
a	0°	8°	—
All Dimensions in mm			

Package Outline Dimensions (All dimensions in mm.)

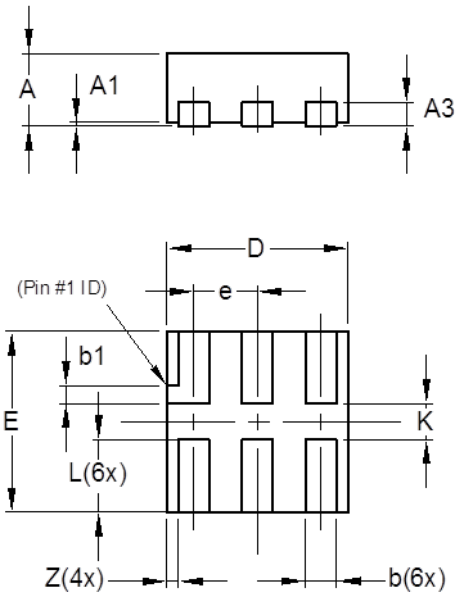
Please see http://www.diodes.com/package-outlines.html for the latest version.

(3) Package Type: SOT563



SOT563			
Dim	**Min**	**Max**	**Typ**
A	0.15	0.30	0.20
B	1.10	1.25	1.20
C	1.55	1.70	1.60
D	—	—	0.50
G	0.90	1.10	1.00
H	1.50	1.70	1.60
K	0.55	0.60	0.60
L	0.10	0.30	0.20
M	0.10	0.18	0.11
All Dimensions in mm			

(4) Package Type X2-DFN1010-6

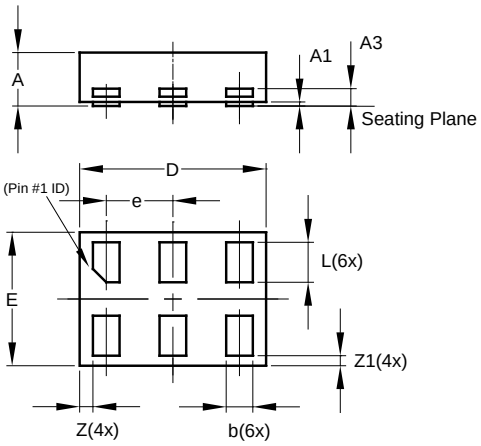


X2-DFN1010-6			
Dim	**Min**	**Max**	**Typ**
A	—	0.40	0.39
A1	0.00	0.05	0.02
A3	—	—	0.13
b	0.14	0.20	0.17
b1	0.05	0.15	0.10
D	0.95	1.05	1.00
E	0.95	1.05	1.00
e	—	—	0.35
L	0.35	0.45	0.40
K	0.15	—	—
Z	—	—	0.065
All Dimensions in mm			

Package Outline Dimensions (All dimensions in mm.)

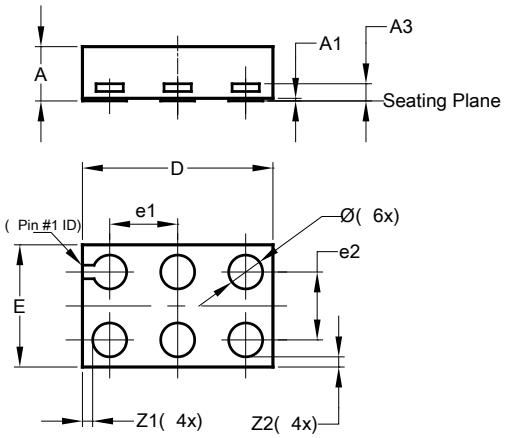
Please see http://www.diodes.com/package-outlines.html for the latest version.

(5) Package Type: X2-DFN1410-6



X2-DFN1410-6			
Dim	**Min**	**Max**	**Typ**
A	—	0.40	0.39
A1	0.00	0.05	0.02
A3	—	—	0.13
b	0.15	0.25	0.20
D	1.35	1.45	1.40
E	0.95	1.05	1.00
e	—	—	0.50
L	0.25	0.35	0.30
Z	—	—	0.10
Z1	0.045	0.105	0.075
All Dimensions in mm			

(6) Package Type: X2-DFN1409-6

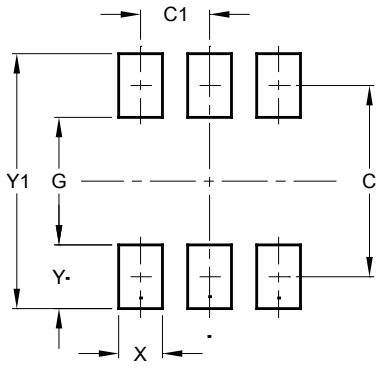


X2-DFN1409-6			
Dim	**Min**	**Max**	**Typ**
A	-	0.40	0.39
A1	0	0.05	0.02
A3	-	-	0.13
Ø	0.20	0.30	0.25
D	1.35	1.45	1.40
E	0.85	0.95	0.90
e1	-	-	0.50
e2	-	-	0.50
Z1	-	-	0.075
Z2	-	-	0.075
All Dimensions in mm			

Suggested Pad Layout

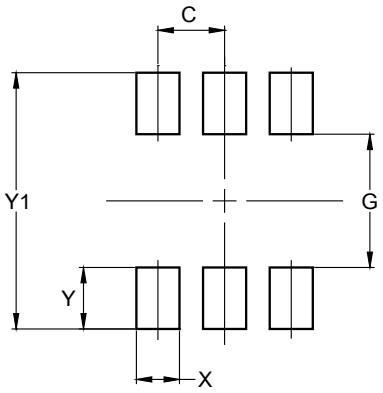
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: SOT26



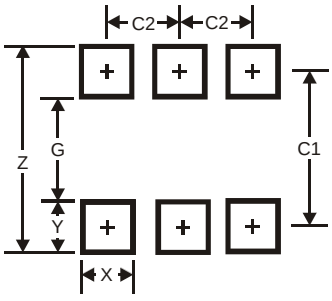
Dimensions	Value (in mm)
C	2.40
C1	0.95
G	1.60
X	0.55
Y	0.80
Y1	3.20

(2) Package Type: SOT363



Dimensions	Value (in mm)
C	0.650
G	1.300
X	0.420
Y	0.600
Y1	2.500

(3) Package Type: SOT563

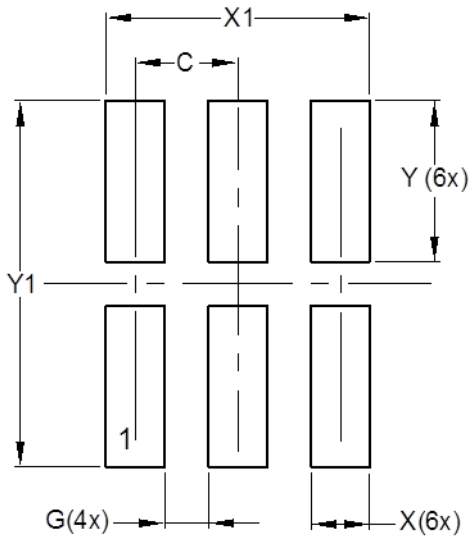


Dimensions	SOT563
Z	2.2
G	1.2
X	0.375
Y	0.5
C1	1.7
C2	0.5

Suggested Pad Layout

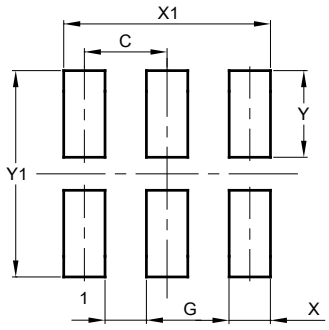
Please see http://www.diodes.com/package-outlines.html for the latest version.

(4) Package Type X2-DFN1010-6



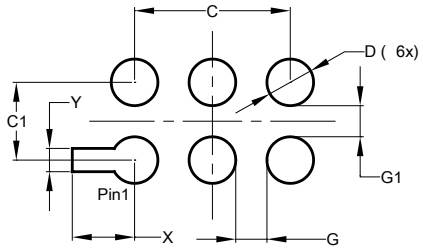
Dimensions	Value (in mm)
C	0.350
G	0.150
X	0.200
X1	0.900
Y	0.550
Y1	1.250

(5) Package Type: X2-DFN1410-6



Dimensions	Value (in mm)
C	0.500
G	0.250
X	0.250
X1	1.250
Y	0.525
Y1	1.250

(6) Package Type: X2-DFN1409-6



Dimensions	Value (in mm)
C	1.000
C1	0.500
D	0.300
G	0.200
G1	0.200
X	0.400
Y	0.150

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