THE DATASHEET OF

TDA8023TT/C1

TDA8023

Low power IC card interface

Rev. 2.0 — 24 June 2016 Product data sheet

1. General description

The TDA8023 is a complete cost-efficient, low-power analog interface for synchronous or asynchronous smart cards. It can be placed between the card and the microcontroller with very few external components to perform all supply, protection and control functions.

2. Features and benefits

- I^2C-bus controlled IC card interface in TSSOP28
- Supply voltage from 2.7 V to 6.5 V
- Independant supply voltage $V_{DD(INTF)}$ for interface signals with the microcontroller
- Shutdown input for very low power consumption when the part is not used
- Power reduction modes when the card is active
- DC-to-DC converter for V_{CC} generation (capacitive doubler, tripler, or inductive, or follower automatically selected according to supply voltage and card voltage)
- 1 specific protected half duplex bidirectional buffered I/O line, with current limitation at ±15 mA, maximum frequency 1 MHz
- 2 auxiliary card I/O lines controlled by I^2C-bus (C4 and C8)
- V_{CC} regulation: 5 V, 3 V or 1.8 V ± 8 %, I_{CC} < 55 mA, current spikes of 40 nAs up to 20 MHz, with controlled rise and fall times, filtered overload detection approximately 80 mA, current limitation about 120 mA
- Thermal and short-circuit protections on all card contacts
- Automatic activation and deactivation sequences: initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, V_{DD} or $V_{DD(DCDC)}$ drop-out
- Enhanced ElectroStatic Discharge (ESD) protection on card side (> 6 kV)
- 20 MHz clock input
- Clock generation for the card up to 10 MHz (CLKIN divided by 1, 2, 4 or 5) with synchronous frequency changes; stop HIGH or LOW or free running 1 MHz in cards Low-power mode; current limitation on pin CLK (C3)
- RST signal (C2) with current limitation at 20 mA, controlled by an embedded programmable CLK pulse counter on asynchronous cards or by a register on synchronous cards
- ISO 7816-3, GSM 11.11 and EMVCo 4.3 compatibility
- Supply voltage supervisor for spike killing during power-on and emergency deactivation at power-off: threshold internally fixed or set via an external resistor bridge; pulse width internally fixed or set via an external capacitor
- Card presence input with 10 ms built-in debouncing system
- One interrupt signal $\overline{INT}$

3. Applications

- Banking terminals
- Internet terminals
- Set-top boxes
- Portable IC card readers

4. Quick reference data

Table 1. Quick reference data

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage	on pin V_{DD}	2.7	-	6.5	V
$V_{DD(DCDC)}$	DC-to-DC converter supply voltage	on pin V_{DDP}	2.7	-	6.5	V
$V_{DD(INTF)}$	interface supply voltage	on pin V_{DDI}	1.5	-	6.5	V
I_{DD}	supply current	Shutdown mode [1]	-	-	10	µA
		Inactive mode; CLKIN LOW or HIGH [1]	-	-	200	µA
		Active mode; V_{CC} = 5 V; f_{CLK} = 5 MHz [1]				
		capacitive; I_{CC} = 5 mA	-	-	15	mA
		capacitive; I_{CC} = 55 mA	-	-	200	mA
		inductive; I_{CC} = 5 mA	-	-	15	mA
		inductive; I_{CC} = 55 mA	-	-	150	mA
		Power-down mode; V_{CC} = 5 V; I_{CC} = 100 µA; CLK stopped; CLKIN HIGH or LOW; capacitive or inductive [1]	-	-	2	mA
Supply voltage for the card: pin V_{CC} [2]						
V_{CC}	supply voltage	Active mode; 2.7 V < V_{DD} < 6.5 V [3]				
		5 V card; I_{CC} < 60 mA; V_{CC} = 5 V	4.75	5	5.25	V
		3 V card; I_{CC} < 55 mA; V_{CC} = 3 V	2.80	3	3.15	V
		1.8 V card; I_{CC} < 35 mA; V_{CC} = 1.8 V	1.66	1.8	1.94	V
		Active mode; AC current pulses with I < 200 mA, t < 400 ns and f < 20 MHz [3]				
		5 V card; current pulses of 40 nAs	4.65	-	5.35	V
		3 V card; current pulses of 24 nAs	2.76	-	3.24	V
		1.8 V card; current pulses of 15 nAs	1.62	-	1.98	V
$V_{ripple(p-p)}$	peak-to-peak ripple voltage	on V_{CC}; 20 kHz to 200 MHz	-	-	350	mV
I_{CC}	supply current	V_{DD} > 2.7 V				
		5 V card; V_{CC} = 0 V to 5 V	-	-	–55	mA
		3 V card; V_{CC} = 0 V to 3 V	-	-	–55	mA
		1.8 V card; V_{CC} = 0 V to 1.8 V	-	-	–35	mA

Table 1. Quick reference data *...continued*

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
t_{deact}	deactivation time	total sequence	60	80	100	µs
P_{tot}	total power dissipation	T_{amb} = −25 °C to +85 °C	-	-	500	mW
T_{amb}	ambient temperature		−40	-	+85	°C

[1] Sum of currents on pins V_{DD} and V_{DDI}.

[2] Two ceramic multilayer capacitors of minimum 100 nF with low Equivalent Series Resistance (ESR) should be used in order to meet these specifications.

[3] Output voltage towards the card, including ripple.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8023TT	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

6. Block diagram

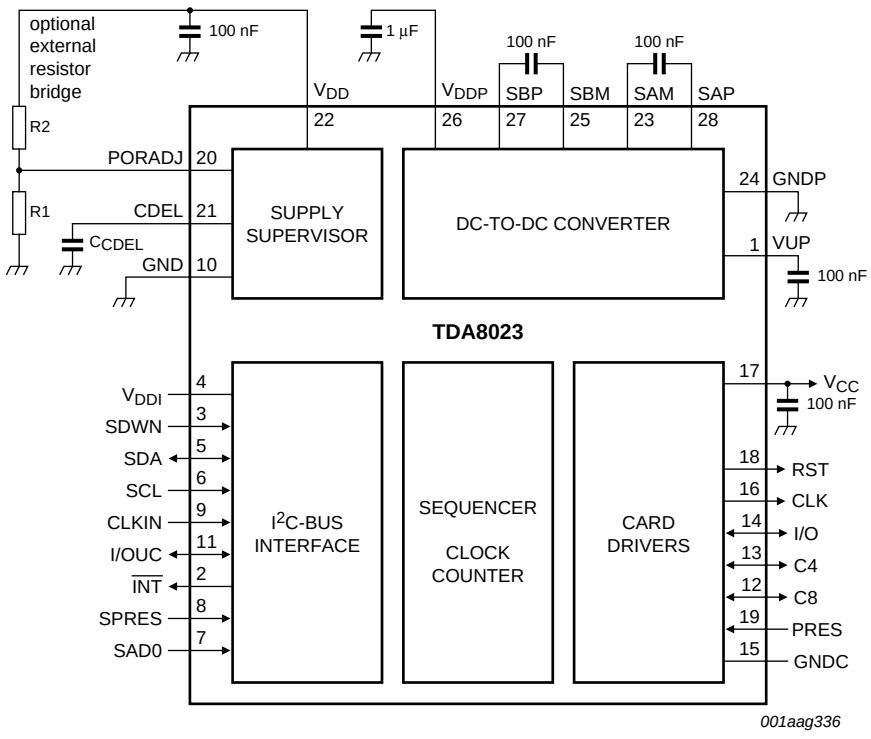


Fig 1. Block diagram with capacitive DC-to-DC converter

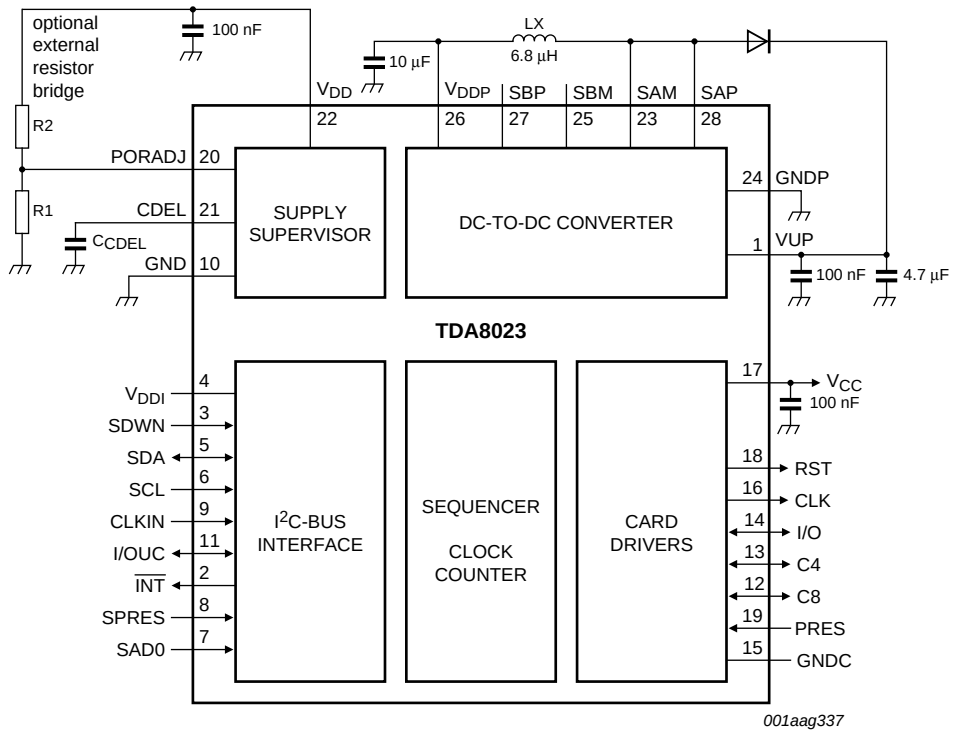


Fig 2. Block diagram with inductive DC-to-DC converter

7. Pinning information

7.1 Pinning

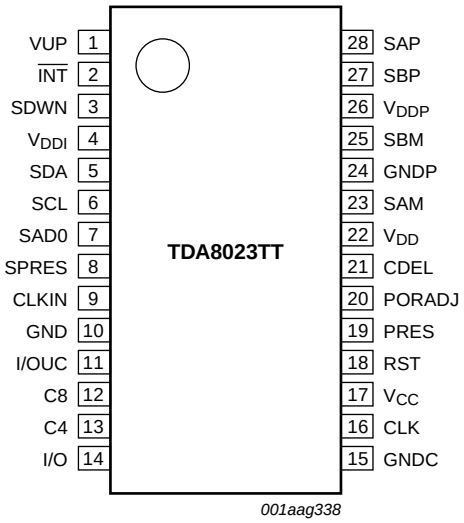


Fig 3. Pin configuration TDA8023TT

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
VUP	1	O	output of the DC-to-DC converter
$\overline{INT}$	2	O	Negative-channel Metal Oxide Semiconductor (NMOS) interrupt to the host (active LOW and open-drain) (see fault detection in Section 8.7 “Protection”)
SDWN	3	I	shutdown and reset input
V_{DDI}	4	S	interface positive supply voltage
SDA	5	I/O	serial data line to/from the I^2C-bus master (open-drain)
SCL	6	I	serial clock line from the I^2C-bus master
SAD0	7	I	I^2C-bus address selection
SPRES	8	I	select PRES mode[2]
CLKIN	9	I	external clock input
GND	10	S	ground connection
I/OUC	11	I/O[3]	data in/out from/to microcontroller
C8	12	I/O[4]	auxiliary input/output to/from the card (contact C8)
C4	13	I/O[4]	auxiliary input/output to/from the card (contact C4)
I/O	14	I/O[4]	data input/output to/from (contact C7 of) the card
GNDC	15	S	ground connection for the card (contact C5)
CLK	16	O	clock output to (contact C3 of) the card
V_{CC}	17	S	supply voltage for the card (contact C1)
RST	18	O	reset output to (contact C2 of) the card
PRES	19	I	card presence input with a 10 ms built-in debouncing system[2]
PORADJ	20	I	input for changing the power-on reset threshold with an external resistor bridge. **In case no external resistor bridge is used, it is mandatory to connect this pin to GND to avoid possible perturbations.**
CDEL	21	C	delay capacitor connection for the voltage supervisor (1 ms per 2 nF)
V_{DD}	22	S	power supply
SAM	23	C	connection for the DC-to-DC converter
GNDP	24	S	ground connection for the DC-to-DC converter
SBM	25	C	connection for the DC-to-DC converter
V_{DDP}	26	S	positive supply for the DC-to-DC converter
SBP	27	C	connection for the DC-to-DC converter
SAP	28	C	connection for the DC-to-DC converter

[1] I = input, O = output, S = supply, C = configuration.

[2] PRES is active-HIGH when SPRES = LOW and PRES is active-LOW when SPRES = HIGH.

[3] With integrated pull-up to $V_{DD(INTF)}$.

[4] With integrated pull-up to V_{CC}.

8. Functional description

Remark: Throughout this document, it is assumed that the reader is familiar with ISO 7816 and EMV terminology.

8.1 Power supplies

The supply pins for the TDA8023 are V_{DD} and GND. V_{DD} should be in the range from 2.7 V to 6.5 V. The supply voltages V_{DD}, $V_{DD(INTF)}$ and $V_{DD(DCDC)}$ may be applied to the TDA8023 in any time sequence.

All interface signals with the system controller are referenced to a separate supply voltage $V_{DD(INTF)}$ on pin V_{DDI}, that may be lower or higher than V_{DD}.

For generating a supply voltage V_{CC} of 5 V ± 5 % or 3 V ± 5 % used by the card, an integrated DC-to-DC converter is incorporated. This DC-to-DC converter should be separately supplied by $V_{DD(DCDC)}$ on pin V_{DDP} and GNDP (from 2.7 V to 6.5 V).

The I^2C-bus signals SDA and SCL may be externally referenced to a voltage higher than V_{DD}.

8.2 Voltage supervisor

8.2.1 Without external divider on pin PORADJ

The voltage supervisor surveys the V_{DD} supply voltage. It is used as Power-On Reset (POR) and as supply dropout detection during a card session. Supply dropout detection ensures that a proper deactivation sequence is followed before the voltage is too low. A reset pulse of duration t_W (see Figure 4) is used internally for maintaining the TDA8023 in the Inactive mode during powering up or powering down of V_{DD}.

As long as V_{DD} is less than $V_{th(POR)H}$ the TDA8023 will remain inactive whatever the levels on the command lines are. This also lasts for the duration of t_W after V_{DD} has reached a level higher than $V_{th(POR)H}$. When V_{DD} falls below $V_{th(POR)L}$ an automatic deactivation sequence of the contacts is performed.

In this case (no external resistor bridge) it is mandatory to connect pin PORADJ to GND.

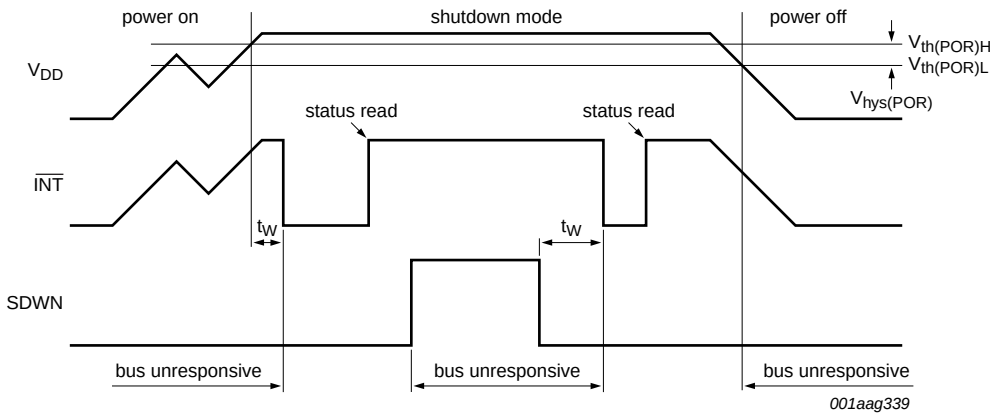


Fig 4. Voltage supervisor and Shutdown mode

8.2.2 With external divider on pin PORADJ

If an external resistor bridge is connected to pin PORADJ (R1 to GND and R2 to V_{DD} as shown in Figure 1 and Figure 2), then the internal threshold voltages and the internal hysteresis voltage are overridden by externally determined ones.

The voltage on pin PORADJ is:

$$V_{PORADJ} = \frac{R1}{R1 + R2} \times V_{DD} = k \times V_{DD}$$

where

$$k = \frac{R1}{R1 + R2}$$

The thresholds that are applied by the TDA8023 to this voltage V_{PORADJ} are:

$$V_{th(H)(PORADJ)} = V_{bg(int)} + \frac{V_{hys}}{2} \text{ (rising)}$$

$$V_{th(L)(PORADJ)} = V_{bg(int)} - \frac{V_{hys}}{2} \text{ (falling)}$$

where

$V_{bg(int)}$ = 1.25 V (typ)

V_{hys} = 60 mV (typ)

The thresholds and hysteresis on V_{DD} can then be calculated from:

$$V_{th(POR)H} = \frac{V_{th(H)(PORADJ)}}{k} = \frac{\left(V_{bg(int)} + \frac{V_{hys}}{2}\right)}{k} \text{ (rising)}$$

$$V_{th(POR)L} = \frac{V_{th(L)(PORADJ)}}{k} = \frac{\left(V_{bg(int)} - \frac{V_{hys}}{2}\right)}{k} \text{ (falling)}$$

$$V_{hys(POR)} = \frac{V_{hys}}{k}$$

The minimum threshold voltage $V_{th(POR)L}$ should be chosen higher than 2 V.

Input PORADJ is biased internally with a pull-down current source of 4 μA which is cut when the voltage on this pin exceeds 1 V. This ensures that after detection of the external bridge during power-on, the input current on this pin does not cause inaccuracy of the bridge voltage.

8.2.3 External capacitor on pin CDEL

The width of the POR pulse (t_W) is externally set by the value of the CDEL capacitor: the typical value is 1 ms per 2 nF. Usually C_{CDEL} = 22 nF, therefore t_W = 10 ms (typ).

8.2.4 Shutdown mode

When pin SDWN = HIGH, the TDA8023 is in Shutdown mode; the consumption in this mode is less than 10 μA. The I²C-bus is unresponsive.

If the card is extracted or inserted when the TDA8023 is in Power-down mode, pin $\overline{\text{INT}}$ becomes LOW and stays LOW as long as pin SDWN = HIGH.

When pin SDWN is pulled LOW, the TDA8023 leaves Shutdown mode and executes a complete power-on reset sequence.

8.3 I²C-bus

A 400 kHz I²C-bus slave interface is used for configuring the TDA8023 and reading the status.

8.3.1 I²C-bus protocol

The I²C-bus is for 2-way 2-line communication between ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA) and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH; changes in the data line while the clock line is HIGH will be interpreted as control signals

8.3.2 Bus conditions

The following bus conditions have been defined.

Bus not busy — Both data and clock lines remain HIGH.

Start data transfer — A change in the state of the data line from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer — A change in the state of the data line from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid — The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

8.3.3 Data transfer

Each data transfer is initiated with a START condition and terminated with a STOP condition (see Figure 7). See Table 15 for timing information.

Data transfer is unlimited in the Read mode. The information is transmitted in bytes and each receiver acknowledges with a 9th bit.

Within the I²C-bus specifications, a Standard mode (100 kHz clock rate) and a Fast-speed mode (400 kHz clock rate) are defined. The TDA8023 operates in both Fast-speed and Standard modes.

By definition, a device that sends a signal is called a transmitter and a device that receives the signal is called a receiver. The device that controls the signal is called the master. The devices that are controlled by the master are called slaves.

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge-related clock pulse. The slave receiver that is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master generation of the STOP condition.

8.3.4 Device addressing

Each TDA8023 has 2 different addresses, one for each of its two registers.

Two TDA8023s may be used in parallel due to the address selection pin SAD0. Pin SAD0 is externally hardwired to pin V_{DD} or pin GND. The voltage on pin SAD0 sets address bit b2: HIGH sets bit b2 to logic 1, LOW resets b2 to logic 0.

Address bit b1 selects Register 0 or Register 1.

Address bit b0 defines Read or Write operation: 1 means Read, 0 means Write.

The addresses for the TDA8023 are shown in Table 4 and Table 5.

Table 4. Device addressing

b7	b6	b5	b4	b3	b2	b1	b0
0	1	0	0	0	SAD0	0/1	R/W

Table 5. I²C-bus addresses for write mode

Pin SAD0	Register 0	Register 1
L	40h	42h
H	44h	46h

8.3.5 Registers

Table 6. Table of registers

Bit	Register 0		Register 1			
	Read mode	Write mode	Read/Write mode			
	Status	Command	REG1 = 0		REG1 = 1	
			REG0 = 0	REG0 = 1	REG0 = 0	REG0 = 1
7	ACTIVE	VCC1V8	TEST	D7	C15	C7
6	EARLY	I/OEN	RSTIN	D6	C14	C6
5	MUTE	REG1	C8	D5	C13	C5
4	PROT	REG0	C4	D4	C12	C4
3	SUPL	PDWN	CLKPD2	D3	C11	C3
2	CLKSW	5V/3VN	CLKPD1	D2	C10	C2
1	PRESL	WARM	CLKDIV2	D1	C9	C1
0	PRES	START	CLKDIV1	D0	C8	C0

Table 7. Status - Register 0 in Read mode bit description

Bit	Symbol	Description
7	ACTIVE	set if the card is active; reset if the card is inactive
6	EARLY	set during Answer To Reset (ATR) when the selected card has answered too early
5	MUTE	set during ATR when the card has not answered during the ISO 7816 time slots
4	PROT	set when an overload or an overheating has occurred during a session; reset when the status has been read
3	SUPL	set when the voltage supervisor has signalled a fault; reset when the status has been read
2	CLKSW	set when the TDA8023 is in Power-down mode and the clock has changed
1	PRESL	set when the card has been inserted or extracted; reset when the status has been read
0	PRES	set when the card is present; reset when the card is not present

When at least one of the bits PRESL, PROT, MUTE and EARLY is set, pin $\overline{INT}$ goes LOW until the status byte has been read. After power-on, bit SUPL is set until the status byte has been read, and pin $\overline{INT}$ = LOW until the voltage supervisor becomes inactive.

Table 8. Command - Register 0 in Write mode bit description

Bit	Symbol	Description
7	VCC1V8	1: V_{CC} = 1.8 V 0: V_{CC} is defined by bit 5V/3VN this bit can not change if bit START is logic 1
6	I/OEN	1: signal on pin I/OUC is transferred to pin I/O 0: pin I/OUC and pin I/O are high-impedance
5 and 4	REG[1:0]	selection of subaddress in Register 1 (see Table 9, 10, 11 and 12)

Table 8. Command - Register 0 in Write mode bit description *...continued*

Bit	Symbol	Description
3	PDWN	1: applies on pin CLK the frequency that is defined by bits CLKPD[2:1] and reduces power consumption (in Synchronous mode); this bit can not change if bit START is logic 1
2	5V/3VN	1: V_{CC} = 5 V 0: V_{CC} = 3 V this bit can not change if bit START is logic 1
1	WARM	1: initiates a warm reset procedure this bit will be automatically reset by hardware when bit MUTE is set to logic 1
0	START	1: initiates an activation sequence and a cold reset procedure (only if bit SUPL = 0 and the bit PRES = 1) 0: initiates a deactivation sequence

Table 9. R1_00 - Register 1 subaddress 00 in Read/Write mode bit description

Bit	Symbol	Description
7	TEST	1: the circuit is in Test mode 0: the circuit is in Operational mode
6	RSTIN[1]	defines the voltage on pin RST: 1: V_{CC} 0: 0 V
5	C8	defines the voltage on pin C8: 1: V_{CC} 0: 0 V
4	C4	defines the voltage on pin C4: 1: V_{CC} 0: 0 V
3 and 2	CLKPD[2:1]	clock pulse definition: 00: CLK stop LOW 01: CLK stop HIGH 10: frequency on pin CLK: $f_{CLK} = f_{osc(int)} / 2$ 11: no change in Synchronous mode bit CLKPD2 is always logic 0 by hardware and bit CLKPD1 controls the voltage on pin CLK: 1: V_{CC} 0: 0 V
1 and 0	CLKDIV[2:1]	clock divider: 00: $f_{CLK} = f_{CLKIN}$ 01: $f_{CLK} = f_{CLKIN} / 2$ 10: $f_{CLK} = f_{CLKIN} / 4$ 11: $f_{CLK} = f_{CLKIN} / 5$ in Synchronous mode, bits CLKDIV[2:1] are always 00 by hardware

[1] Synchronous or asynchronous cards management are defined when bit START is set: the TDA8023 will be in asynchronous cards management when bit RSTIN = 1 when bit START is set to logic 1.

Table 10. R1_01 - Register 1 subaddress 01 in Read/Write mode bit description

Bit	Symbol	Description
7 to 0	D[7:0]	8-bit programmable CLK period count register; range: 0 to 255; initial value: 170

Table 11. R1_10 - Register 1 subaddress 10 in Read/Write mode bit description

Bit	Symbol	Description
7 to 0	C[15:8]	8-bit programmable CLK period count register; range in combination with C[7:0]: 0 to 65535; initial value: 164

Table 12. R1_11 - Register 1 subaddress 11 in Read/Write mode bit description

Bit	Symbol	Description
7 to 0	C[7:0]	8-bit programmable CLK period count register; range in combination with C[15:8]: 0 to 65535; initial value: 116

If bit RSTIN = 0 when bit START is set to logic 1, then pin RST is controlled by bit RSTIN. Else, pin RST = LOW during a number of CLK periods, defined by the 16-bit CLK count register C[15:0], and goes HIGH afterwards.

There are two synchronous card management types:

- If bit PDWN = 0 when bit START is set to logic 1, then the output CLK is controlled by input CLKIN (without division)
- If bit PDWN = 1 when bit START is set to logic 1, then the output CLK is controlled by bit CLKPD1

8.4 DC-to-DC converter

For generating a supply voltage V_{CC} of 5 V ± 5 % or 3 V ± 5 % to the card, an integrated voltage converter is incorporated. This DC-to-DC converter should be separately supplied by $V_{DD(DCDC)}$ on pin V_{DDP} and GNDP (from 2.7 V to 6.5 V).

The DC-to-DC conversion is either capacitive or inductive, according to the external components (automatic detection).

8.4.1 Capacitive configuration

The external components are three 100 nF capacitors (low-ESR), see Figure 1.

The DC-to-DC converter is either tripler, doubler or follower according to the respective values of V_{CC} and $V_{DD(DCDC)}$. An hysteresis of 100 mV is present on both thresholds:

- Follower:
  - If V_{CC} = 5 V and $V_{DD(DCDC)}$ > 5.8 V
  - If V_{CC} = 3 V and $V_{DD(DCDC)}$ > 4 V
  - If V_{CC} = 1.8 V

- Doubler:
  - If V_{CC} = 5 V and $V_{DD(DCDC)}$ = 4 V to 5.8 V
  - If V_{CC} = 3 V and $V_{DD(DCDC)}$ < 4 V
- Tripler:
  - If V_{CC} = 5 V and $V_{DD(DCDC)}$ < 4 V

8.4.2 Inductive configuration

The external components are a diode, a coil of 6.8 μH and a capacitor of 4.7 μF (see Figure 2). In this configuration the DC-to-DC converter acts as follows.

- If V_{CC} = 5 V then V_{VUP} is regulated at 5.5 V
- If V_{CC} = 3 V then V_{VUP} is regulated at 4 V
- If V_{CC} = 1.8 V then the DC-to-DC converter acts as a follower

8.5 V_{CC} buffer

In all modes (follower, doubler, tripler), the DC-to-DC converter is able to deliver 60 mA over the whole V_{DD} range (2.7 V to 6.5 V) or 90 mA if V_{DD} > 3 V.

The current on the V_{CC} buffer has an internal limitation of around 90 mA. When this limit is reached, an automatic deactivation sequence is performed.

The V_{CC} voltage should be decoupled with a low-ESR capacitor between 100 nF and 168 nF. If the card socket is not very close to the TDA8023, one capacitor should be placed near the TDA8023, and a second one near the card contacts.

8.6 Sequencer and clock counter

The sequencer takes care of ensuring activation and deactivation sequences according to ISO 7816 and EMVCo 4.3, even in case of emergency (card removal during transaction, supply dropout or hardware problem).

The sequencer is clocked with an internal oscillator.

The activation of a card is initiated by setting bit START in the Command register, which is only possible if the card is present and if the voltage supervisor is not active. The activation sequence is described in Section 8.6.1.

The deactivation is initiated either by the system controller or automatically in case of a hardware problem or a supply dropout. The deactivation sequence is described in Section 8.6.2.

Outside a session, card contacts are forced low-impedance with respect to pin GNDC.

8.6.1 Activation sequence

When the card is inactive, pins V_{CC}, CLK, RST and I/O are LOW, which is low-impedance with respect to pin GNDC. The DC-to-DC converter is stopped.

When everything is satisfactorily present (voltage supply, card present, no hardware problems) the system controller may initiate an activation sequence of a present card:

1. The internal oscillator changes to its high frequency (t_0, see Figure 5).
2. The DC-to-DC converter is started (t_1).
3. V_{CC} starts rising from 0 V to 5 V, 3 V or 1.8 V with a controlled rise time (t_2).
4. The voltage on pin I/O rises to V_{CC}, due to integrated 14 kΩ pull-ups to V_{CC} (t_3).
5. CLK is sent to the card and pin RST is enabled ($t_4 = t_{act}$).

During the activation sequence, the answer from the card (ATR) is monitored and the steps are the following:

1. If a start bit is detected on pin I/O during the first 200 CLK pulses, then it is simply ignored, and the CLK count goes on.
2. If a start bit is detected whilst pin RST = LOW (between 200 and 42100 CLK pulses or the value written in C[15:0]), then the bits EARLY and MUTE are set in the Status register. Pin RST will remain LOW. It is up to the software to decide whether to accept the card or not.
3. If no start bit has been detected within 42100 CLK pulses, then pin RST is toggled to HIGH (t_5).
4. If, again, a start bit is detected within 370 CLK pulses (200 + 170 or the value defined in D[7:0]), bit EARLY in the Status register is set.
5. If the card does not answer within 42100 new CLK pulses, then bit MUTE in the Status register is set.
6. If the card answers within the correct time window, then the CLK count is stopped and the system controller can send commands to the card.

The sequencer is clocked by $\frac{f_{osc(int)}}{64}$ which leads to a time interval T = 25 µs (typical).

Thus $t_1 = 0$ s to $\frac{T}{64}$, $t_2 = t_1 + \frac{3T}{2}$, $t_3 = t_1 + \frac{7T}{2}$ and $t_4 = t_1 + 4T$.

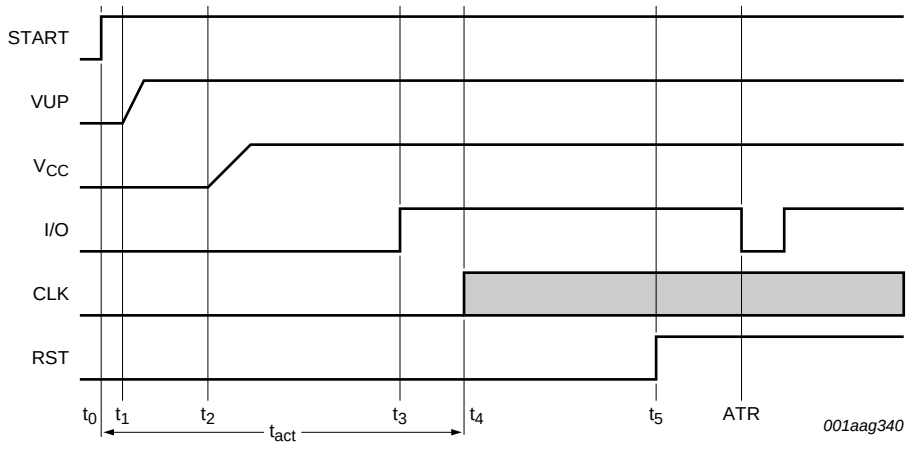


Fig 5. Activation sequence

8.6.2 Deactivation sequence

When the session is completed, the microcontroller resets bit START to logic 0 (t_{10}, see Figure 6). The circuit then executes an automatic deactivation sequence:

1. Card reset: pin RST falls to LOW (t_{11}).
2. CLK is stopped (t_{12}).
3. Pin I/O falls to 0 V (t_{13}).
4. Pin V_{CC} falls to 0 V with a controlled slew rate (t_{14}).
5. The DC-to-DC converter is stopped and pins CLK, RST, V_{CC} and I/O become low-impedance with relation to GNDC (t_{15}).
6. The internal oscillator changes to its low frequency (t_{15}).

$$t_{11} = t_{10} + \frac{T}{64},\ t_{12} = t_{11} + \frac{T}{2},\ t_{13} = t_{11} + T,\ t_{14} = t_{11} + \frac{3T}{2} \text{ and } t_{15} = t_{11} + \frac{7T}{2}.$$

The deactivation time t_{deact} is the time that V_{CC} needs for going down to less than 0.4 V, counted from the moment bit START is reset.

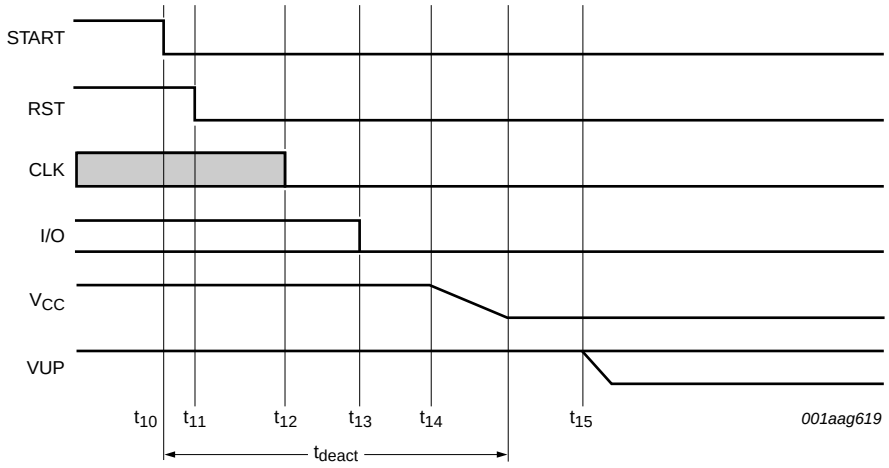


Fig 6. Deactivation sequence

8.7 Protection

All card contacts are protected against any short with any other card contact.

The currents on various pins are limited:

- on pin CLK: limited to ±70 mA
- on pin I/O: limited to ±10 mA (typical value)
- on pin RST: limited (only when this pin is LOW) to ±20 mA
- on pin V_{CC}: limited to 90 mA

If any of these currents exceeds its limit, an emergency deactivation sequence is performed: pin $\overline{INT}$ is pulled LOW and bit PROT in the Status register is set.

In case of overcurrent on pin V_{CC}, removal of the card during a session, overheating, supply dropout, DC-to-DC out of limits, or overcurrent on pin RST, the TDA8023 performs an automatic emergency deactivation sequence on the card, resets bit START and pulls pin INT LOW.

9. Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	on pin V_{DD}	–0.5	+6.5	V
$V_{DD(DCDC)}$	DC-to-DC converter supply voltage	on pin V_{DDP}	–0.5	+6.5	V
$V_{DD(INTF)}$	interface supply voltage	on pin V_{DDI}	–0.5	+6.5	V
V_{IH}	HIGH-level input voltage	on pins SAP, SAM, SBP, SBM, VUP	–0.5	+7.5	V
		on pins SDA, SCL	–0.5	+6.5	V
		on all other pins	–0.5	V_{DD} + 0.5	V
P_{tot}	total power dissipation	T_{amb} = –25 °C to +85 °C	-	500	mW
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		-	150	°C
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM) [1]			
		on card pins I/O, V_{CC}, CLK, GNDC, PRES, RST	–6	+6	kV
		on all other pins	–2	+2	kV
		Machine Model (MM)			
		all pins, excluding card pins	–200	+200	V

[1] Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM; 1500 Ω; 100 pF) defines 3 pulses positive and 3 pulses negative on each pin referenced to ground.

10. Thermal characteristics

Table 14. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		100	K/W

11. Characteristics

Table 15. Supply

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage	on pin V_{DD}		2.7	-	6.5	V
$V_{DD(DCDC)}$	DC-to-DC converter supply voltage	on pin V_{DDP}		2.7	-	6.5	V
$V_{DD(INTF)}$	interface supply voltage	on pin V_{DDI}		1.5	-	6.5	V
I_{DD}	supply current	Shutdown mode	[1]	-	-	10	µA
		Inactive mode; CLKIN LOW or HIGH	[1]	-	-	200	µA
		Active mode; V_{CC} = 5 V; f_{CLK} = 5 MHz	[1]				
		capacitive; I_{CC} = 5 mA		-	-	15	mA
		capacitive; I_{CC} = 55 mA		-	-	200	mA
		inductive; I_{CC} = 5 mA		-	-	15	mA
		inductive; I_{CC} = 55 mA		-	-	150	mA
		Power-down mode; V_{CC} = 5 V; I_{CC} = 100 µA; CLK stopped; CLKIN HIGH or LOW; capacitive or inductive	[1]	-	-	2	mA
$I_{DD(INTF)}$	interface supply current	on pin V_{DDI}		-	-	120	µA
$V_{th(POR)L}$	LOW-level power-on reset threshold voltage	decreasing voltage on pin V_{DD}; see Figure 4		2.30	-	2.60	V
$V_{hys(POR)}$	power-on reset hysteresis voltage	on pin V_{DD}; see Figure 4		50	-	150	mV

[1] Sum of currents on pins V_{DD} and V_{DDI}.

Table 16. Supply supervisor

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin PORADJ							
$V_{th(H)(PORADJ)}$	HIGH-level threshold voltage on pin PORADJ	rising voltage; see Section 8.2.2		1.25	1.28	1.31	V
$V_{th(L)(PORADJ)}$	LOW-level threshold voltage on pin PORADJ	falling voltage; see Section 8.2.2		1.19	1.22	1.25	V
V_{hys}	hysteresis voltage	$V_{th(H)(PORADJ)} - V_{th(L)(PORADJ)}$; see Section 8.2.2		30	60	90	mV
$\Delta V_{th}/\Delta T$	threshold voltage variation with temperature	on $V_{th(H)(PORADJ)}$ and $V_{th(L)(PORADJ)}$		-	-	0.25	mV/°C
I_L	leakage current	V_{PORADJ} < 0.6 V		0	4	10	µA
		V_{PORADJ} > 0.8 V		−1	-	+1	µA
Pin CDEL							
V_{CDEL}	voltage on pin CDEL			-	-	V_{DD} + 0.3	V
I_{CDEL}	current on pin CDEL	pin grounded (charge)		-	−2	0	µA
		V_{CDEL} = V_{DD} (discharge)		-	−5	-	mA
t_W	pulse width	internal alarm pulse; C_{CDEL} = 22 nF		-	10	-	ms

Table 17. DC-to-DC converter

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{osc(int)}$	internal oscillator frequency			2	2.5	3	MHz
V_{VUP}	voltage on pin VUP	5 V card		5.3	5.5	5.8	V
		3 V card		3.5	4	4.2	V
		1.8 V card		-	$V_{DD(DCDC)}$	-	V
V_{det}	detection voltage	on pin V_{DDP}					
		5 V card; Follower mode		5.5	5.8	6	V
		3 V card; Follower mode		3.8	4	4.2	V
		5 V card; Tripler mode		-	3.5	-	V

Table 18. Card drivers

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply voltage for the card: pin V_{CC} [1]							
$V_{o(inact)}$	inactive mode output voltage	no load		0	-	0.1	V
		$I_{o(inact)}$ = 1 mA		0	-	0.3	V
$I_{o(inact)}$	inactive mode output current	at grounded pin V_{CC}		-	-	–1	mA
V_{CC}	supply voltage	Active mode; 2.7 V < V_{DD} < 6.5 V	[2]				
		5 V card; I_{CC} < 60 mA; V_{CC} = 5 V		4.75	5	5.25	V
		3 V card; I_{CC} < 55 mA; V_{CC} = 3 V		2.80	3	3.15	V
		1.8 V card; I_{CC} < 35 mA; V_{CC} = 1.8 V		1.66	1.8	1.94	V
		Active mode; AC current pulses with I < 200 mA, t < 400 ns and f < 20 MHz	[2]				
		5 V card; current pulses of 40 nAs		4.65	-	5.35	V
		3 V card; current pulses of 24 nAs		2.76	-	3.24	V
		1.8 V card; current pulses of 15 nAs		1.62	-	1.98	V
$V_{ripple(p-p)}$	peak-to-peak ripple voltage	on V_{CC}; 20 kHz < f < 200 MHz		-	-	350	mV
I_{CC}	supply current	V_{DD} > 2.7 V					
		5 V card; V_{CC} = 0 V to 5 V		-	-	–55	mA
		3 V card; V_{CC} = 0 V to 3 V		-	-	–55	mA
		1.8 V card; V_{CC} = 0 V to 1.8 V		-	-	–35	mA
		V_{CC} shorted to GND					
		5 V card or 3 V card		-	–90	–120	mA
		1.8 V card		-	–70	–90	mA
SR	slew rate	rise or fall; maximum load capacitor C_L = 300 nF					
		5 V card		0.080	0.140	0.200	V/µs
		3 V card		0.050	0.080	0.110	V/µs
		1.8 V card		0.025	0.045	0.080	V/µs

Table 18. Card drivers *...continued*

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reset output to the card: pin RST							
$V_{o(inact)}$	inactive mode output voltage	no load		0	-	0.1	V
		$I_{o(inact)}$ = 1 mA		0	-	0.3	V
$I_{o(inact)}$	inactive mode output current	at grounded pin RST		0	-	−1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA		0	-	0.15 Vcc	V
V_{OH}	HIGH-level output voltage	I_{OH} < −200 μA		V_{CC} − 0.5	-	V_{CC}	V
t_r	rise time	C_L = 30 pF		-	-	0.1	μs
t_f	fall time	C_L = 30 pF		-	-	0.1	μs
Clock output to the card: pin CLK							
$V_{o(inact)}$	inactive mode output voltage	no load		0	-	0.1	V
		$I_{o(inact)}$ = 1 mA		0	-	0.3	V
$I_{o(inact)}$	inactive mode output current	at grounded pin CLK		0	-	−1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA		0	-	0.15 Vcc	V
V_{OH}	HIGH-level output voltage	I_{OH} < −200 μA		V_{CC} − 0.5	-	V_{CC}	V
t_r	rise time	C_L = 30 pF		-	-	8	ns
t_f	fall time	C_L = 30 pF		-	-	8	ns
f_{CLK}	frequency on pin CLK	operational		0	-	10	MHz
δ	clock duty cycle	C_L = 30 pF		45	-	55	%
SR	slew rate	rise and fall; C_L = 30 pF		0.2	-	-	V/ns
Data lines: pins I/O, C4 and C8							
$V_{o(inact)}$	inactive mode output voltage	no load		0	-	0.1	V
		$I_{o(inact)}$ = 1 mA		-	-	0.3	V
$I_{o(inact)}$	inactive mode output current	at grounded pin I/O	[3]	-	-	−1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA		0	-	0.15 Vcc	V
V_{OH}	HIGH-level output voltage	no DC load		$0.9V_{CC}$	-	V_{CC} + 0.1	V
		I_{OH} < −20 μA		$0.8V_{CC}$	-	V_{CC} + 0.1	V
		I_{OH} < −40 μA		$0.75V_{CC}$	-	V_{CC} + 0.1	V
V_{IL}	LOW-level input voltage			−0.3	-	0.2 Vcc	V
V_{IH}	HIGH-level input voltage			0.6 Vcc	-	V_{CC}	V
I_{IL}	LOW-level input current	at pin I/O; V_{IL} = 0 V	[3]				
		V_{CC} = 5 V		-	-	600	μA
		V_{CC} = 3 V		-	-	500	μA
I_{LIH}	HIGH-level input leakage current	at pin I/O; V_{IH} = V_{CC}	[3]	-	-	10	μA

Table 18. Card drivers *...continued*

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{pu}	pull-up current	at pin I/O; $V_{OH} = 0.9V_{CC}$; C_L = 30 pF	[3]	–1	-	-	mA
t_d	delay time	between edges on pin I/O and pin I/OUC; corresponds to width of active pull-up pulse	[3][4]	-	500	650	ns
t_r	rise time	inputs; from $V_{IL(max)}$ to $V_{IH(min)}$		-	-	1.5	µs
t_R and t_F	IO rise anf fall time	output transition time; from 10 % of V_{CC} to 90 % of V_{CC}; C_L < 30 pF; no DC load		-	-	0.1	µs
C_i	input capacitance	on pin I/O	[3]	-	-	10	pF
$R_{pu(int)}$	internal pull-up resistance	between pin I/O and V_{CC}	[3]	10	13.5	17	kΩ
f_{max}	maximum input clock frequency	on pin I/O	[3]	-	-	500	kHz
Card presence input: pin PRES, active-HIGH when pin SPRES = LOW or active-LOW when pin SPRES = HIGH							
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
I_{LIL}	LOW-level input leakage current	$V_I = 0.3V_{DD}$; pin SPRES = HIGH		0	-	5	µA
		$V_I = 0.3V_{DD}$; pin SPRES = LOW		10	-	40	µA
I_{LIH}	HIGH-level input leakage current	$V_I = 0.7V_{DD}$; pin SPRES = HIGH		–40	-	–10	µA
		$V_I = 0.7V_{DD}$; pin SPRES = LOW		–5	-	0	µA

[1] Two ceramic multilayer capacitors of minimum 100 nF with low Equivalent Series Resistance (ESR) should be used in order to meet these specifications.

[2] Output voltage towards the card, including ripple.

[3] Pin I/O has an internal 15 kΩ pull-up resistor to V_{CC}.

[4] Pin I/OUC has an internal 11 kΩ pull-up resistor to $V_{DD(INTF)}$.

Table 19. Sequencer and clock counter

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{act}	activation time	total sequence	-	-	135	µs
t_{deact}	deactivation time	total sequence	60	80	100	µs

Table 20. Interface signals to host controller

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Data line: pin I/OUC[1]							
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA		0	-	0.3	V
V_{OH}	HIGH-level output voltage	no DC load		$0.9V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.2	V
		I_{OH} < –10 µA		$0.75V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.2	V
V_{IL}	LOW-level input voltage			–0.3	-	$0.25V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
I_{IL}	LOW-level input current	V_{IL} = 0 V		-	-	600	µA
I_{LIH}	HIGH-level input leakage current	$V_{IH} = V_{DD(INTF)}$		-	-	10	µA

Table 20. Interface signals to host controller *…continued*

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	input; from $V_{IL(max)}$ to $V_{IH(min)}$		-	-	1	µs
t_{TLH}	clock rise time	output transition time; from 10 % to 90 % of $V_{DD(INTF)}$; C_L < 30 pF		-	-	0.1	µs
$R_{pu(int)}$	internal pull-up resistance	between pin I/OUC and pin V_{DDI}	[1]	11	15	19	kΩ
Clock input: pin CLKIN							
f_{CLKIN}	frequency on pin CLKIN			0	-	25	MHz
V_{IL}	LOW-level input voltage	$V_{DD(INTF)}$ > 2 V		0	-	$0.3V_{DD(INTF)}$	V
		1.5 V < $V_{DD(INTF)}$ < 2 V		0	-	$0.15V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage	$V_{DD(INTF)}$ > 2 V		$0.7V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
		1.5 V < $V_{DD(INTF)}$ < 2 V		$0.85V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	ns
t_r	rise time			-	-	$0.1 / f_{CLKIN}$	ns
t_f	fall time			-	-	$0.1 / f_{CLKIN}$	ns
Logic inputs: pins SAD0, SPRES and SDWN							
V_{IL}	LOW-level input voltage			–0.3	-	$0.3V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	$V_{DD(INTF)}$ + 0.3	V
I_{LIL}	LOW-level input leakage current			-	-	±1	µA
I_{LIH}	HIGH-level input leakage current			-	-	±1	µA
C_i	input capacitance			-	-	10	pF
Interrupt line: pin $\overline{INT}$; open-drain active-LOW output							
V_{OL}	LOW-level output voltage	I_o = 2 mA		-	-	0.3	V
I_{LH}	HIGH-level leakage current			-	-	10	µA
Serial data input/output: pin SDA; open-drain							
V_{IL}	LOW-level input voltage			–0.3	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	6.5	V
V_{OL1}	LOW-level output voltage	I_{OL} = 3 mA		-	-	0.3	V
I_{LH}	HIGH-level leakage current	input or output		-	-	1	µA
I_{LL}	LOW-level leakage current	depends on the pull-up resistance; input or output		-	-	1	µA
Serial clock input: pin SCL							
V_{IL}	LOW-level input voltage			–0.3	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	6.5	V
I_{LIH}	HIGH-level input leakage current			-	-	1	µA
I_{IL}	LOW-level input current	depends on the pull-up resistance		-	-	1	µA

Table 20. Interface signals to host controller *…continued*

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I²C-bus timing; see Figure 7							
f_{SCL}	SCL clock frequency			0	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	hold time after which first clock pulse is generated		0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{HD;DAT}$	data hold time		[2]	0	-	-	ns
$t_{SU;DAT}$	data set-up time			100	-	-	ns
t_r	rise time of both SDA and SCL signals			-	-	300	ns
t_f	fall time of both SDA and SCL signals			-	-	300	ns
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs

[1] Pin I/OUC has an internal 11 kΩ pull-up resistor to $V_{DD(INTF)}$.

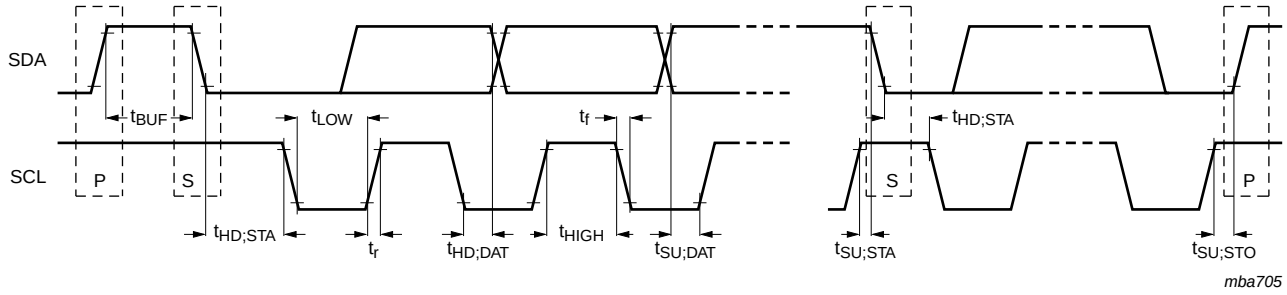
[2] The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

Table 21. Protection and limitations

V_{DD} = 3.3 V; $V_{DD(INTF)}$ = 1.5 V; f_{CLKIN} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	ambient temperature			–40	-	+85	°C
T_{sd}	shutdown temperature	at die		-	150	-	°C
I_{Ilim}	input current limit	on pin I/O	[1]	–15	-	+15	mA
I_{Olim}	output current limit	on pin I/O	[1]	–15	-	+15	mA
		on pin CLK		–70	-	+70	mA
		shutdown current; on pin RST		–20	-	+20	mA
		shutdown current; on pin V_{CC}		-	–90	-	mA

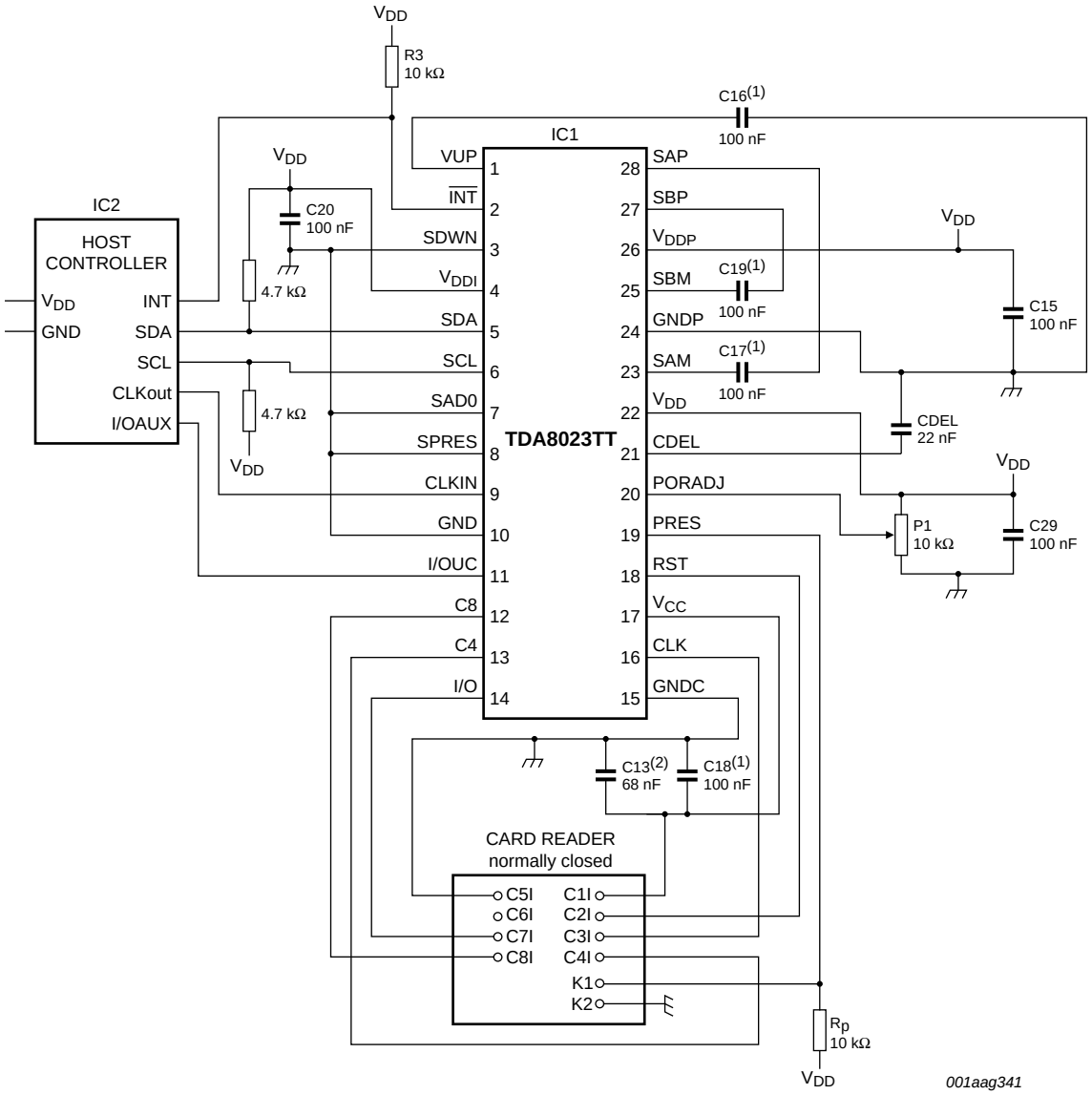
[1] Pin I/O has an internal 15 kΩ pull-up resistor to V_{CC}.



P = STOP condition; S = START condition.

Fig 7. Timing requirements for the I²C-bus

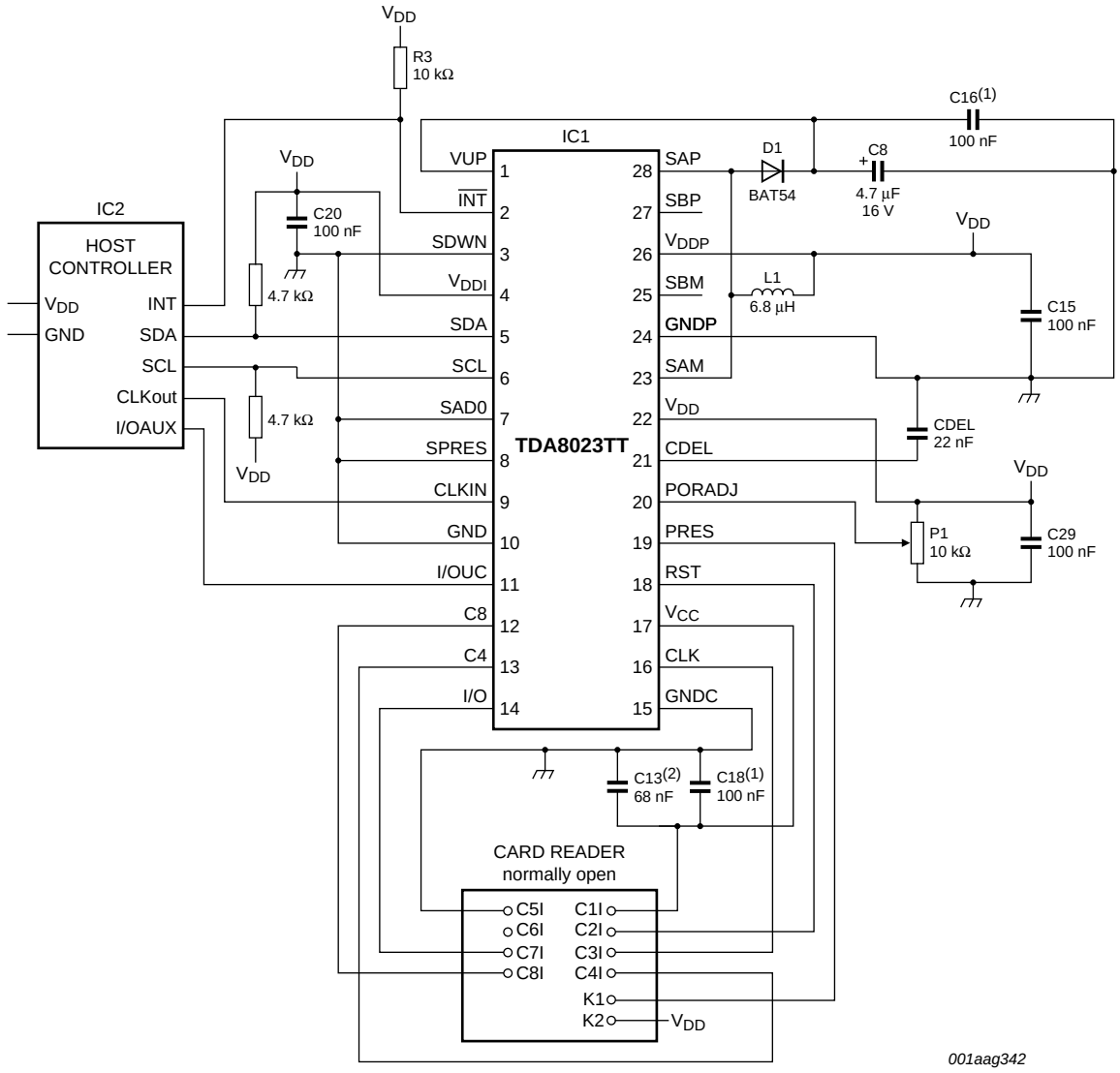
12. Application information



(1) Low-ESR capacitor, placed near the IC.

(2) Low-ESR capacitor, placed near the C1 contact.

Fig 8. Application diagram: typical TDA8023TT application with capacitive DC-to-DC converter



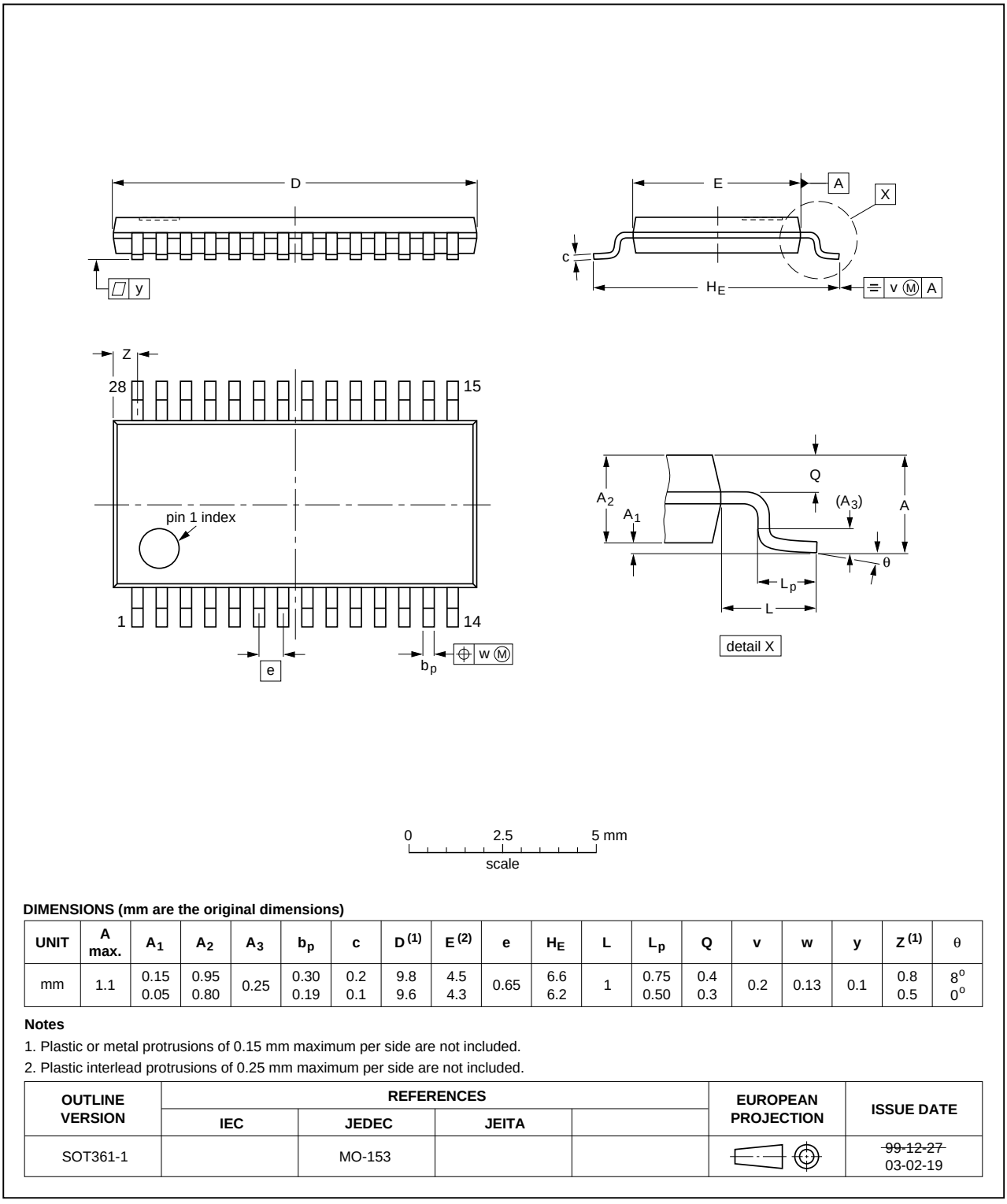
(1) Low-ESR capacitor, placed near the IC.

(2) Low-ESR capacitor, placed near the C1 contact.

Fig 9. Application diagram: typical TDA8023TT application with inductive DC-to-DC converter

13. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT361-1 (TSSOP28)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 22 and 23

Table 22. SnPb eutectic process (from J-STD-020D)

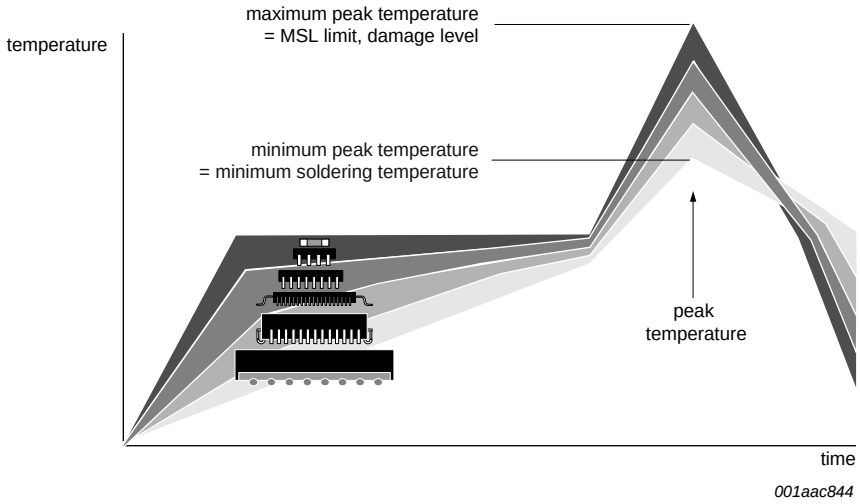
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 23. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Revision history

Table 24. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8023 v.2.0	20160624	Product data sheet	-	TDA8023_1
Modifications:	• Table 1 “Quick reference data”: V_{CC} at 1.8 V updated • Table 18 “Card drivers”: V_{IL} V_{OL} V_{OH} updated according to EMVCo 4.3. • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
TDA8023_1	20070716	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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