



**THE DATASHEET OF  
CY7C1061GN30-10ZSXI**



**16-Mbit (1 M words × 16 bit) Static RAM**

**Features**

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 90 \text{ mA}$  at 100 MHz
- Low CMOS standby current
  - $I_{SB2} = 20 \text{ mA}$  (typ)
- Operating voltages of 2.2 V to 3.6 V
- 1.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 54-pin TSOP II, and 48-ball VFBGA packages
- Offered in dual Chip Enable options

**Functional Description**

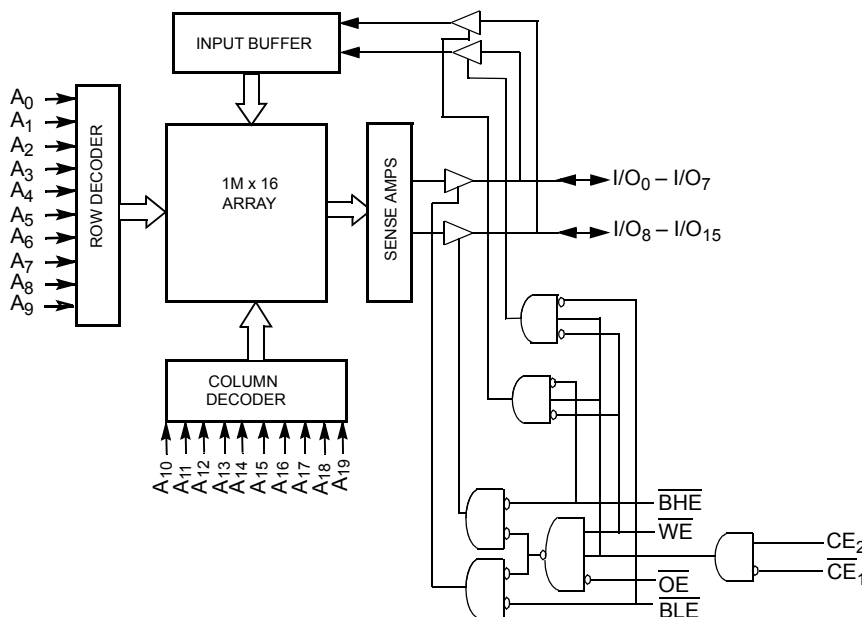
The CY7C1061GN30 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

To write to the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, take Chip Enables ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See Truth Table on page 12 for a complete description of Read and Write modes.

The input or output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH/ $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

**Logic Block Diagram**



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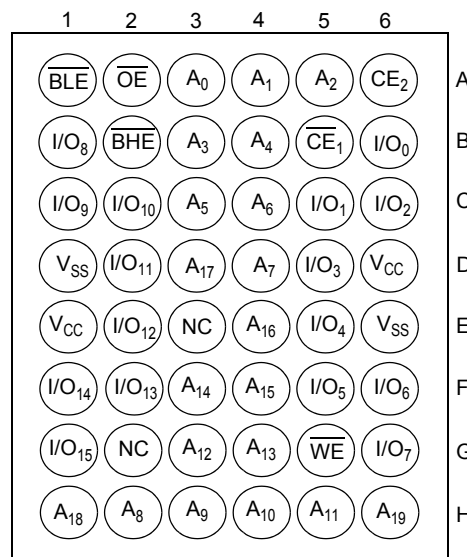
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### Selection Guide

Description	-10	Unit
Maximum access time	10	ns
Maximum operating current	110	mA
Maximum CMOS standby current	30	mA

### Pin Configurations

Figure 1. 48-ball VFBGA (8 × 9.5 × 1 mm) Dual Chip Enable pinout (Top View) <sup>[1]</sup>

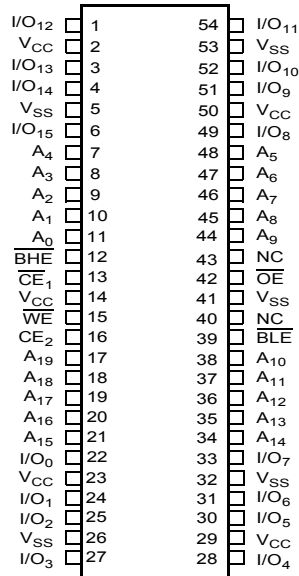


**Note**

1. NC pins are not connected internally to the die.

Pin Configurations (continued)

Figure 2. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout (Top View) [2]



Note

- NC pins are not connected internally to the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....	-65 °C to +150 °C
Ambient Temperature with Power Applied .....	-55 °C to +125 °C
Supply Voltage on V <sub>CC</sub> relative to GND [3] .....	-0.5 V to V <sub>CC</sub> + 0.5 V
DC Voltage Applied to Outputs in High Z State [3] .....	-0.5 V to V <sub>CC</sub> + 0.5 V

DC Input Voltage [3] .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015) .....	>2001 V
Latch Up Current .....	>200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10			Unit
			Min	Typ [4]	Max	
V <sub>OH</sub>	Output HIGH voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA			V
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA			
V <sub>OL</sub>	Output LOW voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2 mA			V
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA			
V <sub>IH</sub>	Input HIGH voltage [3]	2.2 V to 2.7 V	-			V
		2.7 V to 3.6 V	-			
V <sub>IL</sub>	Input LOW voltage [3]	2.2 V to 2.7 V	-			V
		2.7 V to 3.6 V	-			
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	-	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels	-	90	110	mA
I <sub>SB1</sub>	Automatic CE power down current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	-	40	mA
I <sub>SB2</sub>	Automatic CE power down current – CMOS inputs	Max V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3$ V, CE <sub>2</sub> ≤ 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0	-	20	30	mA

### Note

- V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of less than 2 ns.
- Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3 V (for a V<sub>CC</sub> range of 2.2 V–3.6 V), T<sub>A</sub> = 25 °C.

### Capacitance

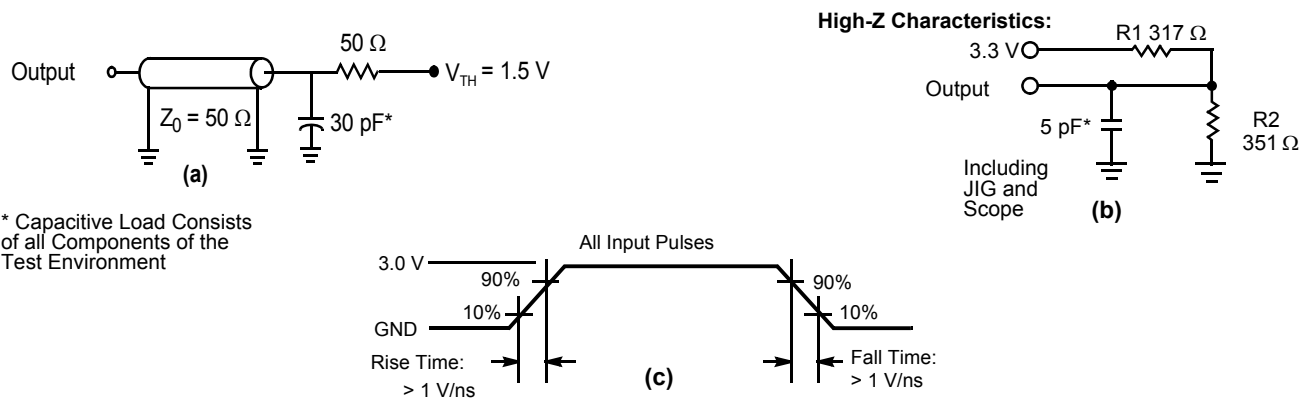
Parameter <sup>[5]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	10	10	pF
C <sub>OUT</sub>	I/O capacitance		10	10	pF

### Thermal Resistance

Parameter <sup>[5]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	31.50	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		21.58	15.75	°C/W

### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms <sup>[6]</sup>



\* Capacitive Load Consists of all Components of the Test Environment

#### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V<sub>DD</sub> (3.0 V). 100 μs (t<sub>power</sub>) after reaching the minimum operating V<sub>DD</sub>, normal SRAM operation begins including reduction in V<sub>DD</sub> to the data retention (V<sub>CCDR</sub>, 1.0 V) voltage.

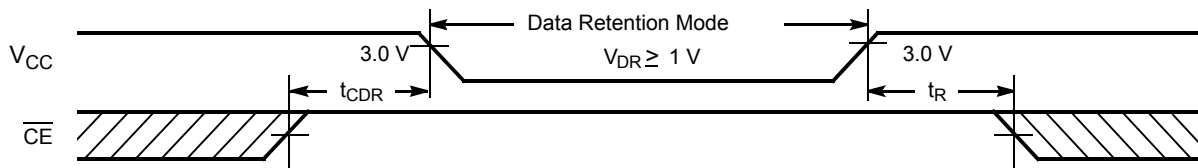
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention	–	1	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = 1.2\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ , $CE_2 \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	30	mA
$t_{CDR}^{[7]}$	Chip deselect to data retention time	–	0	–	ns
$t_R^{[8]}$	Operation recovery time	–	10	–	ns

## Data Retention Waveform

Figure 4. Data Retention Waveform <sup>[9]</sup>



### Notes

7. Tested initially and after any design or process changes that may affect these parameters.
8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 100\ \mu\text{s}$  or stable at  $V_{CC(min.)} \geq 100\ \mu\text{s}$ .
9.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

## AC Switching Characteristics

Over the Operating Range

Parameter <sup>[10]</sup>	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}$	$V_{CC}$ (typical) to the first access <sup>[11]</sup>	100	–	$\mu$ s
$t_{RC}$	Read cycle time	10	–	ns
$t_{AA}$	Address to data valid	–	10	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to data valid	–	10	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[12]</sup>	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[12]</sup>	–	5	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to low Z <sup>[12]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to high Z <sup>[12]</sup>	–	5	ns
$t_{PU}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to power-up <sup>[13]</sup>	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH/ $CE_2$ LOW to power-down <sup>[13]</sup>	–	10	ns
$t_{DBE}$	Byte enable to data valid	–	5	ns
$t_{LZBE}$	Byte enable to low Z	0	–	ns
$t_{HZBE}$	Byte disable to high Z	–	6	ns
<b>Write Cycle</b> <sup>[14, 15]</sup>				
$t_{WC}$	Write cycle time	10	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW/ $CE_2$ HIGH to write end	7	–	ns
$t_{AW}$	Address setup to write end	7	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	ns
$t_{SD}$	Data setup to write end	5	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[12,13]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[12,13]</sup>	–	5	ns
$t_{BW}$	Byte Enable to End of Write	7	–	ns

### Notes

10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part (a) of [Figure 3 on page 6](#), unless specified otherwise.
11.  $t_{POWER}$  gives the minimum amount of time that the power supply is at typical  $V_{CC}$  values until the first memory access is performed.
12.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$ ,  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ , and  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of [Figure 3 on page 6](#). Transition is measured when output goes into high impedance.
13. These parameters are guaranteed by design and are not tested.
14. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . Chip enables must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
15. The minimum write cycle time for Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [16, 17]

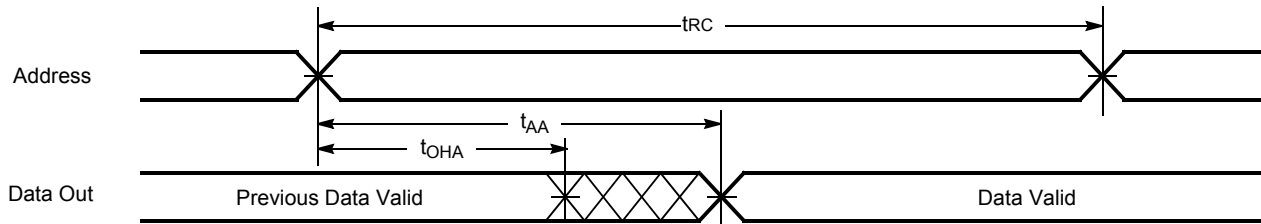
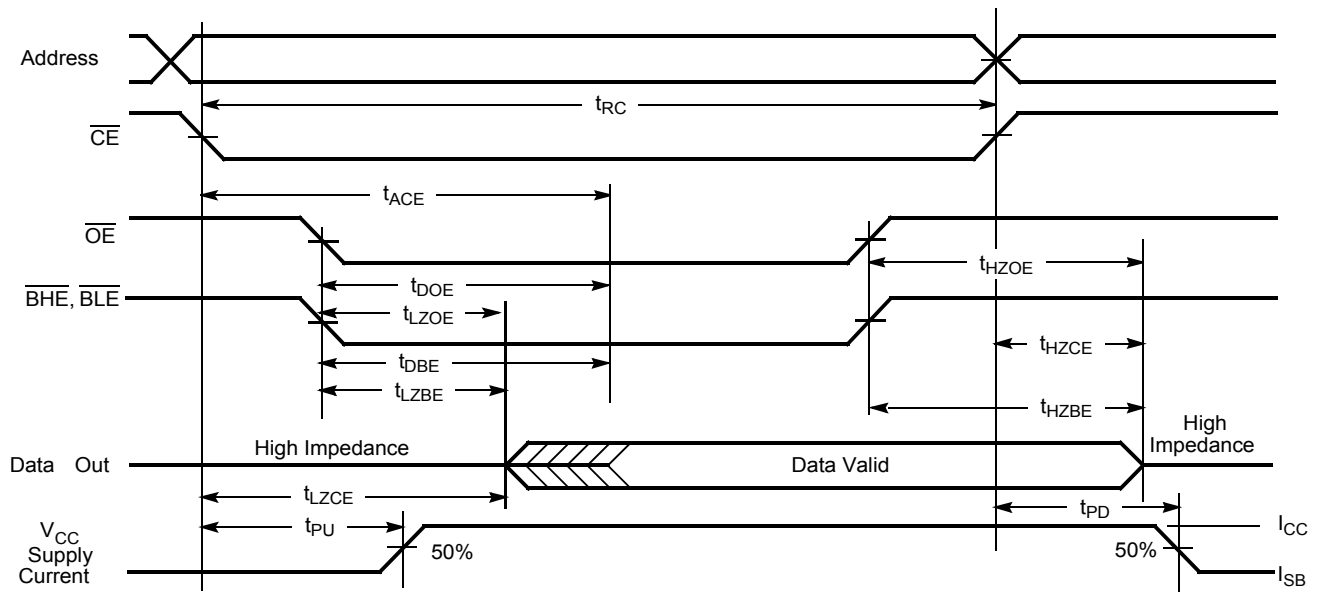


Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [17, 18, 19]



**Notes**

16. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ .

17.  $\overline{WE}$  is HIGH for read cycle.

18.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

19. Address valid before or similar to  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [20, 21, 22]

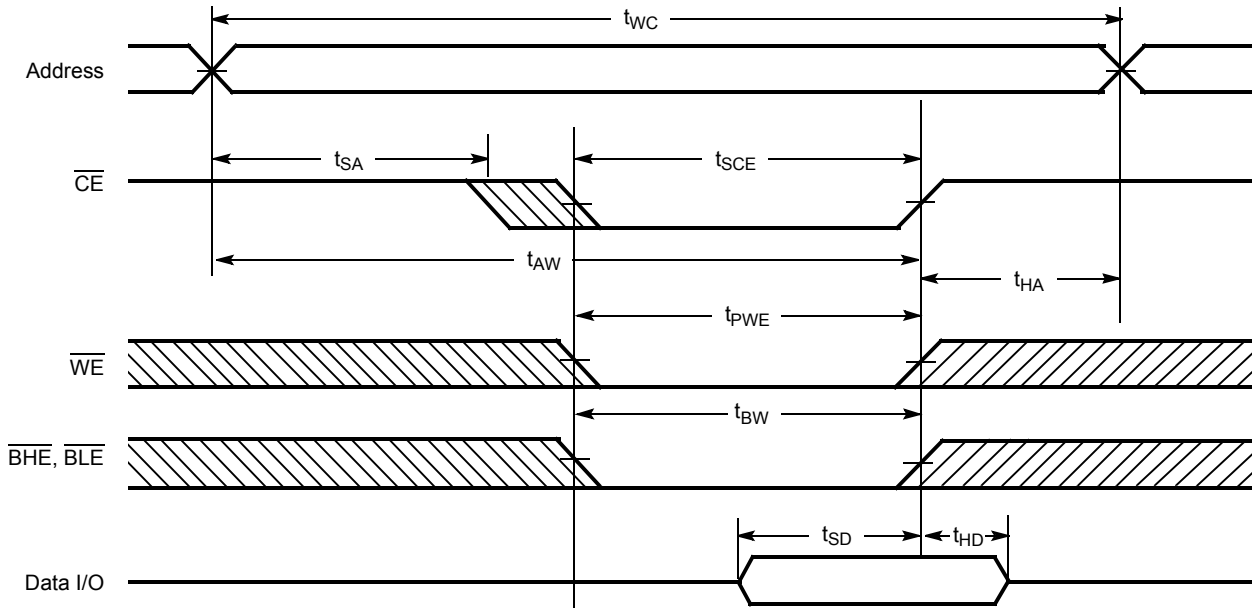
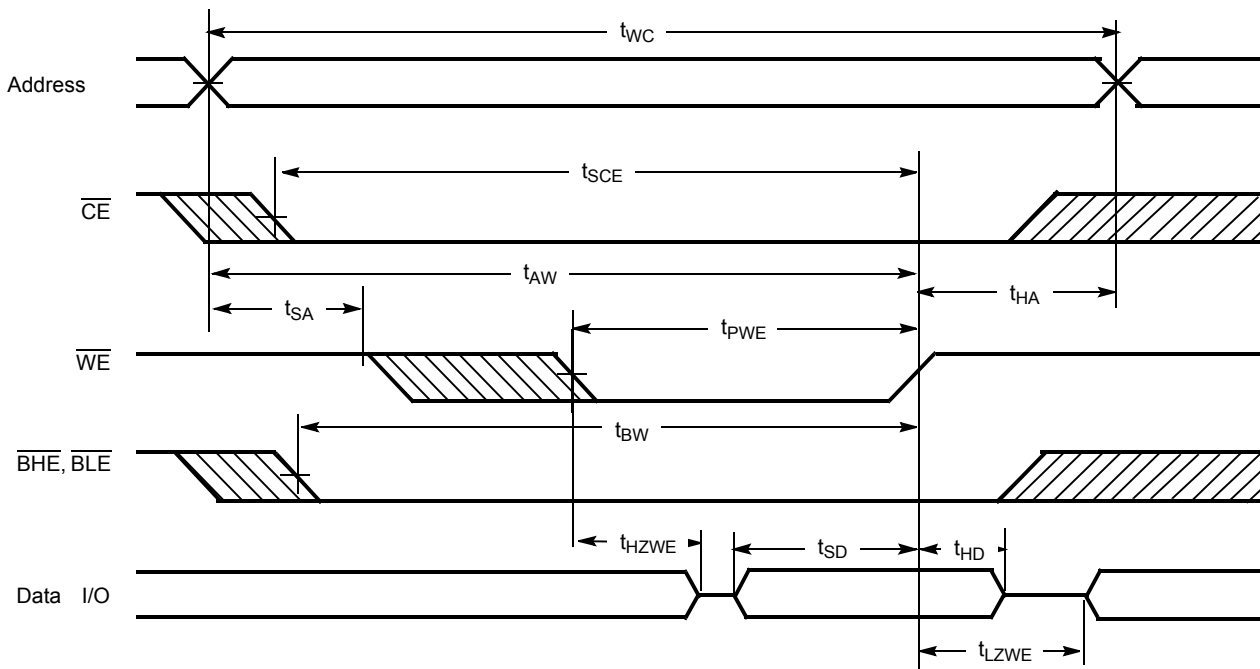


Figure 8. Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [20, 21, 22]



Notes

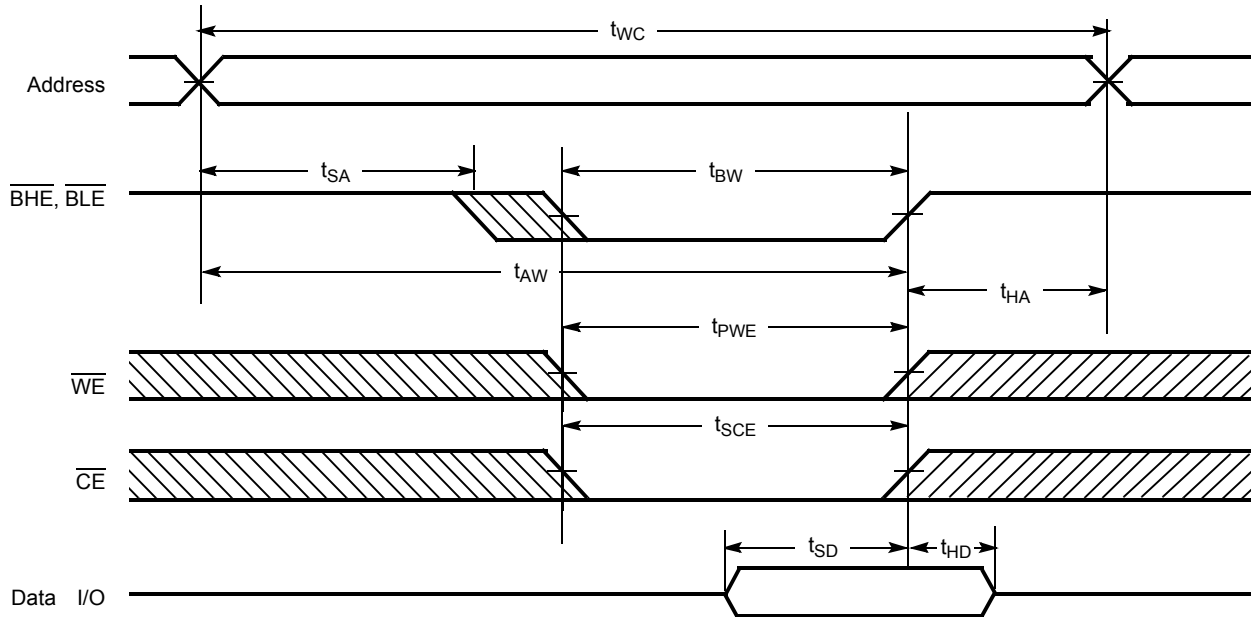
20.  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

21. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

22. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Figure 9. Write Cycle No. 3 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled) [23]**



**Note**

23.  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.

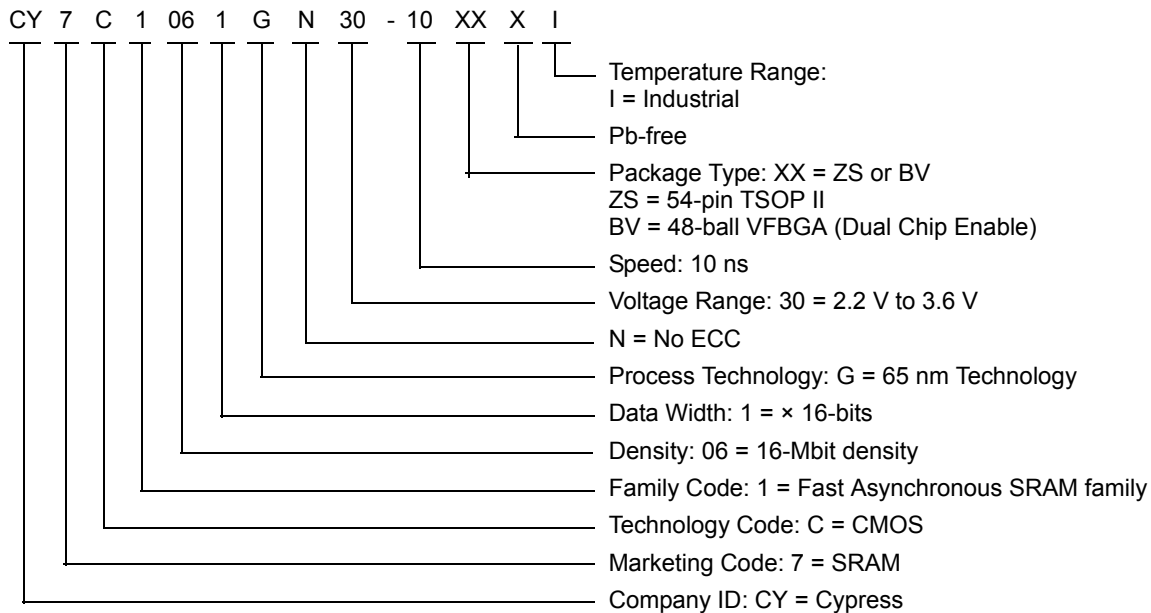
**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	High Z	Power down	Standby (I <sub>SB</sub> )
L	H	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	H	L	H	L	H	Data out	High Z	Read lower bits only	Active (I <sub>CC</sub> )
L	H	L	H	H	L	High Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	H	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	H	X	L	L	H	Data in	High Z	Write lower bits only	Active (I <sub>CC</sub> )
L	H	X	L	H	L	High Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

### Ordering Information

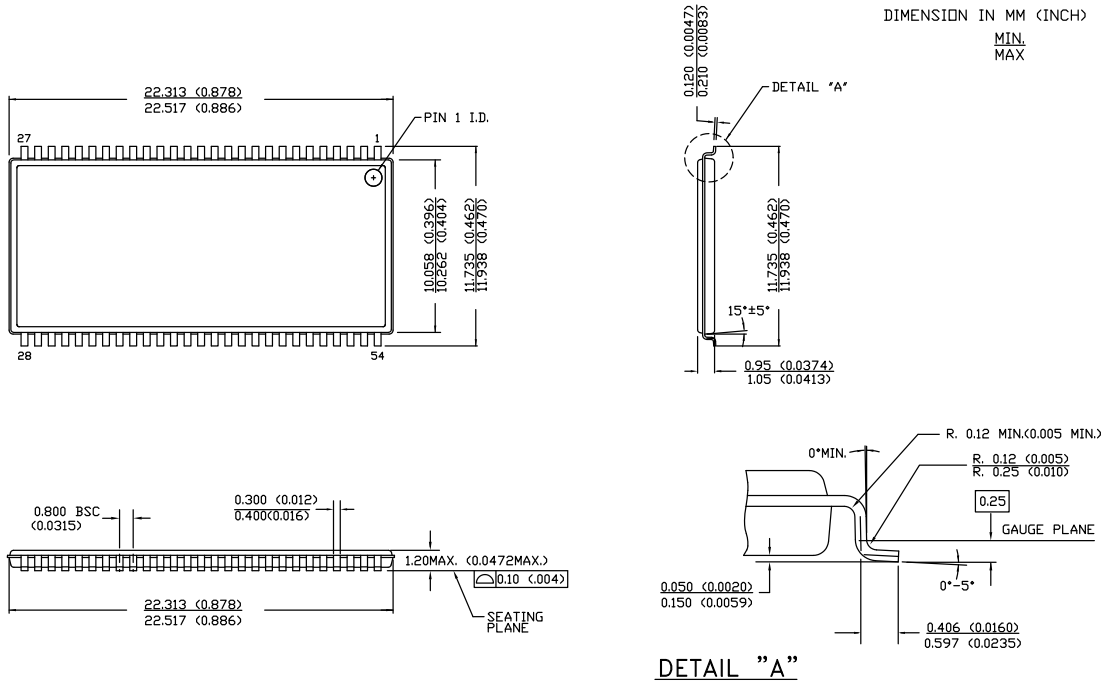
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1061GN30-10ZSXI	51-85160	54-pin TSOP II (22.4 × 11.84 × 1.0 mm) (Pb-free)	Industrial
	CY7C1061GN30-10BVXI	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free) (Dual Chip Enable)	

### Ordering Code Definitions



Package Diagrams

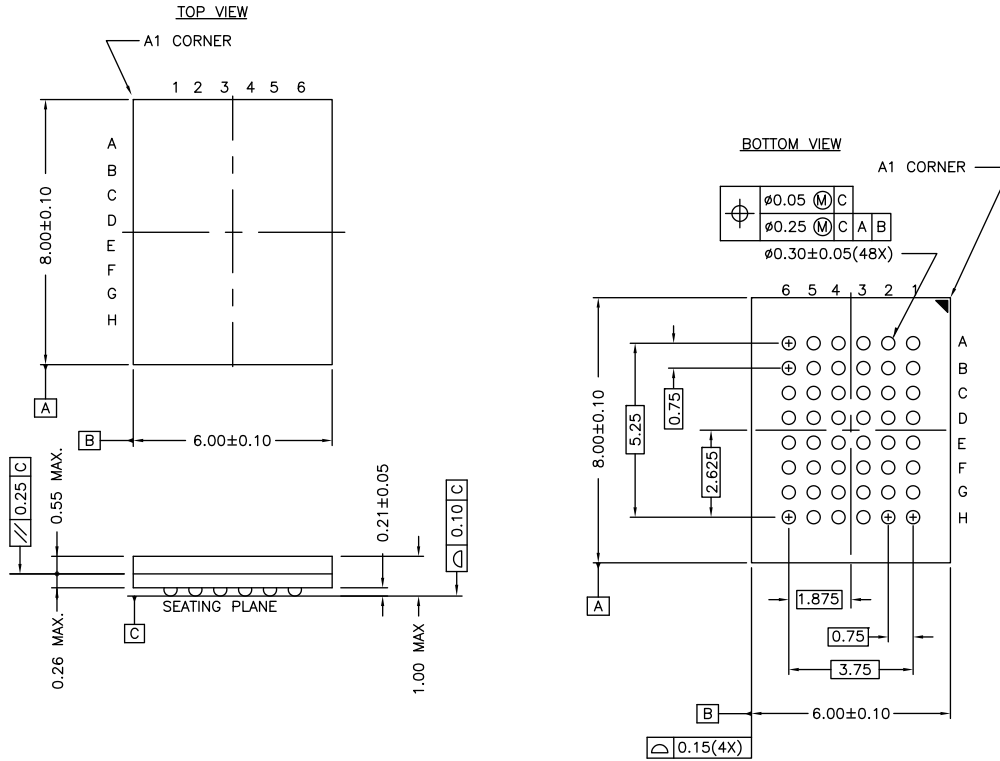
Figure 10. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 \*E

Package Diagrams (continued)

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
 posted on the Cypress web.

51-85150 \*H

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1061GN30, 16-Mbit (1 M words × 16 bit) Static RAM Document Number: 001-93680				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	4505531	VINI	01/02/2015	New data sheet.
*A	4900408	NILE	09/11/2015	<p>Updated <a href="#">DC Electrical Characteristics</a>:  Updated details in "Test Conditions" column of V<sub>OH</sub> and V<sub>OL</sub> parameters.  Updated <a href="#">Ordering Information</a>:  No change in part numbers.  Replaced "51-85178" with "51-85150" in "Package Diagram" column.  Replaced "8 × 9.5 × 1 mm" with "6 × 8 × 1.0 mm" in "Package Type" column.  Updated <a href="#">Package Diagrams</a>:  Removed spec 51-85178 *C.  Added spec 51-85150 *H.  Updated to new template.</p>

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